Buck-Boost, High Efficiency POL Module

VPN12AD02-FU

FEATURES:

- High Density Fully Integration Module
- Constant Current Mode: IOUT Maximum 2A
  Output Voltage Range: 3V to 40V
  Maximum Output Power: 40W
  Input Voltage Range from 5.5V to 36V
- Constant Voltage Mode: IOUT Maximum 4A
  Output Voltage Range: 12V
  Maximum Output Power: 48W
  Input Voltage Range from 8V to 36V
- Output LED OVP, Open, Short Protection
- Analog and PWM dimming
- LED and Input Current Dedicated Sense
- Switching Frequency 350kHz
- Spread Spectrum Frequency Modulation
- Adjustable Soft Start
- Automotive AEC Qualified
- Compact Size: 15mm x 15mm x 8.2mm
- Wettable Flank Package
- Pb-free for RoHS compliant
- MSL 3, 260C Reflow

APPLICATIONS:

- Automotive LED Headlanp Lighting
- General purpose Constant Current LED driver.
- VOUT 12V Buck-Boost application

GENERAL DESCRIPTION:

The VPN12AD02-FU is non-isolated dc-dc converters. The PWM switching regulator, high frequency power inductor, and most of components are integrated in one hybrid package.

The VPN12AD02-FU is a synchronous MOSFET DC/DC Module with built in protection features. This concept is beneficial for driving high power LEDs with maximum system efficiency. The VPN12AD02-FU offers both analog and digital (PWM) dimming. A built in spread spectrum switching frequency modulation and the forced continuous current regulation mode improve the overall EMC behavior. The adjustable soft start feature limits the current peak as well as voltage overshoot at start-up. The VPN12AD02-FU is suitable for using in the harsh automotive environment.

The low profile and compact size package (15mm × 15mm x 8.2mm) is suitable for automated assembly by standard surface mount equipment. VPN12AD02-FU is Pb-free and RoHS compliance.

TYPICAL APPLICATION CIRCUIT & PACKAGE SIZE:

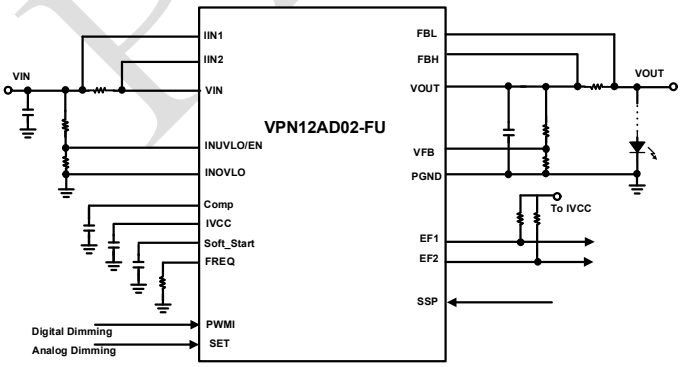


FIGURE.1 TYPICAL APPLICATION CIRCUIT

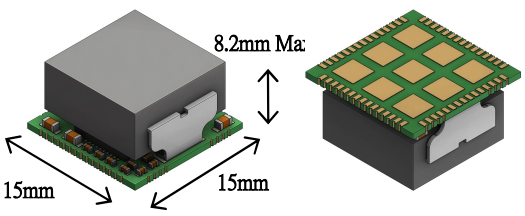


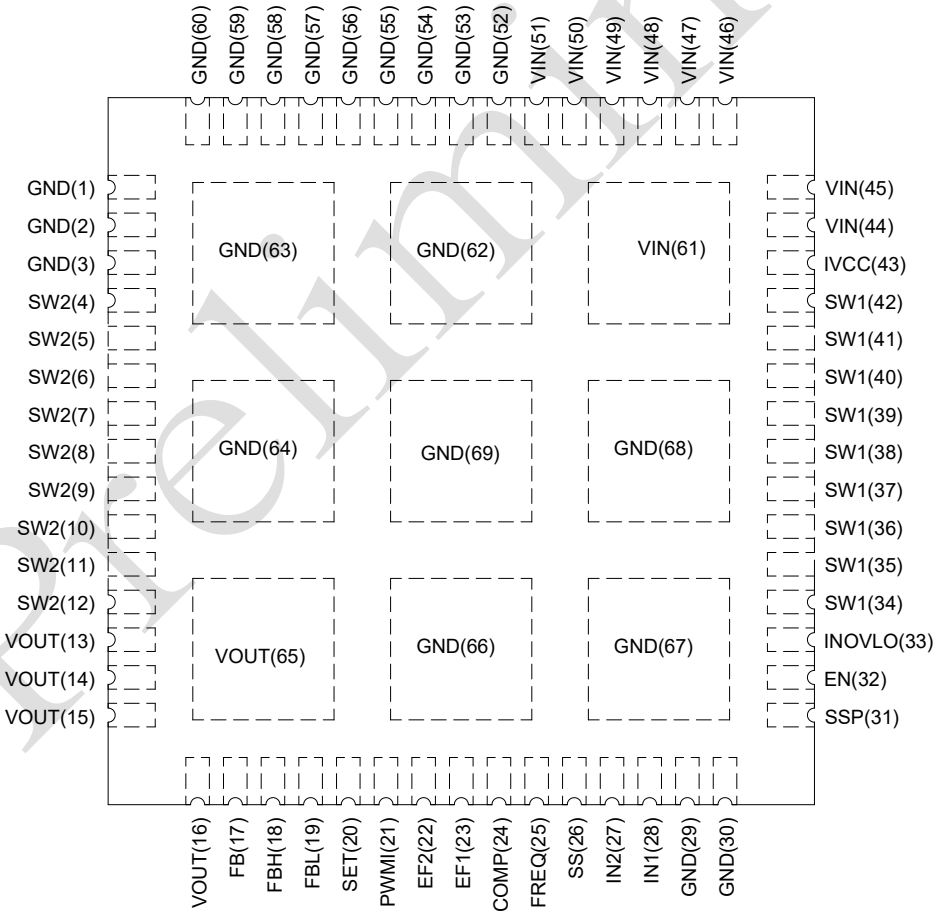
FIGURE.2 HIGH DENSITY uPOL MODULE

ORDER INFORMATION:

Part Number	Ambient Temp. Range (°C)	Package (Pb-Free)	MSL	Note
VPN12AD02-FU	-40 ~ +105	QFN	Level 3	-

Order Code	Packing	Quantity
VPN12AD02-FU	Tray	390

PIN CONFIGURATION:



TOP VIEW

PIN CONFIGURATION:

Symbol	#	Type	Description
GND	1~3, 29, 30, 52~60, 62~64, 66~69	PWR	Power ground
SW2	4~12	PWR	The boost side switching node
VOUT	13~16, 65	PWR	Power output pin.
FB	17	Analog I	Output over voltage protection function.
FBH	18	Analog I	Output current Feedback Positive
FBL	19	Analog I	Output current Feedback Negative
SET	20	Analog I	Analog dimming input pin
PWMI	21	Digital I	Digital dimming input pin
EF2	22	Digital O	An open drain output for Fault information
EF1	23	Digital O	An open drain output for Fault information
COMP	24	Analog O	Connect R and C network to pin as Compensator
FREQ	25	Analog O	Connect an external resistor to GND to set frequency.
SS	26	Analog O	Connect a capacitor to GND to set soft start ramp.
IN2	27	Analog I	Inverting Input (-), connect to VIN if input current monitor is not needed.
IN1	28	Analog I	Non Inverting Input (+), connect to VIN if input current monitor is not needed.
SSP	31	Digital I	High active for the spread Spectrum function.
EN	32	Analog I	Enable function with under voltage threshold capability via external components.
INOVLO	33	Analog I	Connect to GND directly
SW1	34~42	PWR	The buck side switching node
IVCC	43	Analog O	Used for internal biasing and gate driver supply. Bypass with external capacitor 16V/10uF/X7R close to the pin.
VIN	44~51, 61	PWR	Power input pin

ELECTRICAL SPECIFICATIONS:

CAUTION: Do not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Description	Min.	Typ.	Max.	Unit
■ Absolute Maximum Ratings					
VIN, IN1, IN2, FBH, FBL		-0.3	-	60	V
IVCC		-0.3	-	6	V
IN1-IN2, FBH-FBL		-0.5	-	0.5	V
SW1, SW2		-1	-	60	V
GND		-0.3	-	0.3	V
EN/INUVLO		-0.3	-	60	V
PWMI, SSP, VFB, INOVLO, EF1, EF2, SET		-0.3	-	5.5	V
COMP, SS, FREQ		-0.3	-	3.6	V
Tc	Case Temperature of Inductor	-40	-	+135	°C
Tj	Junction Temperature, Main IC	-40	-	+150	°C
Tstg	Storage Temperature	-40	-	+135	°C
Ta	Ambient Tamperture	-40	-	+105	°C
■ Recommendation Operating Ratings for Constant Current Application					
VIN	Device Extended Supply Voltage Range	+5.5	-	+36	V
POWER	Output Power Range	0	-	40	W
VOUT	Adjuested Output Voltage	+3	-	+40	V
Ta	Ambient Tamperture	-40	-	+105	°C
■ Recommendation Operating Ratings for Constant Voltage Application					
VIN	Device Extended Supply Voltage Range	+8	-	+36	V
POWER	Output Power Range	0	-	48	W
VOUT	Adjuested Output Voltage	-	+12	-	V
Ta	Ambient Tamperture	-40	-	+105	°C
■ Thermal Information					
Rth(j_{choke}-a)	Thermal resistance from junction to ambient.	-	21	-	°C/W

NOTES:
1. Rth(j_{choke}-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The test board size is 80mm×80mm×1.6mm with 4 layers 2oz per layer. The test condition is complied with JEDEC EIJ/JESD 51 Standards.

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: T_A = 25 ºC, unless otherwise specified.
For CC mode, VIN = 12V, Cin =10uF/50V/1210/X7R x 2, Cout = 10uF/50V/1210/X7R x 2.
For CV mode, VIN = 12V, VOUT=12V, Cin =10uF/X7R x 2 + 82uF EP-CAP, Cout = 22uF/X7R x 2 + 270uF EP-CAP

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Input Characteristics						
$V_{VIN(ON)}$	Input Voltage Startup	VIN increasing; VEN/INUVLO = HIGH;	-	-	4.7	V
$V_{VIN(OFF)}$	Input Undervoltage switch OFF	VIN decreasing; VEN/INUVLO = HIGH;	-	-	4.5	V
$I_{VIN(ACTIVE)}$	Device operating current	ACTIVE mode; CC mode Fsw=350 KHz; VPWMI = 0 V;	-	4.4	6	mA
$I_{VIN(ACTIVE)}$	Device operating current	ACTIVE mode; CV mode Fsw=350 KHz; VOUT=12V	-	25	-	mA
$I_{VIN(SLEEP)}$	VIN Sleep mode supply current	VEN/INUVLO = 0 V; VIN = 13.5 V; V_{IVCC} = 0 V;	-	1.5	-	uA
■ Regulator Characteristics						
$V_{IIN1-IIN2}$	Input Current Sense Threshold		-	50	-	mV
$V_{FBH-FBL}$	V_{FBH} - V_{FBL} Threshold	VSET = 2V;	145	150	155	mV
$V_{FBH-FBL\_10}$	V_{FBH} - V_{FBL} Threshold at analog dimming 10%	VSET = 0.32 V; CC mode	-	15	-	mV
D_{BOOST_MAX}	Maximum Boost Duty Cycle	Fsw= 300 kHz;	-	91	-	%
F_{SW}	Switching Frequency	Tj = 25°C; RFREQ= 30 kΩ;	-	350	-	kHz
F_{DEV}	Frequency Deviation	SSP=HIGH	-	+/-16	-	%
ΔV_{OUT} / V_{OUT}	Line regulation accuracy	VIN = 8V to 24V; CV mode VOUT = 12V, IOUT = 2A	-	1.0	-	%
ΔV_{OUT} / V_{OUT}	Load regulation accuracy	IOUT = 0A to 2A; CV mode VIN = 12V, VOUT = 12V	-	0.5	-	%

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: T_A = 25 ºC, unless otherwise specified.
For CC mode, VIN = 12V, Cin =10uF/50V/1210/X7R x 2, Cout = 10uF/50V/1210/X7R x 2.
For CV mode, VIN = 12V, VOUT=12V, Cin =10uF/X7R x 2 + 82uF EP-CAP, Cout = 22uF/X7R x 2 + 270uF EP-CAP

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Control Input Characteristics						
V_{PWI_ON}	PWMI Turn On Threshold		2	-	-	V
V_{PWI_OFF}	PWMI Turn Off Threshold		-	-	0.8	V
V_{SSP_ON}	Rising threshold voltage		2	-	-	V
V_{SSP_OFF}	Falling threshold voltage		-	-	0.8	V
■ Fault Protection						
$V_{EN/INUVLOTH}$	Input Under voltage Falling Threshold		1.55	1.75	1.95	V
$V_{EN/INUVLO\_HYS}$	Input Over voltage Threshold Hysteresis		-	90	-	mV
V_{VFB_VOTH}	VFB Over Voltage Threshold		1.41	1.46	1.51	V
$V_{VFB\_VOTH\_HYS}$	VFB Over Voltage Threshold Hysteresis		-	40	-	mV
V_{VFB_S2G}	Short to GND Threshold	V_{FB} decreasing	0.52	0.563	0.6	V
T_{J_SD}	Over Temperature Shutdown		-	175	-	℃
$T_{J\_SD\_HYST}$	Over Temperature Shutdown Hysteresis		-	10	-	℃

TYPICAL PERFORMANCE CHARACTERISTICS: Constant Current Mode

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 75mm×58mm, 2 layers 2oz.
VIN = 12V, Cin =10uF/50V/1210/X7R x 2, Cout = 10uF/50V/1210/X7R x 2.

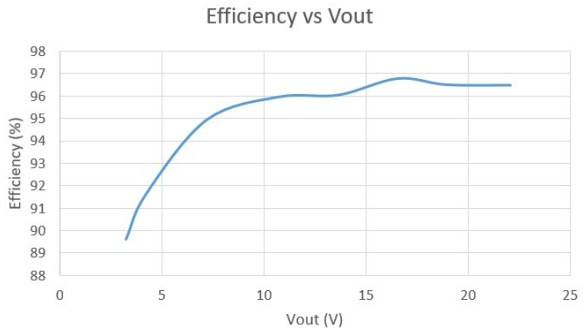


FIG.3 EFFICIENCY V.S. VOUT (VIN=12V, IOUT=2A. The Efficiency includes the output current sense resistor)

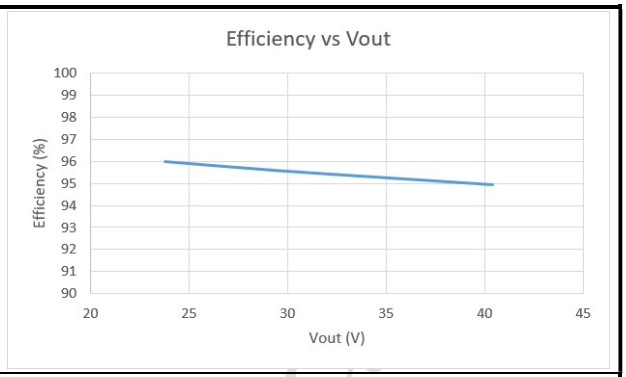


FIG.4 EFFICIENCY V.S. VOUT (VIN=12V, IOUT=1A. The Efficiency includes the output current sense resistor)

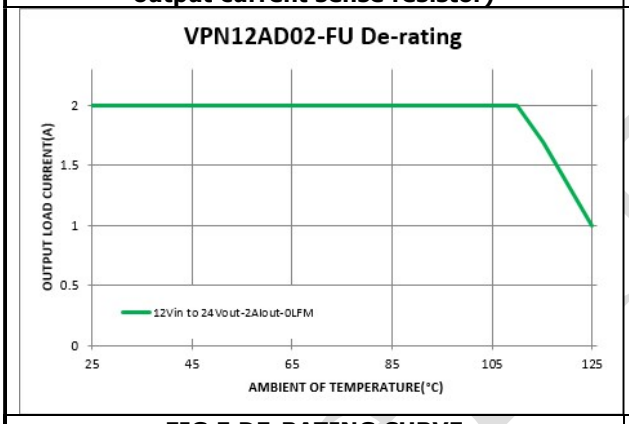


FIG.5 DE-RATING CURVE (VIN=12V, VOUT=24V)

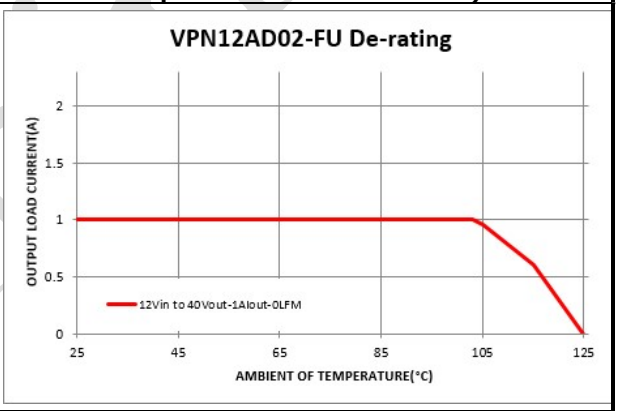


FIG.6 DE-RATING CURVE (VIN=12V, VOUT=40V)

TYPICAL PERFORMANCE CHARACTERISTICS: Constant Voltage Mode

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 75mm×58mm, 2 layers 2oz.
VOUT=12V, Cin =10uF/X7R x 2 + 82uF EP-CAP, Cout = 22uF/X7R x 2 + 270uF EP-CAP

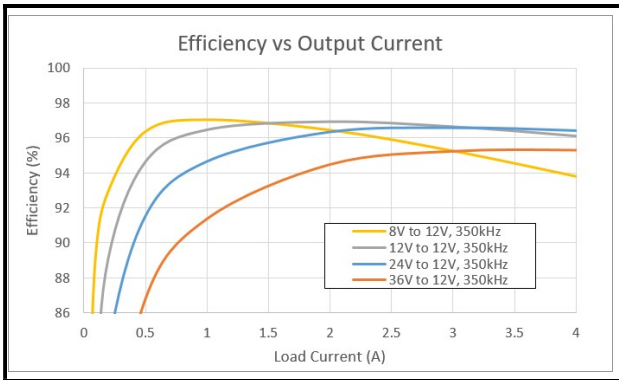


FIG.7 EFFICIENCY V.S. VOUT (VOUT=12V)

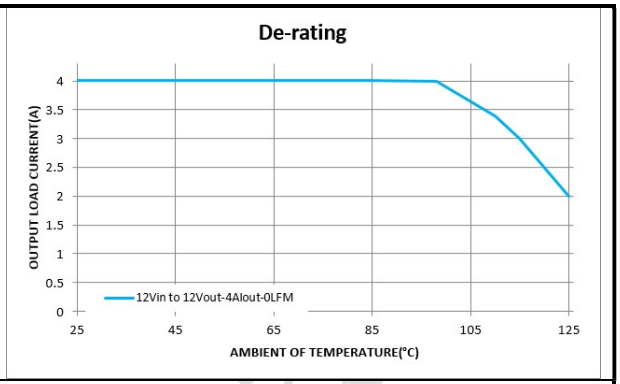


FIG.8 DE-RATING CURVE (VIN=12V, VOUT=12V, Load=4A)

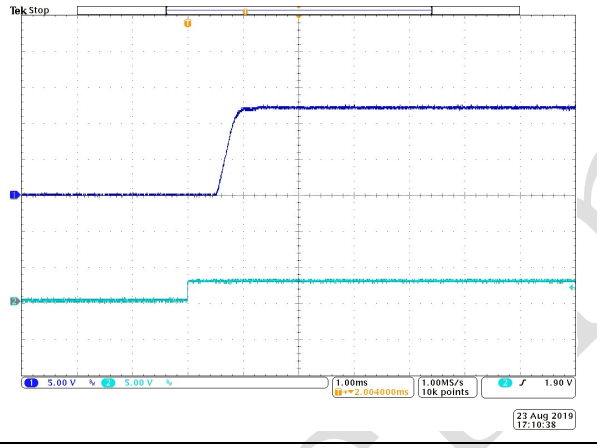


FIG.9 Enable on (VIN=12V, VOUT=12V, Load=0A)

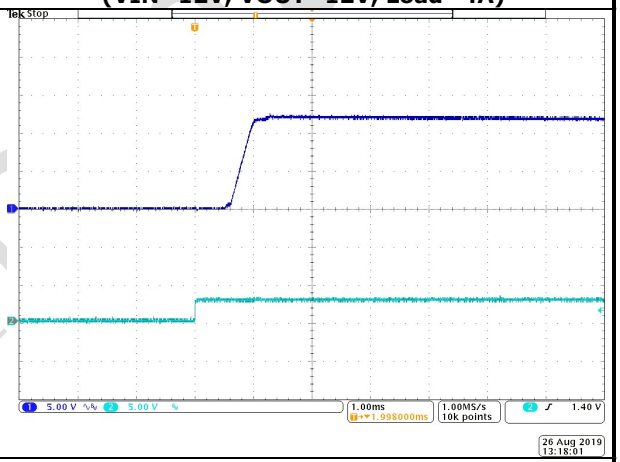


FIG.10 EFFICIENCY V.S. VOUT (VIN=12V, VOUT=12V, Load=2A)

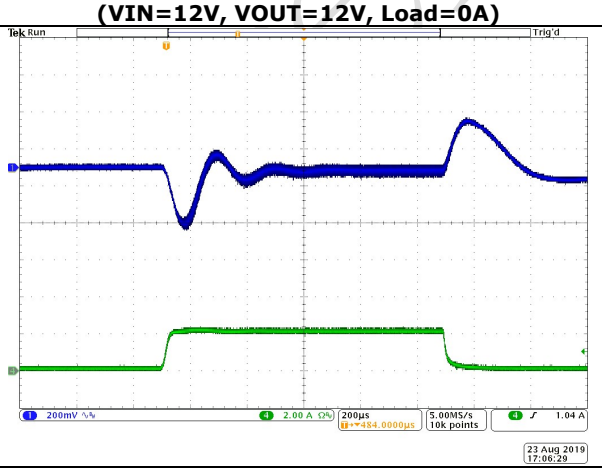


FIG.11 Load Transient (VIN=12V, VOUT=12V, Load=0 to 2A)

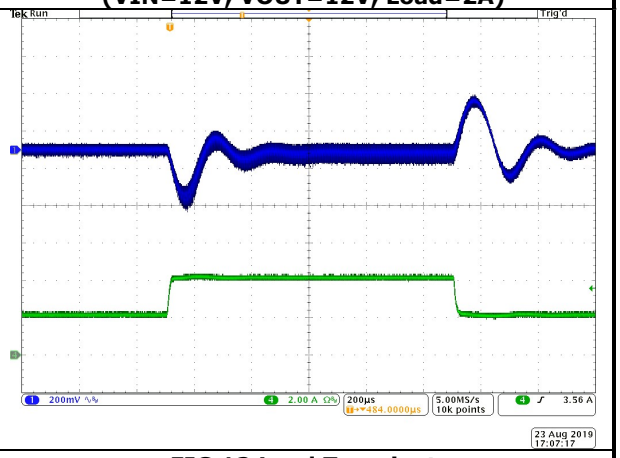


FIG.12 Load Transient (VIN=12V, VOUT=12V, Load=2A to 4A)

TYPICAL PERFORMANCE CHARACTERISTICS: Constant Voltage Mode

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 75mm×58mm, 2 layers 2oz.
VOUT=12V, Cin =10uF/X7R x 2 + 82uF EP-CAP, Cout = 22uF/X7R x 2 + 270uF EP-CAP

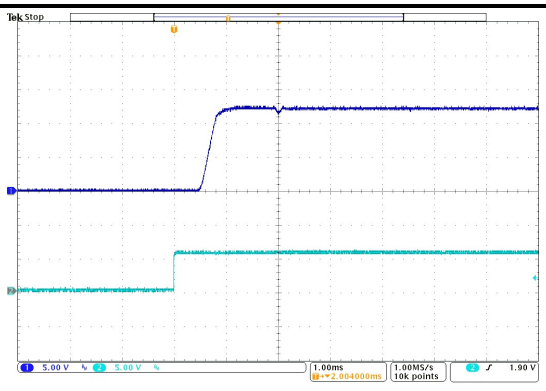


FIG.13 Enable on
(VIN=24V, VOUT=12V, Load=0A)

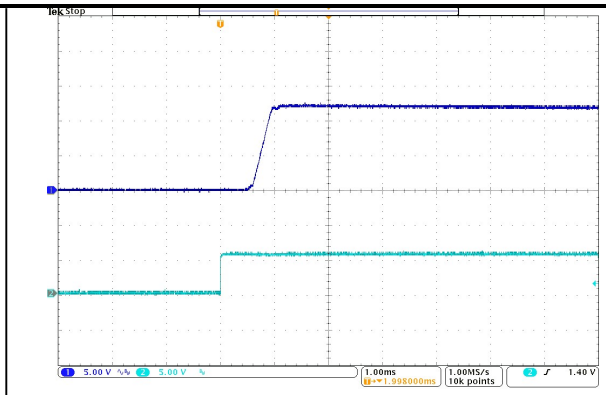


FIG.14 Enable on
(VIN=24V, VOUT=12V, Load=2A)

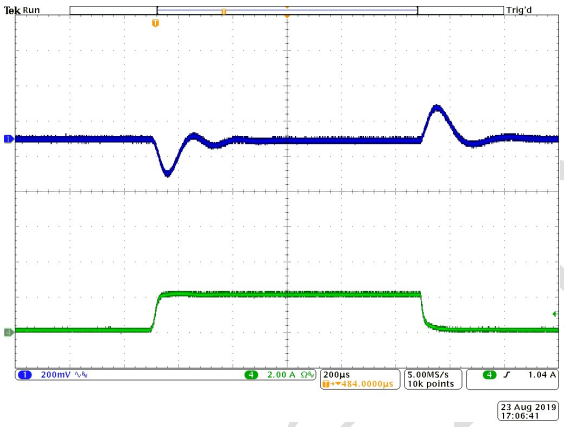


FIG.15 Load Transient
(VIN=24V, VOUT=12V, Load=0 to 2A)

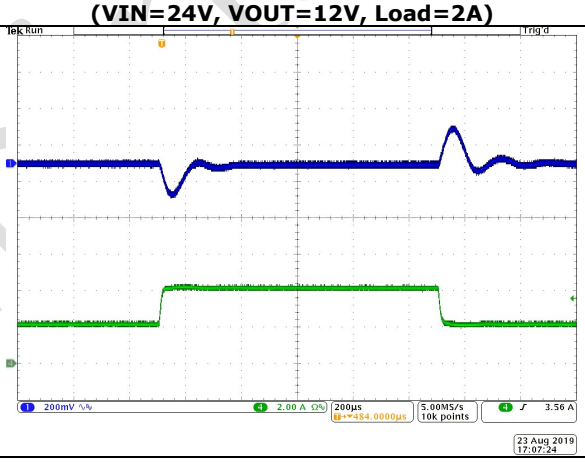


FIG.16 Load Transient
(VIN=24V, VOUT=12V, Load=2A to 4A)

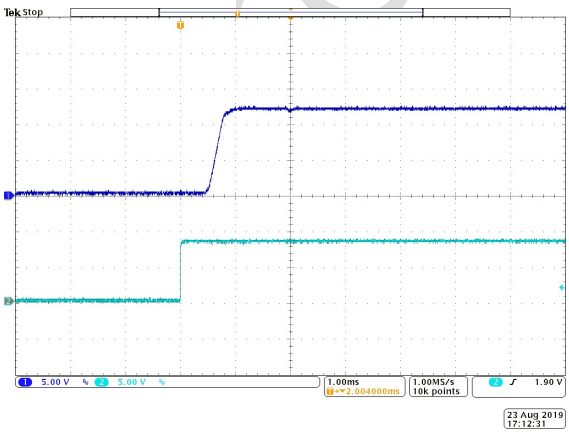


FIG.17 Enable on
(VIN=36V, VOUT=12V, Load=0A)

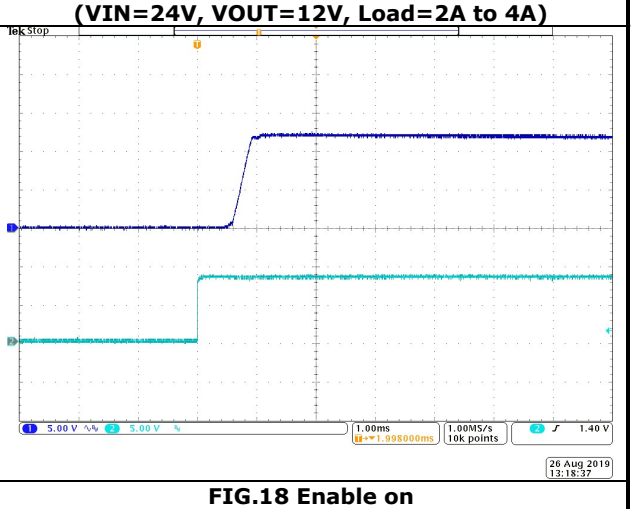


FIG.18 Enable on
(VIN=36V, VOUT=12V, Load=2A)

TYPICAL PERFORMANCE CHARACTERISTICS: Constant Voltage Mode

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 75mm×58mm, 2 layers 2oz.
VOUT=12V, Cin =10uF/X7R x 2 + 82uF EP-CAP, Cout = 22uF/X7R x 2 + 270uF EP-CAP

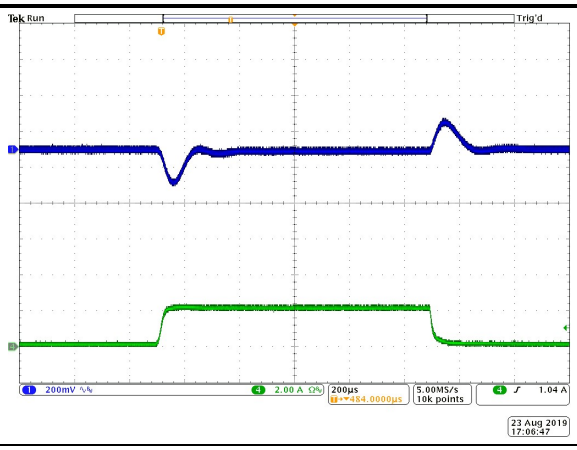


FIG.19 Load Transient
(VIN=36V, VOUT=12V, Load=0 to 2A)

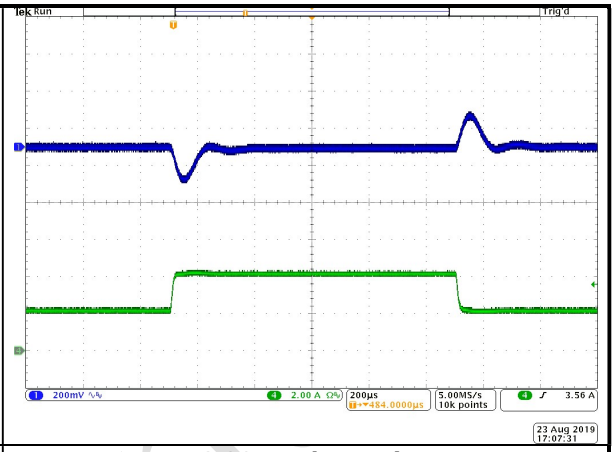


FIG.20 Load Transient
(VIN=36V, VOUT=12V, Load=2A to 4A)

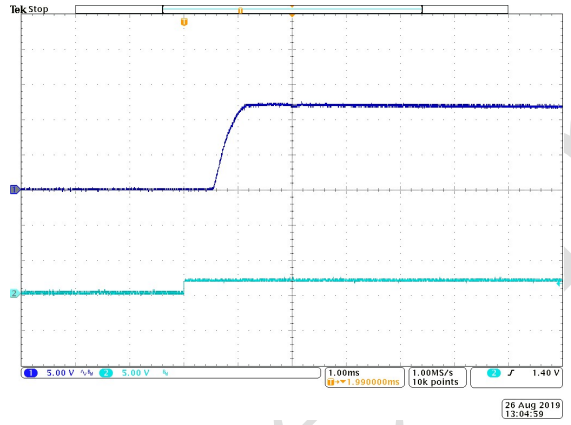


FIG.21 Enable on
(VIN=8V, VOUT=12V, Load=0A)

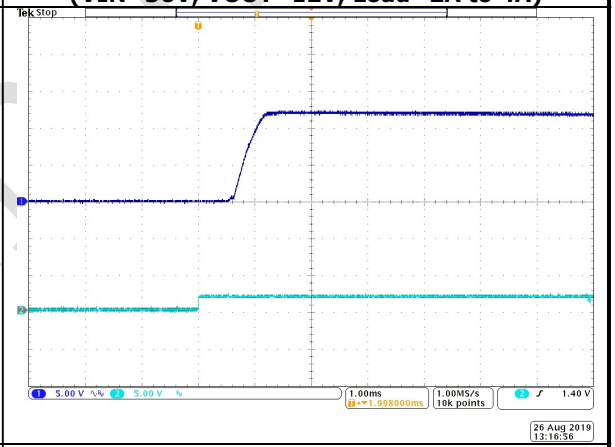


FIG.22 Enable on
(VIN=8V, VOUT=12V, Load=2A)

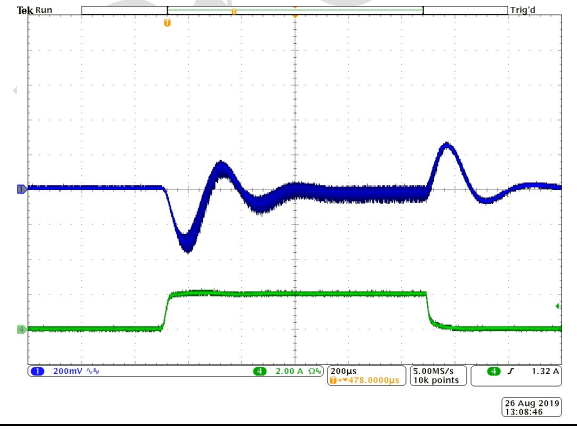


FIG.23 Load Transient
(VIN=8V, VOUT=12V, Load=0 to 2A)

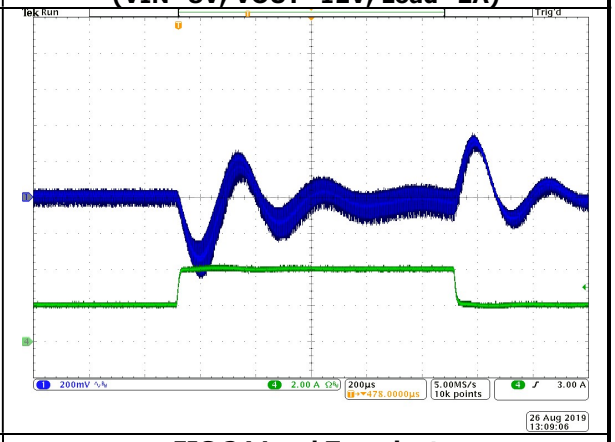


FIG.24 Load Transient
(VIN=8V, VOUT=12V, Load=2A to 4A)

APPLICATIONS INFORMATION:

Reference Circuit for General Application:

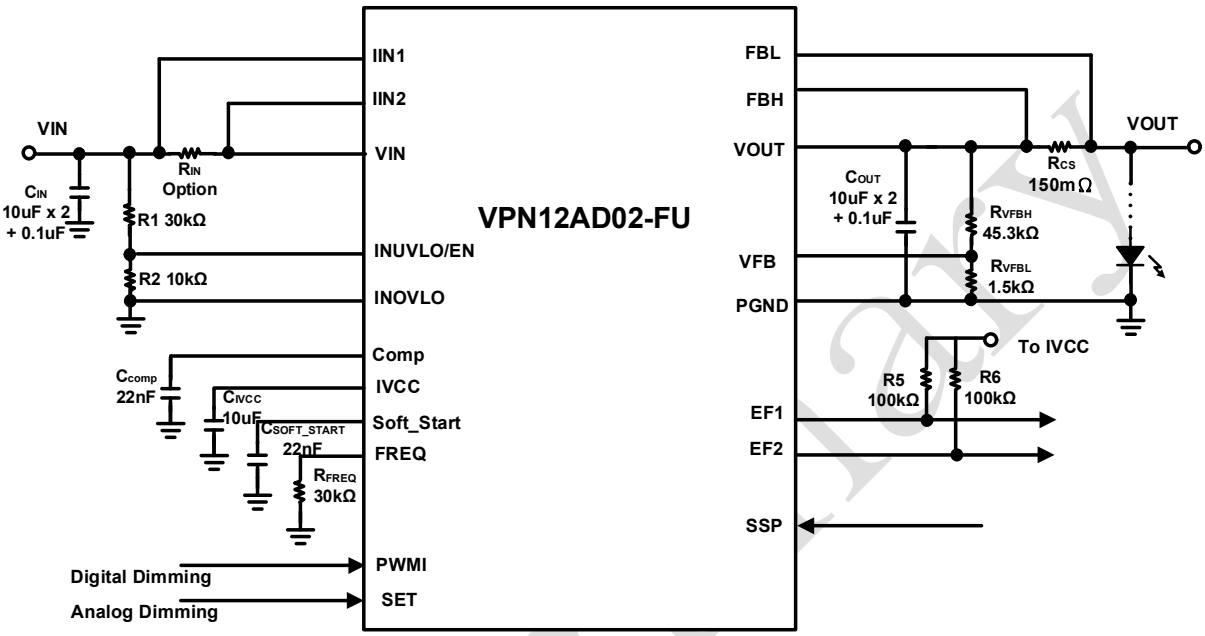


FIG.25 Constant Current Mode, ILED=1A, Fsw=350kHz Application Circuit.

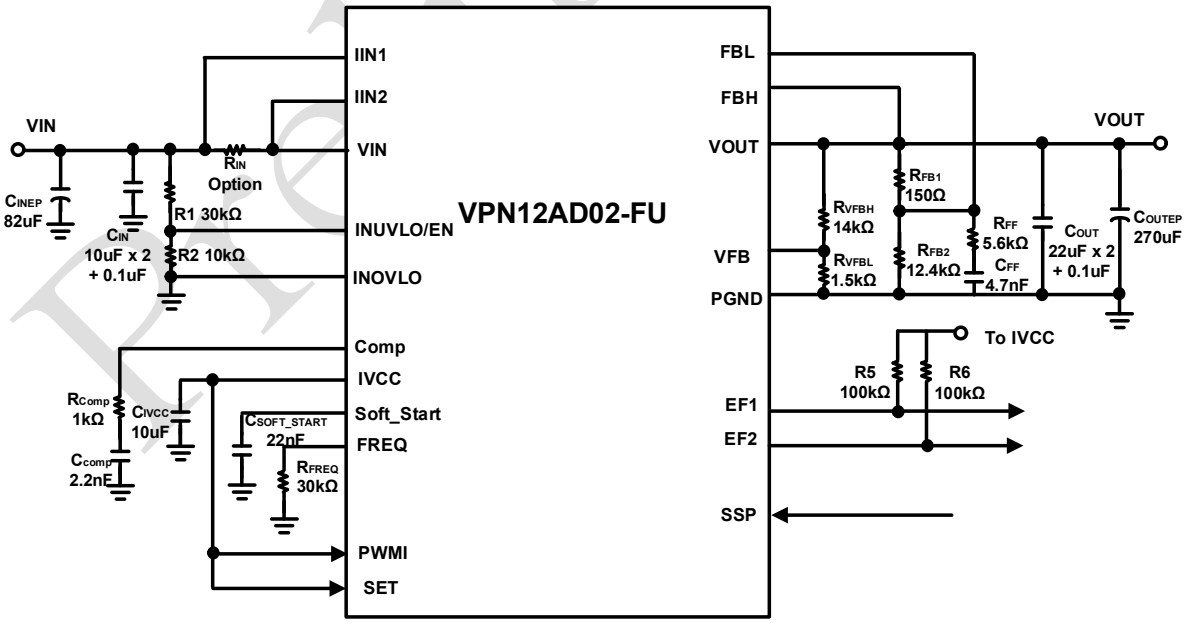


FIG.26 Constant Voltage Mode, VOUT=12V, Fsw=350kHz Application Circuit.

Switching Frequency Setup:

The switching frequency can be set from 200 kHz to 400 kHz by an external resistor connected from the FREQ pin to GND. Select the switching frequency according to the following approximate formulas.

$$R_{FREQ}[k\Omega] = 46023 \cdot (F_{SW}[kHz])^{-1.25}$$

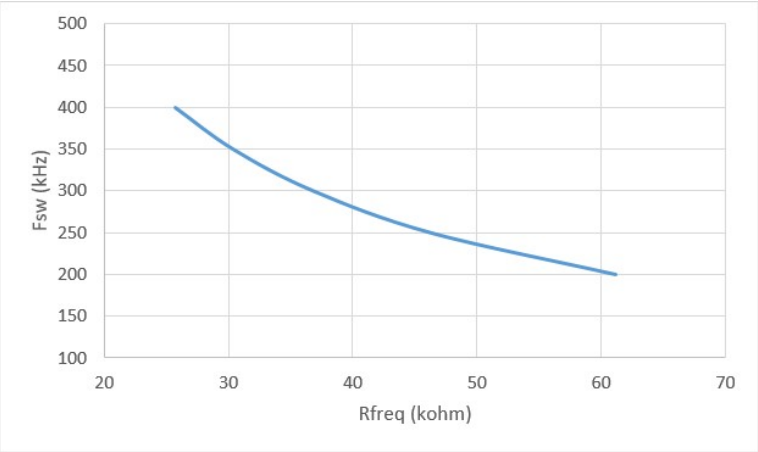


FIG.27 Switching Frequency vs Frequency Select Resistor.

LED Constant Current Setting in Constant Current Mode

$V_{FBH-FBL}$ typical value is 150mV. Set the LED current with an external resistor according to the following approximate formulas.

$$I_{LED} = \frac{V_{FBH-FBL}}{R_{CS}}$$

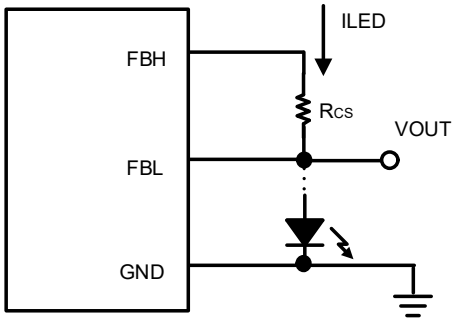


FIG.28 Current Setting in Constant Current Mode

VOUT Voltage Setting in Constant Voltage Mode:

For a voltage regulator, the output voltage can be set by selecting the values R_{FB1}, R_{FB2} according to the following equation. I_{FBL} value is about 30uA .

$$VOUT = \left(\frac{V_{FBH-FBL}}{R_{FB1}} - I_{FBL} \right) \cdot R_{FB2} + V_{FBH-FBL}$$

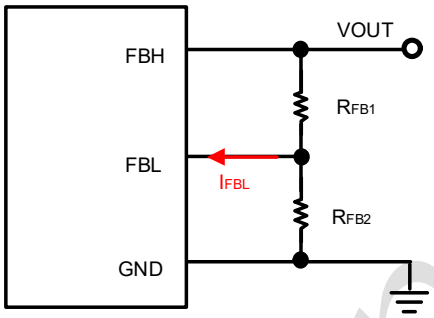


FIG.29 VOUT Voltage Setting in Constant Voltage Mode

Input Voltage UVLO and Current Limitation:

Input under voltage shutdown levels EN/INUVLO can both be defined through an external resistor divider. The two inputs (IIN1, IIN2) can be used to limit the Input current. IINmax. If the input current limitation is not used, it needs to short IIN1 and IIN2 to VIN and short RIN. Following are the equations and figure for these protections. 10kΩ is suggested for R2.

$$UVth = \left(1 + \frac{R1}{R2} \right) \cdot V_{EN/INUVLOTH}$$

$$IINmax = \frac{V_{IIN1-IIN2}}{R_{IN}}$$

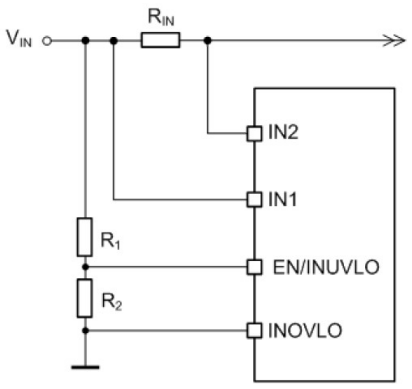


FIG.30 Input Voltage/Current Protection

Output Protection:

The VFB pin measures the VOUT to detect the protection of short to ground, open load and output overvoltage. The Fault pins of EF1 and EF2 diagnostic truth table are as following.

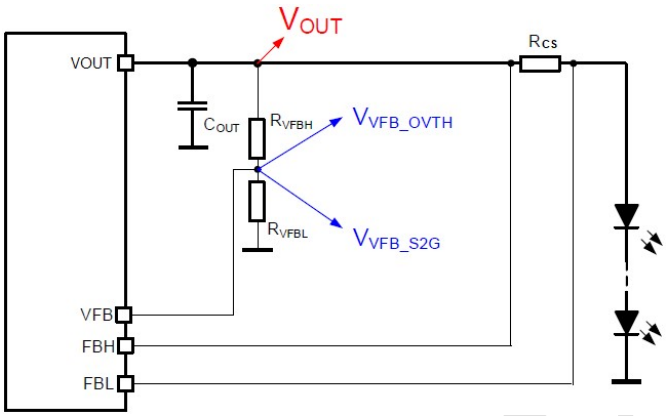


FIG.31 VFB Protection Pin

Fault Condition	EF1	EF2	Gate Driver	IVCC
No Fault occur	H	H	Switching	Active
Output over voltage	H	L	L	Active
Output short circuit	L	H	L	Active
Over temperature	L	L	L	Shutdown

FIG.32 Diagnostic Truth Table

Overvoltage Protection:

The pin VFB rise over the threshold voltage V_{VFB_OVTH} overvoltage protection via VFB. A voltage divider between V_{OUT}, VFB pin is used to adjust the overvoltage protection threshold as following equation. 1.5kΩ is suggested for R_{VFBL}.

$$VOUT\_OVP = V_{VFB\_OVTH} \cdot \left(\frac{R_{VFBH} + R_{VFBL}}{R_{VFBL}} \right)$$

Short Circuit Protection:

The VFB pin falls below the V_{VFB_S2G} short circuit threshold is ignored until the soft start finishes. A voltage divider between V_{OUT}, VFB pin is used to adjust the application short circuit thresholds as following equation. 1.5kΩ is suggested for R_{VFBL}.

$$VLED\_SHORT = V_{VFB\_S2G} \cdot \left(\frac{R_{VFBH} + R_{VFBL}}{R_{VFBL}} \right)$$

Digital Dimming:

The PWMI pin can be fed with a pulse width modulated (PWM) signals, this enables when HIGH and disables when LOW the gate drivers of the main switches.

To avoid unwanted output overshoots due to not soft start assisted startups, PWM dimming in LOW state should not be used to suspend the output current for long time intervals. To stop in a safe manner EN/INUVLO=LOW can be used. Following shows the timing diagram of LED PWM dimming and start up behavior example.

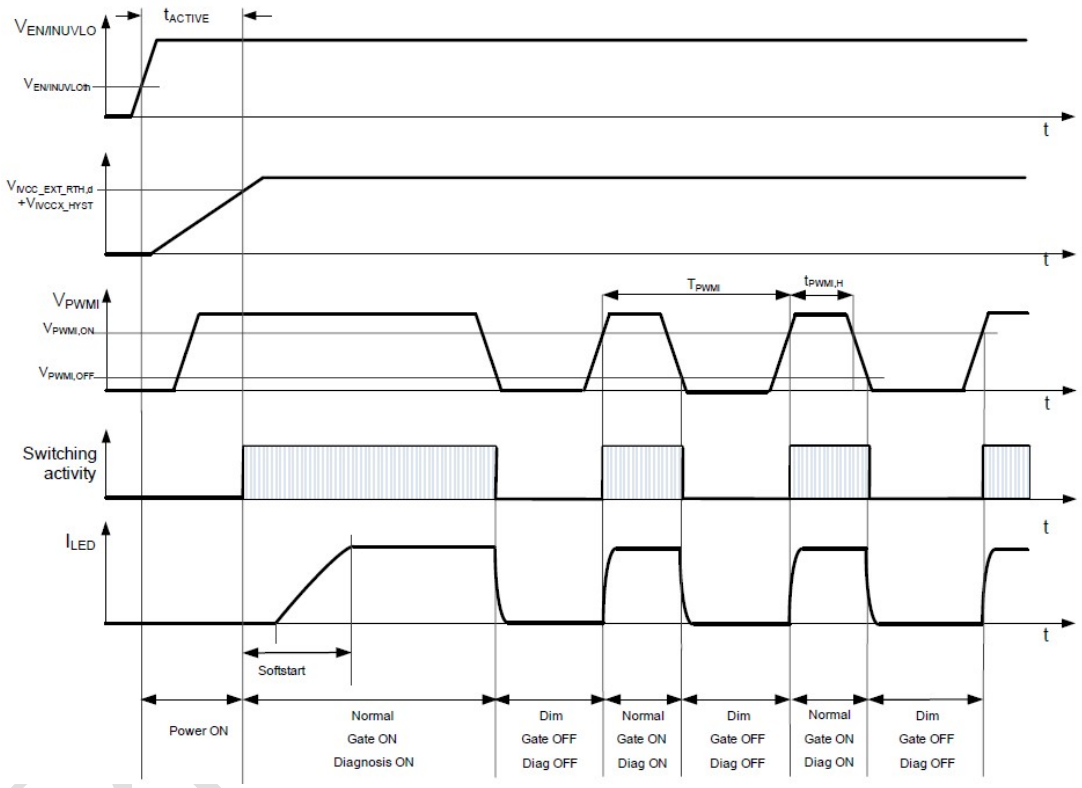


FIG.33 Timing Diagram LED Dimming and Start up behavior example

Analog Dimming:

The analog dimming feature SET pin can adjust the average load current level via the control of the feedback error Amplifier voltage ($V_{FBH-FBL}$). The V_{SET} range where analog dimming is enabled is from 200 mV to 1.5 V. The linear average output current can be adjusted by controlling the voltage at the SET pin between 0.2 V and 1.4 V. The mathematical relation is given as following equation.

$$ILED = \frac{V_{SET} - 200mV}{8 \cdot R_{FB}}$$

If V_{SET} is 200 mV (typ.) the LED current is only determined by the internal offset voltages of the comparators. To assure the switching activity is stopped and I_{OUT} = 0, V_{SET} has to be < 100 mV.

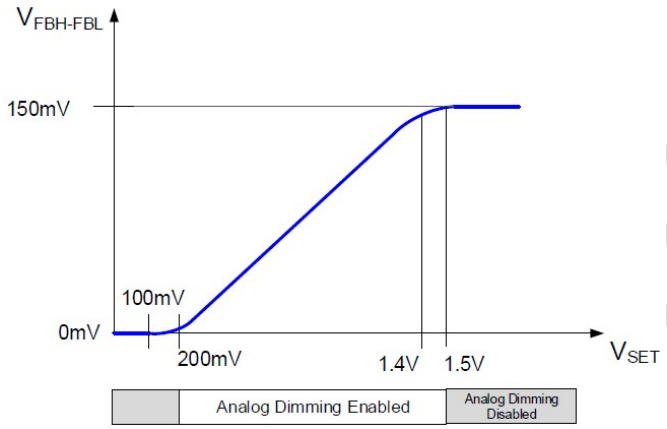


FIG.34 Analog Dimming

Soft Start Setting:

The soft start ramp is defined by a capacitor placed at the Soft_Start pin. Selection of the capacitor can be done according to the following approximate formula. Vss_th_eff is the soft start effectiveness threshold that depends on load condition. Its value is about 0.7 V for the buck mode and 1.4 V for the boost mode

$$TSOFT\_START = C_{SOFT\_START} \cdot \frac{V_{ss\_th\_eff}}{26uA}$$

Layout Example

Following figures are the layout suggestion.

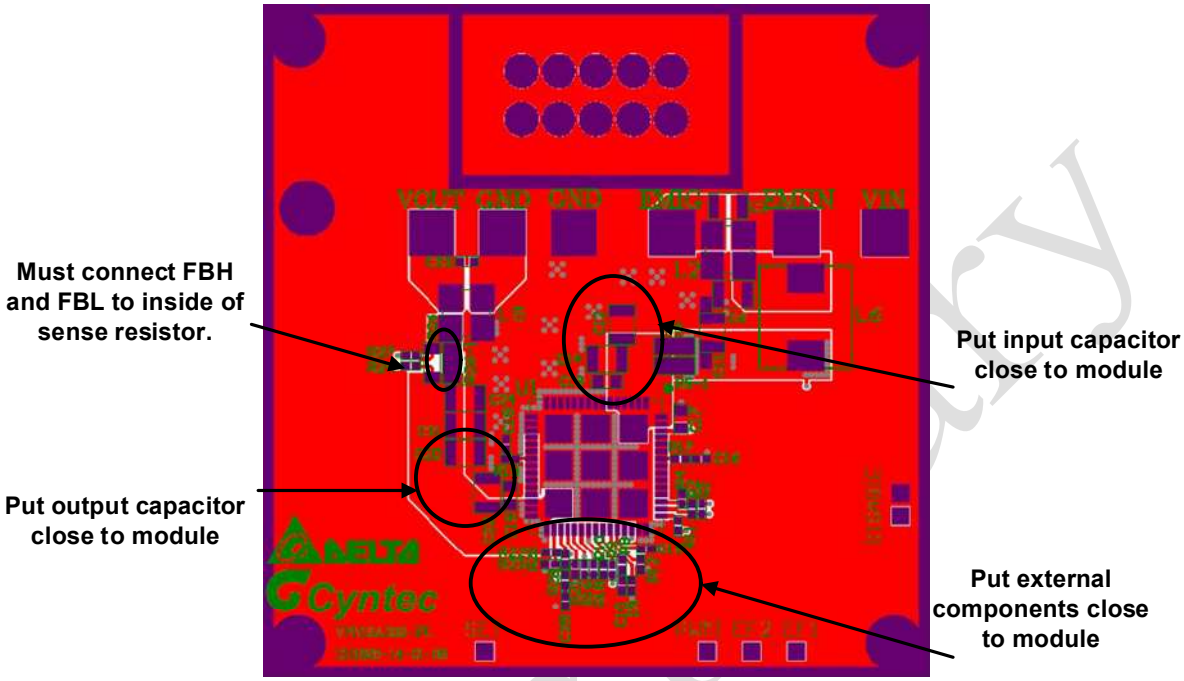


FIG.35 First layer (Top layer)

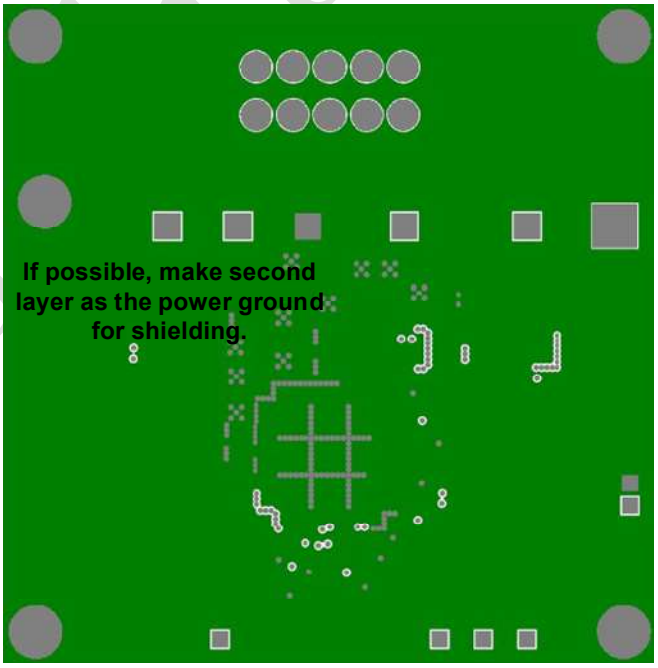


FIG.36 Second layer

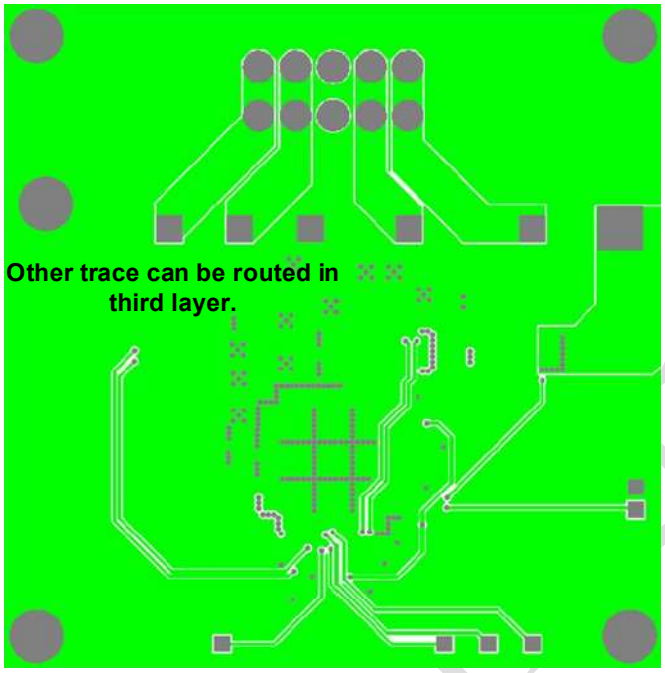


FIG.37 Third layer

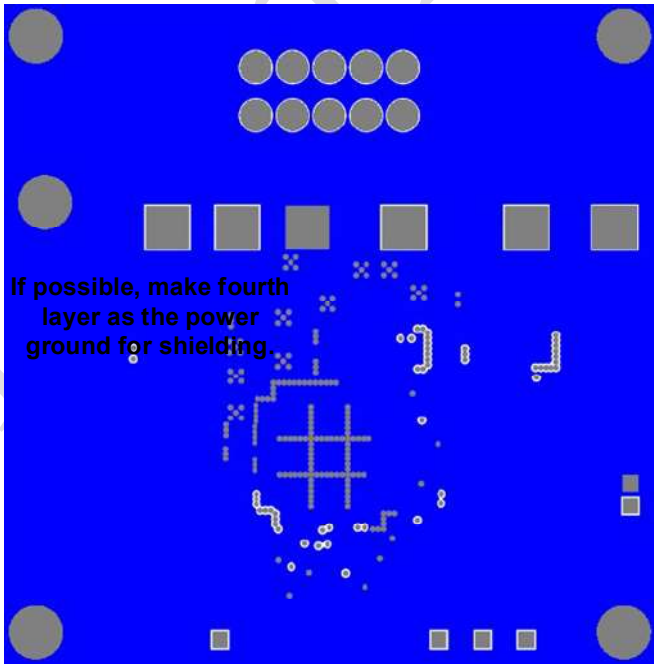


FIG.38 Fourth layer (bottom layer)

REFLOW PARAMETERS:

Lead-free soldering process is a standard of electronic products production. Solder alloys like Sn/Ag, Sn/Ag/Cu and Sn/Ag/Bi are used extensively to replace the traditional Sn/Pb alloy. Sn/Ag/Cu alloy (SAC) is recommended for this power module process. In the SAC alloy series, SAC305 is a very popular solder alloy containing 3% Ag and 0.5% Cu and easy to obtain. Following figure shows an example of the reflow profile diagram. Typically, the profile has three stages. During the initial stage from room temperature to 150°C, the ramp rate of temperature should not be more than 3°C/sec. The soak zone then occurs from 150°C to 200°C and should last for 60 to 120 seconds. Finally, keep at over 217°C for 60 seconds limit to melt the solder and make the peak temperature at the range from 240°C to 250°C. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and one should adopt it for optimization according to various solder type and various manufacturers' formulae.

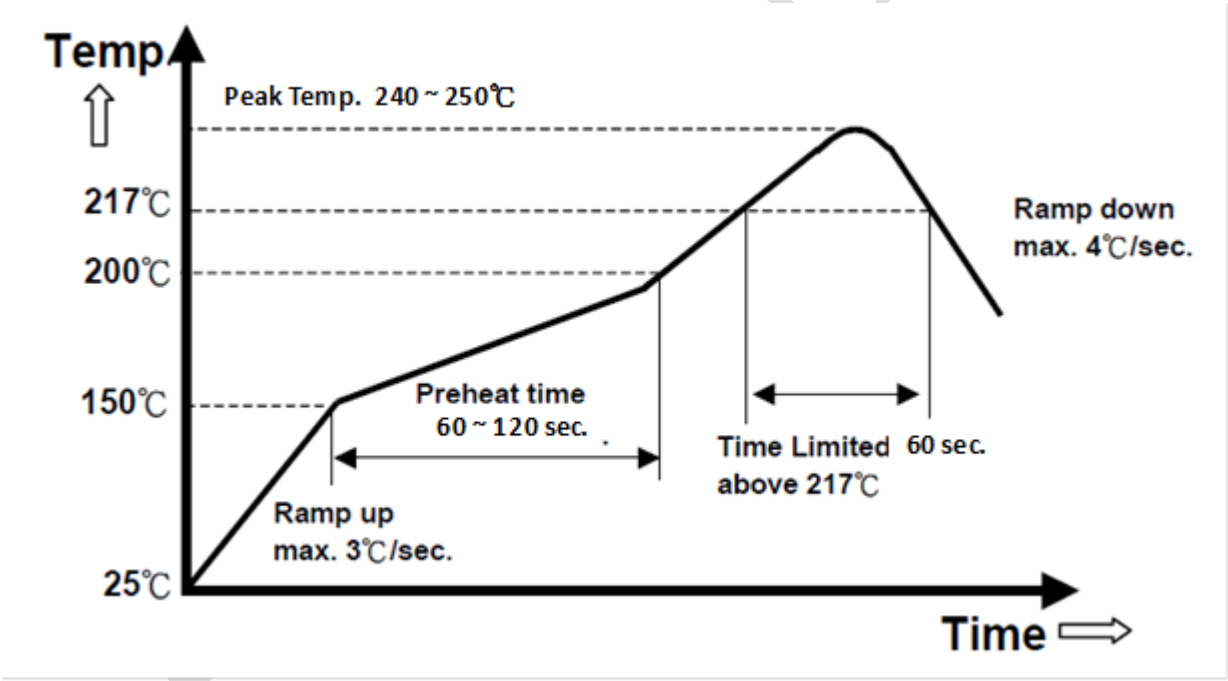
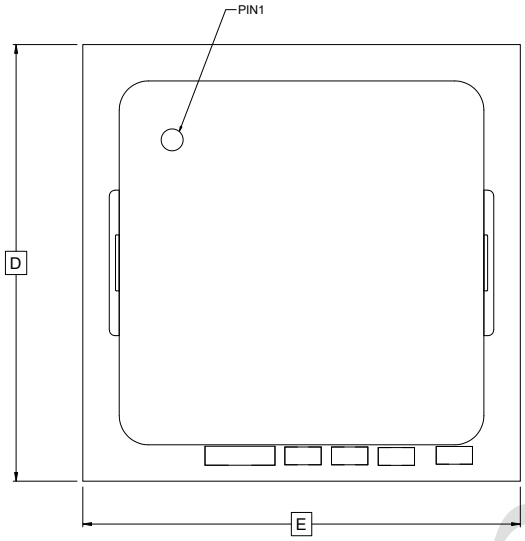


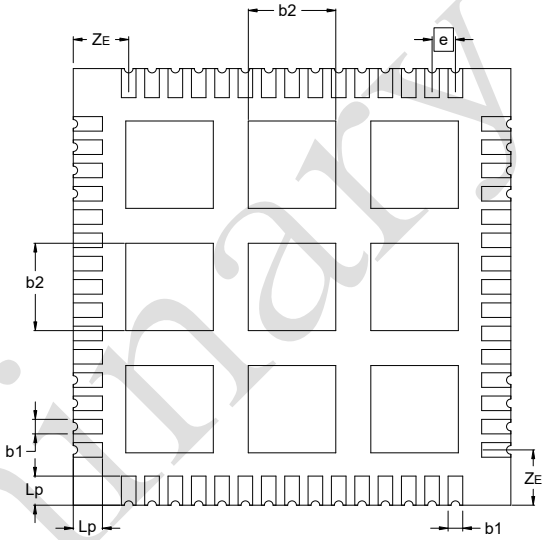
FIG.39 Recommendation Reflow Profile

PACKAGE OUTLINE DRAW:

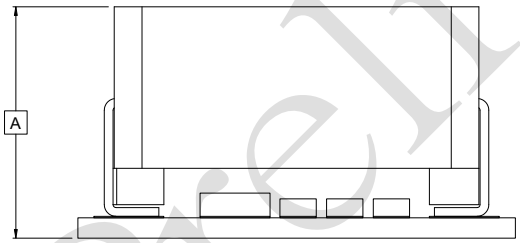
Unit:mm



Top View



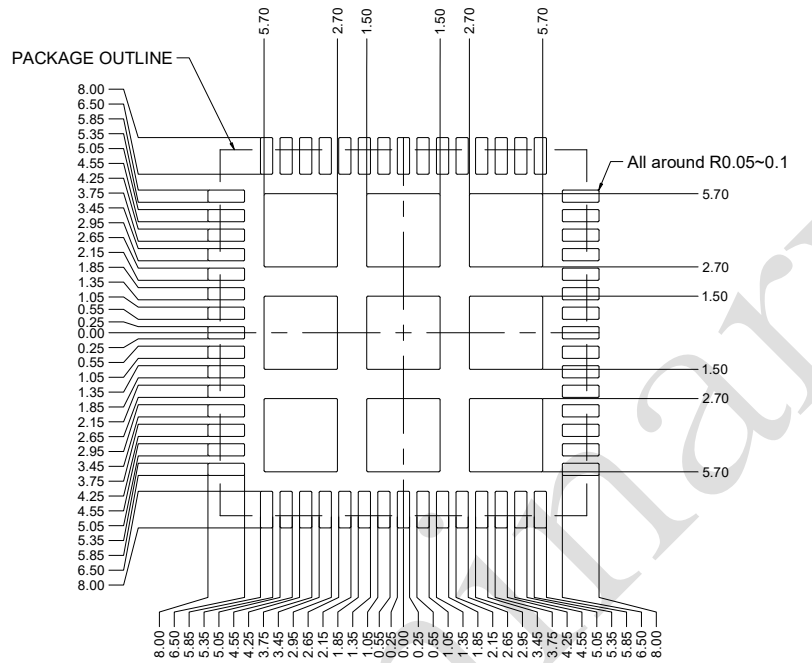
Bottom View



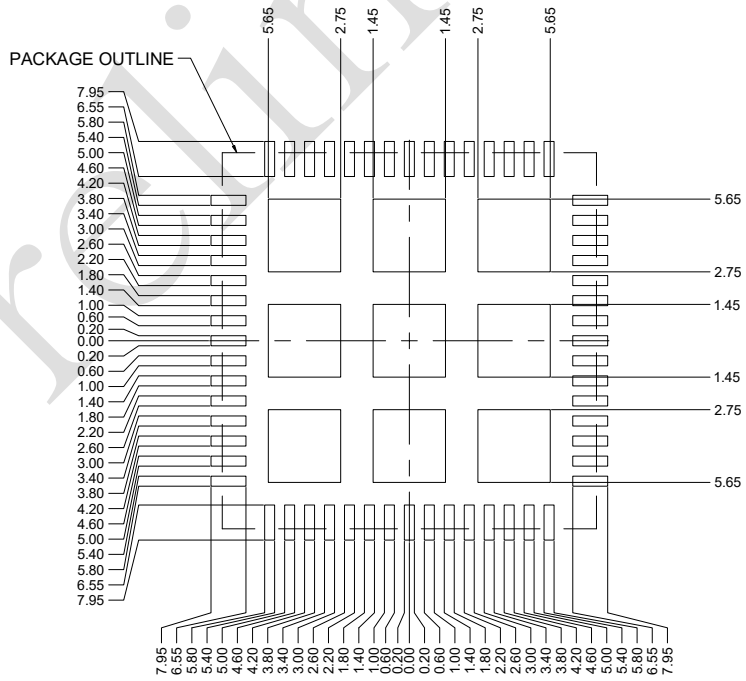
Side View

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	-	-	8.2
D	14.8	15	15.2
E	14.8	15	15.2
e	0.75	0.8	0.85
ZE	1.8	1.9	2.0
Lp	0.95	1.0	1.05
b1	0.45	0.5	0.55
b2	2.95	3.0	3.05

LAND PATTERN REFERENCE:



TOP VIEW.TYPICAL RECOMMENDED LAND PATTERN



TOP VIEW.STENCIL PATTERN WITH SQUARE PADS

REVISION HISTORY:

Date	Revision	Changes
2019.05.13	P00	Release the preliminary spec
2019.05.27	P01	Add the application information and reflow parameters
2019.06.03	P02	Modify the application information and typical performance
2019.06.05	P03	Modify the recommendation operating range
2019.08.14	P04	Modify the pin configuration, the package outline and electrical specification
2019.12.02	P05	Add the constant voltage mode application and reorganize pin 1 place.