RICOH

R5323x SERIES

150mA 2ch LDO REGULATOR

NO.EA-089-0607

OUTLINE

The R5323x Series are CMOS-based voltage regulator ICs with high output voltage accuracy, low supply current, low dropout, and high ripple rejection. Each of these voltage regulator ICs consists of a voltage reference unit, an error amplifier, resistors for setting Output Voltage, a current limit circuit, and a chip enable circuit.

These ICs perform with low dropout voltage due to built-in transistor with low ON resistance, and a chip enable function prolongs the battery life of each system. The line transient response and load transient response of the R5323x Series are excellent, thus these ICs are very suitable for the power supply for hand-held communication equipment.

The output voltage of these ICs is internally fixed with high accuracy. Since the packages for these ICs are SOT-23-6, PLP1820-6 and WL-CSP-6 package, 2ch LDO regulators are included in each package, high density mounting of the ICs on boards is possible.

FEATURES

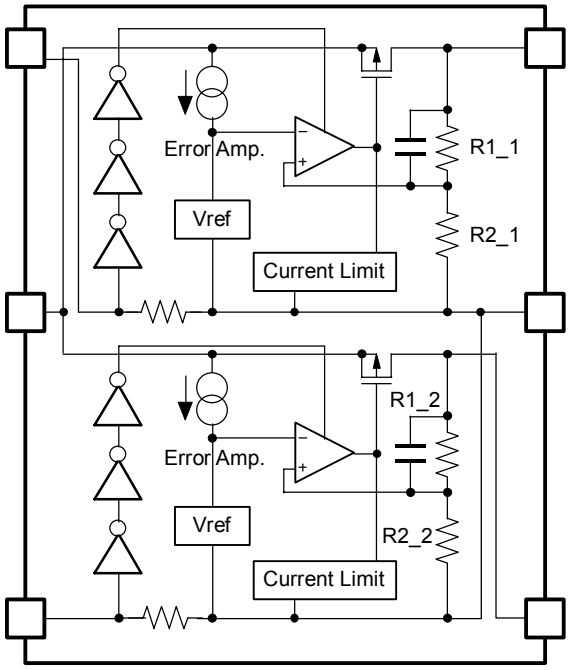
- Low Supply Current ..... Typ. 90μA (VR1, VR2)
- Standby Mode ..... Typ. 0.1μA (VR1, VR2)
- Low Dropout Voltage ..... Typ. 0.22V (I_{OUT}=150mA , Output Voltage Type)
- High Ripple Rejection ..... Typ. 75dB($V_{OUT} \leqq$ 2.4V) , Typ. 70dB($V_{OUT} \leqq$ 2.5V) (f=1kHz)
  Typ. 65dB($V_{OUT} \leqq$ 2.4V) , Typ. 60dB($V_{OUT} \leqq$ 2.5V) (f=10kHz)
- Low Temperature-drift Coefficient of Output Voltage .... Typ. ±100ppm/°C
- Excellent Line Regulation Typ.0.02%/V
- High Output Voltage Accuracy ..... ±2.0%
- Small Packages SOT-23-6, PLP1820-6, WL-CSP-6
- Output Voltage ..... Stepwise setting with a step of 0.1V in the range of 1.5V to 4.0V is possible
- Built-in chip enable circuit (A/B: active high)
- Built-in fold-back protection circuit ..... Typ. 40mA (Current at short mode)
- Ceramic Capacitor is recommended. (1.0μF or more)

APPLICATIONS

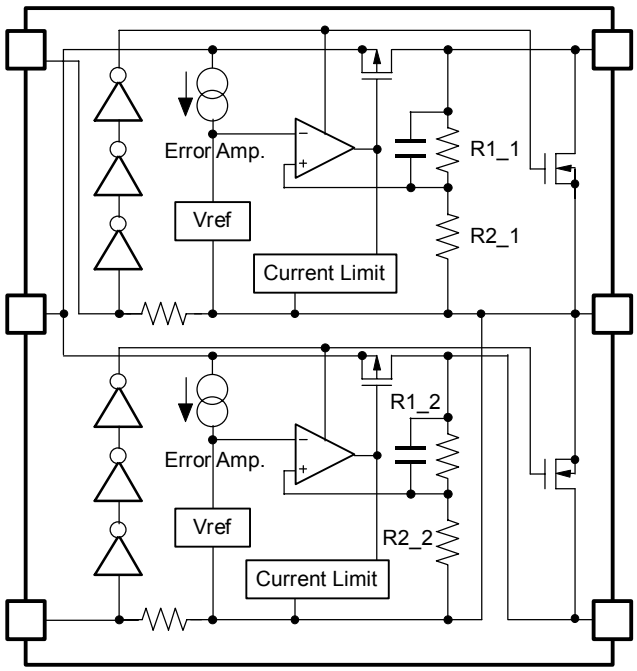
- Power source for handheld communication equipment.
- Power source for electrical appliances such as cameras, VCRs and camcorders.
- Power source for battery-powered equipment.

BLOCK DIAGRAMS

R5323xxxxA



R5323xxxxB



SELECTION GUIDE

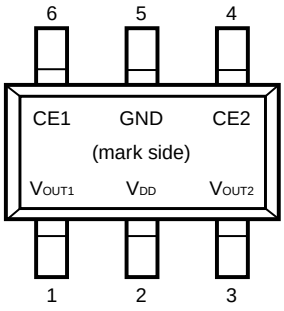
The output voltage, mask option, and the taping type for the ICs can be selected at the user's request. The selection can be made with designating the part number as shown below;

R5323xxxxx-xx-x ←Part Number
↑ ↑ ↑ ↑ ↑
a b c d e

Code	Contents
a	Designation of Package Type: N : SOT-23-6 K : PLP1820-6 Z : WL-CSP-6
b	Setting combination of 2ch Output Voltage (V_{OUT}) : Serial Number for Voltage Setting, Stepwise setting with a step of 0.1V in the range of 1.5V to 4.0V is possible for each channel.
c	Designation of Mask Option: A version: without auto discharge function at OFF state. B version: with auto discharge function at OFF state.
d	Designation of Taping Type: Ex. TR (refer to Taping Specifications; TR type is the standard direction.)
e	Designation of composition of plating: –F : Lead free plating (SOT-23-5,WL-CSP-6) None : Au plating (PLP1820-6)

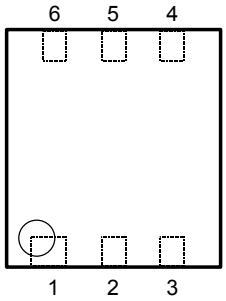
PIN CONFIGURATION

- **SOT-23-6**

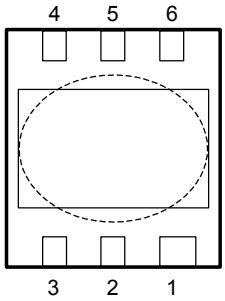


- **PLP1820-6**

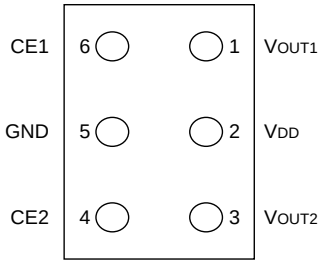
Top View



Bottom View



- **WLCSP-6**



PIN DESCRIPTIONS

- **SOT-23-6**

Pin No.	Symbol	Description
1	V_{OUT1}	Output Pin 1
2	V_{DD}	Input Pin
3	V_{OUT2}	Output Pin 2
4	CE2	Chip Enable Pin 2
5	GND	Ground Pin
6	CE1	Chip Enable Pin 1

PLP1820-6

Pin No.	Symbol	Description
1	V_{OUT2}	Output Pin 2
2	V_{DD}	Input Pin
3	V_{OUT1}	Output Pin 1
4	GND	Ground Pin
5	CE1	Chip Enable Pin 1
6	CE2	Chip Enable Pin 2

* Tab in the ◌ parts have GND level.
(They are connected to the reverse side of this IC.)
Do not connect to other wires or land patterns.

- **WLCSP-6**

Pin No.	Symbol	Description
1	V_{OUT1}	Output Pin 1
2	V_{DD}	Input Pin
3	V_{OUT2}	Output Pin 2
4	CE2	Chip Enable Pin 2
5	GND	Ground Pin
6	CE1	Chip Enable Pin 1

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	6.5	V
V_{CE}	Input Voltage (CE Pin)	6.5	V
V_{OUT}	Output Voltage	−0.3 to V_{IN} + 0.3	V
I_{OUT1}	Output Current 1	200	mA
I_{OUT2}	Output Current 2	200	mA
P_D	Power Dissipation (SOT-23-6)*1	420	mW
	Power Dissipation (PLP1820-6) *1	880	
	Power Dissipation (WL-CSP-6)	633	
Topt	Operating Temperature Range	−40 to 85	°C
Tstg	Storage Temperature Range	−55 to 125	°C

∗1 For Power Dissipation, please refer to PACKAGE INFORMATION to be described.

ELECTRICAL CHARACTERISTICS

- **R5323xxxxA/B**

Topt=25°C

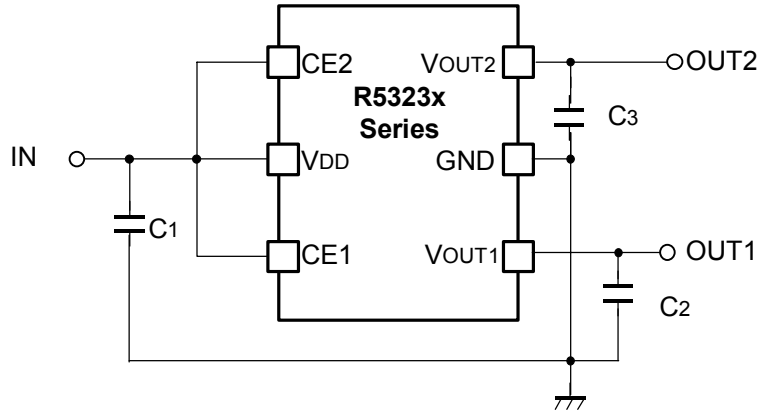
Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{OUT}	Output voltage	V_{IN}=Set V_{OUT}+1V 1mA ≦ I_{OUT} ≦ 30mA	V_{OUT} ×0.98		V_{OUT} ×1.02	V
I_{OUT}	Output Current	V_{IN}–V_{OUT} = 1.0V	150			mA
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	V_{IN}=Set V_{OUT}+1V 1mA ≦ I_{OUT} ≦ 150mA		15	40	mV
V_{DIF}	Dropout Voltage	Refer to the Electrical Characteristics by Output Voltage				
I_{SS}	Supply Current	V_{IN}=Set V_{OUT}+1V		90	120	μA
Istandby	Supply Current(Standby)	V_{IN}=Set V_{OUT}+1V V_{CE}=GND		0.1	1.0	μA
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	Set V_{OUT}+0.5V ≦ V_{IN} ≦ 6.0V I_{OUT}=30mA		0.02	0.10	%/V
RR	Ripple Rejection	Ripple 0.5Vp–p V_{IN}=Set V_{OUT}+1V I_{OUT}=30mA (In case that V_{OUT} ≦ 1.7V, V_{IN}=Set V_{OUT}+1.2V)		75 ∗Note1 65 ∗Note2		dB
V_{IN}	Input Voltage		2.0		6.0	V
ΔV_{OUT}/ ΔTopt	Output Voltage Temperature Coefficient	I_{OUT}=30mA –40°C ≦ Topt ≦ 85°C		±100		ppm /°C
Ilim	Short Current Limit	V_{OUT}=0V		40		mA
R_{PD}	Pull-down resistance for CE pin		0.7	2.0	8.0	MΩ
V_{CEH}	CE Input Voltage “H”		1.5		6.0	V
V_{CEL}	CE Input Voltage “L”		0.0		0.3	V
en	Output Noise	BW=10Hz to 100kHz		30		μVrms
R_{LOW}	Low Output Nch Tr. ON Resistance (of B version)	V_{CE}=0V		60		Ω

∗Note1: f=1kHz, 70dB as to V_{OUT} ≧ 2.5V Output type.
∗Note2: f=10kHz, 60dB as to V_{OUT} ≧ 2.5V Output type.

- **Electrical Characteristics by Output Voltage**

Output Voltage V_{OUT} (V)	Dropout Voltage V_{DIF} (V)		
	Condition	Typ.	Max.
V_{OUT}=1.5	I_{OUT}=150mA	0.38	0.70
V_{OUT}=1.6		0.35	0.65
V_{OUT}=1.7		0.33	0.60
1.8V ≦ V_{OUT} ≦ 2.0V		0.32	0.55
2.1V ≦ V_{OUT} ≦ 2.7V		0.28	0.50
2.8V ≦ V_{OUT} ≦ 4.0V		0.22	0.35

TYPICAL APPLIATION



(External Components)
Ceramic Capacitor Type C_1,C_2,C_3
Recommended Ceramic capacitor for Output: GRM219R61A105K (Murata)
General Example of External Components
Ceramic Capacitors: C1608X5R0J105K (TDK)
GRM188R60J105K (Murata)

TEST CIRCUIT

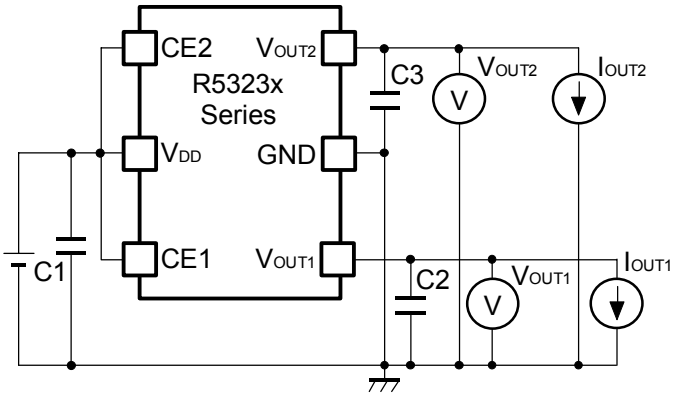


Fig.1 Standard test Circuit

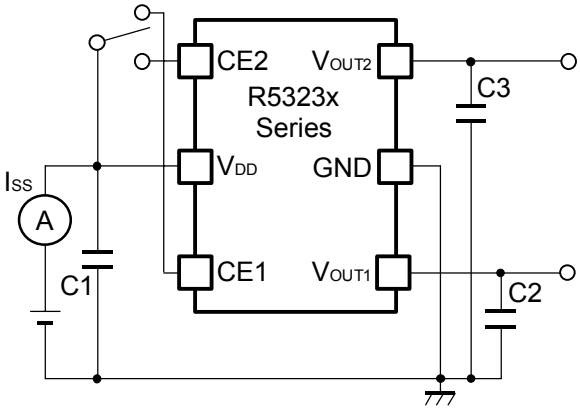


Fig.2 Supply Current Test Circuit

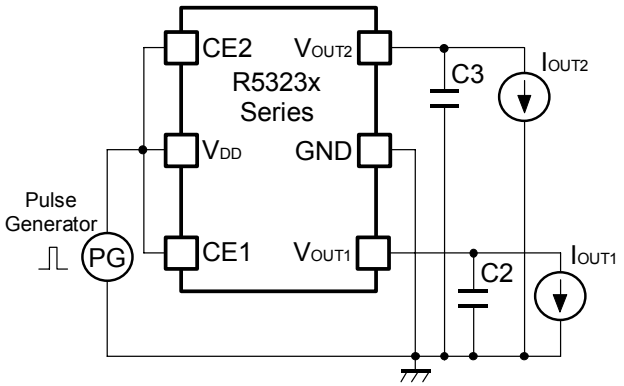


Fig.3 Ripple Rejection, Line Transient Response Test Circuit

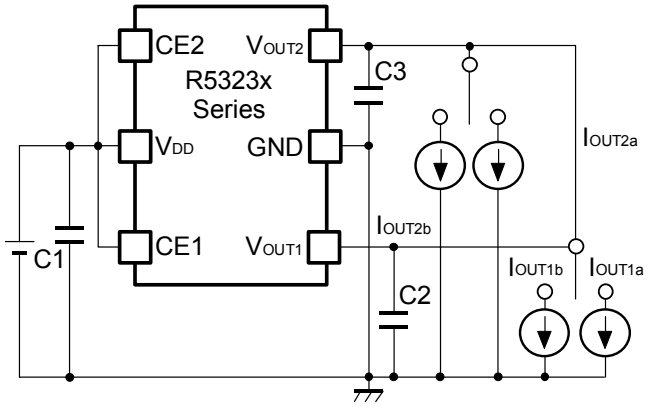
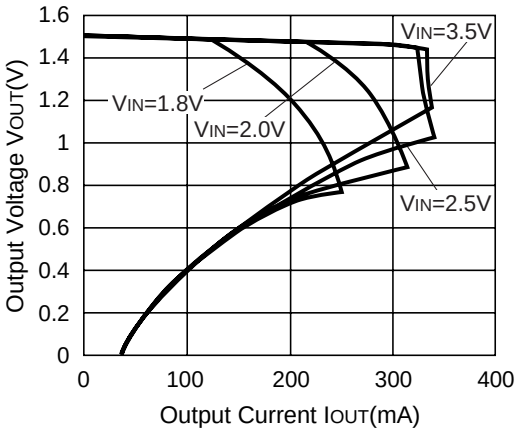


Fig.4 Load Transient Response Test Circuit

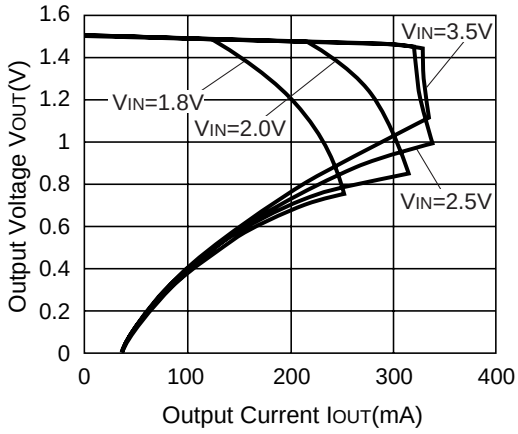
TYPICAL CHARACTERISTICS

1) Output Voltage vs. Output Current (Topt=25°C)

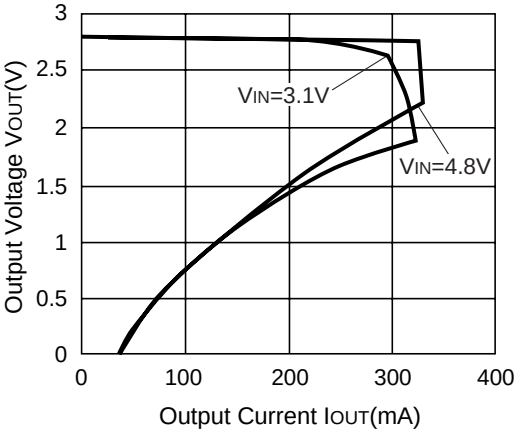
1.5V (VR1)



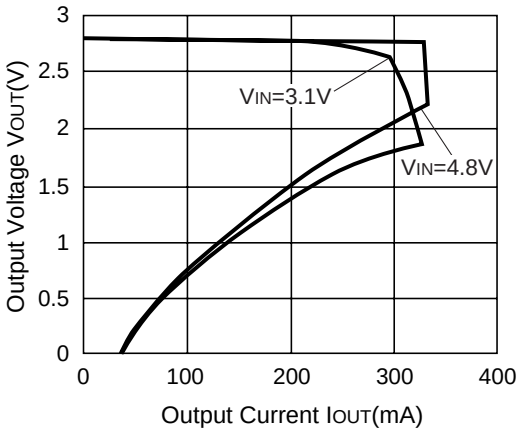
1.5V (VR2)



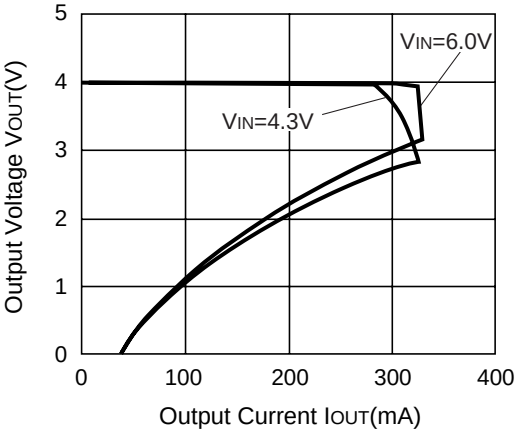
2.8V (VR1)



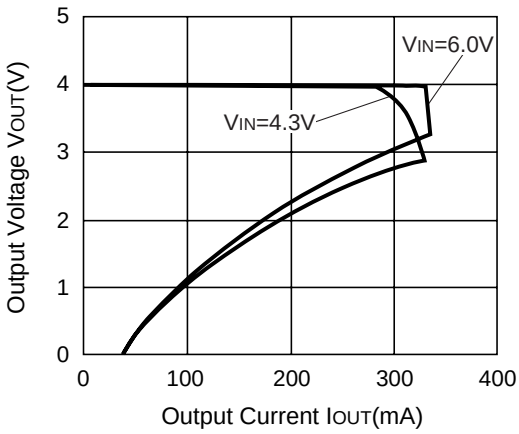
2.8V (VR2)



4.0V (VR1)

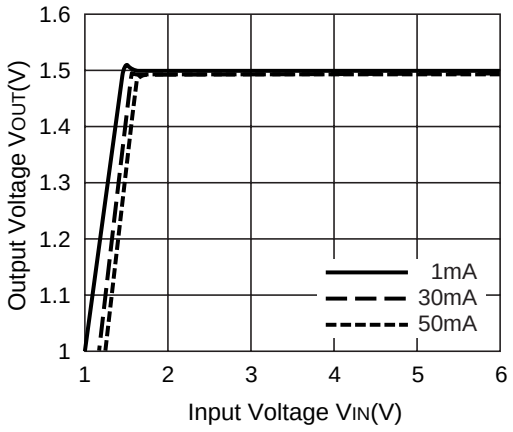


4.0V (VR2)

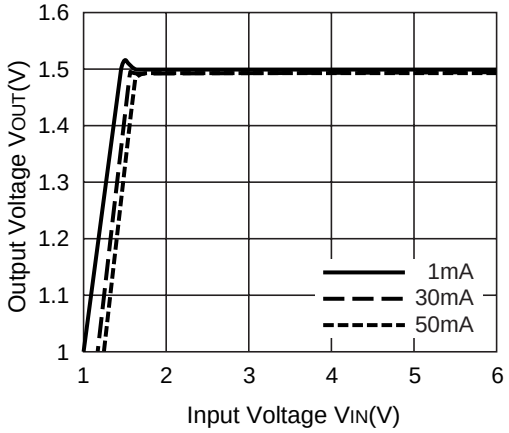


2) Output Voltage vs. Input Voltage (Topt=25°C)

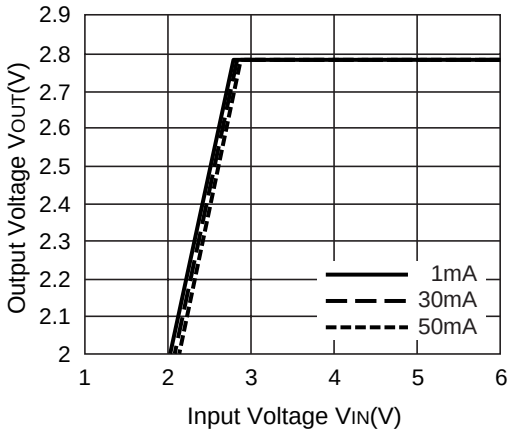
1.5V (VR1)



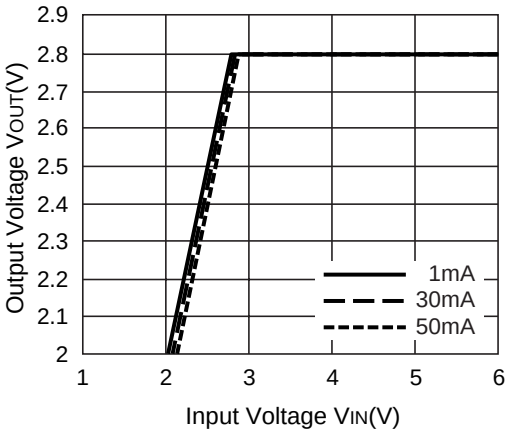
1.5V (VR2)



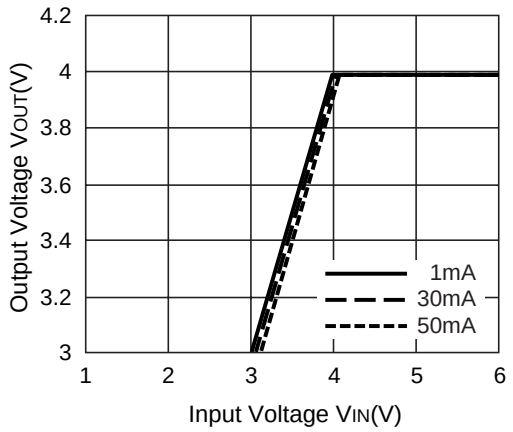
2.8V (VR1)



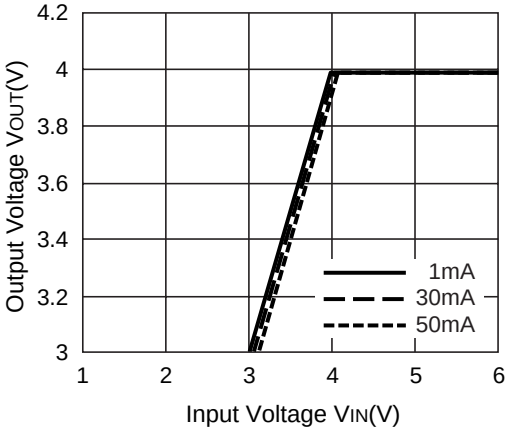
2.8V (VR2)



4.0V (VR1)

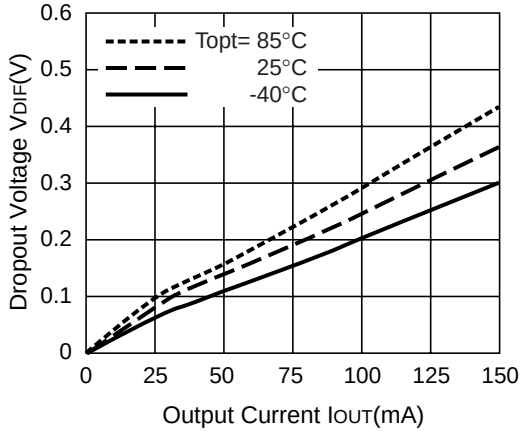


4.0V (VR2)

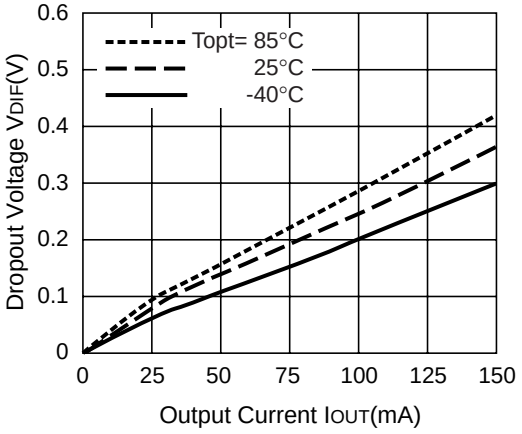


3) Dropout Voltage vs. Temperature

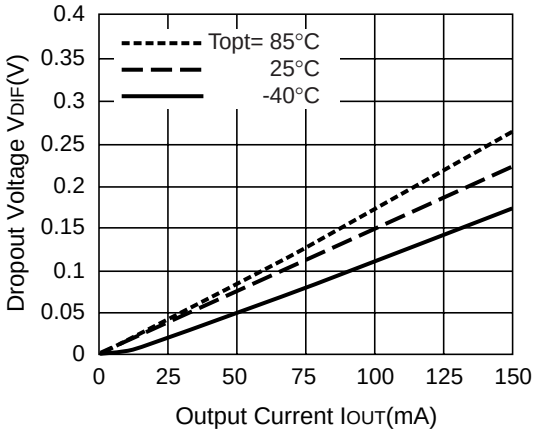
1.5V (VR1)



1.5V (VR2)



2.8V (VR1)



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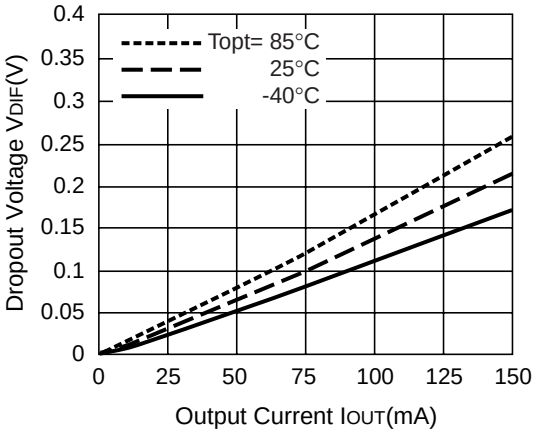
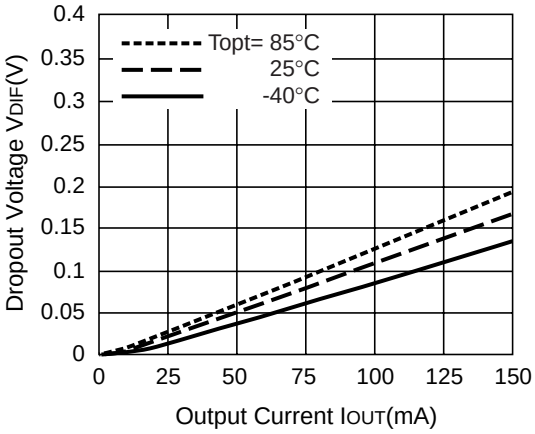
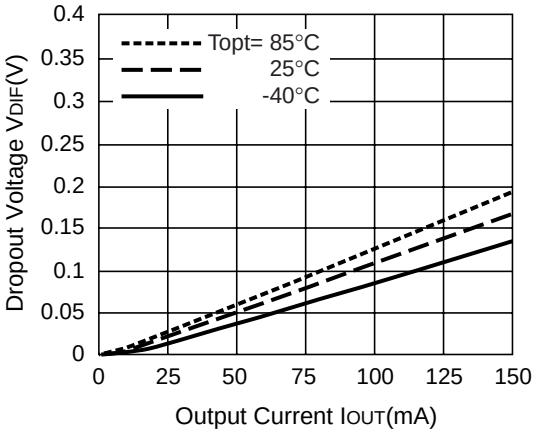


4.0V (VR1)

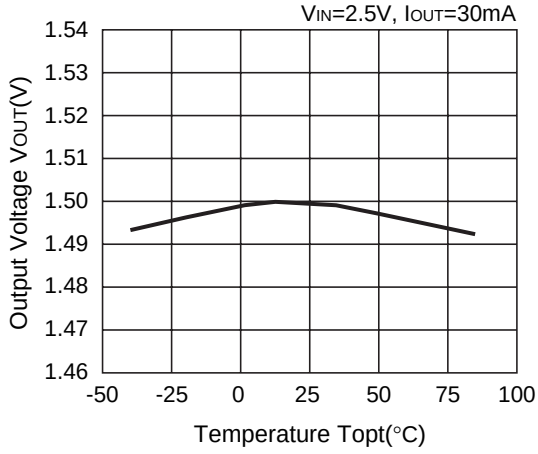


4.0V (VR2)

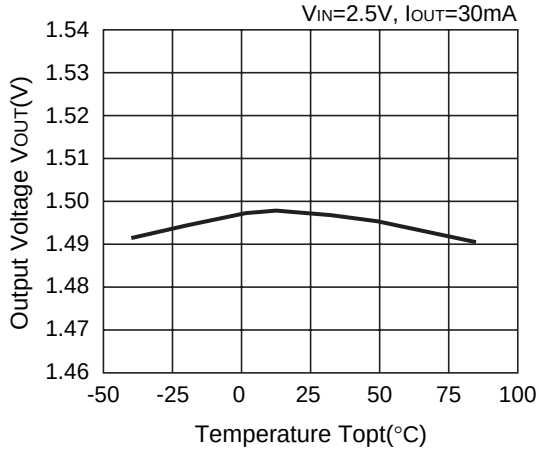


4) Output Voltage vs. Temperature

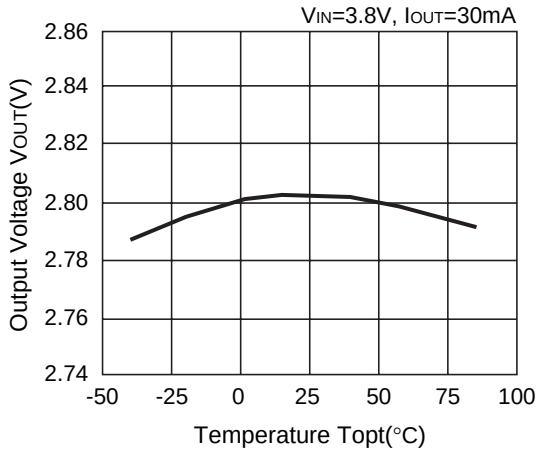
1.5V (VR1)



1.5V (VR2)



2.8V (VR1)



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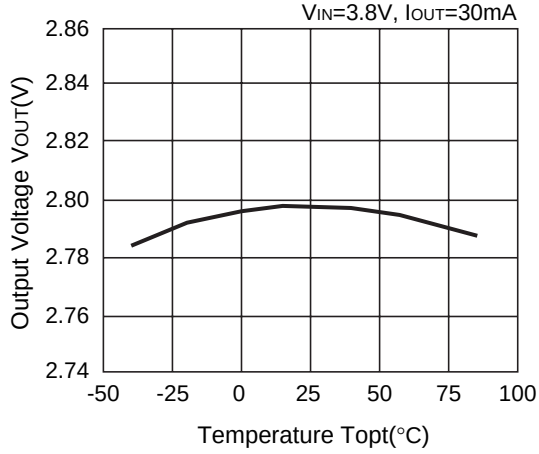
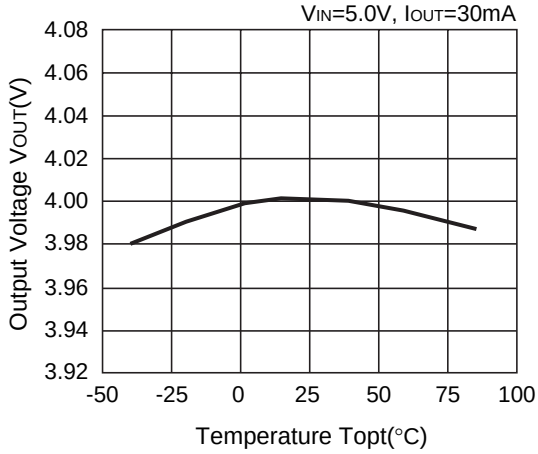
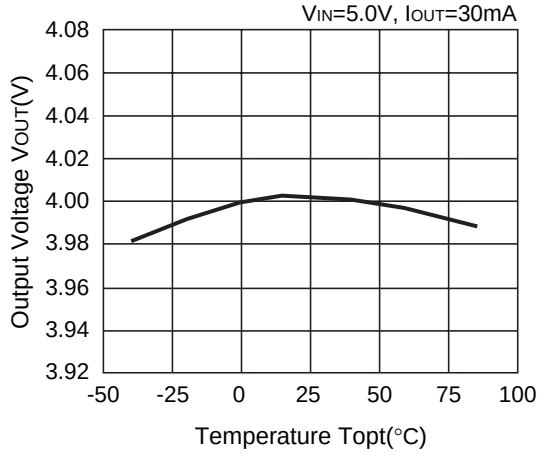


4.0V (VR1)

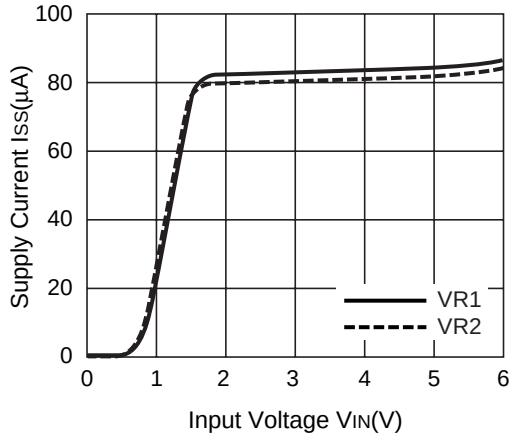


4.0V (VR2)

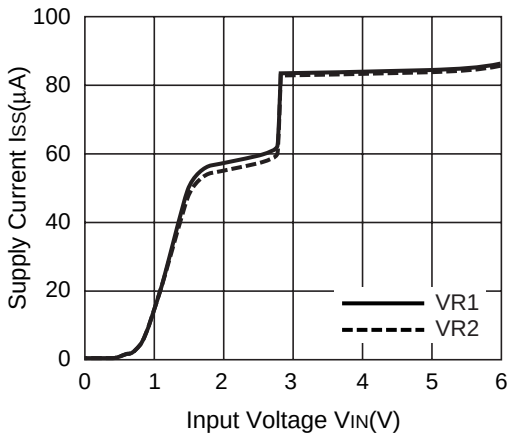


5) Supply Current vs. Input Voltage (Topt=25°C)

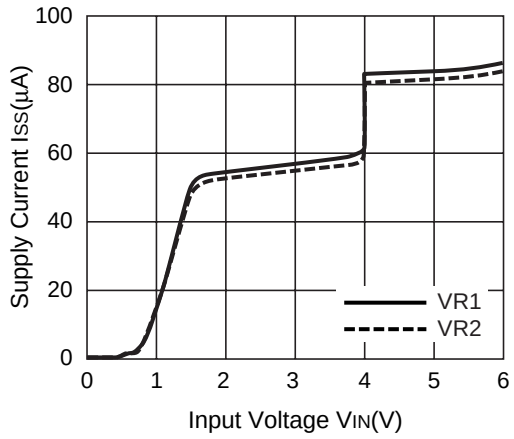
1.5V



2.8V

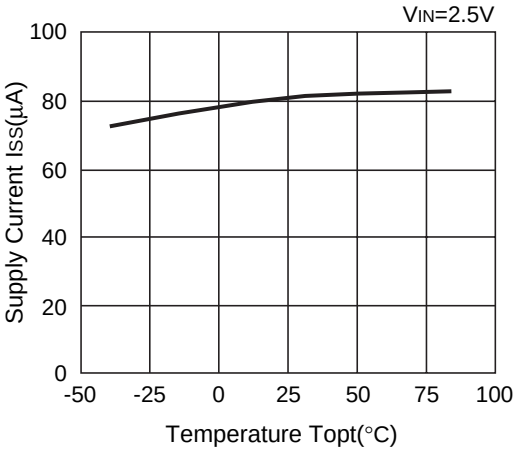


4.0V

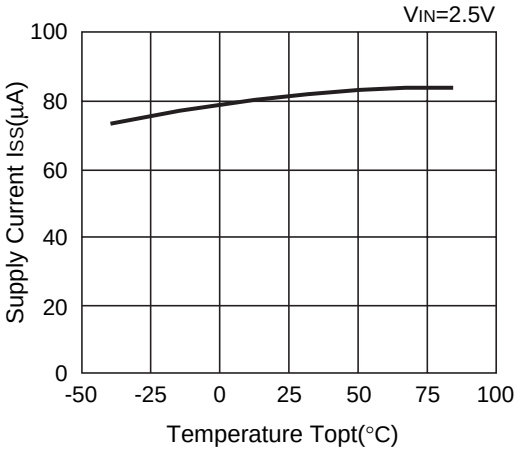


6) Supply Current vs. Temperature

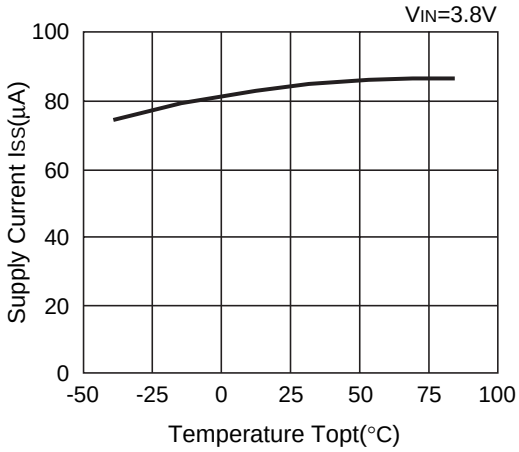
1.5V (VR1)



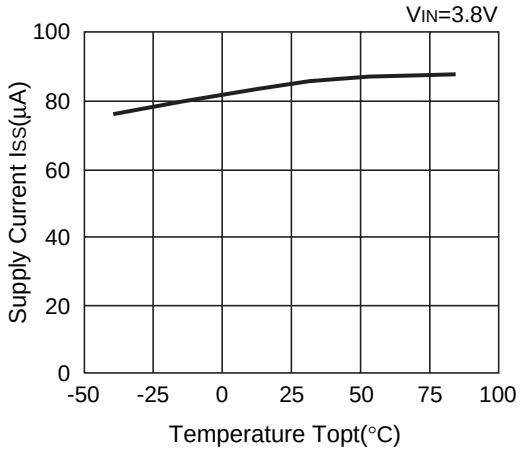
1.5V (VR2)



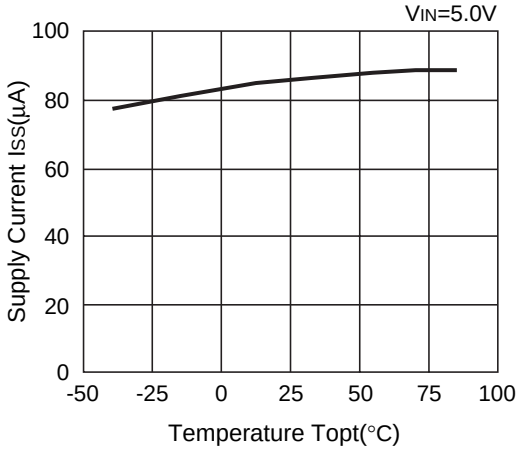
2.8V (VR1)



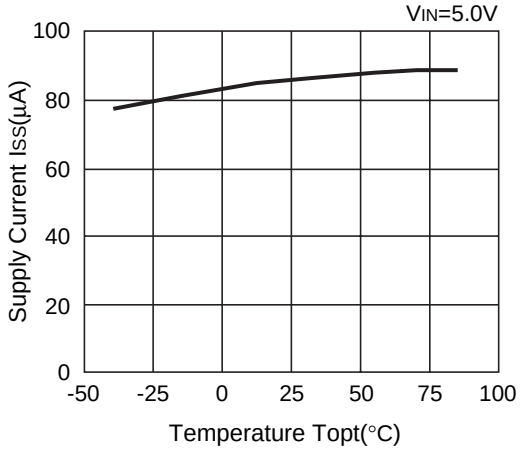
2.8V (VR2)



4.0V (VR1)

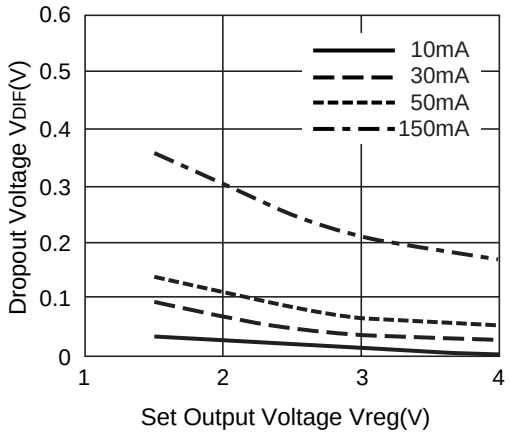


4.0V (VR2)

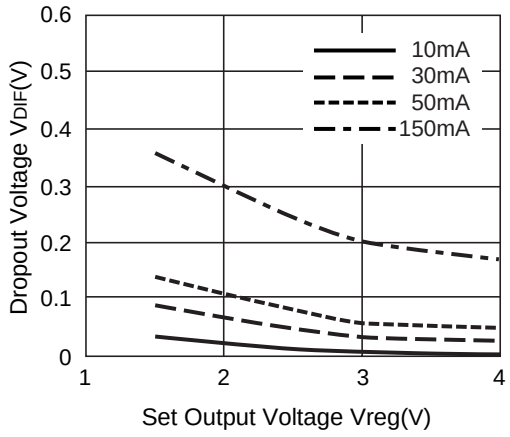


7) Dropout Voltage vs. Set Output Voltage (Topt=25°C)

VR1

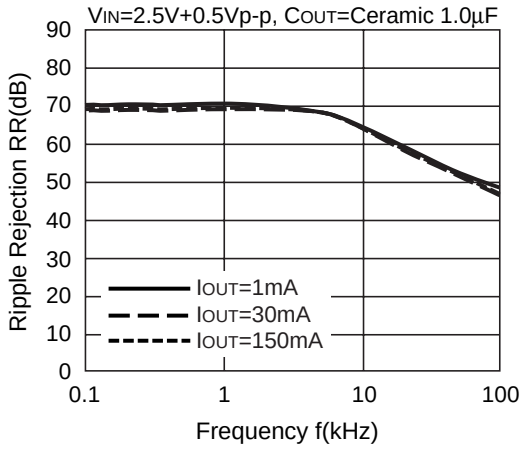


VR2

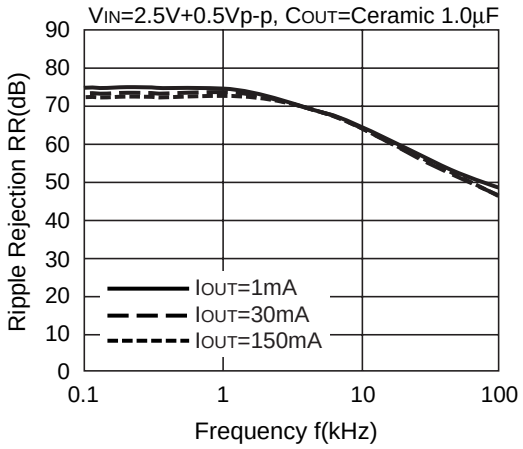


8) Ripple Rejection vs. Frequency (Topt=25°C)

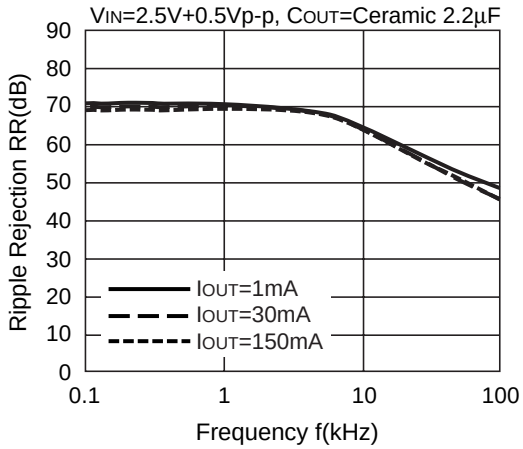
1.5V (VR1)



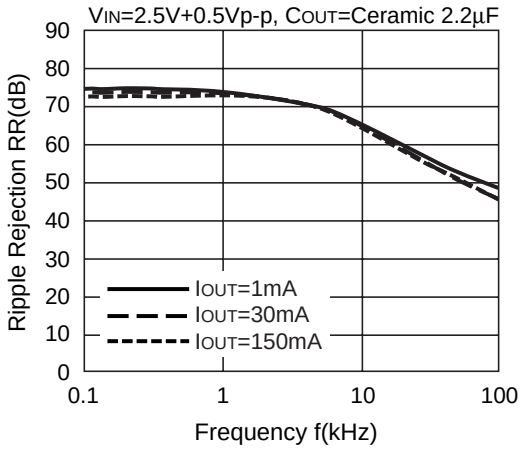
1.5V (VR2)



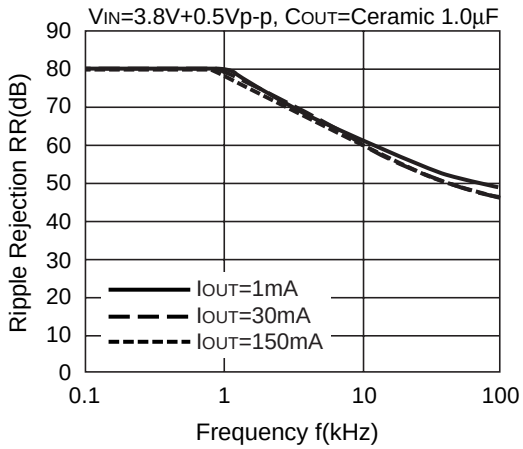
1.5V (VR1)



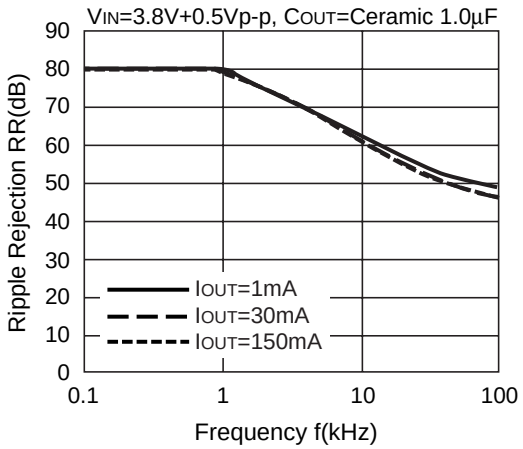
1.5V (VR2)



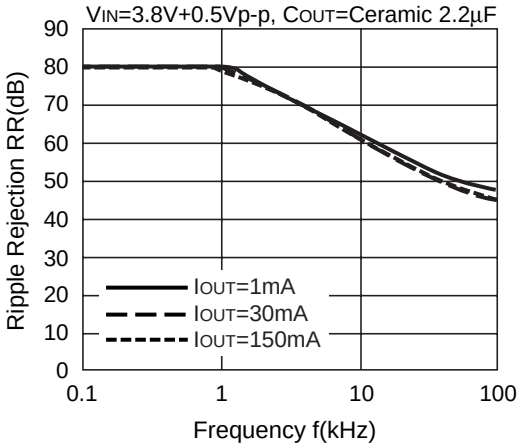
2.8V (VR1)



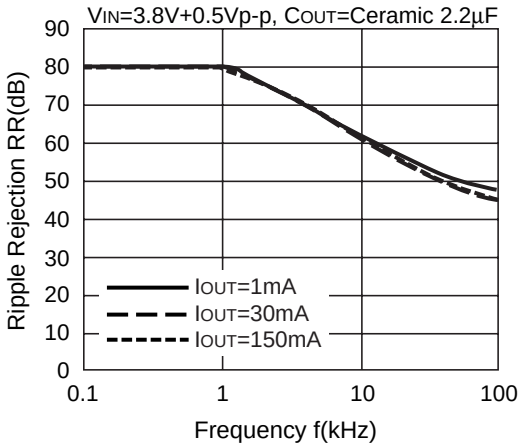
2.8V (VR2)



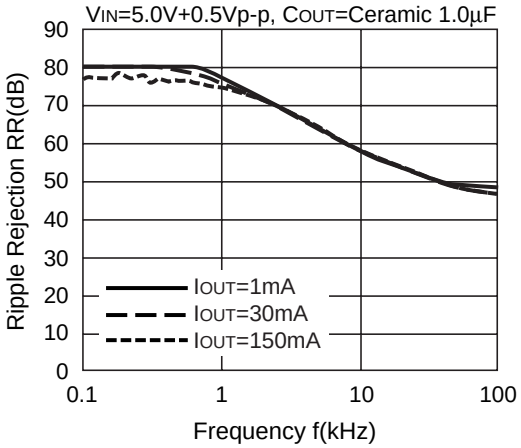
2.8V (VR1)



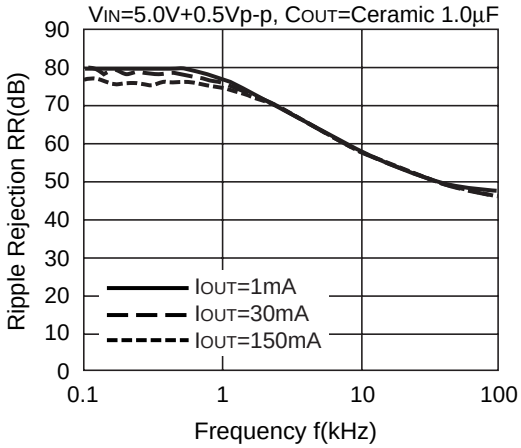
2.8V (VR2)



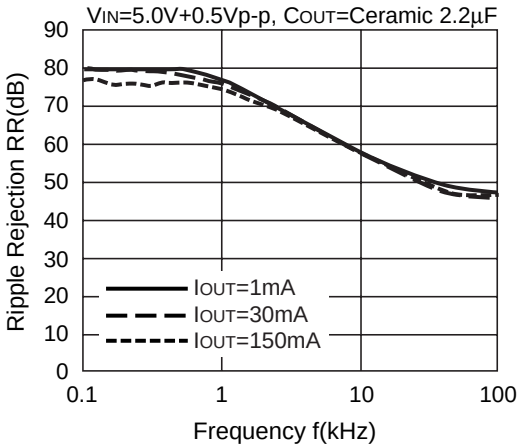
4.0V (VR1)



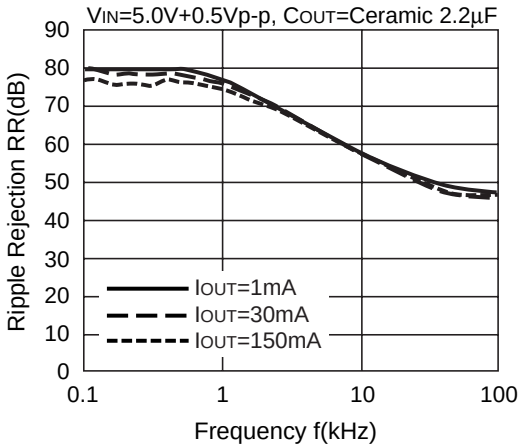
4.0V (VR2)



4.0V (VR1)

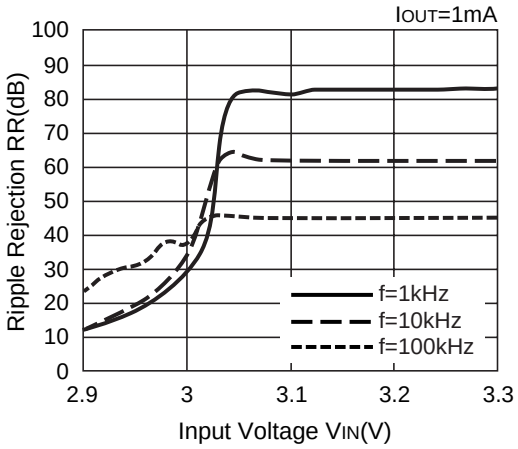


4.0V (VR2)

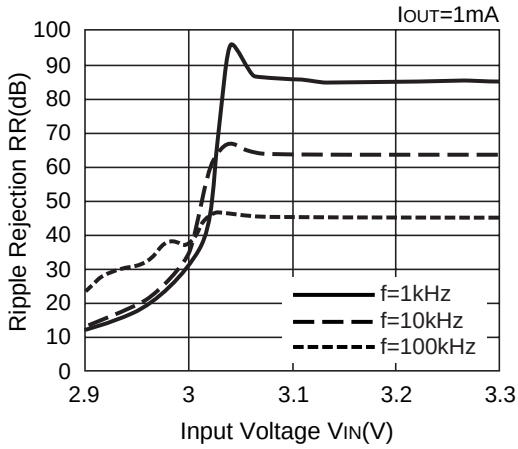


9) Ripple Rejection vs. Input Voltage (DC bias) C_{OUT} = Ceramic 1.0μF (Topt=25°C)

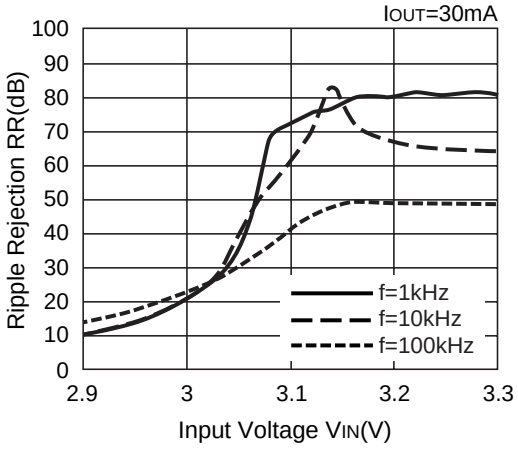
2.8V (VR1)



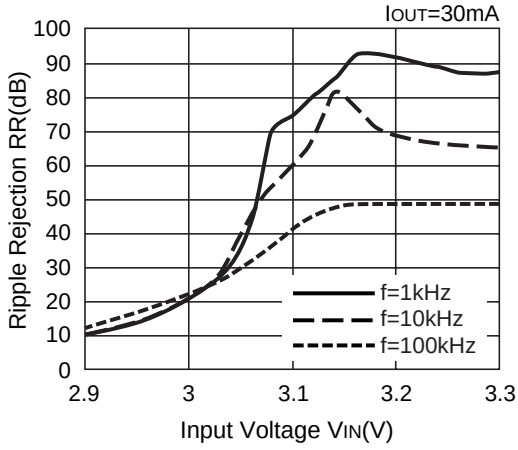
2.8V (VR2)



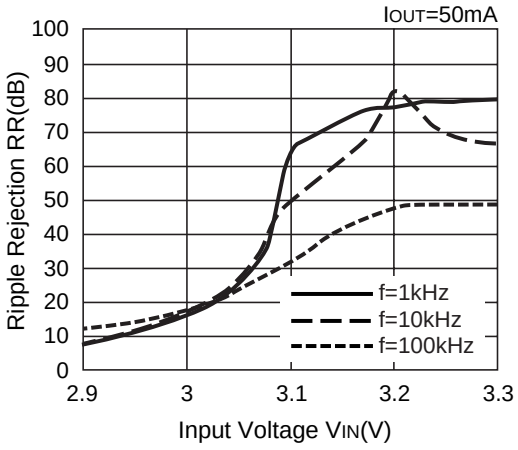
2.8V (VR1)



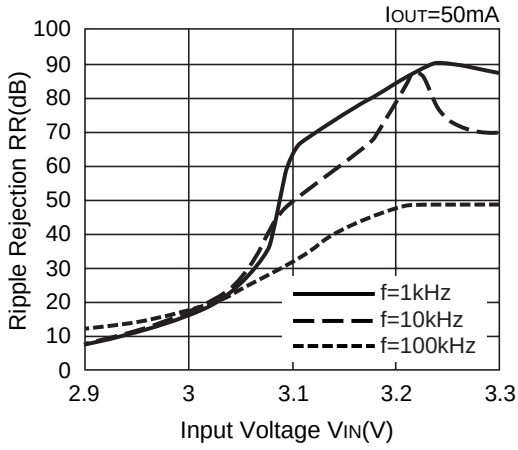
2.8V (VR2)



2.8V (VR1)



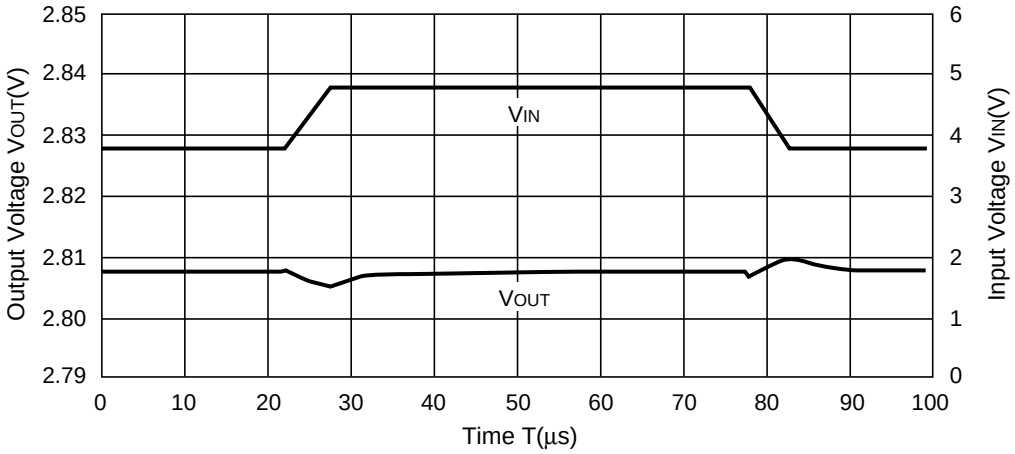
2.8V (VR2)



10) Input Transient Response

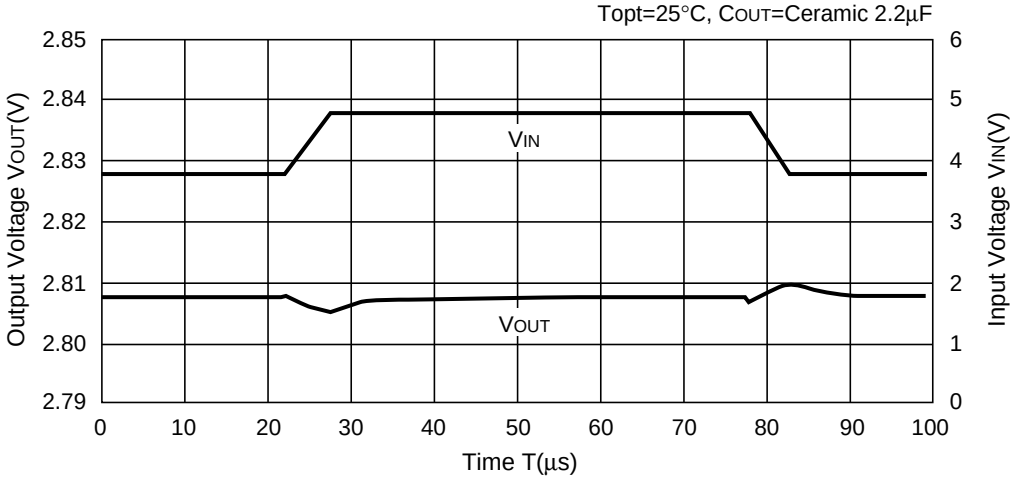
R5323N001x(2.8V, VR1)

I_{OUT}=30mA, tr=tf=5µs, C_{OUT}=Ceramic 1.0µF



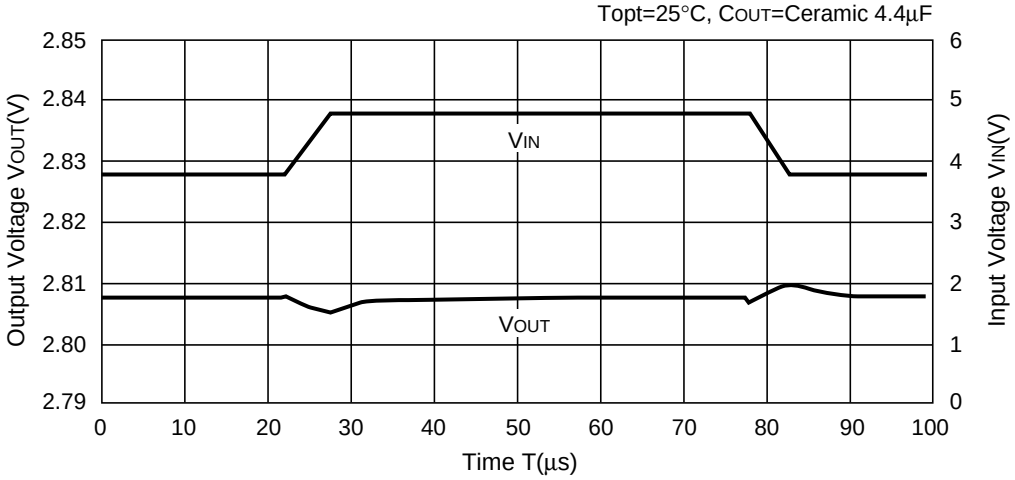
R5323N001x(2.8V, VR1)

Topt=25°C, C_{OUT}=Ceramic 2.2µF



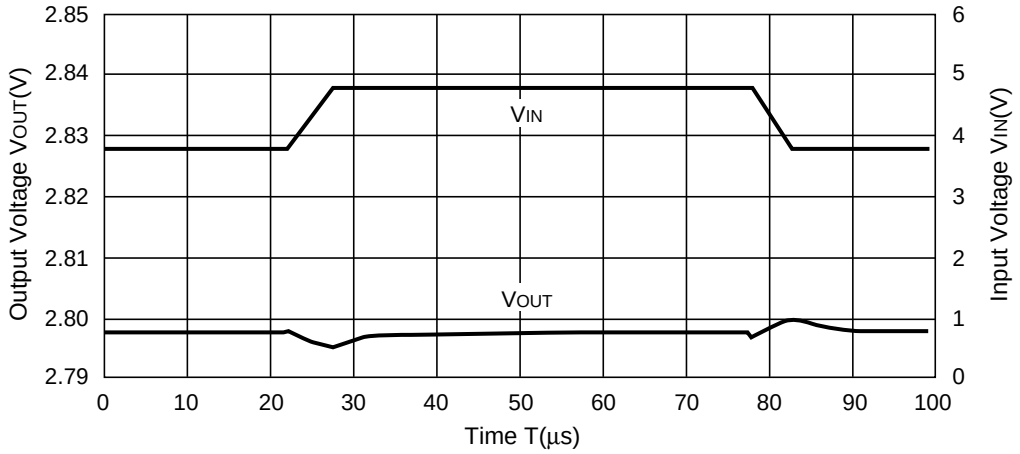
R5323N001x(2.8V, VR1)

Topt=25°C, C_{OUT}=Ceramic 4.4µF



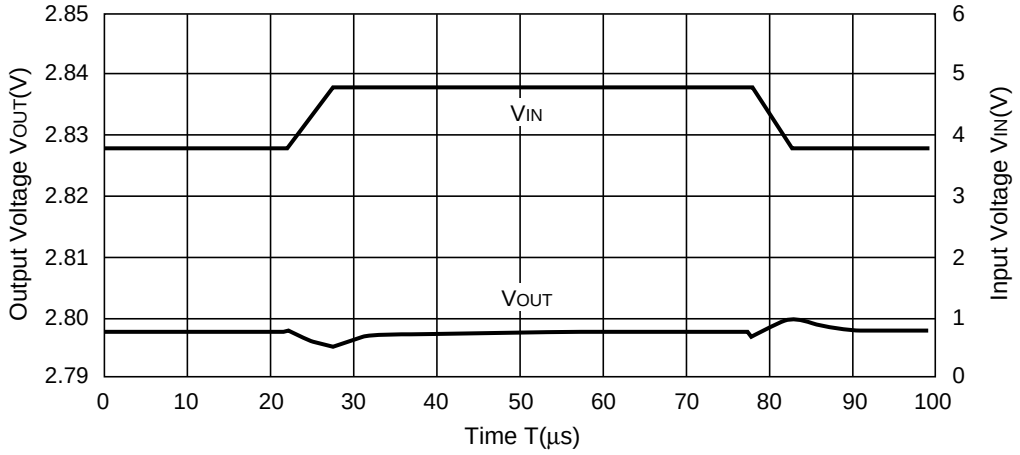
R5323N001x(2.8V, VR2)

Topt=25°C, COUT=Ceramic 1.0µF



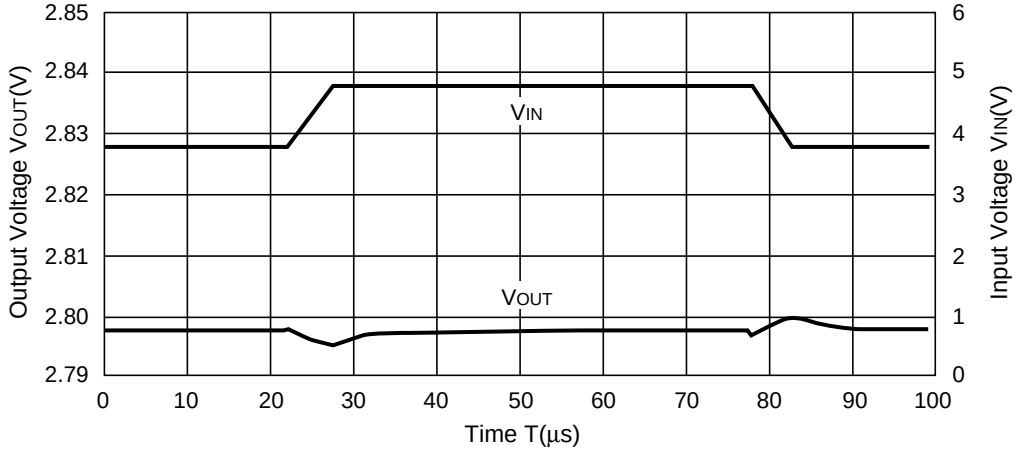
R5323N001x(2.8V, VR2)

Topt=25°C, COUT=Ceramic 2.2µF



R5323N001x(2.8V, VR2)

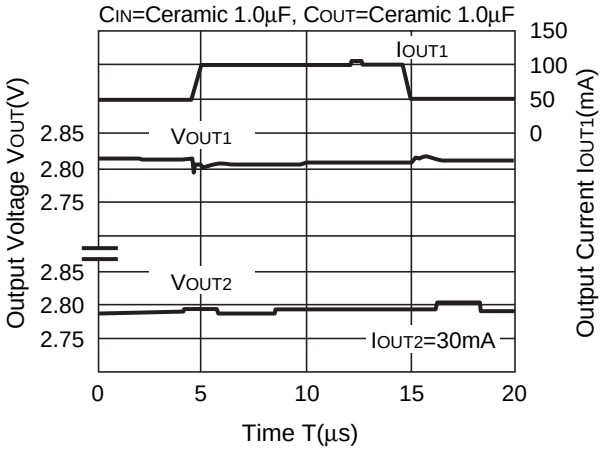
Topt=25°C, COUT=Ceramic 4.4µF



11) Load Transient Response

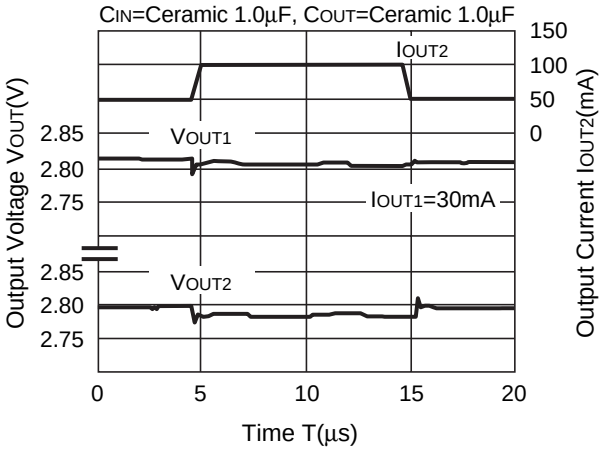
2.8V (VR1)

CIN=Ceramic 1.0µF, COUT=Ceramic 1.0µF



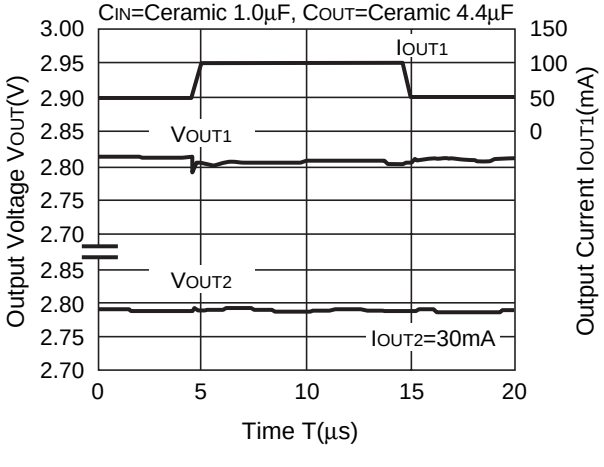
2.8V (VR2)

CIN=Ceramic 1.0µF, COUT=Ceramic 1.0µF



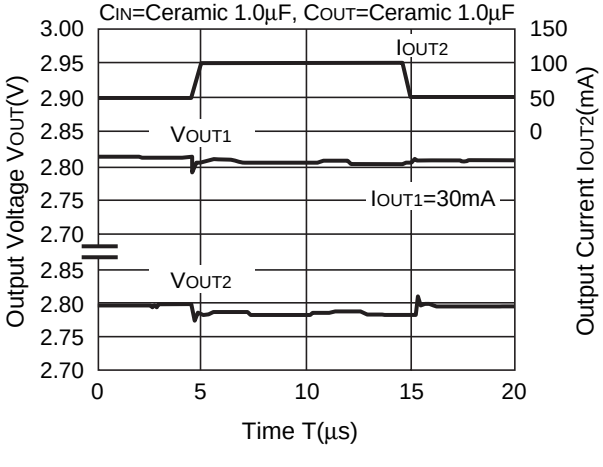
2.8V (VR1)

CIN=Ceramic 1.0µF, COUT=Ceramic 4.4µF



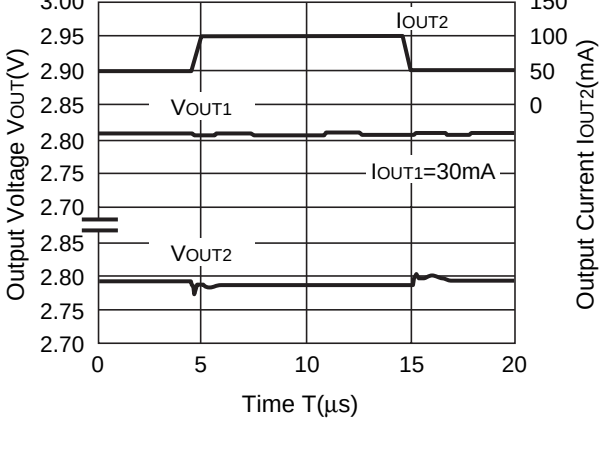
2.8V (VR2)

CIN=Ceramic 1.0µF, COUT=Ceramic 1.0µF



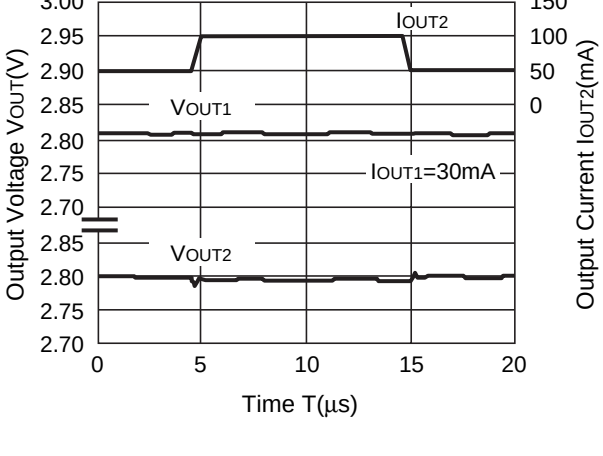
2.8V (VR2)

CIN=Ceramic 1.0µF, COUT=Ceramic 2.2µF



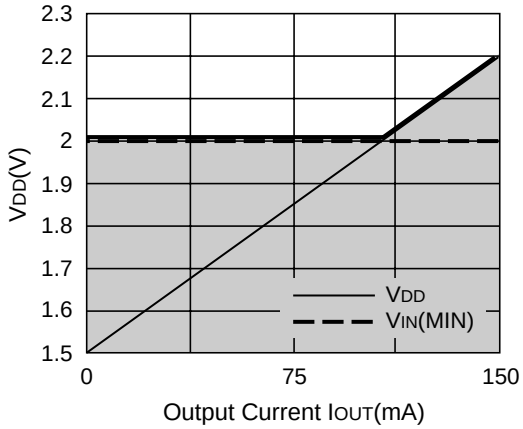
2.8V (VR2)

CIN=Ceramic 1.0µF, COUT=Ceramic 4.4µF



12) Minimum Operating Voltage

1.5V Minimum Operating Voltage Range



TECHNICAL NOTES

When using these ICs, consider the following points:

In these ICs, phase compensation is made for securing stable operation even if the load current is varied. For this purpose, be sure to use a 1.0μF or more capacitance C_{OUT} with good frequency characteristics and ESR (Equivalent Series Resistance) of which is in the range described as follows:

The relations between I_{OUT} (Output Current) and ESR of Output Capacitor are shown in the typical characteristics above. The conditions when the white noise level is under 40μV (Avg.) are marked as the hatched area in the graph.

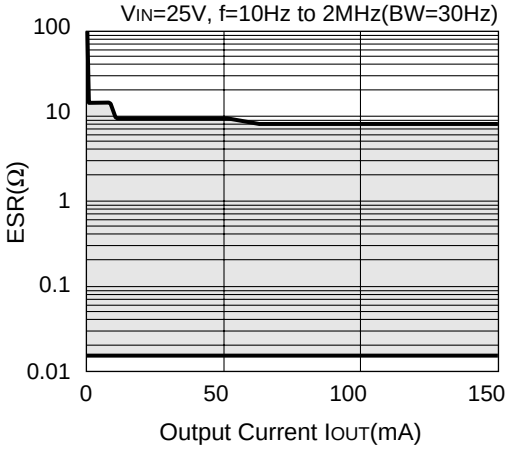
Test these ICs with as same external components as ones to be used on the PCB.

- Make V_{DD} and GND lines sufficient. When their impedance is high, the noise pick-up or incorrect operation may result.
- Connect the capacitor with a capacitance of 1μF or more between V_{DD} and GND as close as possible.
- Set external components, especially Output Capacitor, as close as possible to the ICs and make wiring as short as possible.

ESR vs. Output Current

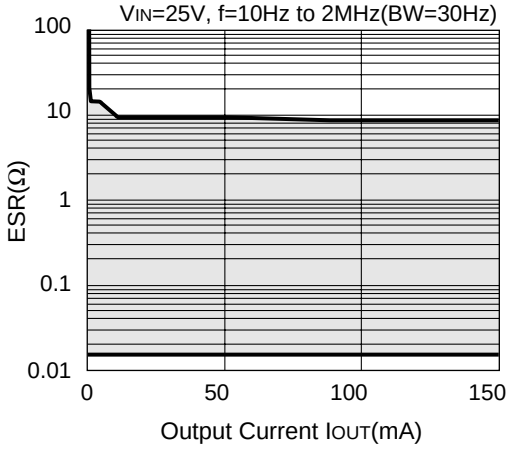
R5323N/K 1.5V (VR1)

Topt=25°C, CIN=COUT=Ceramic 1.0µF,
VIN=25V, f=10Hz to 2MHz(BW=30Hz)



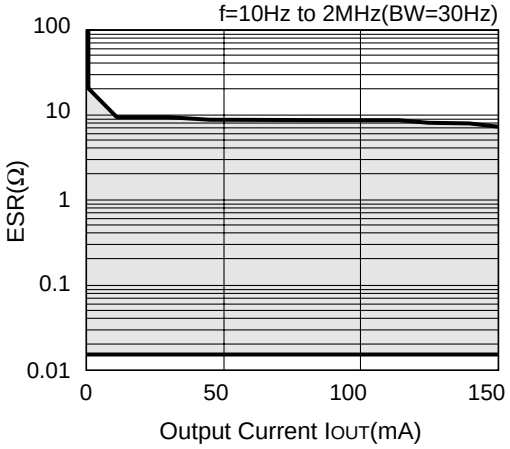
R5323N/K 1.5V (VR2)

Topt=25°C, CIN=COUT=Ceramic 1.0µF,
VIN=25V, f=10Hz to 2MHz(BW=30Hz)



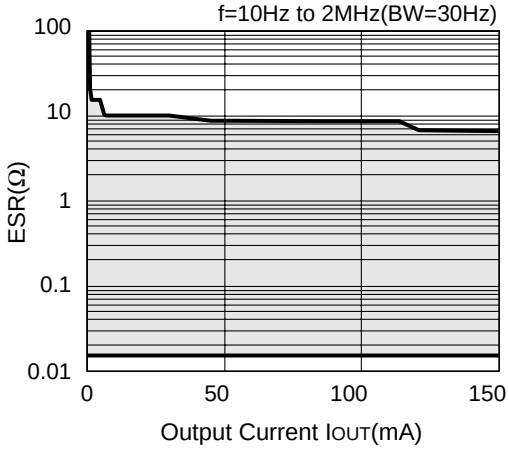
R5323N/K 2.8V (VR1)

CIN=COUT=Ceramic 1.0µF, VIN=2.5V,
f=10Hz to 2MHz(BW=30Hz)



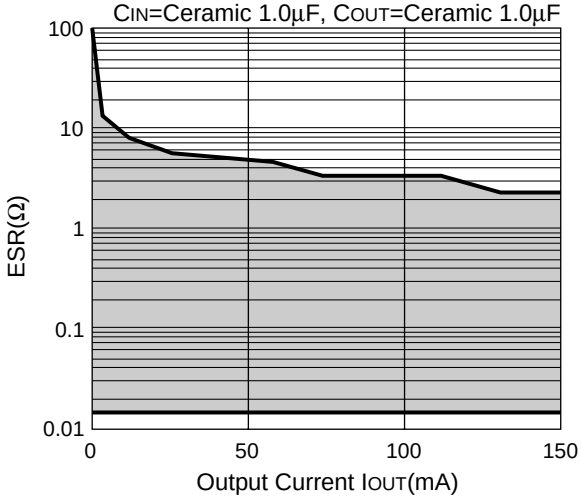
R5323N/K 2.8V (VR2)

CIN=COUT=Ceramic 1.0µF, VIN=2.5V,
f=10Hz to 2MHz(BW=30Hz)



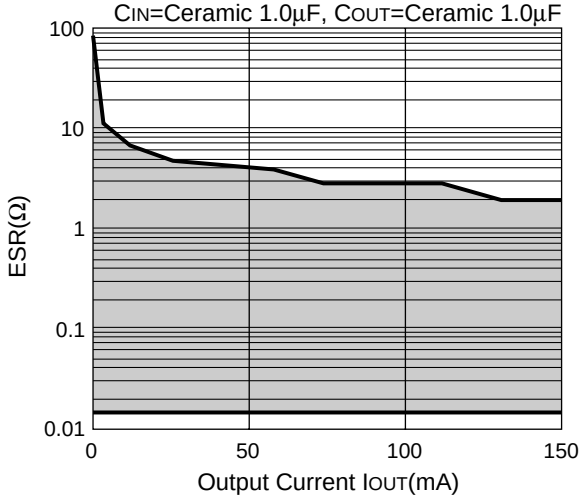
R5323Z 1.5V (VR1/VR2)

CIN=Ceramic 1.0µF, COUT=Ceramic 1.0µF



R5323Z 2.8V (VR1/VR2)

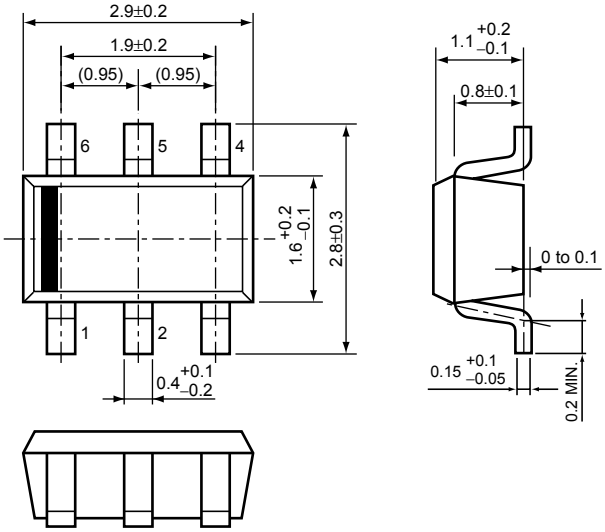
CIN=Ceramic 1.0µF, COUT=Ceramic 1.0µF



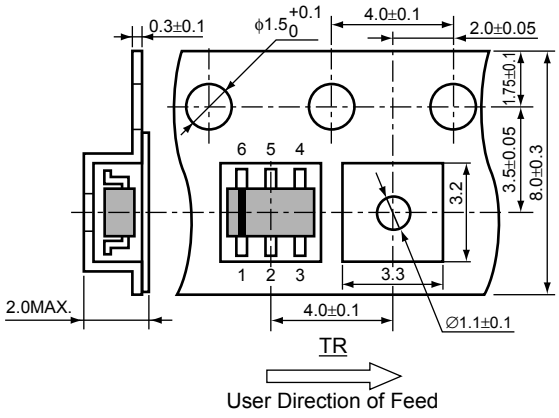
- **SOT-23-6 (SC-74)**

Unit: mm

PACKAGE DIMENSIONS

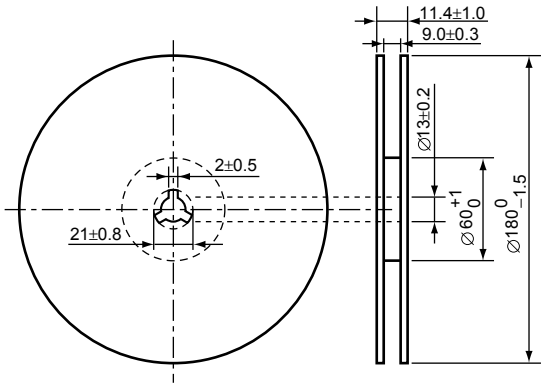


TAPING SPECIFICATION



TAPING REEL DIMENSIONS

(1reel=3000pcs)



POWER DISSIPATION (SOT-23-6)

This specification is at mounted on board. Power Dissipation (P_D) depends on conditions of mounting on board. This specification is based on the measurement at the condition below:

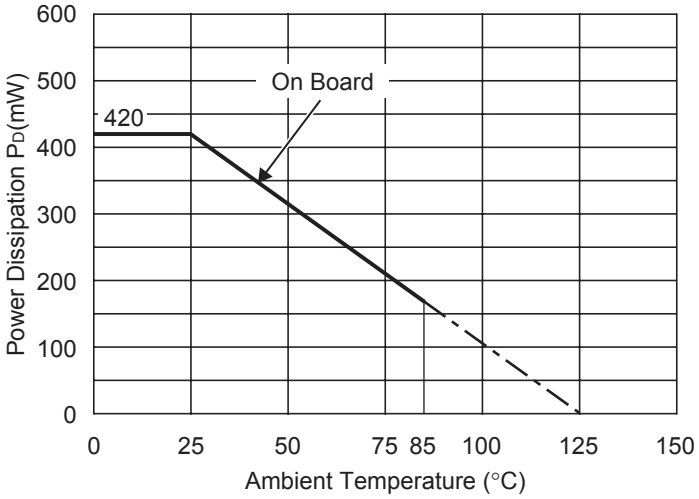
Measurement Conditions

	Standard Land Pattern
Environment	Mounting on Board (Wind velocity=0m/s)
Board Material	Glass cloth epoxy plactic (Double sided)
Board Dimensions	40mm × 40mm × 1.6mm
Copper Ratio	Top side : Approx. 50% , Back side : Approx. 50%
Through-hole	ϕ0.5mm × 44pcs

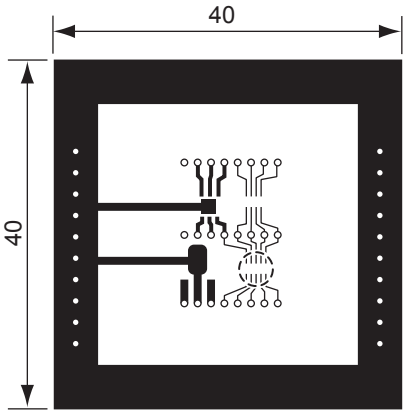
Measurement Result

(Topt=25°C,Tjmax=125°C)

	Standard Land Pattern	Free Air
Power Dissipation	420mW	250mW
Thermal Resistance	θja=(125−25°C)/0.42W=263°C/W	400°C/W



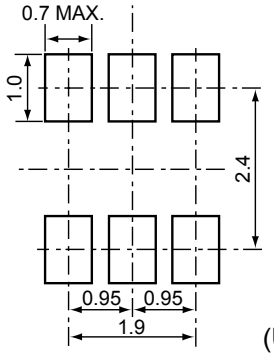
Power Dissipation



Measurement Board Pattern

IC Mount Area Unit : mm

RECOMMENDED LAND PATTERN

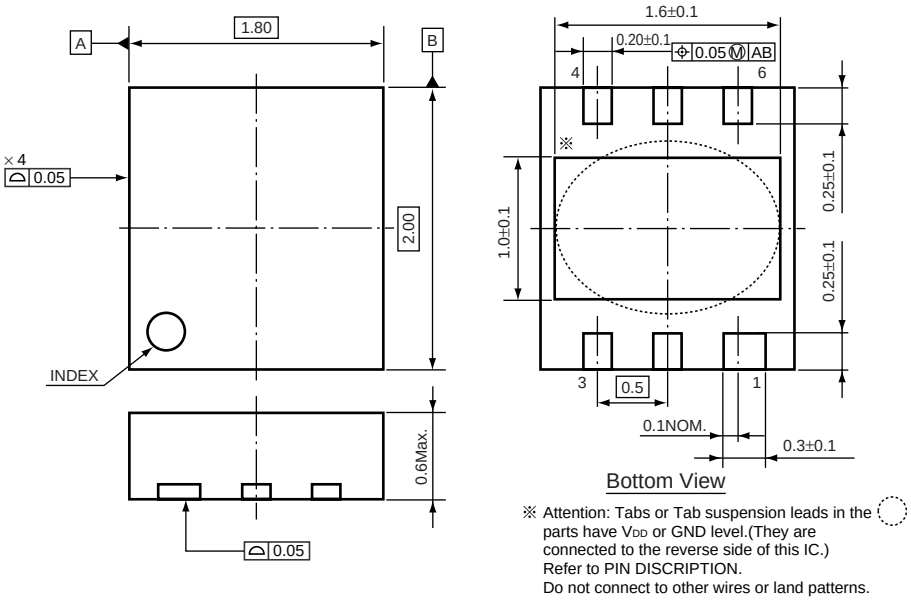


(Unit: mm)

- **PLP1820-6**

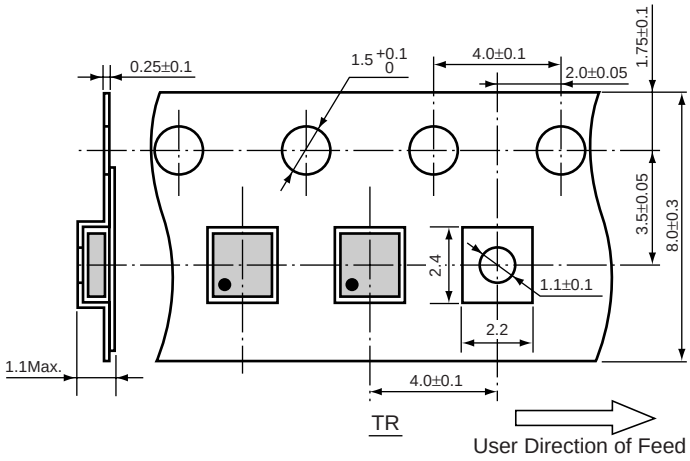
Unit: mm

PACKAGE DIMENSIONS



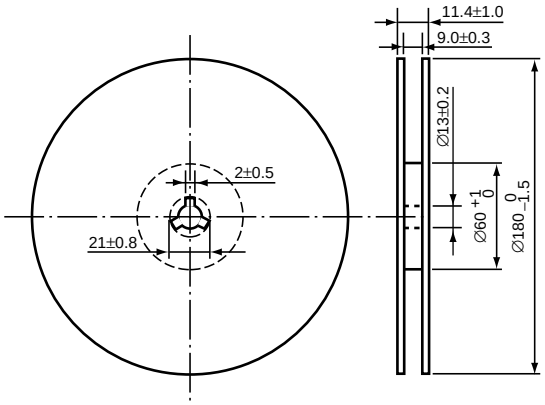
※ Attention: Tabs or Tab suspension leads in the parts have V_{DD} or GND level.(They are connected to the reverse side of this IC.) Refer to PIN DISCRIPTION. Do not connect to other wires or land patterns.

TAPING SPECIFICATION



TAPING REEL DIMENSIONS REUSE REEL (EIAJ-RRM-08Bc)

(1reel=5000pcs)
(R5323K,R5325K : 1reel=3000pcs)



POWER DISSIPATION (PLP1820-6)

This specification is at mounted on board. Power Dissipation (P_D) depends on conditions of mounting on board. This specification is based on the measurement at the condition below:

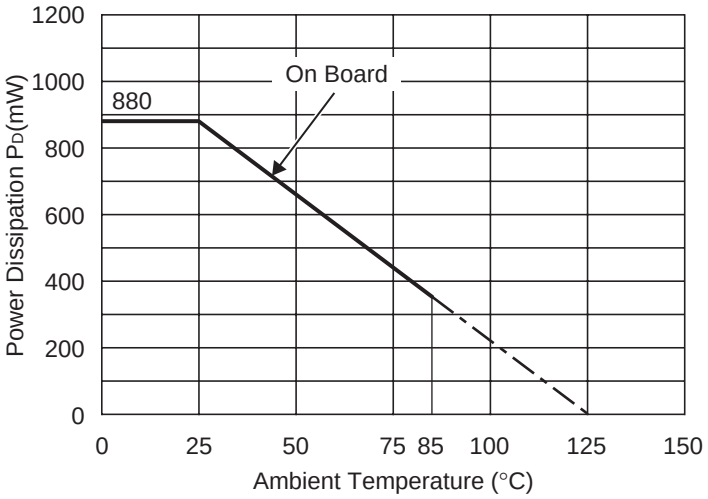
Measurement Conditions

	Standard Land Pattern
Environment	Mounting on Board (Wind velocity=0m/s)
Board Material	Glass cloth epoxy plactic (Double sided)
Board Dimensions	40mm × 40mm × 1.6mm
Copper Ratio	Top side : Approx. 50% , Back side : Approx. 50%
Through-hole	ϕ0.54mm × 30pcs

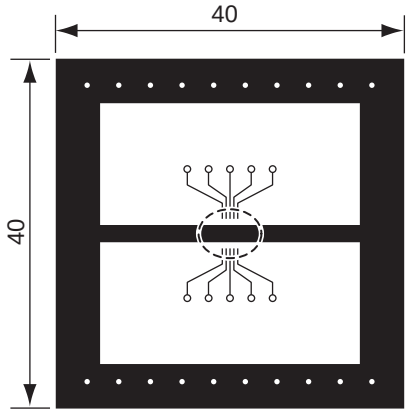
Measurement Result

(Topt=25°C,Tjmax=125°C)

	Standard Land Pattern
Power Dissipation	880mW
Thermal Resistance	θja=(125−25°C)/0.88W=114°C/W



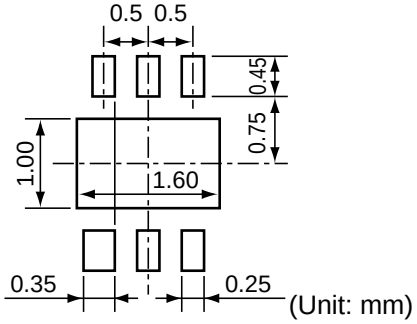
Power Dissipation



Measurement Board Pattern

IC Mount Area Unit : mm

RECOMMENDED LAND PATTERN

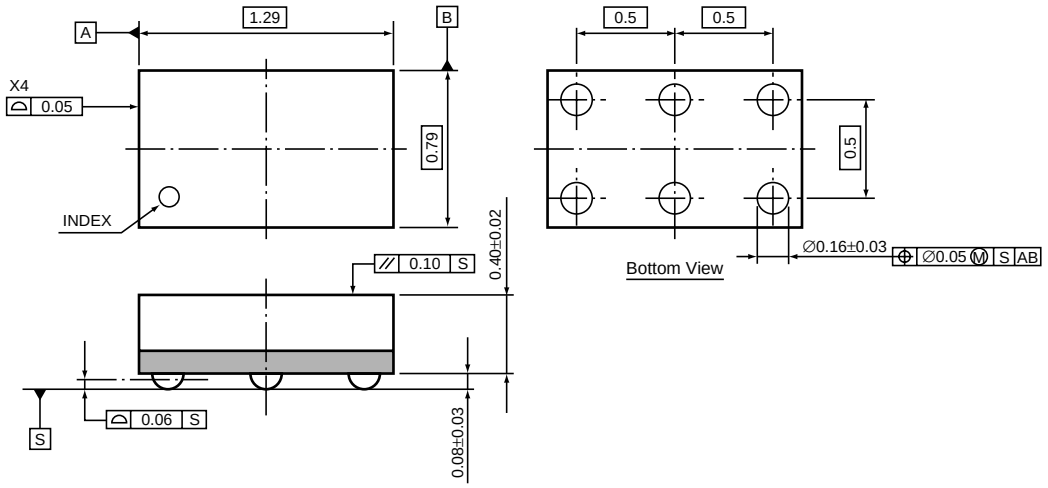


(Unit: mm)

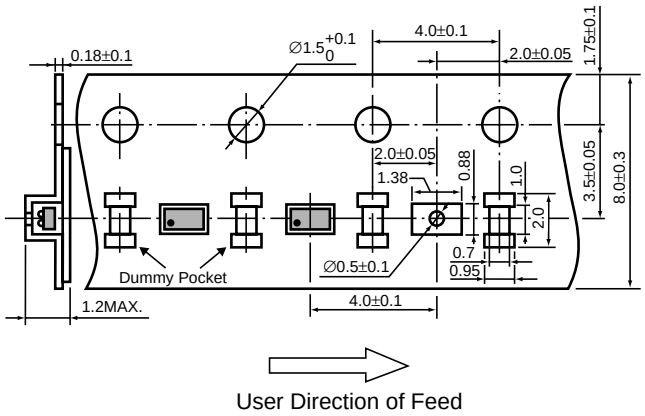
- **WLCSP-6-P1**

Unit: mm

PACKAGE DIMENSIONS

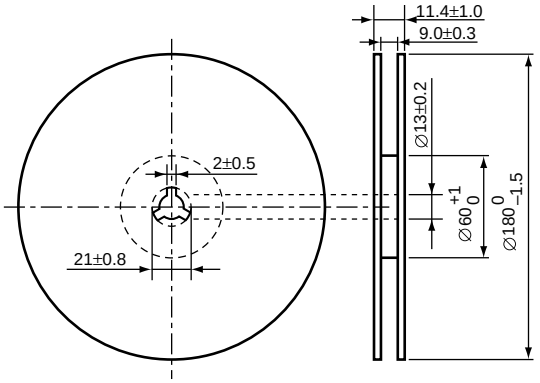


TAPING SPECIFICATION(TR: Standard Type)



TAPING REEL DIMENSIONS

(1reel=3000pcs)



POWER DISSIPATION (WLCSP-6-P1)

This specification is at mounted on board. Power Dissipation (P_D) depends on conditions of mounting on board. This specification is based on the measurement at the condition below:

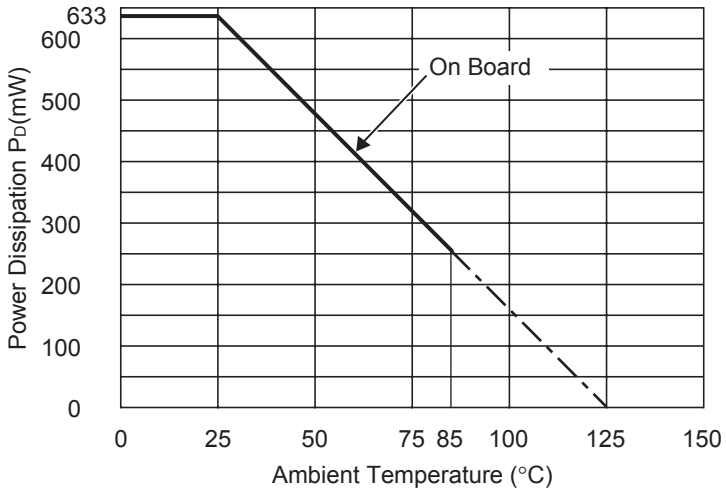
Measurement Conditions

	Standard Land Pattern
Environment	Mounting on Board (Wind velocity=0m/s)
Board Material	Glass cloth epoxy plactic (Double sided)
Board Dimensions	40mm × 40mm × 1.6mm
Copper Ratio	Top side : Approx. 50% , Back side : Approx. 50%
Through-hole	–

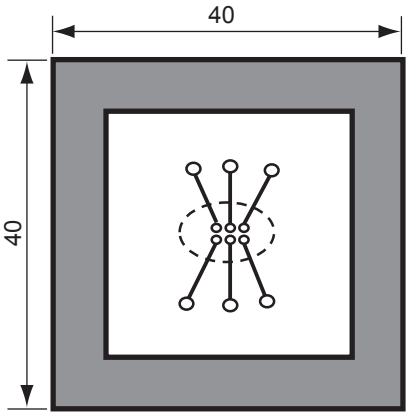
Measurement Result

(Topt=25°C,Tjmax=125°C)

	Standard Land Pattern
Power Dissipation	633mW
Thermal Resistance	θja=(125–25°C)/0.633W=158°C/W



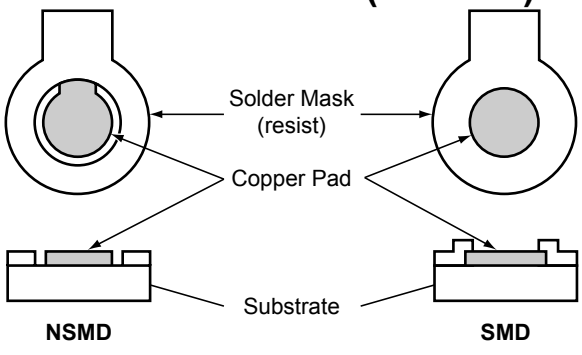
Power Dissipation



Measurement Board Pattern

IC Mount Area (Unit : mm)

RECOMMENDED LAND PATTERN (WLCSP)



(Unit : mm)

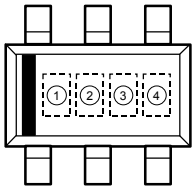
NSMD and SMD Pad Definition

Pad definition	Copper Pad	Solder Mask Opening
NSMD (Non-Solder Mask defined)	0.20mm	Min. 0.30mm
SMD (Solder Mask defined)	Min. 0.30mm	0.20mm

* Pad layout and size can be modified by customers material, equipment, method.
* Please adjust pad layout according to your conditions.
* Recommended Stencil Aperture Size....ø0.3mm
* Since lead free WL-CSP components are not compatible with the tin/lead solder process, you shall not mount lead free WL-CSP components using the tin/lead solder paste.

R5323N SERIES MARK SPECIFICATION

- **SOT-23-6 (SC-74)**



①, ② : Product Code (refer to Part Number vs. Product Code)

③, ④ : Lot Number

- **Part Number vs. Product Code**

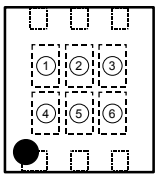
Part Number	Product Code	
	①	②
R5323N001B	N	0
R5323N002B	N	1
R5323N003B	N	2
R5323N004B	N	3
R5323N005B	N	4
R5323N006B	N	5
R5323N007B	N	6
R5323N008B	N	7
R5323N009B	N	8
R5323N010B	N	B
R5323N011B	U	6
R5323N012B	N	W
R5323N013B	N	T
R5323N014B	N	D
R5323N015B	N	E
R5323N016B	N	F
R5323N017B	N	G
R5323N018B	N	H
R5323N019B	N	K
R5323N020B	N	M
R5323N021B	N	N
R5323N022B	N	P
R5323N023B	N	R
R5323N024B	U	D
R5323N025B	U	E
R5323N026B	N	X
R5323N027B	N	U
R5323N028B	U	F
R5323N029B	N	V

Part Number	Product Code	
	①	②
R5323N030B	N	Z
R5323N031B	U	0
R5323N032B	U	1
R5323N033B	U	2
R5323N034B	U	3
R5323N035B	U	4
R5323N036B	U	5
R5323N037B	U	7
R5323N038B	U	8
R5323N039B	U	9
R5323N040B	U	A
R5323N041B	U	B
R5323N042B	U	C
R5323N043B	U	H
R5323N044B	U	J

Part Number	Product Code	
	①	②
R5323N001A	U	G
R5323N002A	N	9
R5323N003A	N	A
R5323N013A	N	C
R5323N019A	N	J
R5323N020A	N	L
R5323N023A	N	Q
R5323N024A	N	S
R5323N030A	N	Y

R5323K SERIES MARK SPECIFICATION

- **PLP1820-6**



① to ④ : Product Code (refer to Part Number vs. Product Code)

⑤, ⑥ : Lot Number

- **Part Number vs. Product Code**

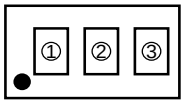
Part Number	Product Code			
	①	②	③	④
R5323K001B	C	0	0	1
R5323K002B	C	0	0	2
R5323K003B	C	0	0	3
R5323K004B	C	0	0	4
R5323K005B	C	0	0	5
R5323K006B	C	0	0	6
R5323K007B	C	0	0	7
R5323K008B	C	0	0	8
R5323K009B	C	0	0	9
R5323K010B	C	0	1	2
R5323K011B	C	0	4	1
R5323K012B	C	0	3	1
R5323K013B	C	0	2	8
R5323K014B	C	0	1	4
R5323K015B	C	0	1	5
R5323K016B	C	0	1	6
R5323K017B	C	0	1	7
R5323K018B	C	0	1	8
R5323K019B	C	0	2	0
R5323K020B	C	0	2	2
R5323K021B	C	0	2	3
R5323K022B	C	0	2	4
R5323K023B	C	0	2	6
R5323K024B	C	0	4	8
R5323K025B	C	0	4	9
R5323K026B	C	0	3	2
R5323K027B	C	0	2	9
R5323K028B	C	0	5	0
R5323K029B	C	0	3	0

Part Number	Product Code			
	①	②	③	④
R5323K030B	C	0	3	4
R5323K031B	C	0	3	5
R5323K032B	C	0	3	6
R5323K033B	C	0	3	7
R5323K034B	C	0	3	8
R5323K035B	C	0	3	9
R5323K036B	C	0	4	0
R5323K037B	C	0	4	2
R5323K038B	C	0	4	3
R5323K039B	C	0	4	4
R5323K040B	C	0	4	5
R5323K041B	C	0	4	6
R5323K042B	C	0	4	7
R5323K043B	C	0	5	2
R5323K044B	C	0	5	3

Part Number	Product Code			
	①	②	③	④
R5323K001A	C	0	5	1
R5323K002A	C	0	1	0
R5323K003A	C	0	1	1
R5323K013A	C	0	1	3
R5323K019A	C	0	1	9
R5323K020A	C	0	2	1
R5323K023A	C	0	2	5
R5323K024A	C	0	2	7
R5323K030A	C	0	3	3

R5323Z SERIES MARK SPECIFICATION

- **WLCSP-6-P1**



①　　: G (Fixed)

②, ③ : Lot Number

- **Product Code vs. Marking**

Part Number	Product Code
	①
R5323Z001A	G
R5323Z002A	G
R5323Z003A	G
R5323Z004A	G
R5323Z005A	G
R5323Z006A	G
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R5323Z011A	G
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R5323Z014A	G
R5323Z015A	G
R5323Z016A	G
R5323Z017A	G
R5323Z018A	G
R5323Z019A	G
R5323Z020A	G

Part Number	Product Code
	①
R5323Z021A	G
R5323Z022A	G
R5323Z023A	G
R5323Z024A	G
R5323Z025A	G
R5323Z026A	G
R5323Z027A	G
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R5323Z036A	G
R5323Z037A	G
R5323Z038A	G
R5323Z039A	G
R5323Z040A	G
R5323Z041A	G

Part Number	Product Code
	①
R5323Z001B	G
R5323Z002B	G
R5323Z003B	G
R5323Z004B	G
R5323Z005B	G
R5323Z006B	G
R5323Z007B	G
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R5323Z015B	G
R5323Z016B	G
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R5323Z018B	G
R5323Z019B	G
R5323Z020B	G

Part Number	Product Code
	①
R5323Z021B	G
R5323Z022B	G
R5323Z023B	G
R5323Z024B	G
R5323Z025B	G
R5323Z026B	G
R5323Z027B	G
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