Freescale Semiconductor
Data Sheet

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MPC8610 Integrated Host Processor Hardware Specifications

Features

- High-performance, 32-bit e600 core, that implements the Power Architecture™ technology
  - Eleven execution units and three register files
  - Two separate 32-Kbyte instruction and data level 1 (L1) caches
  - Integrated 256-Kbyte, eight-way set-associative unified instruction and data level 2 (L2) cache with ECC
  - 36-bit real addressing
  - Multiprocessing support features
  - Power and thermal management
- MPX coherency module (MCM)
- Address translation and mapping units (ATMUs)
- DDR/DDR2 memory controller
  - 64- or 32-bit data path (72-bit with ECC)
  - Up to 533-MHz DDR2 data rate and up to 400 MHz DDR data rate
  - Up to 16 Gbytes memory
- Enhanced local bus controller (eLBC)
  - Operating at up to 133 MHz
  - Eight chip selects
- Display interface unit
  - Maximum display resolution: 1280 × 1024
  - Maximum display refresh rate: 60 Hz
  - Display color depth: up to 24 bpp
  - Display interface: parallel TTL
- OpenPIC-compliant programmable interrupt controller (PIC)
  - Supports 16 programmable interrupt and processor task priority levels
  - Supports 12 discrete external interrupts and 48 internal interrupts
  - Eight global high resolution timers/counters that can generate interrupts
  - Support for PCI Express message-shared interrupts (MSIs)
- Dual I^2C controllers
  - Master or slave I^2C mode support
  - Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via I^2C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I^2C addressing mode
- DUART
- Fast InfraRed interface
- Serial peripheral interface
  - Master or slave support
- Dual integrated four-channel DMA controllers
  - All channels accessible by both local and remote masters
  - Supports transfers to or from any local memory or I/O port
  - Ability to start and flow control each DMA channel from external 3-pin interface
- Watchdog timer
- Dual global timer modules
- 32-bit PCI interface, 33 or 66 MHz bus frequency
- Dual PCI Express® controllers
  - PCI Express 1.0a compatible
  - PCI Express controller 1 supports x1, x2, and x4 link widths; PCI Express controller 2 supports x1, x2, x4, and x8 link widths
  - 2.5 Gbaud, 2.0 Gbps lane
- Device performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter-specific events
  - Supports 64 reference events that can be counted on any of the 8 counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- IEEE Std 1149.1™ compliant, JTAG boundary scan
- Available as 783-pin, flip-chip, plastic ball grid array (FC-PBGA)

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Figure 1 shows the major functional units within the MPC8610.

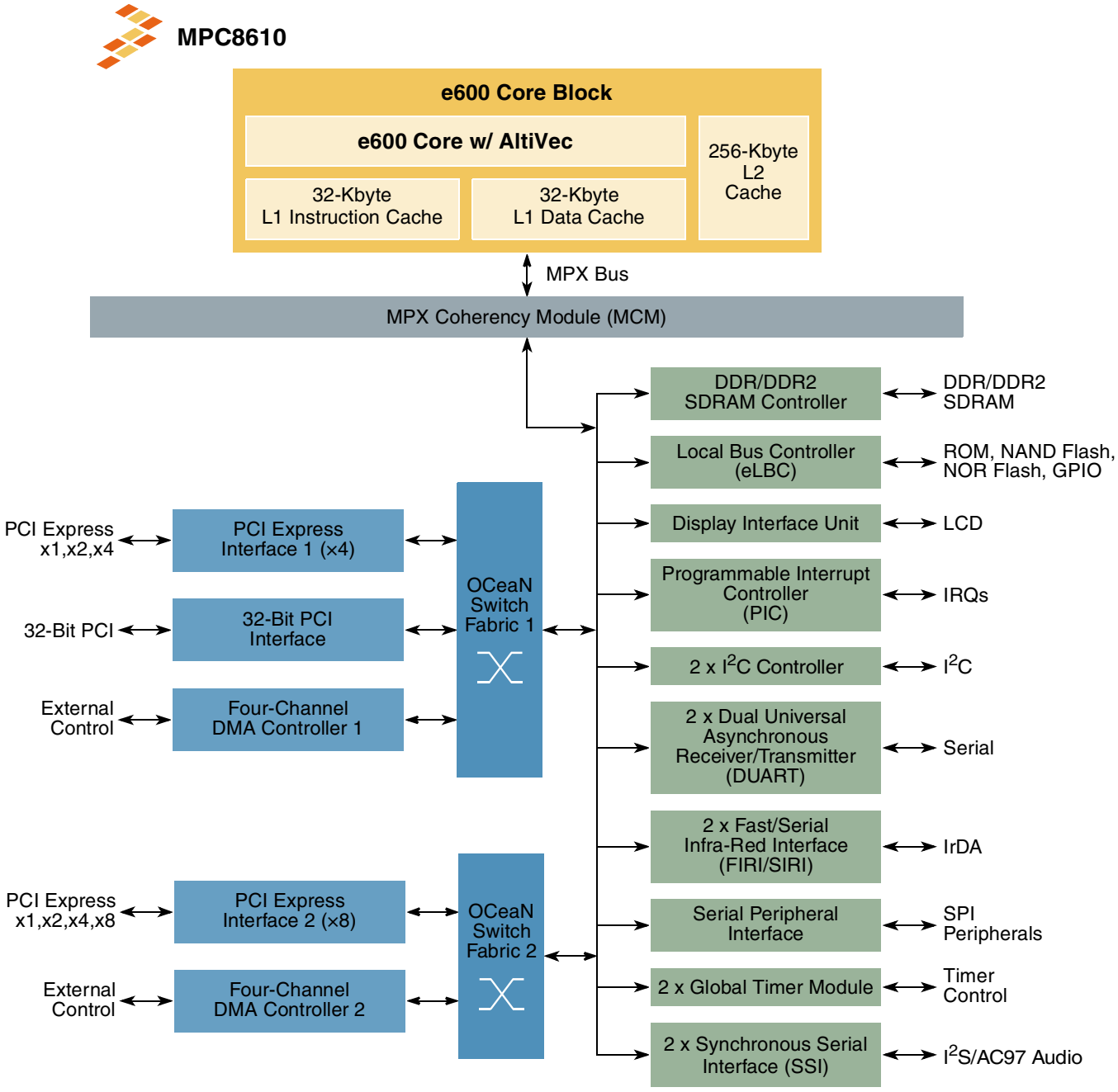


Figure 1. MPC8610 Block Diagram

1 Pin Assignments and Reset States

Table 1 provides the pin assignments for the signals.

Table 1. Signal Reference by Functional Block

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
Clocking Signals[4]				
SYSCLK	D28	I	OV_{DD}	
RTC	A25	I	OV_{DD}	17
DDR Memory Interface Signals[2]				
MA[15:0]	AH28, AH25, AH6, AH24, AH22, AG13, AG22, AG19, AH21, AH19, AH18, AG16, AH16, AG15, AH15, AH14	O	GV_{DD}	
MBA[2:0]	AG25, AH13, AH12	O	GV_{DD}	
$\overline{\text{MCS}}$[0:3]	AH10, AG7, AH9, AG4	O	GV_{DD}	
MDQ[0:63]	W26, Y26, AB24, AC28, W27, Y28, AB27, AB26 AD27, AE27, AD25, AF25, AC26, AD28, AC25, AD24, AG24, AF23, AE21, AG21, AE24, AE23, AF22, AD21, AH20, AC19, AG18, AF17, AE20, AF20, AE18, AC17, AC13, AD12, AG9, AE9, AD13, AE12, AD10, AC10, AF8, AE8, AD6, AH5, AD9, AH8, AG6, AE6, AF4, AD4, AC3, AC1, AF5, AE5, AD2, AC4, AB1, AB2, Y1, Y6, AB6, AA6, Y3, Y4	I/O	GV_{DD}	
MECC[0:7]	AD16, AF16, AC15, AF15, AH17, AE17, AA15, AB15	I/O	GV_{DD}	
MDM[0:8]	Y25, AE26, AH23, AD19, AF11, AF7, AE3, AB4, AC16	O	GV_{DD}	
MDQS[0:8]	AA25, AF26, AD22, AD18, AF10, AC7, AD3, AA5, Y15	I/O	GV_{DD}	
$\overline{\text{MDQS}}$[0:8]	AA27, AF28, AC22, AF19, AE11, AD7, AE2, AB5, AB16	I/O	GV_{DD}	
$\overline{\text{M}}$CAS	AG10	O	GV_{DD}	
$\overline{\text{M}}$WE	AH11	O	GV_{DD}	
$\overline{\text{M}}$RAS	AG12	O	GV_{DD}	
MCK[0:5]	AF14, AG28, AH3, AD15, AH27, AG2	O	GV_{DD}	
$\overline{\text{MCK}}$[0:5]	AF13, AG27, AH2, AD14, AH26, AG1	O	GV_{DD}	
MCKE[0:3]	AB28, AA28, AE28, W28	O	GV_{DD}	18
MDIC[0:1]	AD1, AE1	I/O	GV_{DD}	19
MODT[0:3]	AH7, AH4, AG3, AF1	O	GV_{DD}	
Enhanced Local Bus Signals[4]				

Table 1. Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
LAD[0:31]	AA21, AA22, AA23, Y21, Y22, Y23, Y24, W23, W24, W25, V28, V27, V25, V23, V21, W22, U28, U26, U24, U22, U23, U20, U21, W20, V20, T24, T25, T27, T26, T21, T22, T23	I/O	BV_{DD}	20
LDP[0:3]/LA[6:9]	N28, M28, L28, P25	I/O	BV_{DD}	
LA10/SSI1_TXD	P19	O	BV_{DD}	20, 23
LA11/SSI1_TFS	M27	O	BV_{DD}	23
LA12/SSI1_TCK	U18	O	BV_{DD}	23
LA13/SSI1_RCK	P28	O	BV_{DD}	23
LA14/SSI1_RFS	R18	O	BV_{DD}	23
LA15/SSI1_RXD	R19	O	BV_{DD}	23
LA16/SSI2_TXD	R20	O	BV_{DD}	23
LA17/SSI2_TFS	M18	O	BV_{DD}	23
LA18/SSI2_TCK	N18	O	BV_{DD}	23
LA19/SSI2_RCK	N27	O	BV_{DD}	23
LA20/SSI2_RFS	P20	O	BV_{DD}	23
LA21/SSI2_RXD	P21	O	BV_{DD}	23
LA[22:31]	M19, M21, M22, M23, N23, N24, M26, N20, N21, N22	O	BV_{DD}	20
$\overline{\text{LCS}}$[0:4]	R24, R22, P23, P24, P27	O	BV_{DD}	21
$\overline{\text{LCS5}}$/$\overline{\text{DMA2_DREQ0}}$	R23	O	BV_{DD}	21, 22, 23
$\overline{\text{LCS6}}$/$\overline{\text{DMA2_DACK0}}$	N26	O	BV_{DD}	21, 23
$\overline{\text{LCS7}}$/$\overline{\text{DMA2_DDONE0}}$	R26	O	BV_{DD}	21, 23
$\overline{\text{LWE0}}$/$\overline{\text{LFWE}}$/$\overline{\text{LBS0}}$	T19	O	BV_{DD}	20
$\overline{\text{LWE1}}$/$\overline{\text{LBS1}}$	T20	O	BV_{DD}	20
$\overline{\text{LWE2}}$/$\overline{\text{LBS2}}$	W19	O	BV_{DD}	20
$\overline{\text{LWE3}}$/$\overline{\text{LBS3}}$	T18	O	BV_{DD}	20
LBCTL	T28	O	BV_{DD}	20
LALE	R28	O	BV_{DD}	20
LGPL0/LFCLE	L19	O	BV_{DD}	20
LGPL1/LFALE	L20	O	BV_{DD}	20
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	L21	O	BV_{DD}	20
LGPL3/$\overline{\text{LFWP}}$	L22	O	BV_{DD}	20
$\overline{\text{LGTA}}$/LFR$\overline{\text{B}}$/LGPL4/ LUPWAIT/LPBSE	L23	I/O	BV_{DD}	24

Table 1. Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
LGPL5	L24	O	BV_{DD}	
LCLK[0:2]	R25, M25, L26	O	BV_{DD}	
DIU/LCD Signals[4]				
DIU_LD[23:16]/ GPIO1[15:8]	R3, R10, T10, N7, N4, P6, P5, P4	O	OV_{DD}	5, 23
DIU_LD[15:0]/ GPIO1[31:16]	T3, R9, T9, R8, R7, R6, R4, T7, U5, T6, T5, W4, W5, W6, V4, V6	O	OV_{DD}	5, 14, 20, 23
DIU_VSYNC	V7	O	OV_{DD}	20
DIU_HSYNC	U7	O	OV_{DD}	20
DIU_DE	U4	O	OV_{DD}	20
DIU_CLK_OUT	N6	O	OV_{DD}	
Programmable Interrupt Controller (PIC) Signals[4]				
IRQ[0:5]	L25, J23, K26, E23, K28, K22	I	OV_{DD}	
IRQ6/$\overline{\text{DMA1_DREQ0}}$	G27	I	OV_{DD}	22, 23
IRQ7/$\overline{\text{DMA1_DACK0}}$	J25	I	OV_{DD}	23
IRQ8/$\overline{\text{DMA1_DDONE0}}$	J27	I	OV_{DD}	23
IRQ9/$\overline{\text{DMA1_DREQ3}}$	H26	I	OV_{DD}	22, 23
IRQ10/$\overline{\text{DMA1_DACK3}}$	J26	I	OV_{DD}	23
IRQ11/$\overline{\text{DMA1_DDONE3}}$	K27	I	OV_{DD}	23
$\overline{\text{IRQ_OUT}}$	K23	O	OV_{DD}	21, 25
$\overline{\text{MCP}}$	A24	I	OV_{DD}	
$\overline{\text{SMI}}$	B24	I	OV_{DD}	
I^2C Signals				
IIC1_SDA/GPIO2[10]	D24	I/O	OV_{DD}	21, 23, 25
IIC1_SCL/GPIO2[9]	E24	I/O	OV_{DD}	21, 23, 25
IIC2_SDA/$\overline{\text{SPISEL}}$/ GPIO2[12]	E27	I/O	OV_{DD}	21, 23, 25
IIC2_SCL/SPICLK/ GPIO2[11]	E28	I/O	OV_{DD}	21, 23, 25
DUART Signals[4]				
UART_SIN0/SPIMOSI/ GPIO2[5]	K24	I	OV_{DD}	23
UART_SOUT0/SPIMISO	H25	O	OV_{DD}	23
$\overline{\text{UART_CTS0}}$/GPIO2[6]	G24	I	OV_{DD}	23
$\overline{\text{UART_RTS0}}$	G26	O	OV_{DD}	20

Table 1. Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
UART_SIN1/IR2_RXD/ GPIO2[7]	F25	I	OV_{DD}	23
UART_SOUT1/IR2_TXD	H24	O	OV_{DD}	23
$\overline{\text{UART_CTS}}$1/GPIO2[8]	C23	I	OV_{DD}	23
$\overline{\text{UART_RTS}}$1	D23	O	OV_{DD}	
IrDA Signals[4]				
IR1_TXD/GPIO2[13]	F27	O	OV_{DD}	23
IR1_RXD/GPIO2[14]	E26	I	OV_{DD}	23
IR_CLKIN	F28	I	OV_{DD}	
IR2_TXD/UART_SOUT1	H24	O	OV_{DD}	23
IR2_RXD/UART_SIN1/ GPIO2[7]	F25	I	OV_{DD}	23
SPI Signals				
SPIMOSI/UART_SIN0/ GPIO2[5]	K24	I/O	OV_{DD}	23
SPIMISO/UART_SOUT0	H25	I/O	OV_{DD}	23
$\overline{\text{SPISEL}}$/IIC2_SDA/ GPIO2[12]	E27	I	OV_{DD}	23
SPICLK/IIC2_SCL/ GPIO2[11]	E28	I	OV_{DD}	23
SSI Signals[3, 6]				
SSI1_RXD/LA15	R19	I	BV_{DD}	23
SSI1_TXD/LA10	P19	O	BV_{DD}	23
SSI1_RFS/LA14	R18	I/O	BV_{DD}	23
SSI1_TFS/LA11	M27	I/O	BV_{DD}	23
SSI1_RCK/LA13	P28	I/O	BV_{DD}	23
SSI1_TCK/LA12	U18	I/O	BV_{DD}	23
SSI2_RXD/LA21	P21	I	BV_{DD}	23
SSI2_TXD/LA16	R20	O	BV_{DD}	23
SSI2_RFS/LA20	P20	I/O	BV_{DD}	23
SSI2_TFS/LA17	M18	I/O	BV_{DD}	23
SSI2_RCK/LA19	N27	I/O	BV_{DD}	23
SSI2_TCK/LA18	N18	I/O	BV_{DD}	23
DMA Signals[4]				
$\overline{\text{DMA1_DREQ0}}$/IRQ6/ GPIO2[24]	G27	I	OV_{DD}	22, 23

Table 1. Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
DMA1_DREQ3/IRQ9/ GPIO2[26]	H26	I	OV_{DD}	23
DMA1_DACK0/IRQ7/ GPIO2[25]	J25	O	OV_{DD}	23
DMA1_DACK3/IRQ10/ GPIO2[27]	J26	O	OV_{DD}	23
DMA1_DDONE0/IRQ8	J27	O	OV_{DD}	23
DMA1_DDONE3/IRQ11/ GPIO2[28]	K27	O	OV_{DD}	23
DMA2_DREQ0/LCS5	R23	I	OV_{DD}	23
DMA2_DREQ3/ GPIO2[29]	H27	I	OV_{DD}	23
DMA2_DACK0/LCS6	N26	O	OV_{DD}	23
DMA2_DACK3/ GPIO2[30]	H28	O	OV_{DD}	23
DMA2_DDONE0/LCS7	R26	O	OV_{DD}	23
DMA2_DDONE3/ GPIO2[31]	J28	O	OV_{DD}	23
General-Purpose Timer Signals[4]				
GTM1_TIN1/GPIO2[15]	U3	I	OV_{DD}	23
GTM1_TIN3/GPIO2[21]	W2	I	OV_{DD}	23
GTM1_TGATE1/ GPIO2[16]	V2	I	OV_{DD}	23
GTM1_TGATE3/ GPIO2[22]	U1	I	OV_{DD}	23
GTM1_TOUT1/GPIO2[17]	W3	O	OV_{DD}	23
GTM1_TOUT3/GPIO2[23]	U2	O	OV_{DD}	23
GTM2_TIN1/GPIO2[18]	V1	I	OV_{DD}	23
GTM2_TGATE1/ GPIO2[19]	W1	I	OV_{DD}	23
GTM2_TOUT1/GPIO2[20]	V3	O	OV_{DD}	23
PCI Signals[4]				
PCI_AD[31:0]	M1, M2, M3, M4, M5,M7, L1, L6, J1, K2, K3, K4, K5, K6, K7, H1, H7, G1, G2, G3, G4, G5, G6, F1, F4, F6, F7, F8, D2, D3, E1, E2	I/O	OV_{DD}	
PCI_C/BE[3:0]	L2, J2, H6, F2	I/O	OV_{DD}	
PCI_PAR	H5	I/O	OV_{DD}	
PCI_FRAME	J3	I/O	OV_{DD}	
PCI_TRDY	J6	I/O	OV_{DD}	

Table 1. Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
PCI_IRDY	J5	I/O	OV_{DD}	
PCI_STOP	E4	I/O	OV_{DD}	
PCI_DEVSEL	J7	I/O	OV_{DD}	
PCI_IDSEL	L5	I	OV_{DD}	
PCI_PERR	H2	I/O	OV_{DD}	
PCI_SERR	H3	I/O	OV_{DD}	
PCI_REQ0	N3	I/O	OV_{DD}	
PCI_REQ1/GPIO1[0]	N1	I/O	OV_{DD}	23
PCI_REQ2/GPIO1[2]	P3	I/O	OV_{DD}	23
PCI_REQ3/GPIO1[4]	P1	I/O	OV_{DD}	23
PCI_REQ4/GPIO1[6]	P2	I/O	OV_{DD}	23
PCI_GNT0	N2	I/O	OV_{DD}	
PCI_GNT1/GPIO1[1]	T1	I/O	OV_{DD}	23
PCI_GNT2/GPIO1[3]	T2	I/O	OV_{DD}	23
PCI_GNT3/GPIO1[5]	R1	I/O	OV_{DD}	23
PCI_GNT4/GPIO1[7]	R2	I/O	OV_{DD}	23
PCI_CLK	C1	I	OV_{DD}	
SerDes 1 Signals				
SD1_TX[3:0]	J13, G12, F10, H9	O	$X1V_{DD}$	
SD1_TX[3:0]	H13, F12, G10, J9	O	$X1V_{DD}$	
SD1_RX[3:0]	B9, D8, D5, B4	I	$S1V_{DD}$	
SD1_RX[3:0]	A9, C8, C5, A4	I	$S1V_{DD}$	
SD1_REF_CLK	A7	I	$S1V_{DD}$	
SD1_REF_CLK	B7	I	$S1V_{DD}$	
SD1_PLL_TPD	C7	O	$X1V_{DD}$	9, 10
SD1_PLL_TPA	B6	Analog	$S1V_{DD}$	9, 11
SD1_IMP_CAL_TX	E11	Analog	$X1V_{DD}$	7
SD1_IMP_CAL_RX	B3	Analog	$S1V_{DD}$	8
SerDes 2 Signals				
SD2_TX[7:0]	F22, J21, F20, H19, J17, G16, H15, G14	O	$X2V_{DD}$	
SD2_TX[7:0]	G22, H21, G20, J19, H17, F16, J15, F14	O	$X2V_{DD}$	
SD2_RX[7:0]	B22, D21, B20, D19, C15, B14, C13, A12	I	$S2V_{DD}$	
SD2_RX[7:0]	A22, C21, A20, C19, D15, A14, D13, B12	I	$S2V_{DD}$	
SD2_REF_CLK	A18	I	$S2V_{DD}$	

Table 1. Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{SD2_REF_CLK}}$	B18	I	$S2V_{DD}$	
SD2_PLL_TPD	D17	O	$X2V_{DD}$	9, 10
SD2_PLL_TPA	C17	Analog	$S2V_{DD}$	9, 11
SD2_IMP_CAL_TX	E21	Analog	$X2V_{DD}$	7
SD2_IMP_CAL_RX	B11	Analog	$S2V_{DD}$	8
System Control Signals[4]				
$\overline{\text{HRESET}}$	B23	I	OV_{DD}	
$\overline{\text{HRESET_REQ}}$	J22	O	OV_{DD}	
$\overline{\text{SRESET}}$	A26	I	OV_{DD}	
$\overline{\text{CKSTP_IN}}$	C27	I	OV_{DD}	
$\overline{\text{CKSTP_OUT}}$	F24	O	OV_{DD}	21, 25
Power Management Signals[4]				
ASLEEP	B26	O	OV_{DD}	20
Debug Signals[4]				
TRIG_IN	K20	I	OV_{DD}	
TRIG_OUT/READY/ $\overline{\text{QUIESCE}}$	C28	O	OV_{DD}	14
MSRCID[0:4]	Y20, AB23, AB20, AB21, AC23	O	BV_{DD}	14, 20
MDVAL	AC20	O	BV_{DD}	20
CLK_OUT	G28	O	OV_{DD}	18
Test Signals[4]				
$\overline{\text{LSSD_MODE}}$	G23	I	OV_{DD}	26
TEST_MODE[0:1]	K12, K10	I	OV_{DD}	26
JTAG Signals[4]				
TCK	D26	I	OV_{DD}	
TDI	B25	I	OV_{DD}	27
TDO	D27	O	OV_{DD}	18
TMS	C25	I	OV_{DD}	27
$\overline{\text{TRST}}$	A28	I	OV_{DD}	27
Additional Analog Signals				
TEMP_ANODE	C11	Thermal	—	
TEMP_CATHODE	C10	Thermal	—	
Special Connection Requirement Pins				

Table 1. Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
No Connects	B1, B10, C2, C3, E22, F18, G11, G18, H8, H11, H14, J11, AA1, AA2, AA3, AA4	—	—	16
Power and Ground Signals				
MV_{REF}	AE14	DDR2 reference voltage	$GV_{DD}/2$	
OV_{DD}	C24, C26, D1, E25, F3, G7, G25, H4, J24, K1, L4, L7, N5, P10, P7, T4, T8, V5, V8	LCD, general purpose timer, PCI, MPIC, I^2C, DUART, IrDA, SPI, DMA, system control, clocking, debug, test, JTAG, & power management I/O supply	OV_{DD}	
GV_{DD}	Y2, Y16, AA7, AA24, AA26, AB14, AB17, AC2, AC5, AC6, AC9, AC12, AC18, AC21, AC24, AC27, AE4, AE7, AE10, AE13, AE16, AE19, AE22, AE25, AF2, AG5, AG8, AG11, AG14, AG17, AG20, AG23, AG26, AH1	DDR SDRAM I/O supply	GV_{DD}	
BV_{DD}	L27, M20, M24, P18, P22, P26, U19, U27, V24, W21, AA20	eLBC & SSI I/O voltage	BV_{DD}	
$S1V_{DD}$	A3, A10, B5, B8, D4, D7	Receiver and SerDes core power supply for port 1	$S1V_{DD}$	
$S2V_{DD}$	A11, A15, A19, A23, B13, B17, B21, C14, C18, D12, D16, D20	Receiver and SerDes core power supply for port 2	$S2V_{DD}$	
$X1V_{DD}$	F11, G9, H12, J10, K13	Transmitter power supply for SerDes port 1	$X1V_{DD}$	
$X2V_{DD}$	F13, F17, F21, G15, G19, H18, H22, J16, J20	Transmitter power supply for SerDes port 2	$X2V_{DD}$	
$L1V_{DD}$	K14	Digital logic power supply for SerDes port 1	$L1V_{DD}$	
$L2V_{DD}$	K16, K18	Digital logic power supply for SerDes port 2	$L2V_{DD}$	

Table 1. Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
V_{DD}_Core	L8, L10, M9, M11, M13, M15, N8, N10, N12, N14, N16, P9, P11, P13, P15, R12, R14, R16, T11, T13, T15, U10, U12, U14, U16, V9, V11, V13, V15, W8, W10, W12, W14, W16, Y9, Y11, Y13, Y7, AA8, AA10, AA12, AB9, AB11, AC8	Core voltage supply	V_{DD}_Core	
V_{DD}_PLAT	L12, L14, L16, L18, M17, P17, T17, V17, V19, W18, Y17, Y19, AA18	Platform supply voltage	V_{DD}_PLAT	
AV_{DD}_Core	A27	Core PLL supply	AV_{DD}_Core	
AV_{DD}_PLAT	B28	Platform PLL supply	AV_{DD}_PLAT	
AV_{DD}_PCI	A2		AV_{DD}_PCI	
$SD1AV_{DD}$	A6		$SD1AV_{DD}$	
$SD2AV_{DD}$	A16		$SD2AV_{DD}$	
$SENSEV_{DD}$	AC11	V_{DD}_Core sensing pin		28
$SENSEV_{SS}$	AB12	Core GND sensing pin		28
GND	B2, B27, D25, E3, F26, F5, G8, H23, J4, K25, L11, L13, L15, L17, L3, L9, M10, M12, M14, M16, M6, M8, N11, N13, N15, N17, N19, N25, N9, P12, P14, P16, P8, R11, R13, R15, R17, R21, R27, R5, T12, T14, T16, U11, U13, U15, U17, U25, U6, U8, U9, V10, V12, V14, V16, V18, V22, V26, W11, W13, W15, W17, W7, W9, Y10, Y12, Y14, Y18, Y27, Y5, Y8, AA11AA13, AA14, AA16, AA17, AA19, AA9, AB10, AB13, AB18, AB19, AB22, AB25, AB3, AB7, AB8, AC14, AD11, AD17, AD20, AD23, AD26, AD5, AD8, AE15, AF12, AF18, AF21, AF24, AF27, AF3, AF6, AF9	GND		
SD1AGND	C6	SerDes port 1 ground pin for $SD1AV_{DD}$		
SD2AGND	B16	SerDes port 2 ground pin for $SD2AV_{DD}$		
SGND	A5, A8, A13, A17, A21, B15, B19, C4, C9, C12, C16, C20, C22, D6, D9, D10, D11, D14, D18, D22, E5, E6, E7, E8, E9, E10, E13, E14, E15, E16, E17, E18, E19, E20	Ground pins for SV_{DD}		
XGND	E12, F9, F15, F19, F23, G13, G17, G21, H10, H16, H20, J8, J12, J14, J18, K8, K9, K11, K15, K17, K19, K21	Ground pins for XV_{DD}		

Table 1. Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
Reset Configuration Signals[15]				
LAD[0:31] cfg_gpinout[0:31]	AA21, AA22, AA23, Y21, Y22, Y23, Y24, W23, W24, W25, V28, V27, V25, V23, V21, W22, U28, U26, U24, U22, U23, U20, U21, W20, V20, T24, T25, T27, T26, T21, T22, T23	—	BV_{DD}	
LA10/SSI1_TXD cfg_ssi_la_sel	P19	—	BV_{DD}	
LA[25:26] cfg_elbc_clkdiv[0:1]	M23, N23	—	BV_{DD}	
LA27 cfg_cpu_boot	N24	—	BV_{DD}	
DIU_LD[10], LA[28:31] cfg_sys_pll[0:4]	R6, M26, N20, N21, N22	—	BV_{DD}	
$\overline{\text{LWE0}}$/$\overline{\text{LFWE}}$/$\overline{\text{LBS0}}$ cfg_pci_speed	T19	—	BV_{DD}	
$\overline{\text{LWE}}$/$\overline{\text{LBS}}$[1:3] cfg_host_agt[0:2]	T20, W19, T18	—	BV_{DD}	
LBCTL, $\overline{\text{LALE}}$, LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$, DIU_LD4 cfg_core_pll[0:3]	T28, R28, L21, W4	—	BV_{DD}	
LGPL0/LFCLE cfg_net2_div	L19	—	BV_{DD}	12
LGPL1/LFALE cfg_pci_clk	L20	—	BV_{DD}	
LGPL3/$\overline{\text{LFWP}}$, LGPL5 cfg_boot_seq[0:1]	L22, L24	—	BV_{DD}	
DIU_LD[0] cfg_elbc_ecc	V6	—	OV_{DD}	
DIU_LD[7:9] cfg_io_ports[0:2]	U5, T7, R4	—	OV_{DD}	
DIU_LD[11:12] cfg_dram_type[0:1]	R7, R8	—	OV_{DD}	
DIU_DE, DIU_LD[13:15] cfg_rom_loc[0:3]	U4, T9, R9, T3	—	OV_{DD}	
DIU_VSYNC cfg_pci_impd	V7	—	OV_{DD}	
DIU_HSYNC cfg_pci_arb	U7	—	OV_{DD}	
$\overline{\text{UART_RTS0}}$ cfg_wdt_en	G26	—	OV_{DD}	

Table 1. Signal Reference by Functional Block (continued)

Name[1]	Package Pin Number	Pin Type	Power Supply	Notes
ASLEEP cfg_core_speed	B26	—	OV_{DD}	13
MSRCID0 cfg_mem_debug	Y20	—	BV_{DD}	
MDVAL cfg_boot_vector	AC20	—	BV_{DD}	

Notes:

1. Multi-pin signals such as LDP[0:3] have their physical package pin numbers listed in order corresponding to the signal names.
2. Stub series terminated logic type pins.
3. All SSI signals are multiplexed with eLBC signals.
4. Low voltage transistor-transistor logic (LVTTL) type pins.
5. DIU_LD[23:16] = RED[7:0].
   DIU_LD[15:8] = GREEN[7:0].
   DIU_LD[7:0] = BLUE[7:0].
6. The pins for the SSI interface on the device are multiplexed with certain eLBC signals, which have the ability to operate at a different voltage than the other standard I/O signals. If the device is configured such that the eLBC uses a different voltage than standard I/O and an SSI port on the device is used, then level shifters are required on the SSI signals to ensure they correctly interface to other devices on the board at the proper voltage.
7. This pin should be pulled to ground with a 100-Ω resistor.
8. This pin should be pulled to ground with a 200-Ω resistor.
9. These pins should be left floating.
10. This is a SerDes PLL/DLL digital test signal and is only for factory use.
11. This is a SerDes PLL/DLL analog test signal and is only for factory use.
12. This pin should be pulled down if the platform frequency is 400 MHz or below.
13. This pin should be pulled down if the core frequency is 800 MHz or below.
14. MSRCID[1:2], DIU_LD[5:6] and TRIG_OUT/READY should NOT be pulled down (or driven low) during reset.15. The pins in this section are reset configuration pins. Each pin has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
16. These pins should be left floating.
17. Must be tied low if unused.
18. This output is actively driven during reset rather than being tri-stated during reset.
19. MDIC[0] should be connected to ground with an 18-Ω resistor ± 1 Ω and MDIC[1] should be connected to GV_{DD} with an 18-Ω resistor ± 1 Ω. These pins are used for automatic calibration of the DDR IOs.
20. This pin is a reset configuration pin and appears again in the Reset Configuration Signals section of this table. See the Reset Configuration Signals section of this table for config name and connection details.
21. Recommend a weak pull-up resistor (1–10 kΩ) be placed from this pin to its power supply.
22. This multiplexed pin has input status in one mode and output in another.
23. This pin is a multiplexed signal for different functional blocks and appears more than once in this table.
24. For systems which boot from local bus (GPCM)-controlled flash, a pullup on LGPL4 is required.
25. This pin is open drain signal.
26. These are test signals for factory use only and must be pulled up (100 Ω to 1 kΩ) to OV_{DD} for normal machine operation.
27. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
28. These pins are connected to the power/ground planes internally and may be used by the core power supply to improve tracking and regulation.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications for the MPC8610. The MPC8610 is currently targeted to these specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 2 provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings[1]

Characteristic		Symbol	Recommended Value	Unit	Notes
Core supply voltages		V_{DD}_Core	–0.3 to 1.21	V	
Core PLL supply		AV_{DD}_Core	–0.3 to 1.21	V	
SerDes receiver and core power supply (ports 1 and 2)		$S1V_{DD}$ $S2V_{DD}$	–0.3 to 1.21	V	
SerDes transmitter power supply (ports 1 and 2)		$X1V_{DD}$ $X2V_{DD}$	–0.3 to 1.21	V	
SerDes digital logic power supply (ports 1 and 2)		$L1V_{DD}$ $L2V_{DD}$	–0.3 to 1.21	V	
Serdes PLL supply voltage (ports 1 and 2)		$SD1AV_{DD}$ $SD2AV_{DD}$	–0.3 to 1.21	V	
Platform supply voltage		V_{DD}_PLAT	–0.3 to 1.21	V	
PCI and platform PLL supply voltage		AV_{DD}_PCI AV_{DD}_PLAT	–0.3 to 1.21	V	
DDR/DDR2 SDRAM I/O supply voltages		GV_{DD}	–0.3 to 2.75	V	
Local bus and SSI I/O voltage		BV_{DD}	–0.3 to 3.63	V	
LCD, PCI, general purpose timer, MPIC, IrDA, DUART, DMA, interrupts, system control and clocking, debug, test, JTAG, power management, I^2C, SPI, and miscellaneous I/O voltage		OV_{DD}	–0.3 to 3.63	V	
Input voltage	DDR/DDR2 SDRAM signals	MV_{IN}	(GND – 0.3) to (GV_{DD} + 0.3)	V	2
	DDR/DDR2 SDRAM reference	MV_{REF}	(GND – 0.3) to (GV_{DD}/2 + 0.3)	V	2
	Local bus I/O voltage	BV_{IN}	(GND – 0.3) to (BV_{DD} + 0.3)	V	2
	LCD, PCI, general purpose, MPIC, IrDA, DUART, DMA, interrupts, system control and clocking, debug, test, JTAG, power management, I^2C, SPI and miscellaneous I/O voltage	OV_{IN}	(GND – 0.3) to (OV_{DD} + 0.3)	V	2

Table 2. Absolute Maximum Ratings[1] (continued)

Characteristic	Symbol	Recommended Value	Unit	Notes
Storage temperature range	T_{STG}	–55 to 150	°C	

Notes:

1 Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2 During run time (M, B, O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Table 2.

2.1.2 Recommended Operating Conditions

Table 3 provides the recommended operating conditions for the MPC8610. Note that the values in Table 3 are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed. For details on order information and specific operating conditions for parts, see Section 4, "Ordering Information."

Table 3. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltages	V_{DD}_Core	1.025 ± 50 mV	V	1
		1.00 ± 50 mV		2
Core PLL supply	AV_{DD}_Core	1.025 ± 50 mV	V	1, 3
		1.00 ± 50 mV		2, 3
SerDes receiver and core power supply (ports 1 and 2)	$S1V_{DD}$ $S2V_{DD}$	1.025 ± 50 mV	V	1, 4
		1.00 ± 50 mV		2
SerDes transmitter power supply (ports 1 and 2)	$X1V_{DD}$ $X2V_{DD}$	1.025 ± 50 mV	V	1
		1.00 ± 50 mV		2
SerDes digital logic power supply (ports 1 and 2)	$L1V_{DD}$ $L2V_{DD}$	1.025 ± 50 mV	V	1
		1.00 ± 50 mV		2
Serdes PLL supply voltage (ports 1 and 2)	$SD1AV_{DD}$ $SD2AV_{DD}$	1.025 ± 50 mV	V	1, 3
		1.00 ± 50 mV		2, 3
Platform supply voltage	V_{DD}_PLAT	1.025 ± 50 mV	V	1
		1.00 ± 50 mV		2
PCI and platform PLL supply voltage	AV_{DD}_PCI AV_{DD}_PLAT	1.025 ± 50 mV	V	1, 3
		1.00 ± 50 mV		2, 3
DDR and DDR2 SDRAM I/O supply voltages	GV_{DD}	2.5 V ± 125 mV, 1.8 V ± 90 mV	V	5
Local bus and SSI I/O voltage	BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	

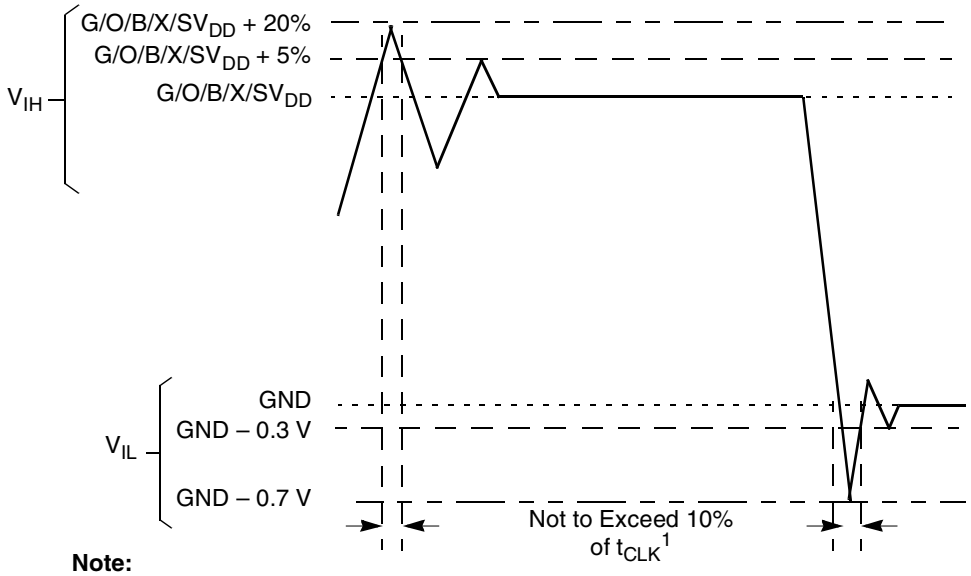
Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
LCD, PCI, general timer, MPIC, IrDA, DUART, DMA, interrupts, system control and clocking, debug, test, JTAG, power management, I^2C, SPI, and miscellaneous I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	6
Input voltage	DDR and DDR2 SDRAM signals	MV_{IN}	(GND – 0.3) to (GV_{DD} + 0.3)	V	7, 5
	DDR and DDR2 SDRAM reference	MV_{REF}	(GND – 0.3) to (GV_{DD}/2 + 0.3)	V	7
	Local Bus I/O voltage	BV_{IN}	(GND – 0.3) to (BV_{DD} + 0.3)		7
	LCD, PCI, general purpose timer, MPIC, IrDA, DUART, DMA, interrupts, system control and clocking, debug, test, JTAG, power management, I^2C, SPI, and miscellaneous I/O voltage	OV_{IN}	(GND – 0.3) to (OV_{DD} + 0.3)	V	7, 6
Junction temperature range		T_J	0 to 105	°C	
			–40 to 105		8

Notes:

1. Applies to devices marked with a core frequency of 1333 MHz. Refer to Table Part Numbering Nomenclature to determine if the device has been marked for a core frequency of 1333 MHz.
2. Applies to devices marked with a core frequency below 1333 MHz. Refer to Table Part Numbering Nomenclature to determine if the device has been marked for a core frequency below 1333 MHz.
3. AVDD measurements are made at the input of the R/C filter described in Section 3.2.1, “PLL Power Supply Filtering,” and not at the processor pin.
4. PCI Express interface of the device is expected to receive signals from 0.175 to 1.2 V. Refer to Section 2.18.4.3, “Differential Receiver (RX) Input Specifications,” for more information.
5. **Caution:** MV_{IN} must meet the overshoot/undershoot requirements for GV_{DD} as shown in Figure 2.
6. **Caution:** OV_{IN} must meet the overshoot/undershoot requirements for OV_{DD} as shown in Figure 2.
7. Timing limitations for (M, B, O) V_{IN} and MV_{REF} during regular run time is provided in Figure 2.
8. Applies to devices marked MC8610TxxyyyyMz for extended temperature range. Note that MC8610Txx1333Jz is not offered.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8610.



Note:
1. t_{CLK} references clocks for various functional blocks as follows:
For DDR, t_{CLK} references MCK.
For LBIU, t_{CLK} references LCLK.
For PCI, t_{CLK} references PCI_CLK or SYSCLK.
For I^2C and JTAG, t_{CLK} references SYSCLK.

Figure 2. Overshoot/Undershoot Voltage for M/B/OV_{IN}

The MPC8610 core voltage must always be provided at nominal V_{DD}_Core (see Table 3 for actual recommended core voltage). Voltage to the external interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD}-based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced to each externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the (SSTL-18 and SSTL-2) electrical signaling standards.

2.1.3 Output Driver Characteristics

Table 4 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
DDR signals	18 36 (half strength mode)	GV_{DD} = 2.5 V	1, 4, 6
DDR2 signals	18 36 (half strength mode)	GV_{DD} = 1.8 V	1, 5, 6

Table 4. Output Drive Capability (continued)

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus	25 35	BV_{DD} = 3.3 V BV_{DD} = 2.5 V	2
	45 (default) 45 (default) 125	BV_{DD} = 3.3 V BV_{DD} = 2.5 V BV_{DD} = 1.8 V	
PCI, DUART, DMA, interrupts, system control and clocking, debug, test, JTAG, power management, and miscellaneous I/O voltage	45	OV_{DD} = 3.3 V	
I^2C	150	OV_{DD} = 3.3 V	
PCI Express	100	XV_{DD} = 1.0 V	3

Notes:
1. See the DDR control driver registers in the *MPC8610 Integrated Host Processor Reference Manual,* for more information.
2. See the POR impedance control register in the *MPC8610 Integrated Host Processor Reference Manual,* for more information about local bus signals and their drive strength programmability.
3. See Section 1, "Pin Assignments and Reset States," for details on resistor requirements for the calibration of SD*n*_IMP_CAL_TX and SD*n*_IMP_CAL_RX transmit and receive signals.
4. Stub series terminated logic (SSTL-25) type pins.
5. Stub series terminated logic (SSTL-18) type pins.
6. The drive strength of the DDR interface in half strength mode is at T_j = 105°C and at GV_{DD} (min).

2.2 Power Sequencing

The MPC8610 requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows:

The chronological order of power up is:

1. OV_{DD}, BV_{DD}
2. V_{DD}_PLAT, AV_{DD}_PLAT, V_{DD}_Core, AV_{DD}_Core, AV_{DD}_PCI, S*n*V_{DD}, X*n*V_{DD}, SD*n*AV_{DD} (this rail must reach 90% of its value before the rail for GV_{DD} and MV_{REF} reaches 10% of its value)
3. GV_{DD}, MV_{REF}
4. SYSCLK

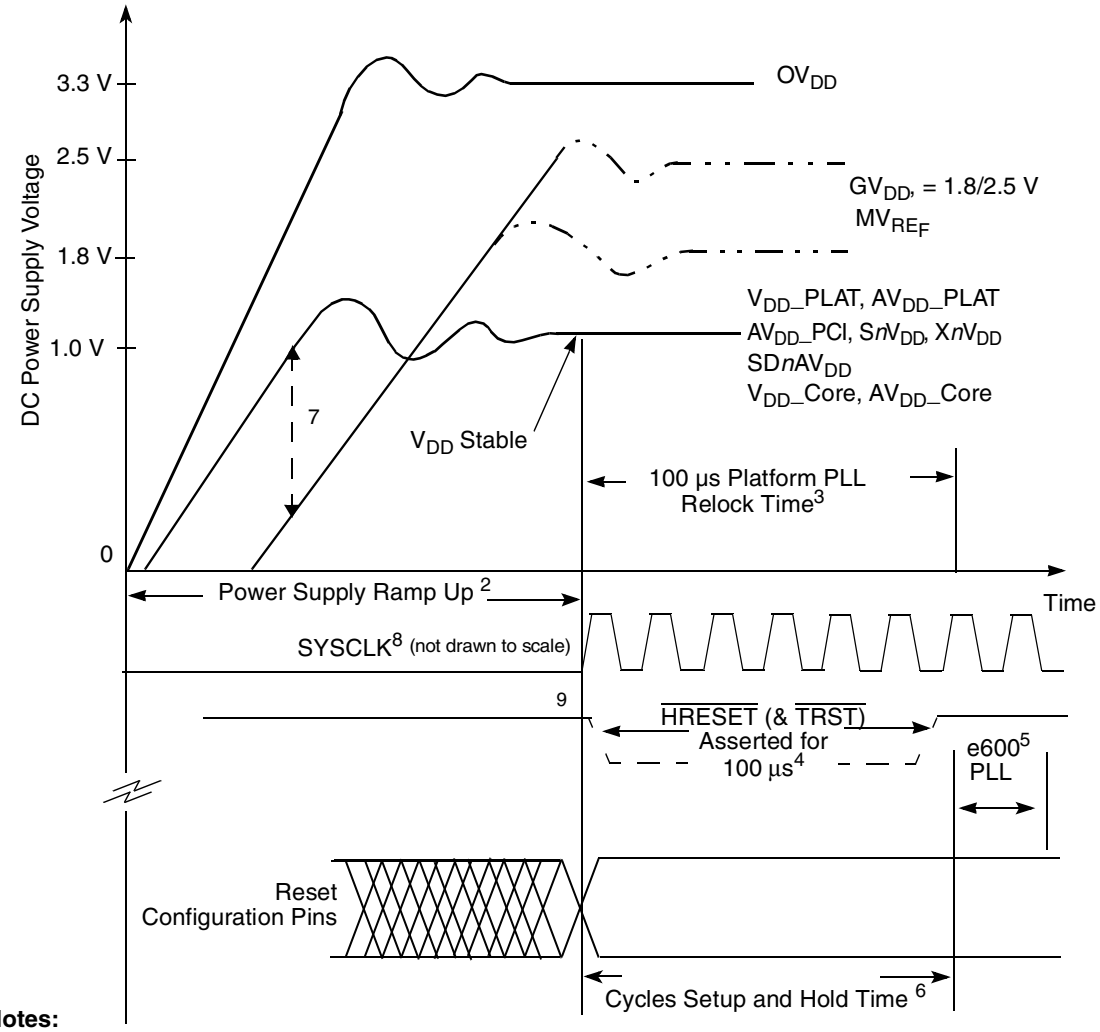
The order of power down is as follows:

1. SYSCLK
2. GV_{DD}, MV_{REF}
3. V_{DD}_PLAT, AV_{DD}_PLAT, V_{DD}_Core, AV_{DD}_Core, AV_{DD}_PCI, S*n*V_{DD}, X*n*V_{DD}, SD*n*AV_{DD}
4. O_{DD}, BV_{DD}

NOTE

AV_{DD} type supplies should be delayed with respect to their source supplies by the RC time constant of the PLL filter circuit described in Section 3.2, "Power Supply Design and Sequencing."

Figure 3 illustrates the power up sequence as described above.



Notes:

1. Dotted waveforms correspond to optional supply values for a specified power supply. See Table 3.
2. Ther recommended maximum ramp up time for power supplies is 20 milliseconds.
3. Refer to Section 2.5, "RESET Initialization" for additional information on PLL relock and reset signal assertion timing requirements.
4. Refer to Table 9 for additional information on reset configuration pin setup timing requirements. In addition see Figure 53 regarding $\overline{\text{HRESET}}$ and JTAG connection details including $\overline{\text{TRST}}$.
5. e600 PLL relock time is 100 microseconds maximum plus 255 MPX_clk cycles.
6. Stable PLL configuration signals are required as stable SYSCLK is applied. All other POR configuration inputs are required 4 SYSCLK cycles before $\overline{\text{HRESET}}$ negation and are valid at least 2 SYSCLK cycles after $\overline{\text{HRESET}}$ has negated (hold requirement). See Section 2.5, "RESET Initialization," for more information on setup and hold time of reset configuration signals.
7. The rail for V_{DD}_PLAT, AV_{DD}_PLAT, V_{DD}_Core, AV_{DD}_Core, AV_{DD}_PCI, SnV_{DD}, XnV_{DD}, and $SDnAV_{DD}$ must reach 90% of its value before the rail for GV_{DD} and MV_{REF} reaches 10% of its value.
8. SYSCLK must be driven only AFTER the power for the various power supplies is stable.
9. The reset configuration signals for DRAM types must be valid before $\overline{\text{HRESET}}$ is asserted.

Figure 3. MPC8610 Power Up Sequencing

2.3 Power Characteristics

The power dissipation for the MPC8610 device is shown in Table 5.

Table 5. MPC8610 Power Dissipation

Power Mode	Core/Platform Frequency (MHz)	V_{DD}_Core, V_{DD}_PLAT (V)	Junction Temperature (°C)	Power (Watts)	Notes
Typical	1333/533	1.025	65	10.7	1, 2
Thermal			105	12.1	1, 3
Maximum				16	1, 4
Typical	1066/533	1.00	65	8.4	1, 2
Thermal			105	9.8	1, 3
Maximum				13	1, 4
Typical	800/400	1.00	65	5.8	1, 2
Thermal			105	7.2	1, 3
Maximum				9.5	1, 4

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}_Core) and 65°C junction temperature (see Table 3) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz with the core at 100% efficiency. This parameter is not 100% tested but periodically sampled.
3. Thermal power is the average power measured at nominal core voltage (V_{DD}_Core) and maximum operating junction temperature (see Table 3) while running the Dhrystone 2.1 benchmark and achieving 2.3 Dhrystone MIPs/MHz on the core and a typical workload on platform interfaces. This parameter is not 100% tested but periodically sampled.
4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}_Core) and maximum operating junction temperature (see Table 3) while running a test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep all the execution units maximally busy on the core.

The estimated maximum power dissipation for individual power supplies of the MPC8610 is shown in Table 6.

Table 6. MPC8610 Individual Supply Maximum Power Dissipation[1]

Component Description	Supply Voltage (V)	Est. Power (Watts)	Notes
Core voltage supply	V_{DD}_Core = 1.025 V @ 1333 MHz	14.0	
	V_{DD}_Core = 1.00 V @ 1066 MHz	12.0	
Core PLL voltage supply	AV_{DD}_Core = 1.025 V @ 1333 MHz	0.0125	
	AV_{DD}_Core = 1.00 V @ 1066 MHz	0.0125	
Platform source supply	V_{DD}_PLAT = 1.025 V @ 1333 MHz	4.5	
	V_{DD}_PLAT = 1.00 V @ 1066 MHz	4.3	

Table 6. MPC8610 Individual Supply Maximum Power Dissipation[1] (continued)

Component Description	Supply Voltage (V)	Est. Power (Watts)	Notes
Platform PLL voltage supply	AV_{DD}_PLAT = 1.025 V @ 1333 MHz	0.0125	
	AV_{DD}_PLAT = 1.00 V @ 1066 MHz	0.0125	

Notes:

1. This is a maximum power supply number which is provided for power supply and board design information. The numbers are based on 100% utilization for each component. The components listed are not expected to have 100% usage simultaneously for all components. Actual numbers may vary based on activity. Note that the production parts should have a total maximum power value based on Table 5. The 'Est.' in the Est. Power column is to emphasize that these numbers are based on theoretical estimates. The device is tested to ensure that the sum of all four supplies does not exceed the power stated in Table 5. No specific supply should ever exceed its individual amount estimated in Table 6.

2.3.1 Frequency Derating

To reduce power consumption, these devices support frequency derating if the reduced maximum processor core frequency and reduced maximum platform frequency requirements are observed. The reduced maximum processor core frequency, resulting maximum platform frequency and power consumption are provided in Table 7. Only those parameters in Table 7 are affected; all other parameter specifications are unaffected.

Table 7. Core Frequency, Platform Frequency and Power Consumption Derating

Maximum Rated Core Frequency (Device Marking)	Maximum Derated Core/Platform Frequency (MHz)	V_{DD}_Core, V_{DD}_PLAT (V)	Typical Power (Watts)	Thermal Power (Watts)	Maximum Power (Watts)
1333J	N/A				
1066J	1000/400	1.00	8.0	9.4	12.5
800G	667/333	1.00	5.0	6.4	8.5

2.4 Input Clocks

Table 8 provides the system clock (SYSCLK) DC specifications for the MPC8610.

Table 8. SYSCLK DC Electrical Characteristics (OV_{DD} = 3.3 V ± 165 mV)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA

[1] Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.4.1 System Clock Timing

Table 9 provides the system clock (SYSCLK) AC timing specifications for the MPC8610.

Table 9. SYSCLK AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	—	—	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	1.2	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3
SYSCLK jitter	—	—	—	±150	ps	4, 5

Notes:
All specifications at recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV.
1. **Caution:** The platform to SYSCLK clock ratio and e600 core to platform clock ratio settings must be chosen such that the resulting SYSCLK, platform, and e600 (core) frequencies do not exceed their respective maximum or minimum operating frequencies. Refer to Section 3.1.2, "Platform/MPX to SYSCLK PLL Ratio" and Section 3.1.3, "e600 Core to MPX/Platform Clock PLL Ratio," for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.4 and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the short term jitter only and is guaranteed by design.
5. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter. Note that the frequency modulation for SYSCLK reduces significantly for the spread spectrum source case. This is to guarantee what is supported based on design.

2.4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are a popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise over a wider spectrum and reducing the peak noise magnitude. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 9 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the MPC8610 input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8610 is compatible with spread spectrum sources if the recommendations listed in Table 10 are observed.

Table 10. Spread Spectrum Clock Source Recommendations

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	50	kHz	1
Frequency spread	—	1.0	%	1, 2

Notes:
All specifications at recommended operating conditions (see Table 3).
1. Guaranteed by design.
2. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 10.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e600 core frequency should avoid violating the stated limits by using down-spreading only.

SD*n*_REF_CLK and $\overline{\text{SD}n\text{_REF_CLK}}$ was designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results use a source without significant unintended modulation.

2.4.2 Real Time Clock Timing

The RTC input is sampled by the platform clock. The output of the sampling latch is then used as an input to the counters of the PIC. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2× the period of the platform clock. That is, minimum clock high time is $2 \times t_{MPX}$, and minimum clock low time is $2 \times t_{MPX}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

2.4.3 PCI/PCI-X Reference Clock Timing

When the PCI/PCI-X controller is configured for asynchronous operation, the reference clock for the PCI/PCI-X controller is not the SYSCLK input, but instead the PCI*n*_CLK. Table 11provides the PCI/PCI-X reference clock AC timing specifications for the MPC8610.

Table 11. PCI*n*_CLK AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
PCI*n*_CLK frequency	f_{PCICLK}	16	—	133	MHz	—
PCI*n*_CLK cycle time	t_{PCICLK}	7.5	—	60	ns	—
PCI*n*_CLK rise and fall time	t_{PCIKH}, t_{PCIKL}	0.6	1.0	2.1	ns	1, 2
PCI*n*_CLK duty cycle	$t_{PCIKHKL}/t_{PCICLK}$	40	—	60	%	2

Notes:
1. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
2. Timing is guaranteed by design and characterization.

2.4.4 Platform Frequency Requirements for PCI-Express

The MPX platform clock frequency must be considered for proper operation of the high-speed PCI Express interface as described below.

For proper PCI Express operation, the MPX clock frequency must be greater than or equal to:

$$\frac{\text{527 MHz x (PCI-Express link width)}}{\text{16 / (1 + cfg_net2_div)}}$$

Note that at MPX = 333 - 400 MHz, cfg_net2_div = 0 and at MPX > 400 MHz, cfg_net2_div = 1. Therefore, when operating PCI Express in x8 link width, the MPX platform frequency must be 333-400 MHz with cfg_net2_div = 0 or greater than or equal to 527 MHz with cfg_net2_div = 1.

2.4.5 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes see the specific section of this document.

2.5 RESET Initialization

Table 12 describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8610.

Table 12. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	µs	
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1
Platform PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	µs	2
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Notes:
1. SYSCLK is he primary clock input for the device.
2. This is related to $\overline{\text{HRESET}}$ assertion time.

Table 13 provides the PLL lock times.

Table 13. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times (platform, PCI and e600 core)	—	100	µs	1

Notes:
1. The PLL lock time for the e600 core PLL requires an additional 255 platform clock cycles.

2.6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8610. Note that DDR SDRAM is GV_{DD} = 2.5 V and DDR2 SDRAM is GV_{DD} = 1.8 V.

2.6.1 DDR SDRAM DC Electrical Characteristics

Table 14 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8610 when GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.125	GV_{DD} + 0.3	V	
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	
Output leakage current	I_{OZ}	–50	50	µA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 15 provides the DDR capacitance when GV_{DD}(typ) = 1.8 V.

Table 15. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 16 provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5 V.

Table 16. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.15	GV_{DD} + 0.3	V	
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.15	V	
Output leakage current	I_{OZ}	–50	50	µA	4

Table 16. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA	
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 17 provides the DDR capacitance when GV_{DD} (typ)=2.5 V.

Table 17. DDR SDRAM Capacitance for GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 18 provides the current draw characteristics for MV_{REF}.

Table 18. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

2.6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR/DDR2 SDRAM interface.

2.6.2.1 DDR SDRAM Input AC Timing Specifications

Table 19 provides the input AC timing specifications for the DDR2 SDRAM when GV_{DD}(typ)=1.8 V.

Table 19. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V

Table 20 provides the input AC timing specifications for the DDR SDRAM when GV_{DD}(typ)=2.5 V.

Table 20. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V

Table 21 provides the input AC timing specifications for the DDR SDRAM interface.

Table 21. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}			ps	1, 2
533 MHz		–300	300		3
400 MHz		–365	365		
333 MHz		–390	390		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[*n*] and any corresponding bit that will be captured with MDQS[*n*]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: $t_{DISKEW} = \pm(T/4 - abs(t_{CISKEW}))$, where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.
3. Maximum DDR1 frequency is 400 MHz.

Figure 4 shows the DDR SDRAM input timing for the MDQS to MDQ skew measurement (t_{DISKEW}).

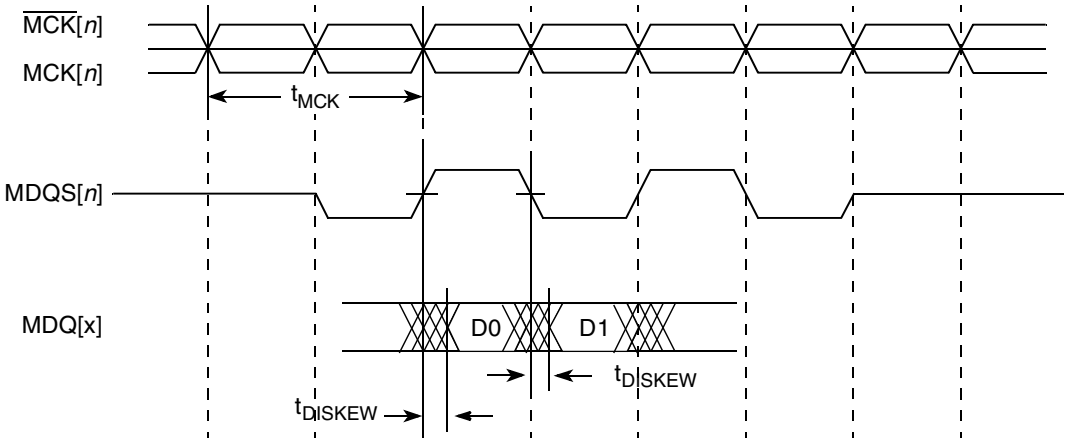


Figure 4. DDR Input Timing Diagram for tDISKEW

2.6.2.2 DDR SDRAM Output AC Timing Specifications

Table 22. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	3	10	ns	2
MCK duty cycle	t_{MCKH}/t_{MCK}			%	
533 MHz		47	53		8
400 MHz		47	53		8
333 MHz		47	53		
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
533 MHz		590	—		7
400 MHz		700	—		
333 MHz		900	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
533 MHz		590	—		7
400 MHz		700	—		
333 MHz		900	—		
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6

Table 22. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8610 Integrated Host Processor Reference Manual,* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[*n*] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. Maximum DDR1 frequency is 400 MHz.
8. Per the JEDEC spec the DDR2 duty cycle at 400 and 533 MHz is the low and high cycle time values.

NOTE

For the ADDR/CMD setup and hold specifications in Table 22, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 5 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

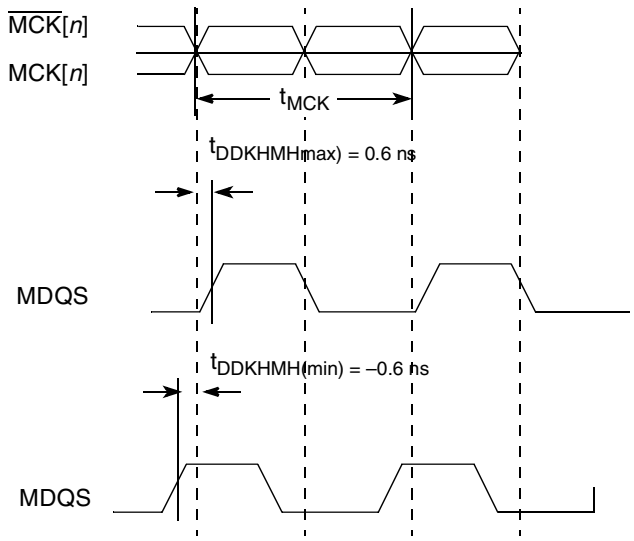


Figure 5. Timing Diagram for tDDKHMH

Figure 6 shows the DDR SDRAM output timing diagram.

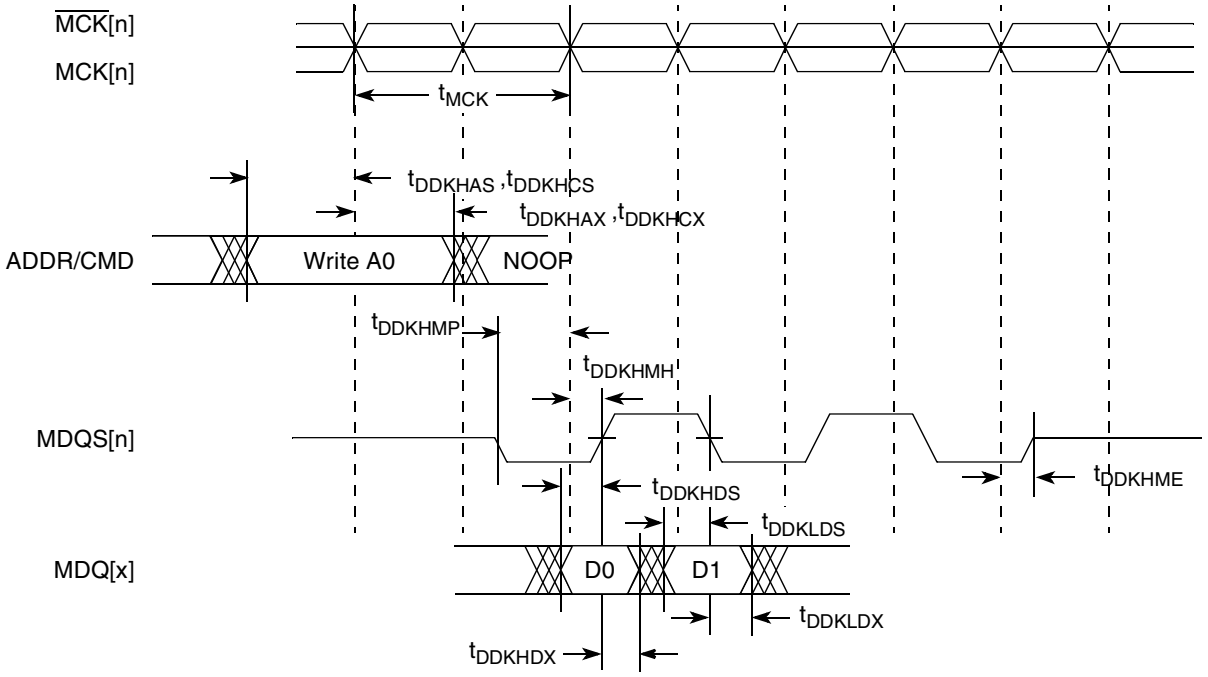


Figure 6. DDR SDRAM Output Timing Diagram

Figure 7 provides the AC test load for the DDR bus.

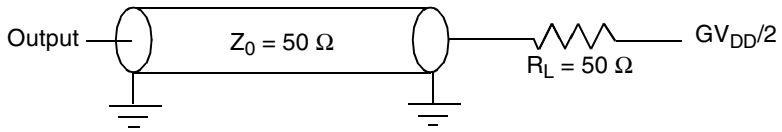


Figure 7. DDR AC Test Load

2.7 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8610.

2.7.1 Local Bus DC Electrical Characteristics

Table 23 provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 3.3 V.

Table 23. Local Bus DC Electrical Characteristics (BV_{DD} = 3.3 V)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±5	μA
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	BV_{DD} – 0.2	—	V

Table 23. Local Bus DC Electrical Characteristics (BV_{DD} = 3.3 V) (continued)

Parameter	Symbol	Min	Max	Unit
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 2 and Table 3.

Table 24 provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 2.5 V DC.

Table 24. Local Bus DC Electrical Characteristics (BV_{DD} = 2.5 V)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	1.70	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.7	V
Input current (V_{IN}[1] = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±15	μA
High-level output voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V

Note:
1. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 2 and Table 3.

Table 25 provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 1.8 V.

Table 25. Local Bus DC Electrical Characteristics (BV_{DD} = 1.8 V)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	1.3	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±15	μA
High-level output voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	1.42	—	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 2 and Table 3.

2.7.2 Local Bus AC Electrical Specifications

Table 26 describes the general timing parameters of the local bus interface at BV_{DD} = 3.3 V, 2.5 V and 1.8 V. For information about the frequency range of local bus see Section 3.1.1, “Clock Ranges.”

Table 26. Local Bus Timing Parameters (BV_{DD} = 3.3 V, 2.5 V and 1.8 V)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	—	ns	
Local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	
LCLK[n] skew to LCLK[m]	$t_{LBKSKEW}$	—	100	ps	2, 7

Table 26. Local Bus Timing Parameters (BV_{DD} = 3.3 V, 2.5 V and 1.8 V) (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	4.5	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	4.3	—	ns	3, 4
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	—	0.8	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	—	0.7	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	0.75	—	ns	5
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	1.1	ns	
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	1.2	ns	3
Local bus clock to address valid for LAD, and LALE	$t_{LBKLOV3}$	—	1.2	ns	3
Local bus clock to LALE assertion	$t_{LBKLOV4}$	—	1.4	ns	
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	-0.6	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	-0.6	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	2.5	ns	6
Local bus clock to output high Impedance for LAD/LDP	$t_{LBKLOZ2}$	—	2.5	ns	6

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$. Skew number is valid only when LCLK[m] and LCLK[n] have the same load.
3. All signals are measured from $BV_{DD}/2$ of the edge of local bus clock to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD.
6. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
7. Guaranteed by design.

Figure 8 provides the AC test load for the local bus.

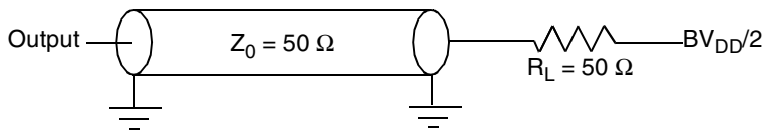


Figure 8. Local Bus AC Test Load

Figure 9 to Figure 11 show the local bus signals.

NOTE

Output signals are latched at the falling edge of LCLK and input signals are captured at the rising edge of LCLK, with the exception of the $\overline{\text{LGTA}}$/LUPWAIT signal, which is captured at the falling edge of LCLK.

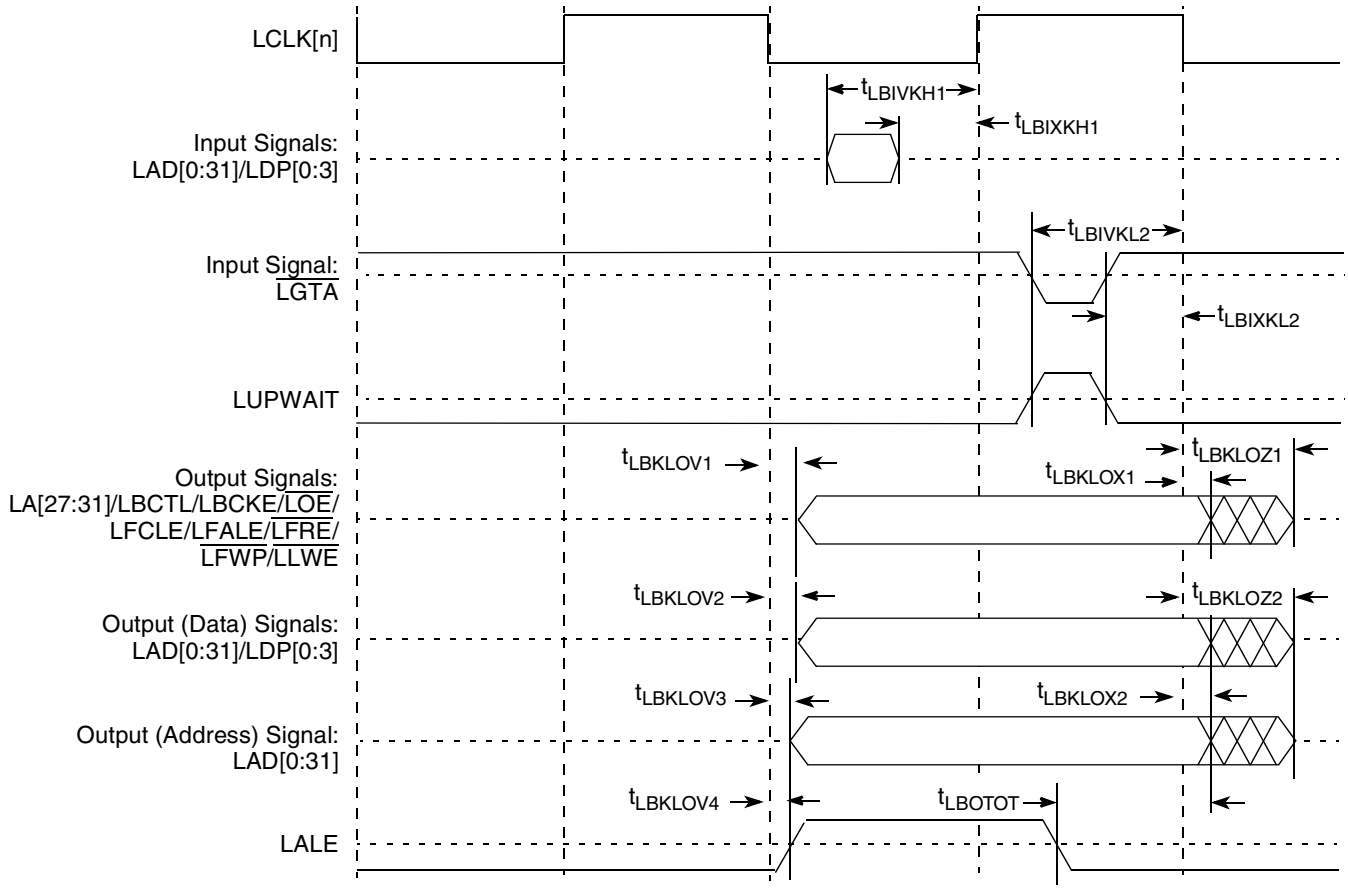


Figure 9. Local Bus Signals

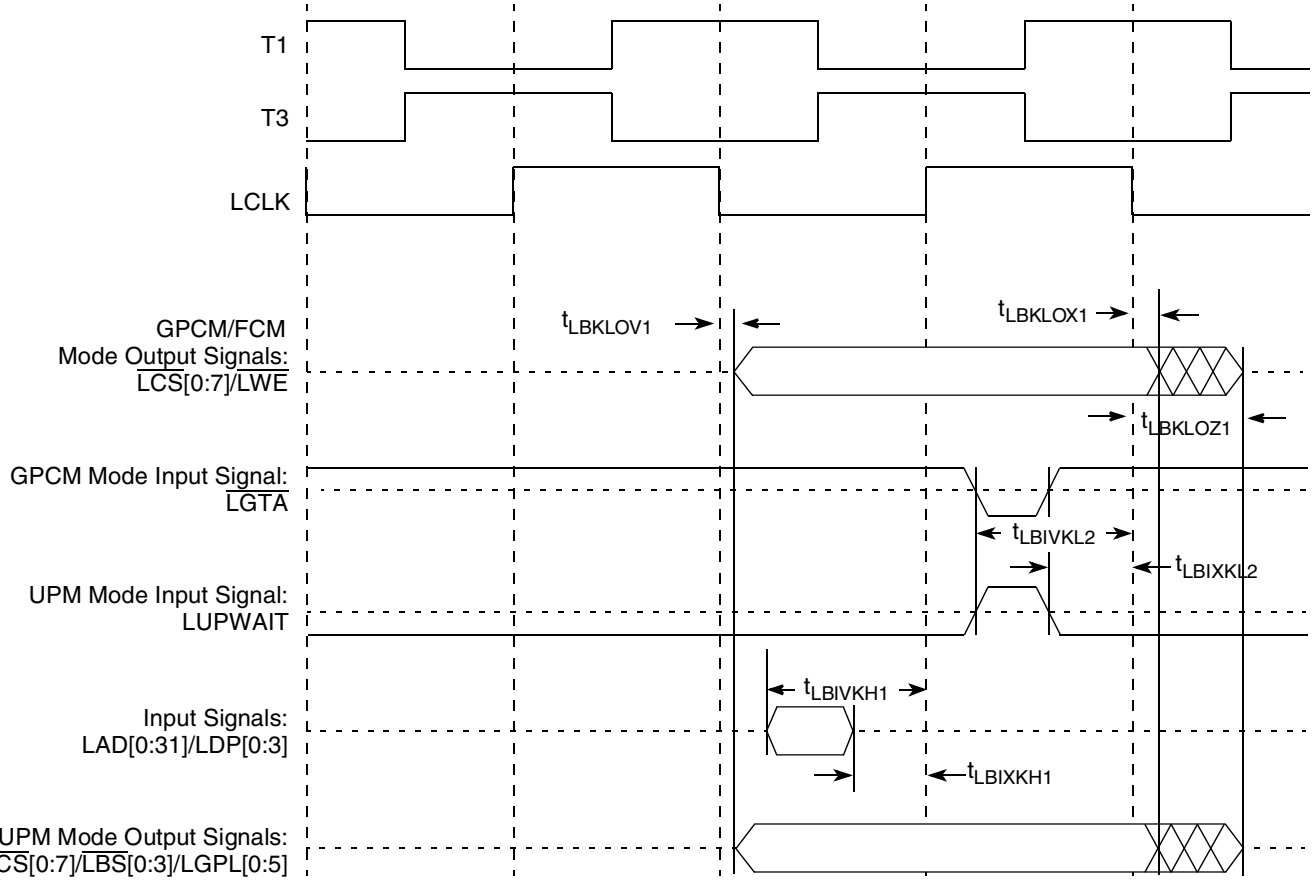


Figure 10. Local Bus Signals, GPCM/UPM/FCM Signals for LCRR[CLKDIV] = 2 (Clock Ratio of 4)

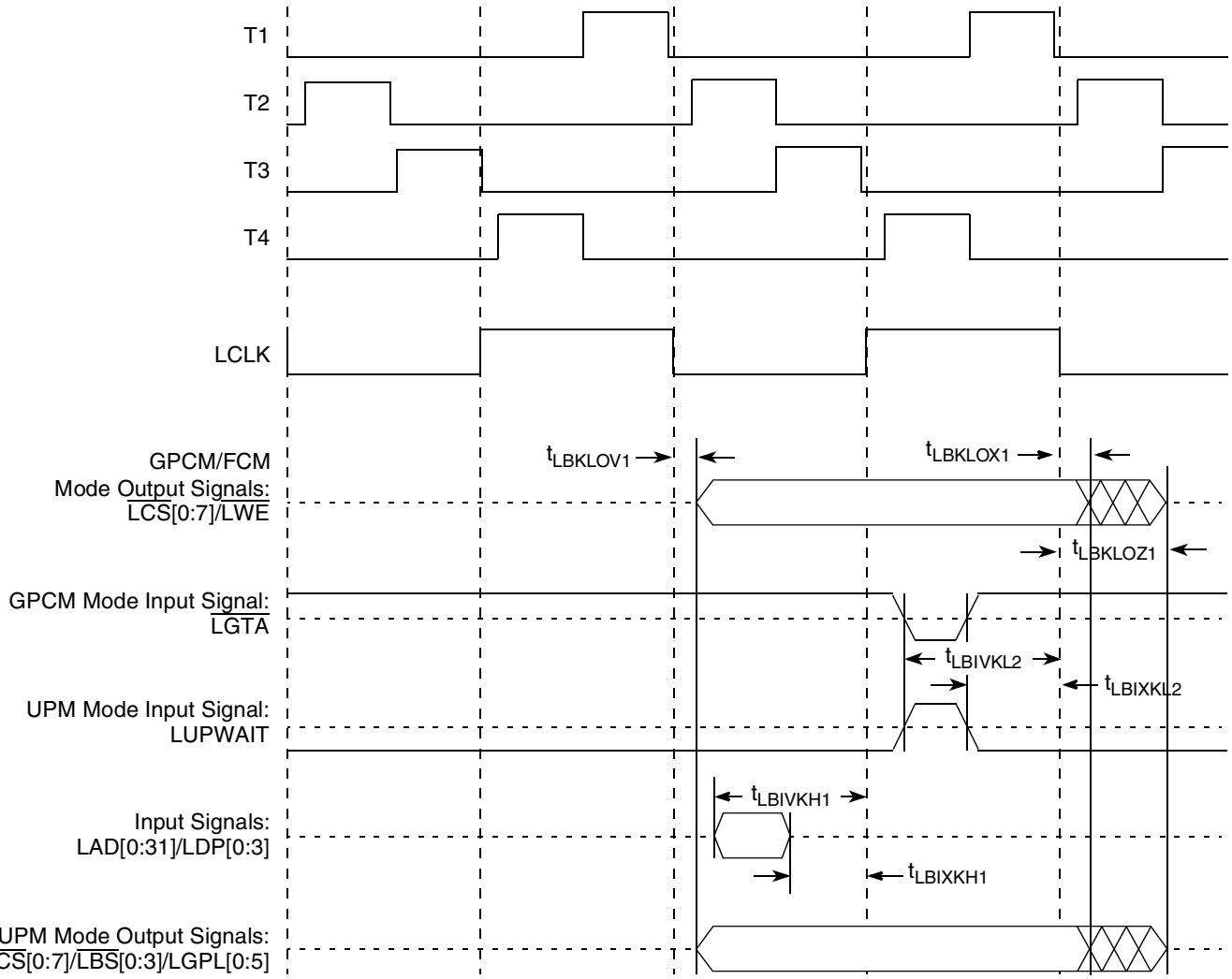


Figure 11. Local Bus Signals, GPCM/UPM/FCM Signals for LCRR[CLKDIV] = 4 or 8 (Clock Ratio of 8 or 16)

2.8 Display Interface Unit

This section describes the DIU DC and AC electrical specifications.

2.8.1 DIU DC Electrical Characteristics

Table 27 provides the DIU DC electrical characteristics.

Table 27. DIU DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = mn, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V

Table 27. DIU DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 µA)	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.8.2 DIU AC Timing Specifications

Figure 12 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All parameters shown in the diagram are programmable. This timing diagram corresponds to positive polarity of the DIU_CLK_OUT signal and active-high polarity of the DIU_HSYNC, DIU_VSYNC, and DIU_DE signals. By default, all control signals and the display data are generated at the rising edge of the internal pixel clock, and the DIU_CLK_OUT output to drive the panel has the same polarity with the internal pixel clock. User can select the polarity of the DIU_HSYNC and DIU_VSYNC signal (via the SYN_POL register), whether active-high or active-low, the default is active-high. The DIU_DE signal is always active-high.

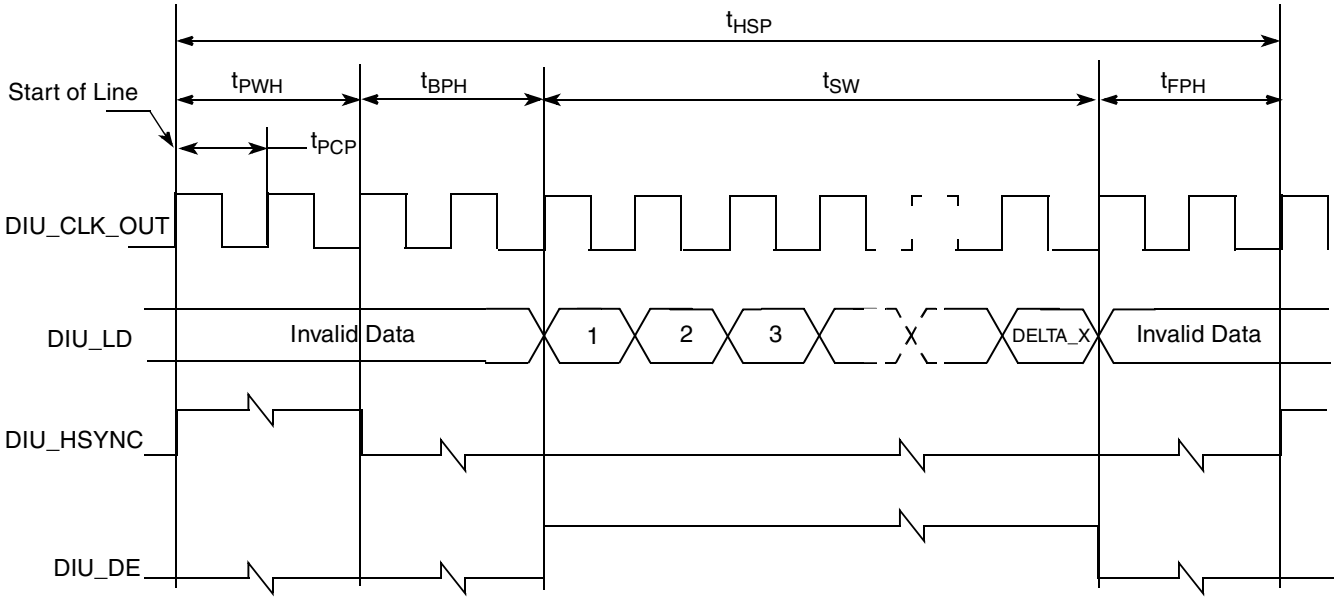


Figure 12. TFT DIU/LCD Interface Timing Diagram—Horizontal Sync Pulse

Figure 13 depicts the vertical timing (timing of one frame), including both the vertical sync pulse and the data. All parameters shown in the diagram are programmable.

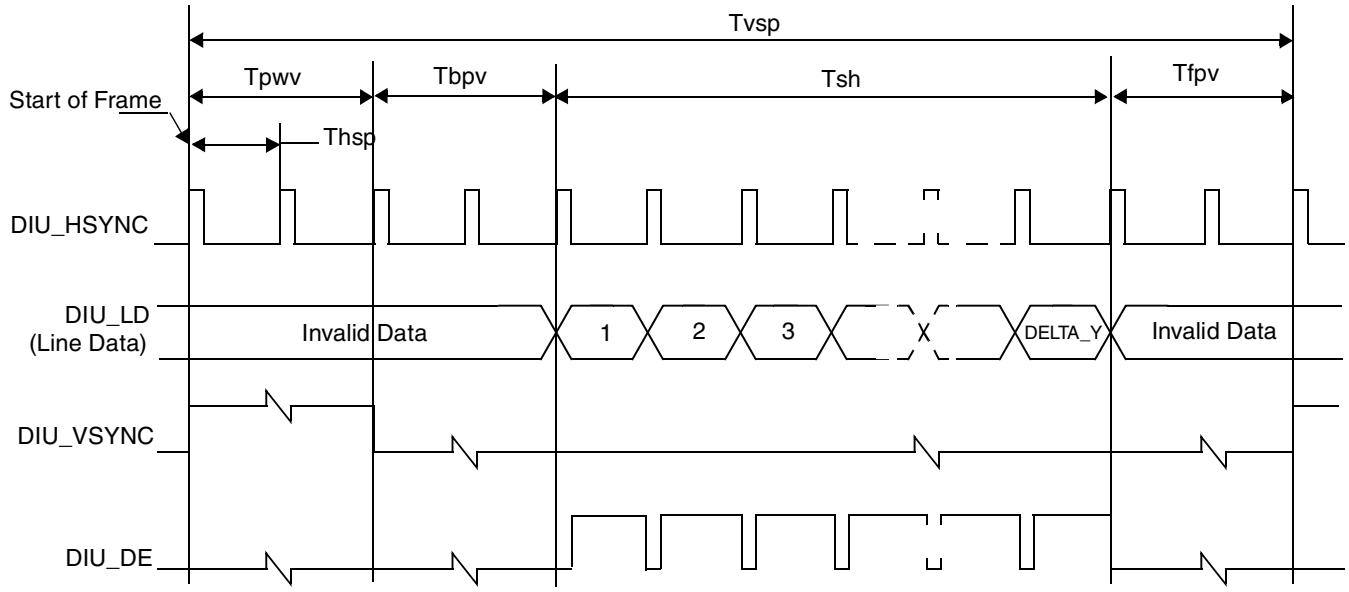


Figure 13. TFT DIU/LCD Interface Timing Diagram—Vertical Sync Pulse

Table 28 shows timing parameters of signals presented in Figure 12 and Figure 13.

Table 28. DIU Interface AC Timing Parameters—Pixel Level

Parameter	Symbol	Value	Unit	Notes
Display pixel clock period	t_{PCP}	7.5 (minimum)	ns	1, 2
HSYNC width	t_{PWH}	PW_H × t_{PCP}	ns	
HSYNC back porch width	t_{BPH}	BP_H × t_{PCP}	ns	
HSYNC front porch width	t_{FPH}	FP_H × t_{PCP}	ns	
Screen width	t_{SW}	DELTA_X × t_{PCP}	ns	
HSYNC (line) period	t_{HSP}	(PW_H + BP_H + DELTA_X + FP_H) × t_{PCP}	ns	
VSYNC width	t_{PWV}	PW_V × t_{HSP}	ns	
HSYNC back porch width	t_{BPV}	BP_V × t_{HSP}	ns	
HSYNC front porch width	t_{FPV}	FP_V × t_{HSP}	ns	
Screen height	t_{SH}	DELTA_Y × t_{HSP}	ns	
VSYNC (frame) period	t_{VSP}	(PW_V + BP_V + DELTA_Y + FP_H) × t_{HSP}	ns	

Notes:

1 Display interface pixel clock period immediate value (in nanoseconds).

2 Display pixel clock frequency must also be less than or equal to 1/3 the platform clock.

The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H, and FP_H parameters are programmed via the HSYN_PARA register; and the PW_V, BP_V, and FP_V parameters are programmed via the VSYN_PARA register.

Figure 14 depicts the synchronous display interface timing for access level, and Table 29 lists the timing parameters.

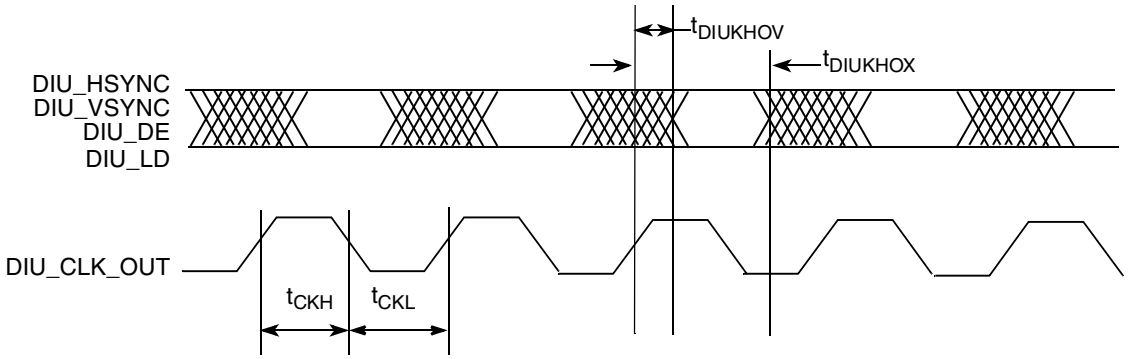


Figure 14. LCD Interface Timing Diagram—Access Level

NOTE

The DIU_OUT_CLK edge and phase delay is selectable via the Global Utilities CKDVDR register.

Table 29. LCD Interface Timing Parameters—Access Level

Parameter	Symbol	Min	Typ	Max	Unit
LCD interface pixel clock high time	t_{CKH}	$0.35 \times t_{PCP}$	$0.5 \times t_{PCP}$	$0.65 \times t_{PCP}$	ns
LCD interface pixel clock low time	t_{CKL}	$0.35 \times t_{PCP}$	$0.5 \times t_{PCP}$	$0.65 \times t_{PCP}$	ns
LCD interface pixel clock to ouput valid	$t_{DIUKHOV}$	—	—	2	ns
LCD interface output hold from pixel clock	$t_{DIUKHOX}$	$t_{PCP} - 2$	—	—	ns

2.9 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8610.

2.9.1 I²C DC Electrical Characteristics

Table 30 provides the DC electrical characteristics for the I²C interfaces.

Table 30. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2

Table 30. I^2C DC Electrical Characteristics (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	µA	3
Capacitance for each I/O pin	C_I	—	10	pF	

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8610 Integrated Host Processor Reference Manual*, for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.9.2 I^2C AC Electrical Specifications

Table 31 provides the AC timing parameters for the I^2C interfaces.

Table 31. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 30).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}[4]	1.3	—	µs
High period of the SCL clock	t_{I2CH}[4]	0.6	—	µs
Setup time for a repeated START condition	t_{I2SVKH}[4]	0.6	—	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}[4]	0.6	—	µs
Data setup time	t_{I2DVKH}[4]	100	—	ns
Data input hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	 — 0[2]	 — —	µs
Data ouput delay time	t_{I2OVKL}	—	0.9 [3]	µs
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Table 31. I^2C AC Electrical Specifications (continued)

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 30).

Parameter	Symbol[1]	Min	Max	Unit
Capacitive load for each bus line	Cb	—	400	pF

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I^2C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I^2C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I^2C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. As a transmitter, the MPC8610 provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of Start or Stop condition. When MPC8610 acts as the I^2C bus master while transmitting, MPC8610 drives both SCL and SDA. As long as the load on SCL and SDA are balanced, MPC8610 would not cause unintended generation of Start or Stop condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for MPC8610 as transmitter, the following setting is recommended for the FDR bit field of the I2CFDR register to ensure both the desired I^2C SCL clock frequency and SDA output delay time are achieved, assuming that the desired I^2C SCL clock frequency is 400 kHz and the digital filter sampling rate register (I2CDFSRR) is programmed with its default setting of 0x10 (decimal 16):

I^2C source clock frequency	533 MHz	400 MHz	333 MHz	266 MHz
FDR bit setting	0x0A	0x07	0x2A	0x05
Actual FDR divider selected	1536	1024	896	704
Actual I^2C SCL frequency generated	347 kHz	391 kHz	371 kHz	378 kHz

   For the detail of I^2C frequency calculation, refer to Freescale application note AN2919, *Determining the I^2C Frequency Divider Ratio for SCL*. Note that the I^2C source clock frequency is equal to the MPX clock frequency for MPC8610.
3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. Guaranteed by design.

Figure 15 provides the AC test load for the I^2C.

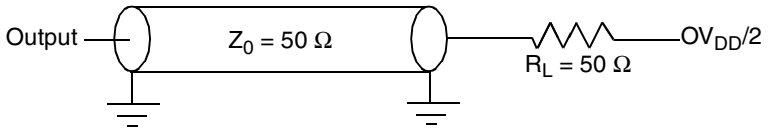


Figure 15. I^2C AC Test Load

Figure 16 shows the AC timing diagram for the I^2C bus.

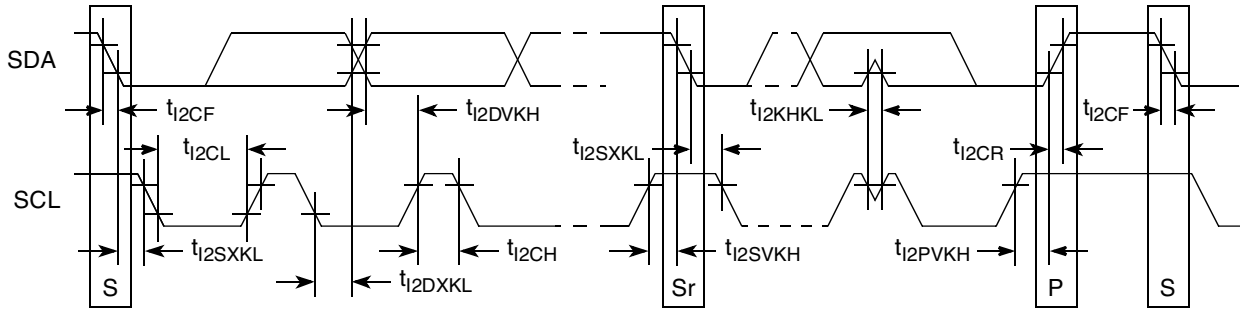


Figure 16. I^2C Bus AC Timing Diagram

2.10 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8610.

2.10.1 DUART DC Electrical Characteristics

Table 32 provides the DC electrical characteristics for the DUART interface.

Table 32. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = mn, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.10.2 DUART AC Electrical Specifications

Table 33 provides the AC timing parameters for the DUART interface.

Table 33. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	Platform clock/1,048,576	baud	1
Maximum baud rate	Platform clock/16	baud	1, 2
Oversample rate	16	—	1, 3

Notes:
1. Guaranteed by design.
2. Actual attainable baud rate will be limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

2.11 Fast/Serial Infrared Interfaces (FIRI/SIRI)

The fast/serial infrared interfaces (FIRI/SIRI) implements asynchronous infrared protocols (FIR, MIR, SIR) that are defined by IrDA (Infrared Data Association). Refer to http://www.IrDA.org for details on FIR and SIR protocols.

2.12 Synchronous Serial Interface (SSI)

This section describes the DC and AC electrical specifications for the SSI interface of the MPC8610.

2.12.1 SSI DC Electrical Characteristics

Table 34 provides SSI DC electrical characteristics.

Table 34. SSI DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (BV_{IN}[1] = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±5	μA
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	BV_{DD} – 0.2	—	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.2	V

Note:
1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 2 and Table 3.

2.12.2 SSI AC Timing Specifications

All timings for the SSI are given for a noninverted serial clock polarity (TSCKP/RSCKP = 0) and a noninverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the following tables and figures.

For internal frame sync operation using external clock, the FS timing will be same as that of Tx Data.

2.12.2.1 SSI Transmitter Timing with Internal Clock

Table 35 provides the transmitter timing parameters with internal clock.

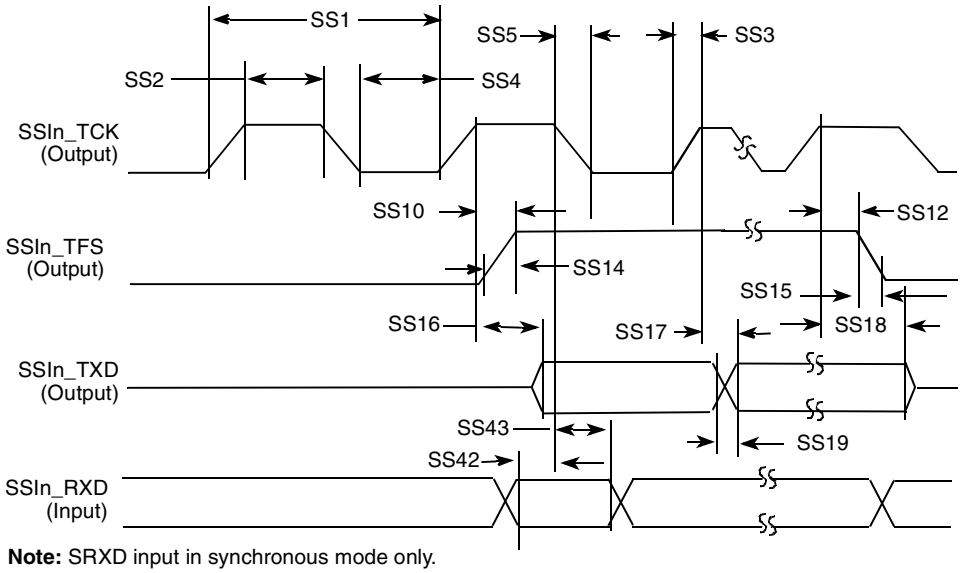
Table 35. SSI Transmitter with Internal Clock Timing Parameters

Parameter	Symbol	Min	Max	Unit
Internal Clock Operation				
(Tx/Rx) CK clock period	SS1	81.4	—	ns
(Tx/Rx) CK clock high period	SS2	36.0	—	ns
(Tx/Rx) CK clock rise time	SS3	—	6	ns
(Tx/Rx) CK clock low period	SS4	36.0	—	ns
(Tx/Rx) CK clock fall time	SS5	—	6	ns
(Tx) CK high to FS high	SS10	—	15.0	ns
(Tx) CK high to FS low	SS12	—	15.0	ns
(Tx/Rx) internal FS rise time	SS14	—	6	ns
(Tx/Rx) internal FS fall time	SS15	—	6	ns
(Tx) CK high to STXD valid from high impedance	SS16	—	15.0	ns
(Tx) CK high to STXD high/low	SS17	—	15.0	ns
(Tx) CK high to STXD high impedance	SS18	—	15.0	ns
STXD rise/fall time	SS19	—	6	ns
Synchronous Internal Clock Operation				
SRXD setup before (Tx) CK falling	SS42	10.0	—	ns

Table 35. SSI Transmitter with Internal Clock Timing Parameters (continued)

Parameter	Symbol	Min	Max	Unit
SRXD hold after (Tx) CK falling	SS43	0	—	ns
Loading	SS52	—	25	pF

Figure 17 provides the SSI transmitter timing with internal clock.



Note: SRXD input in synchronous mode only.

Figure 17. SSI Transmitter with Internal Clock Timing Diagram

2.12.2.2 SSI Receiver Timing with Internal Clock

Table 36 provides the receiver timing parameters with internal clock.

Table 36. SSI Receiver with Internal Clock Timing Parameters

Parameter	Symbol	Min	Max	Unit
Internal Clock Operation				
(Tx/Rx) CK clock period	SS1	81.4	—	ns
(Tx/Rx) CK clock high period	SS2	36.0	—	ns
(Tx/Rx) CK clock rise time	SS3	—	6	ns
(Tx/Rx) CK clock low period	SS4	36.0	—	ns
(Tx/Rx) CK clock fall time	SS5	—	6	ns
(Rx) CK high to FS high	SS11	—	15.0	ns
(Rx) CK high to FS low	SS13	—	15.0	ns
SRXD setup time before (Rx) CK low	SS20	10.0	—	ns
SRXD hold time after (Rx) CK low	SS21	0	—	ns

Figure 18 provides the SSI receiver timing with internal clock.

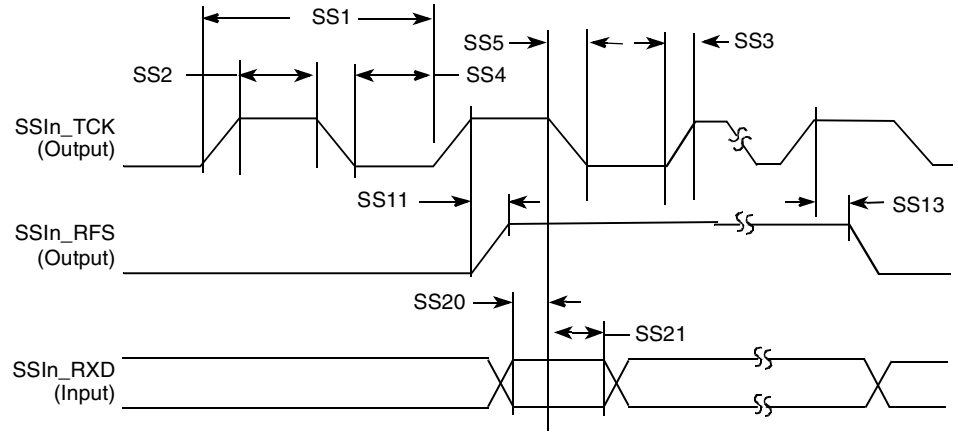


Figure 18. SSI Receiver with Internal Clock Timing Diagram

2.12.2.3 SSI Transmitter Timing with External Clock

Table 37 provides the transmitter timing parameters with external clock.

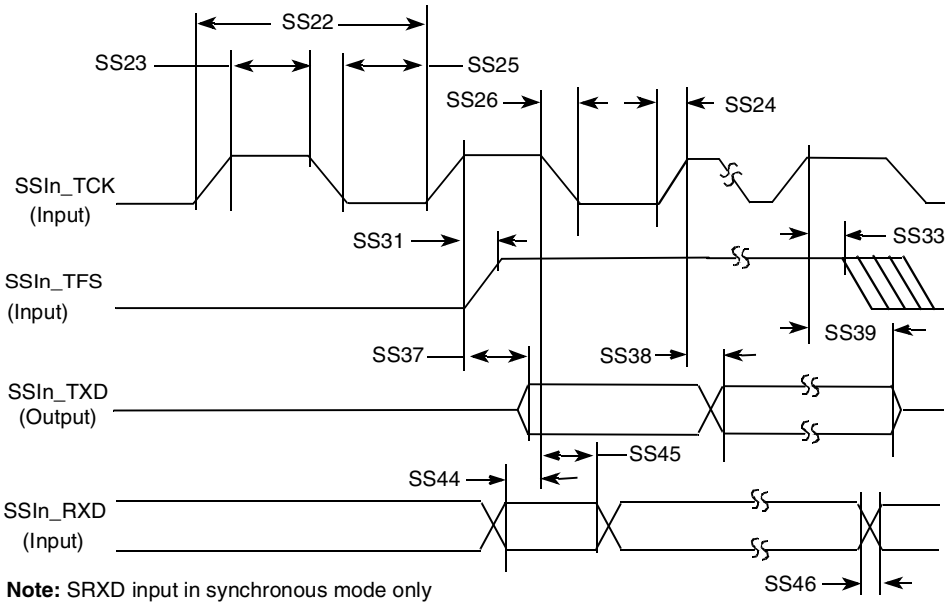
Table 37. SSI Transmitter with External Clock Timing Parameters

Parameter	Symbol	Min	Max	Unit
External Clock Operation				
(Tx/Rx) CK clock period	SS22	81.4	—	ns
(Tx/Rx) CK clock high period	SS23	36.0	—	ns
(Tx/Rx) CK clock rise time	SS24	—	6.0	ns

Table 37. SSI Transmitter with External Clock Timing Parameters (continued)

Parameter	Symbol	Min	Max	Unit
(Tx/Rx) CK clock low period	SS25	36.0	—	ns
(Tx/Rx) CK clock fall time	SS26	—	6.0	ns
(Tx) CK high to FS high	SS31	–10.0	15.0	ns
(Tx) CK high to FS low	SS33	10.0	—	ns
(Tx) CK high to STXD valid from high impedance	SS37	—	15.0	ns
(Tx) CK high to STXD high/low	SS38	—	15.0	ns
(Tx) CK high to STXD high impedance	SS39	—	15.0	ns
Synchronous External Clock Operation				
SRXD setup before (Tx) CK falling	SS44	10.0	—	ns
SRXD hold after (Tx) CK falling	SS45	2.0	—	ns
SRXD rise/fall time	SS46	—	6.0	ns

Figure 19 provides the SSI transmitter timing with external clock.



Note: SRXD input in synchronous mode only

Figure 19. SSI Transmitter with External Clock Timing Diagram

2.12.2.4 SSI Receiver Timing with External Clock

Table 38 provides the receiver timing parameters with external clock.

Table 38. SSI Receiver with External Clock Timing Parameters

Parameter	Symbol	Min	Max	Unit
External Clock Operation				
(Tx/Rx) CK clock period	SS22	81.4	—	ns
(Tx/Rx) CK clock high period	SS23	36.0	—	ns
(Tx/Rx) CK clock rise time	SS24	—	6.0	ns
(Tx/Rx) CK clock low period	SS25	36.0	—	ns
(Tx/Rx) CK clock fall time	SS26	—	6.0	ns
(Rx) CK high to FS high	SS32	–10.0	15.0	ns
(Rx) CK high to FS low	SS34	10.0	—	ns
(Tx/Rx) external FS rise time	SS35	—	6.0	ns
(Tx/Rx) external FS fall time	SS36	—	6.0	ns
SRXD setup time before (Rx) CK low	SS40	10.0	—	ns
SRXD hold time after (Rx) CK low	SS41	2.0	—	ns

Figure 20 provides the SSI receiver timing with external clock.

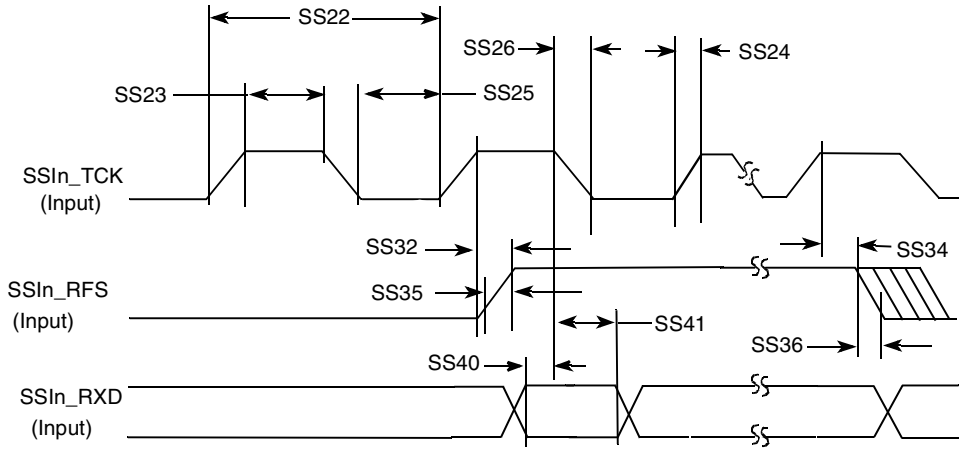


Figure 20. SSI Receiver with External Clock Timing Diagram

2.13 Global Timer Module

This section describes the DC and AC electrical specifications for the global timer module (GTM) of the MPC8610.

2.13.1 GTM DC Electrical Characteristics

Table 39 provides the DC electrical characteristics for the MPC8610 global timer module pins, including GTM*n*_TIN*n*, GTM*n*_$\overline{\text{TOUT}}$*n*, GTM*n*_$\overline{\text{TGATE}}$*n*, and RTC.

Table 39. GTM DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.13.2 GTM AC Timing Specifications

Table 40 provides the GTM input and output AC timing specifications.

Table 40. GTM Input and Output AC Timing Specification[1]

Characteristic	Symbol[2]	Min	Unit	Notes
GTM inputs—minimum pulse width	t_{GTIWID}	7.5	ns	3
GTM outputs—minimum pulse width	t_{GTOWID}	12	ns	

Notes:
1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t_{GTIWID} ns to ensure proper operation.
3. The minimum pulse width is a function of the MPX/platform clock. The minimum pulse width must be greater than or equal to 4 times the MPX/platform clock period.

Figure 21 provides the AC test load for the GTM.

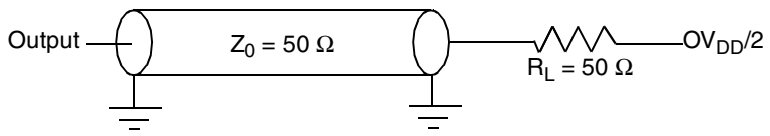


Figure 21. GTM AC Test Load

2.14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8610.

2.14.1 GPIO DC Electrical Characteristics

Table 41 provides the DC electrical characteristics for the GPIO.

Table 41. GPIO DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.14.2 GPIO AC Timing Specifications

Table 42 provides the GPIO input and output AC timing specifications.

Table 42. GPIO Input and Output AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{GPIWID}	7.5	ns	3
GPIO outputs—minimum pulse width	t_{GPOWID}	12	ns	

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.
3. The minimum pulse width is a function of the MPX/platform clock. The minimum pulse width must be greater than or equal to 4 times the MPX/platform clock period.

Figure 22 provides the AC test load for the GPIO.

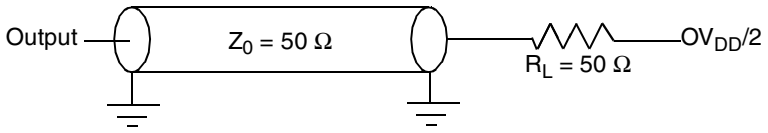


Figure 22. GPIO AC Test Load

2.15 Serial Peripheral Interface (SPI)

This section describes the DC and AC electrical specifications for the SPI interface of the MPC8610.

2.15.1 SPI DC Electrical Characteristics

Table 43 provides the SPI DC electrical characteristics.

Table 43. SPI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = mn, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.15.2 SPI AC Timing Specifications

Table 44 provides the SPI input and output AC timing specifications.

Table 44. SPI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI outputs valid—master mode (internal clock) delay	t_{NIKHOV}		1	ns
SPI outputs hold—master mode (internal clock) delay	t_{NIKHOX}	-0.2		ns
SPI outputs valid—slave mode (external clock) delay	t_{NEKHOV}		8	ns
SPI outputs hold—slave mode (external clock) delay	t_{NEKHOX}	2		ns
SPI inputs—master mode (internal clock input setup time	t_{NIIVKH}	4		ns
SPI inputs—master mode (internal clock input hold time	t_{NIIXKH}	0		ns
SPI inputs—slave mode (external clock) input setup time	t_{NEIVKH}	4		ns
SPI inputs—slave mode (external clock) input hold time	t_{NEIXKH}	2		ns

Notes:
1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

Figure 23 provides the AC test load for the SPI.

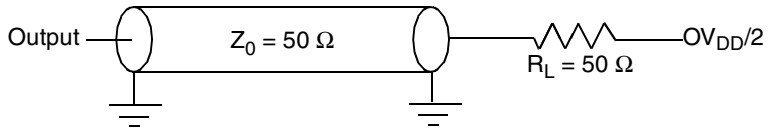
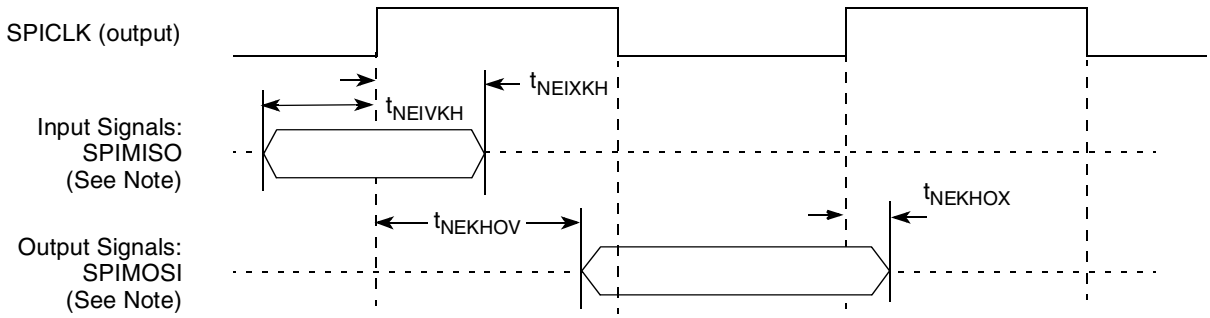


Figure 23. SPI AC Test Load

Figure 24 through Figure 25 represent the AC timings from Table 44. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

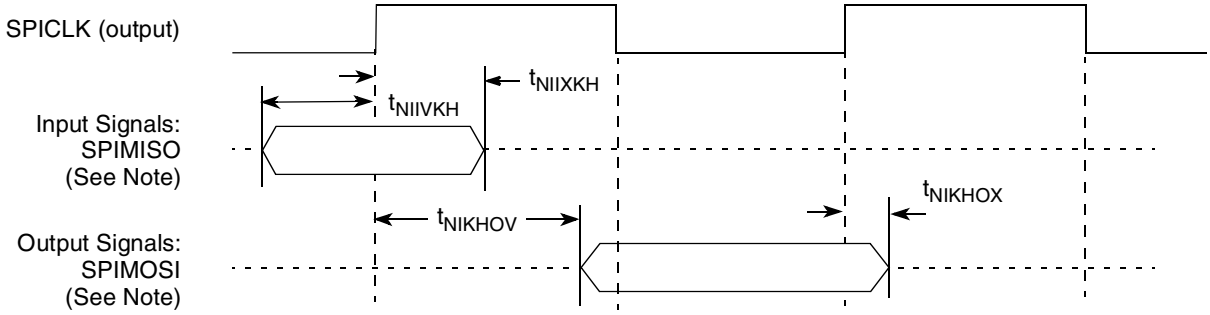
Figure 24 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 24. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 25 shows the SPI timings in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 25. SPI AC Timing in Master Mode (Internal Clock) Diagram

2.16 PCI Interface

This section describes the DC and AC electrical specifications for the PCI bus interface.

2.16.1 PCI DC Electrical Characteristics

Table 45 provides the DC electrical characteristics for the PCI interface.

Table 45. PCI DC Electrical Characteristics[1]

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [2] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Notes:
1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.16.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the SYSCLK signal is used as the PCI input clock. Table 46 provides the PCI AC timing specifications at 66 MHz.

Table 46. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
SYSCLK to output valid	t_{PCKHOV}	1.5	7.4	ns	2, 3, 12
SYSCLK to output high impedance	t_{PCKHOZ}	—	14	ns	2, 4, 11
Input setup to SYSCLK	t_{PCIVKH}	3.7	—	ns	2, 5, 10, 13
Input hold from SYSCLK	t_{PCIXKH}	0.8	—	ns	2, 5, 10, 14
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$ [9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	6, 7, 11
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	7, 11

Table 46. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	8, 11

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.
6. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 3.1, "System Clocking."
7. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
8. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
9. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 µs.
10. Guaranteed by characterization.
11. Guaranteed by design.
12. The timing parameter t_{PCKHOV} is a minimum of 1.5 ns and a maximum of 7.4 ns rather than the minimum of 2 ns and a maximum of 6 ns in the *PCI 2.2 Local Bus Specifications*.
13. The timing parameter t_{PCIVKH} is a minimum of 3.7 ns rather than the minimum of 3 ns in the *PCI 2.2 Local Bus Specifications*.
14. The timing parameter t_{PCIXKH} is a minimum of 0.8 ns rather than the minimum of 0 ns in the *PCI 2.2 Local Bus Specifications*.

Figure 15 provides the AC test load for PCI.

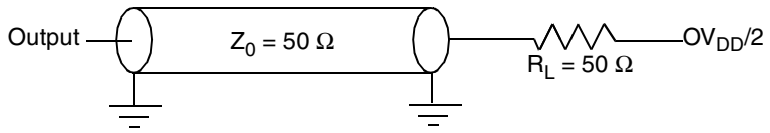


Figure 26. PCI AC Test Load

Figure 27 shows the PCI input AC timing conditions.

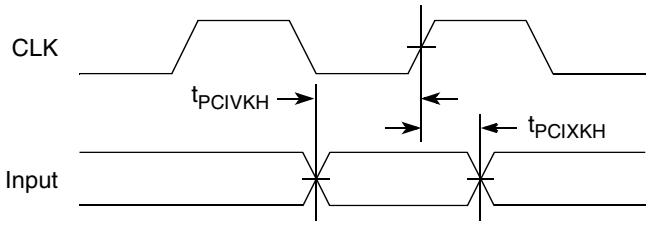


Figure 27. PCI Input AC Timing Measurement Conditions

Figure 28 shows the PCI output AC timing conditions.

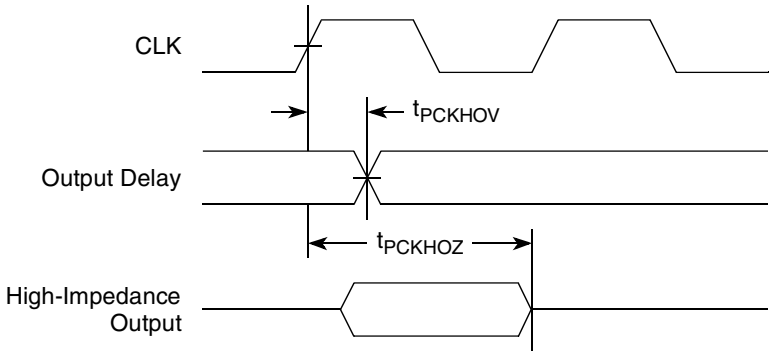


Figure 28. PCI Output AC Timing Measurement Condition

2.17 High-Speed Serial Interfaces (HSSI)

The MPC8610 features two Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 interface is dedicated for PCI Express (x1/x2/x4) data transfers. The SerDes2 interface is dedicated for PCI Express (x1/x2/x4/x8) data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

2.17.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 29 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{_RX}}$). Each signal swings between A volts and B volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. Single-ended swing

   The transmitter output signals and the receiver input signals SD*n*_TX, $\overline{\text{SD}n\text{_TX}}$, SD*n*_RX, and $\overline{\text{SD}n\text{_RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

2. Differential output voltage, V_{OD} (or differential output swing):

   The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SDn_TX} - V_{\overline{SDn_TX}}$. The V_{OD} value can be either positive or negative.

3. Differential input voltage, V_{ID} (or differential input swing):

   The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SDn_RX} - V_{\overline{SDn_RX}}$. The V_{ID} value can be either positive or negative.

4. Differential peak voltage, V_{DIFFp}

   The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

5. Differential peak-to-peak, $V_{DIFFp-p}$

   Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to -(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 * V_{DIFFp} = 2 * |(A - B)|$ volts, which is twice

of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX\text{-}DIFFp\text{-}p} = 2 * |V_{OD}|$.

6. Differential waveform

   The differential waveform is constructed by subtracting the inverting signal ($\overline{SDn_TX}$, for example) from the noninverting signal (SD*n*_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 38 as an example for differential waveform.

7. Common mode voltage, V_{cm}

   The common mode voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{SDn_TX} + V_{\overline{SDn_TX}})/2 = (A + B)/2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It's also referred as the DC offset in some occasion.

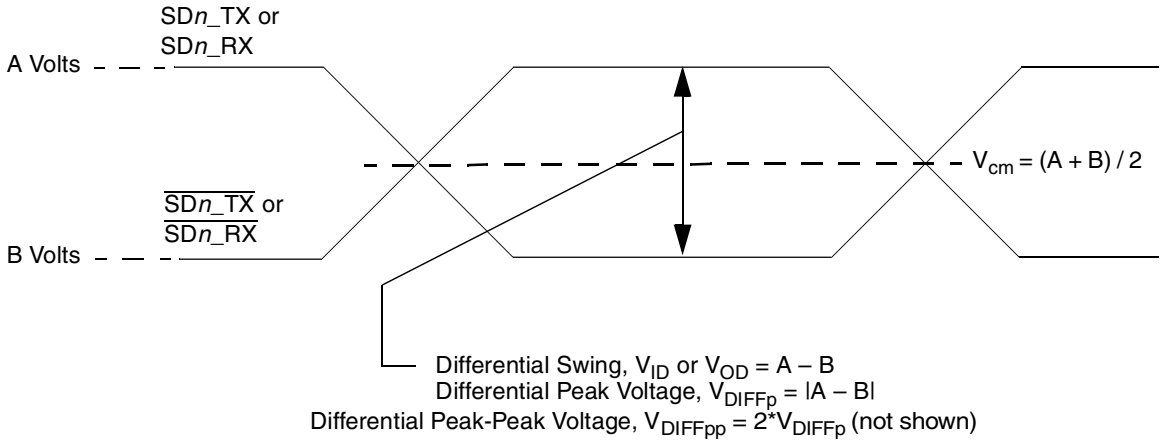


Figure 29. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp\text{-}p}$) is 1000 mV p-p.

2.17.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD*n*_REF_CLK and $\overline{SDn_REF_CLK}$ for PCI Express.

The following sections describe the SerDes reference clock requirements and some application information.

2.17.2.1 SerDes Reference Clock Receiver Characteristics

Figure 30 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for XnV_{DD} are specified in Table 2 and Table 3.

- SerDes reference clock receiver reference circuit structure
  - The SD*n*_REF_CLK and $\overline{\text{SD}n\text{_REF_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 30. Each differential clock input (SD*n*_REF_CLK or $\overline{\text{SD}n\text{_REF_CLK}}$) has a 50-Ω termination to SGND followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{_REF_CLK}}$ inputs cannot drive 50 Ω to SGND DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  - This requirement is described in detail in the following sections.

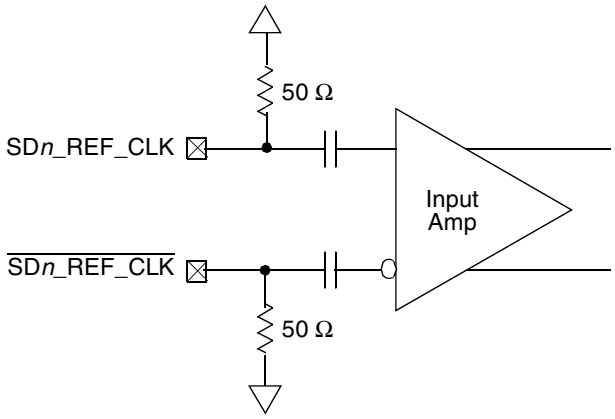


Figure 30. Receiver of SerDes Reference Clocks

2.17.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8610 SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- Differential mode
  - The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-peak (or between 200 and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC- or AC-coupled connection.
  - For external DC-coupled connection, as described in Section 2.17.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV. Figure 31 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

— For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND). Figure 32 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- Single-ended mode
  — The reference clock can also be single-ended. The SD*n*_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-peak (from V_{min} to V_{max}) with $\overline{\text{SD}n\text{_REF_CLK}}$ either left unconnected or tied to ground.
  — The SD*n*_REF_CLK input average voltage must be between 200 and 400 mV. Figure 33 shows the SerDes reference clock input requirement for single-ended signaling mode.
  — To meet the input amplitude requirement, the reference clock inputs might need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SD}n\text{_REF_CLK}}$) through the same source impedance as the clock input (SD*n*_REF_CLK) in use.

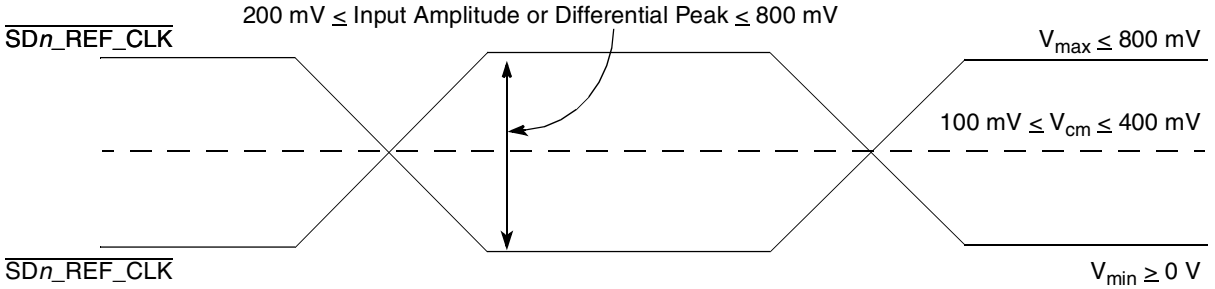


Figure 31. Differential Reference Clock Input DC Requirements (External DC-Coupled)

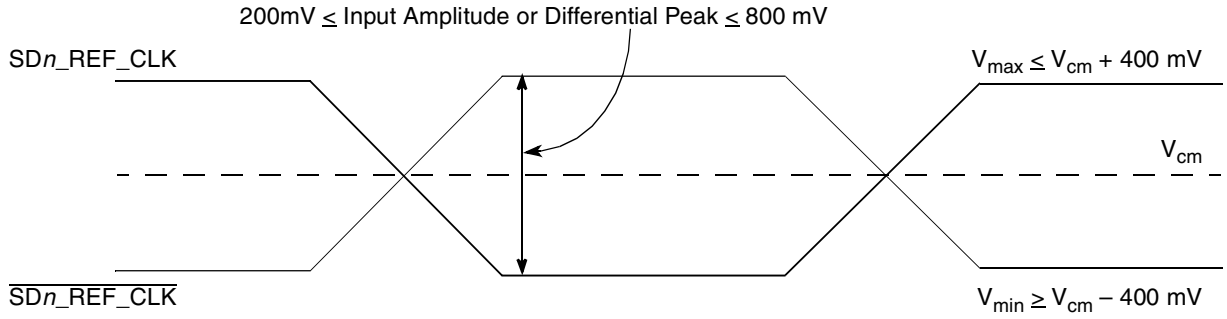


Figure 32. Differential Reference Clock Input DC Requirements (External AC-Coupled)

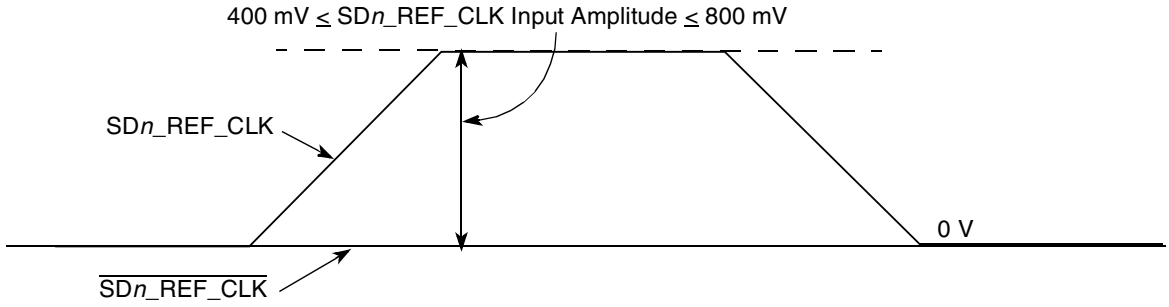


Figure 33. Single-Ended Reference Clock Input DC Requirements

2.17.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to SGND, the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 34 to Figure 37 are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8610 SerDes reference clock receiver requirement provided in this document.

Figure 34 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8610 SerDes reference clock input's DC requirement.

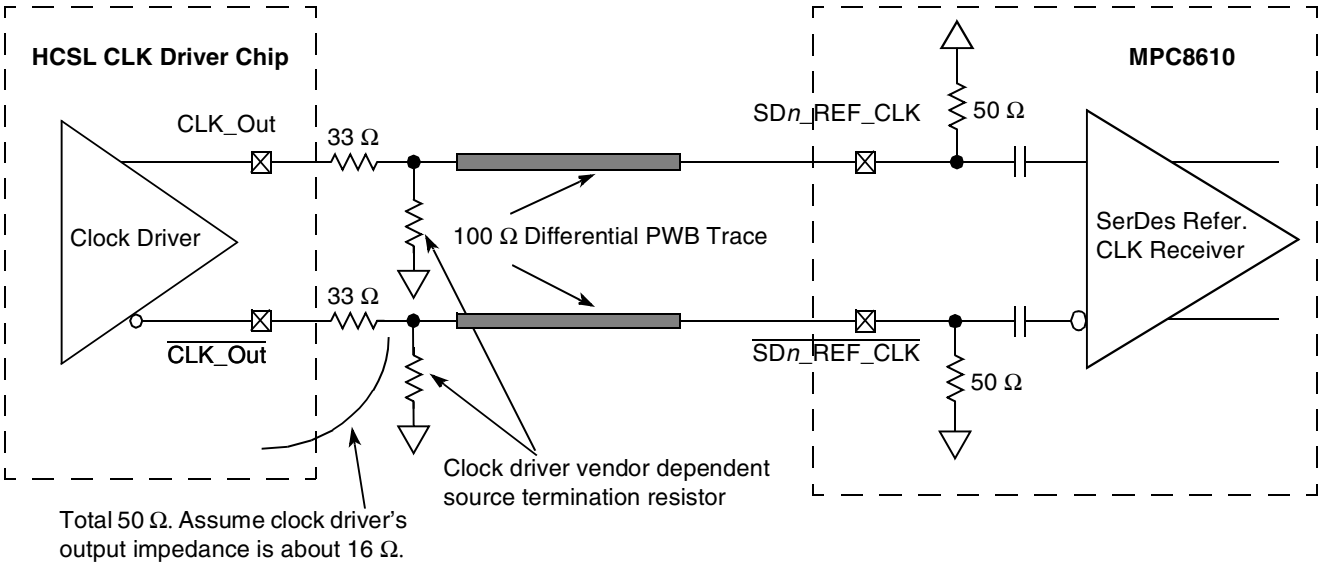


Figure 34. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 35 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8610 SerDes reference clock input's allowed range (100 to 400 mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

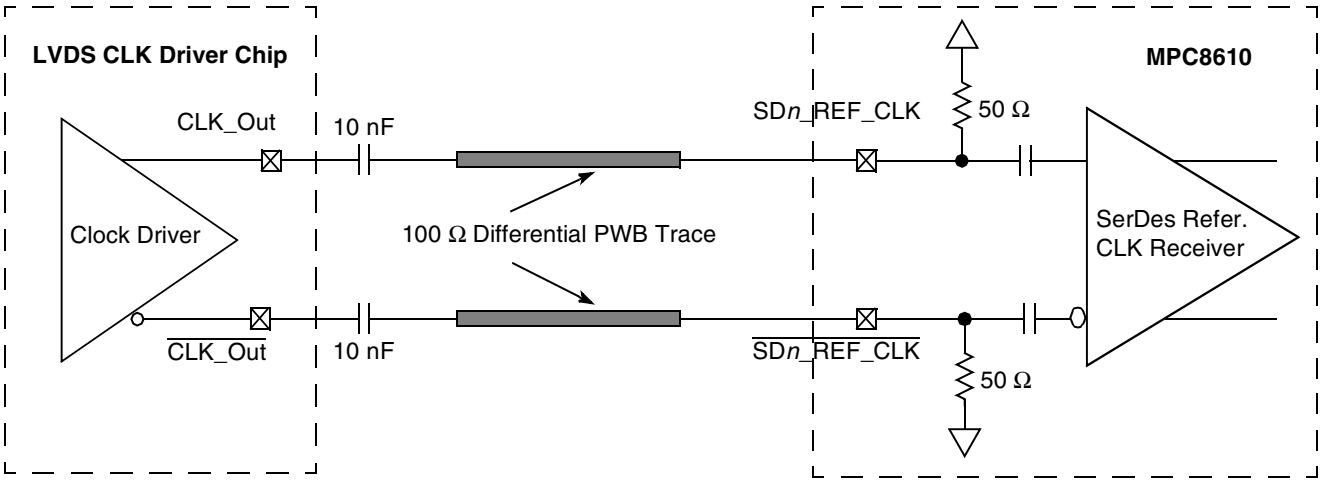


Figure 35. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 36 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8610 SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 36 assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8610 SerDes reference clock's differential input amplitude requirement (between 200 and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

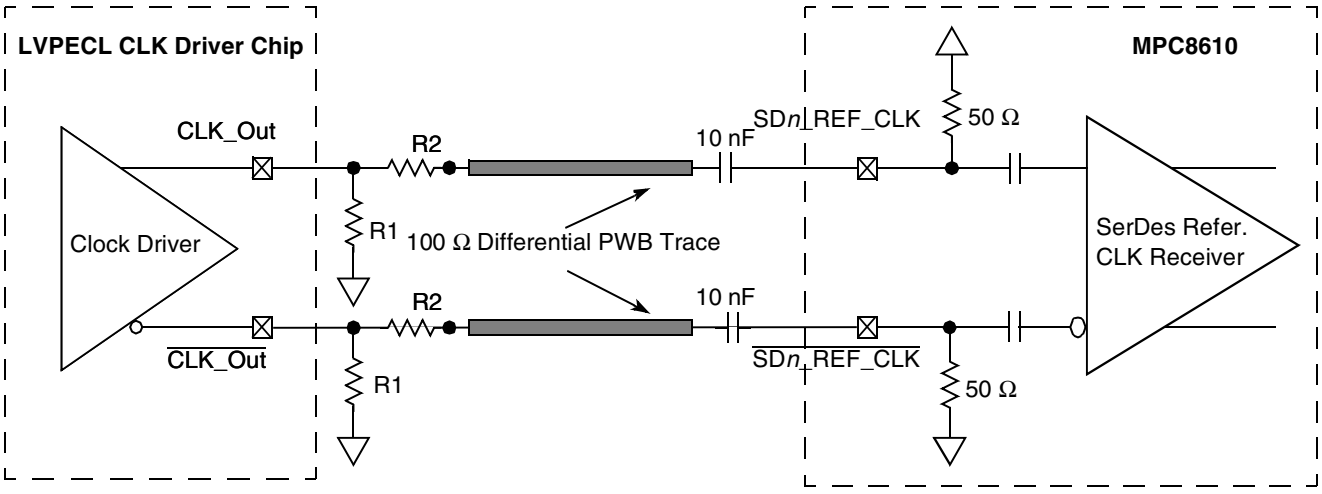


Figure 36. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Figure 37 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8610 SerDes reference clock input's DC requirement.

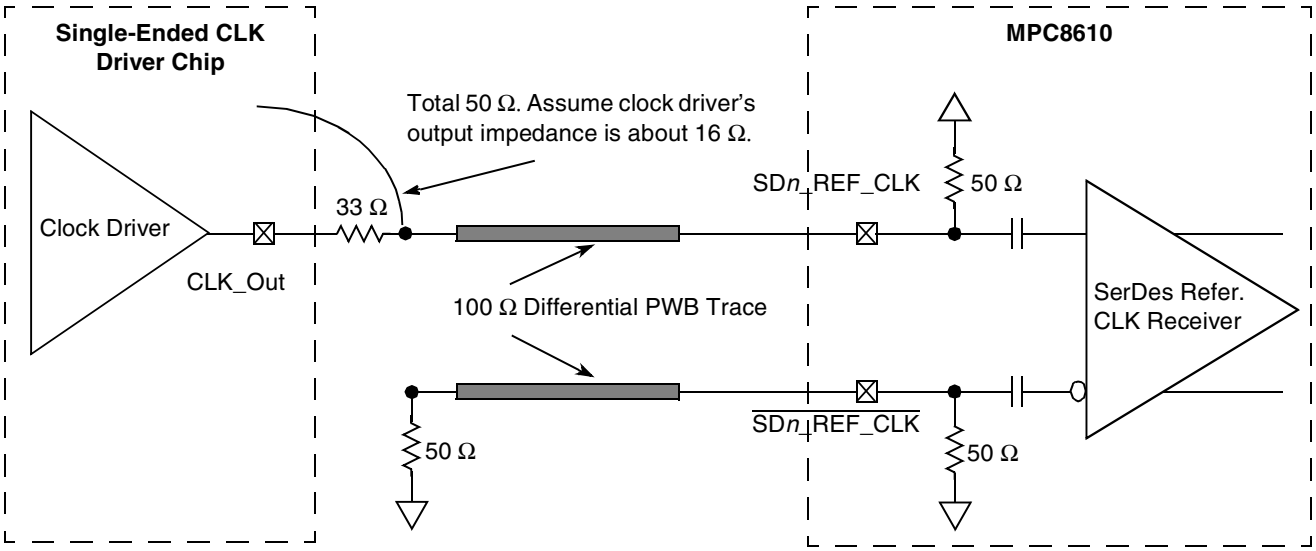


Figure 37. Single-Ended Connection (Reference Only)

2.17.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

Table 47 describes some AC parameters common to PCI Express protocols.

Table 47. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with $X1V_{DD}$ or $X2V_{DD}$ = 1.0 V ± 5% and 1.025 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	+200		mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2

Table 47. SerDes Reference Clock Common AC Parameters (continued)

At recommended operating conditions with $X1V_{DD}$ or $X2V_{DD}$ = 1.0 V ± 5% and 1.025 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Rising edge rate (SD*n*_REF_CLK) to falling edge rate ($\overline{\text{SD}n\text{_REF_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\text{SD}n\text{_REF_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 38.
4. Matching applies to rising edge rate for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{_REF_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SD*n*_REF_CLK rising meets $\overline{\text{SD}n\text{_REF_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK should be compared to the fall edge rate of $\overline{\text{SD}n\text{_REF_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 39.

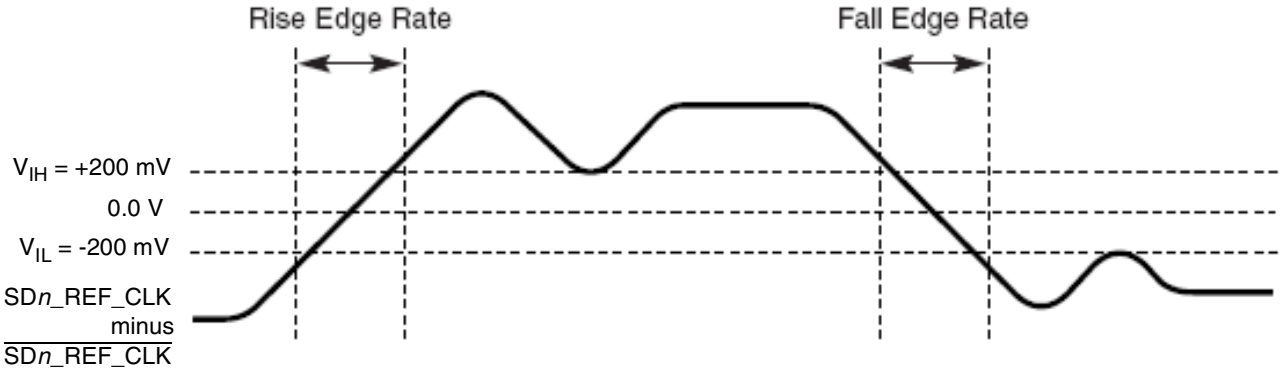


Figure 38. Differential Measurement Points for Rise and Fall Time

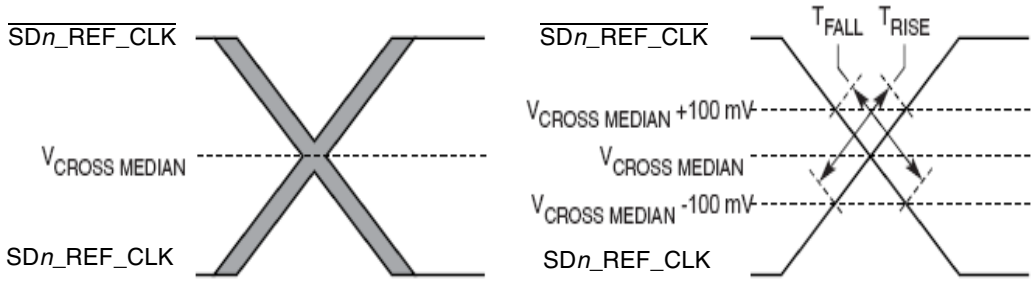


Figure 39. Single-Ended Measurement Points for Rise and Fall Time Matching

The other detailed AC requirements of the SerDes reference clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- Section 2.18.2, “AC Requirements for PCI Express SerDes Clocks”

2.17.3 SerDes Transmitter and Receiver Reference Circuits

Figure 40 shows the reference circuits for SerDes data lane's transmitter and receiver.

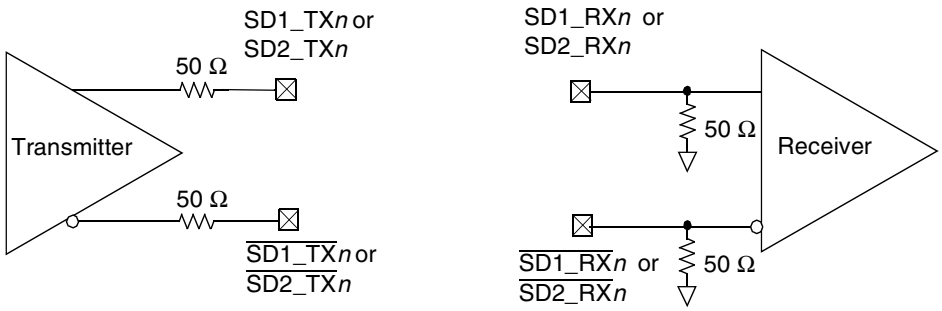


Figure 40. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express) in this document based on the application usage:"

- Section 2.18, "PCI Express"

Note that external AC Coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in specification of each protocol section.

2.18 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8610.

2.18.1 DC Requirements for PCI Express SD*n*_REF_CLK and SD*n*_REF_CLK

For more information, see Section 2.17.2, "SerDes Reference Clocks."

2.18.2 AC Requirements for PCI Express SerDes Clocks

Table 48 lists AC requirements.

Table 48. SD*n*_REF_CLK and SD*n*_REF_CLK AC Requirements

Symbol	Parameter Description	Min	Typ	Max	Units
t_{REF}	REFCLK cycle time	—	10	—	ns
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps

2.18.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

2.18.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer, use the *PCI Express Base Specification*, Rev. 1.0a.

2.18.4.1 Differential Transmitter (TX) Output

Table 49 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 49. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1
$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	0.8		1.2	V	$V_{TX-DIFFp-p} = 2*\|V_{TX-D+} - V_{TX-D-}\|$ See Note 2
$V_{TX-DE-RATIO}$	De- emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2
T_{TX-EYE}	Minimum TX eye width	0.70			UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D– TX output rise/fall time	0.125			UI	See Notes 2 and 5
$V_{TX-CM-ACp}$	RMS AC peak common mode output voltage			20	mV	$V_{TX-CM-ACp} = RMS(\|V_{TXD+} - V_{TXD-}\|/2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} - V_{TX-D-}\|/2$ See Note 2
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common mode voltage during LO and electrical idle	0		100	mV	$\|V_{TX-CM-DC\ (during\ LO)} - V_{TX-CM-Idle-DC\ (During\ Electrical\ Idle)}\|$<=100 mV $V_{TX-CM-DC} = DC_{(avg)}$ of $\|V_{TX-D+} - V_{TX-D-}\|/2$ [LO] $V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $\|V_{TX-D+} - V_{TX-D-}\|/2$ [Electrical Idle] See Note 2
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common mode between D+ and D–	0		25	mV	$\|V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}\|$ <= 25 mV $V_{TX-CM-DC-D+} = DC_{(avg)}$ of $\|V_{TX-D+}\|$ $V_{TX-CM-DC-D-} = DC_{(avg)}$ of $\|V_{TX-D-}\|$ See Note 2

Table 49. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{TX\text{-}IDLE\text{-}DIFFp}$	Electrical idle differential peak output voltage	0		20	mV	$V_{TX\text{-}IDLE\text{-}DIFFp} = \lvert V_{TX\text{-}IDLE\text{-}D+} - V_{TX\text{-}IDLE\text{-}D-} \rvert <= 20$ mV See Note 2
$V_{TX\text{-}RCV\text{-}DETECT}$	The amount of voltage change allowed during receiver detection			600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. See Note 6
$V_{TX\text{-}DC\text{-}CM}$	The TX DC common mode voltage	0		3.6	V	The allowed DC common mode voltage under any conditions. See Note 6
$I_{TX\text{-}SHORT}$	TX short circuit current limit			90	mA	The total current the transmitter can provide when shorted to its ground
$T_{TX\text{-}IDLE\text{-}MIN}$	Minimum time spent in electrical idle	50			UI	Minimum time a transmitter must be in electrical idle utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set
$T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set			20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from LO.
$T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$	Maximum time to transition to valid TX specifications after leaving an electrical idle condition			20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle
$RL_{TX\text{-}DIFF}$	Differential return loss	12			dB	Measured over 50 MHz to 1.25 GHz. See Note 4
$RL_{TX\text{-}CM}$	Common mode return loss	6			dB	Measured over 50 MHz to 1.25 GHz. See Note 4
$Z_{TX\text{-}DIFF\text{-}DC}$	DC differential TX impedance	80	100	120	Ω	TX DC differential mode low impedance
$Z_{TX\text{-}DC}$	Transmitter DC impedance	40			Ω	Required TX D+ as well as D- DC Impedance during all states
$L_{TX\text{-}SKEW}$	Lane-to-lane output skew			500 + 2 UI	ps	Static skew between any two transmitter lanes within a single link
C_{TX}	AC coupling capacitor	75		200	nF	All transmitters shall be AC-coupled. The AC coupling is required either within the media or within the transmitting component itself.

Table 49. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$T_{crosslink}$	Crosslink random timeout	0		1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port. See Note 7

Notes:

1.) No test load is necessarily associated with this value.

2.) Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 43 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 41.)

3.) A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

4.) The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes—see Figure 43). Note that the series capacitors C_{TX} is optional for the return loss measurement.

5.) Measured between 20–80% at transmitter package pins into a test load as shown in Figure 43 for both V_{TX-D+} and V_{TX-D-}.

6.) See Section 4.3.1.8 of the *PCI Express Base Specifications,* Rev. 1.0a.

7.) See Section 4.2.6.3 of the *PCI Express Base Specifications*, Rev. 1.0a.

2.18.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 41 is specified using the passive compliance/test measurement load (see Figure 43) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (i.e., least squares and median deviation fits).

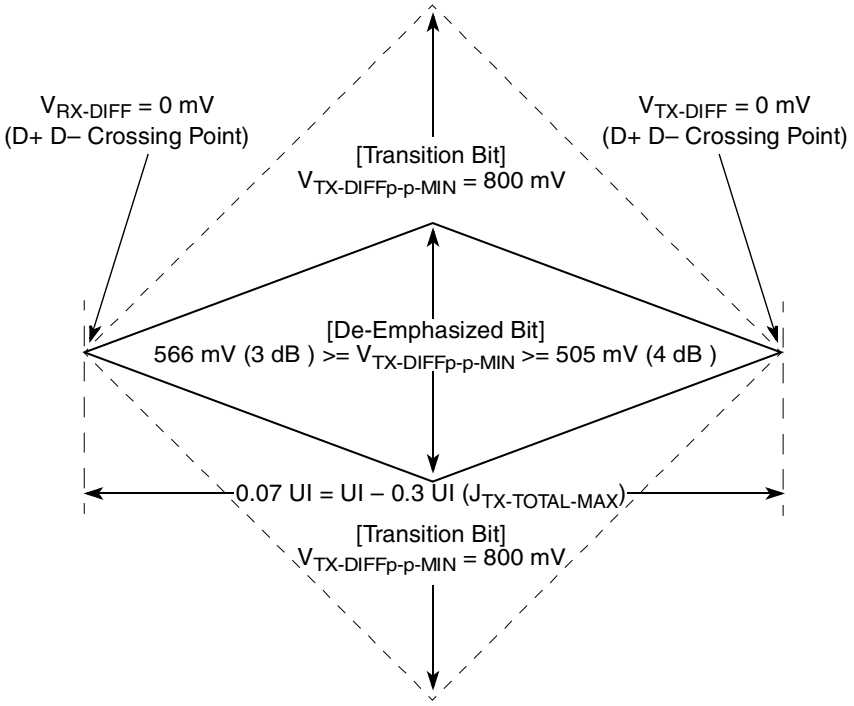


Figure 41. Minimum Transmitter Timing and Voltage Output Compliance Specifications

2.18.4.3 Differential Receiver (RX) Input Specifications

Table 50 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 50. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential peak-to-peak output voltage	0.175		1.200	V	$V_{RX-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ See Note 2
T_{RX-EYE}	Minimum receiver eye width	0.4			UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.			0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 7

Table 50. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{RX-CM-ACp}$	AC peak common mode input voltage			150	mV	$V_{RX-CM-ACp} = \lvert V_{RXD+} - V_{RXD-}\rvert/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} - V_{RX-D-}\rvert/2$ See Note 2
$RL_{RX-DIFF}$	Differential return loss	15			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 and –300 mV, respectively. See Note 4
RL_{RX-CM}	Common mode return loss	6			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4
$Z_{RX-DIFF-DC}$	DC differential input impedance	80	100	120	Ω	RX DC differential mode impedance. See Note 5
Z_{RX-DC}	DC input impedance	40	50	60	Ω	Required RX D+ as well as D– DC impedance (50 ± 20% tolerance). See Notes 2 and 5
$Z_{RX-HIGH-IMP-DC}$	Powered down DC input impedance	200 k			Ω	Required RX D+ as well as D– DC Impedance when the receiver terminations do not have power. See Note 6
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2*\lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the receiver
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time			10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

Table 50. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$L_{TX-SKEW}$	Total skew			20	ns	Skew across all lanes on a link. This includes variation in the length of SKP ordered set (e.g., COM and one to five symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

1.)No test load is necessarily associated with this value.

2.)Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 43 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 42). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

3.)A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

4.)The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a Vector Network Analyzer with 50-Ω probes—see Figure 43). Note that the series capacitors CTX is optional for the return loss measurement.

5.)Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.

6.)The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

7.)It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

2.18.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 42 is specified using the passive compliance/test measurement load (see Figure 43) in place of any real PCI Express RX component.

Note: In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 43) will be larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 42) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (i.e., as measured by a vector network analyzer with 50-Ω probes—see Figure 43). Note that the series capacitors, CTX, are optional for the return loss measurement.

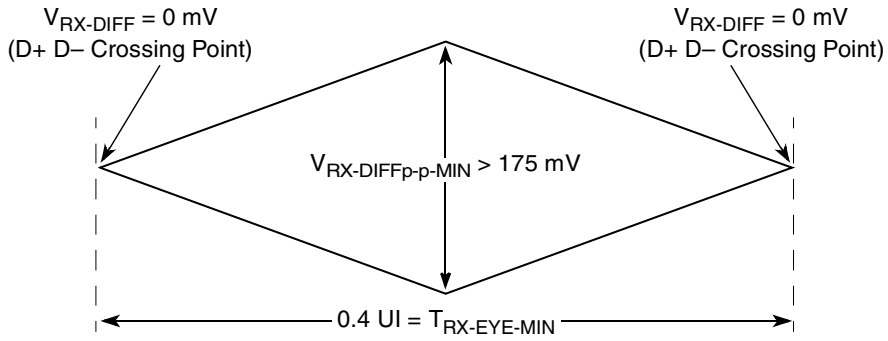


Figure 42. Minimum Receiver Eye Timing and Voltage Compliance Specification

2.18.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 43.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

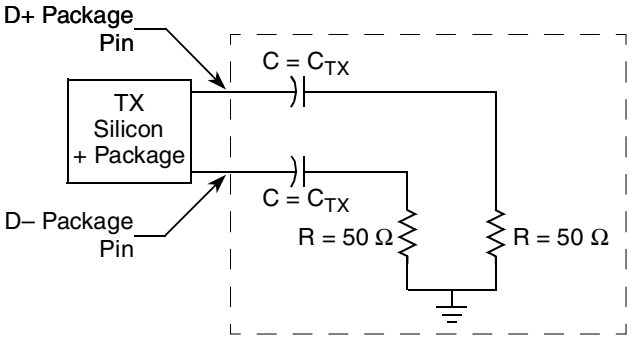


Figure 43. Compliance Test/Measurement Load

2.19 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8610.

2.19.1 JTAG DC Electrical Characteristics

Table 51 provides the JTAG DC electrical characteristics for the JTAG interface.

Table 51. JTAG DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN}[1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA
High-level output voltage (OV_{DD} = mn, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

2.19.2 JTAG AC Electrical Specifications

Table 52 provides the JTAG AC timing specifications as defined in Figure 45 through Figure 47.

Table 52. JTAG AC Timing Specifications (Independent of SYSCLK)[1]

At recommended operating conditions (see Table 3).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	
JTAG external clock cycle time	t_{JTG}	30	—	ns	
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	6
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 0	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 20 25	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 4 4	 20 25	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 30 30	 — —	ns	5

Table 52. JTAG AC Timing Specifications (Independent of SYSCLK)[1] (continued)

At recommended operating conditions (see Table 3).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 3 3	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 15). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design.

Figure 15 provides the AC test load for TDO and the boundary-scan outputs.

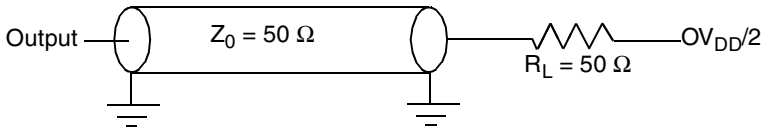


Figure 44. AC Test Load for the JTAG Interface

Figure 45 provides the JTAG clock input timing diagram.

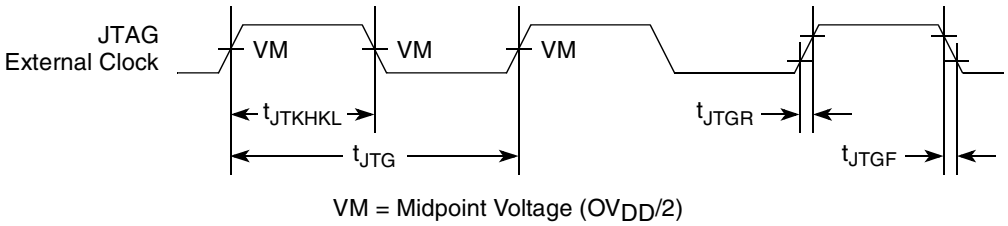


Figure 45. JTAG Clock Input Timing Diagram

Figure 46 provides the $\overline{\text{TRST}}$ timing diagram.

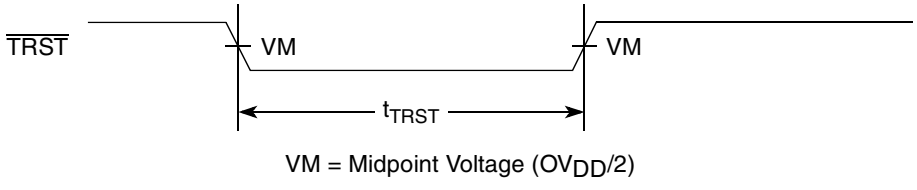


Figure 46. $\overline{\text{TRST}}$ Timing Diagram

Figure 47 provides the boundary-scan timing diagram.

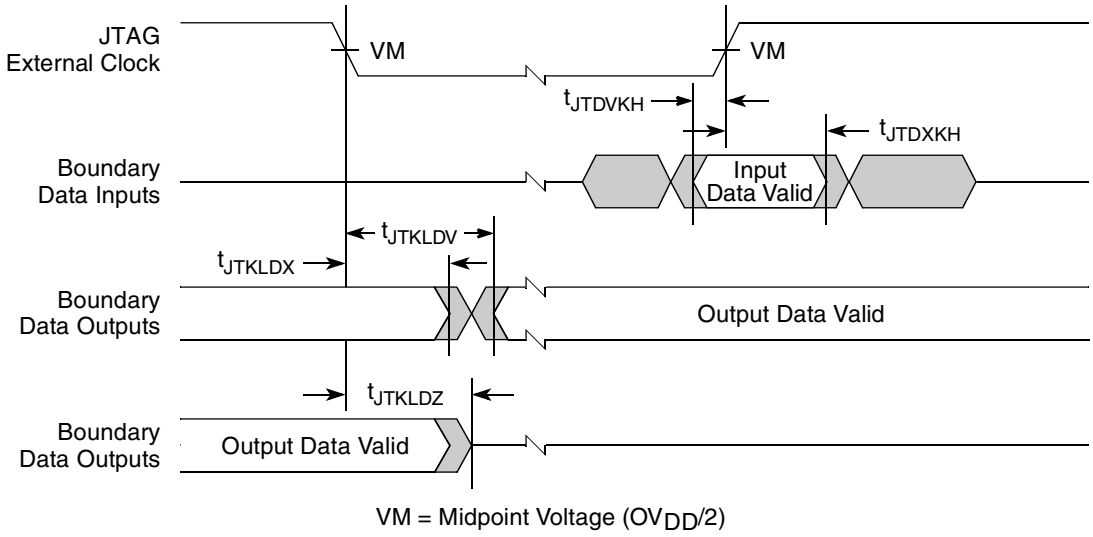


Figure 47. Boundary-Scan Timing Diagram

3 Hardware Design Considerations

This section provides electrical and thermal design recommendations for successful application of the MPC8610.

3.1 System Clocking

This section describes the PLL configuration of the MPC8610. Note that the platform clock is identical to the internal MPX bus clock.

This device includes six PLLs, as follows:

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 3.1.2, “Platform/MPX to SYSCLK PLL Ratio.”
2. The e600 core PLL generates the core clock from the platform clock. The frequency ratio between the e600 core clock and the platform clock is selected using the e600 PLL ratio configuration bits as described in Section 3.1.3, “e600 Core to MPX/Platform Clock PLL Ratio.”
3. The PCI PLL generates the clocking for the PCI bus
4. Each of the two SerDes blocks has a PLL.

3.1.1 Clock Ranges

Table 53 provides the clocking specifications for the processor core.

Table 53. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	800 MHz		1066 MHz		1333 MHz			
	Min	Max	Min	Max	Min	Max		
e600 core processor frequency	666	800	666	1066	666	1333	MHz	1, 2, 3

Notes:
1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 3.1.2, "Platform/MPX to SYSCLK PLL Ratio" and Section 3.1.3, "e600 Core to MPX/Platform Clock PLL Ratio," for ratio settings.
2. The minimum e600 core frequency is based on the minimum platform clock frequency of 333 MHz.
3. The reset config pin cfg_core_speed must be pulled low if the core frequency is 800 MHz or below.

Table 54 provides the clocking specifications for the memory bus.

Table 54. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1066, 1333 MHz			
	Min	Max		
Memory bus clock frequency	166	266	MHz	1, 2

Notes:
1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 3.1.2, "Platform/MPX to SYSCLK PLL Ratio."
2. The memory bus clock speed is half the DDR/DDR2 data rate, hence, half the MPX clock frequency.

Table 55 provides the clocking specifications for the local bus.

Table 55. Local Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1066, 1333 MHz			
	Min	Max		
Local bus clock speed	22	133	MHz	1

Note:
1. The local bus clock speed on LCLK[0:2] is determined by the MPX clock divided by the local bus ratio programmed in LCRR[CLKDIV]. Refer to the *MPC8610 Integrated Host Processor Reference Manual,* for more information.

Table 56 provides the clocking specifications for the Platform/MPX bus.

Table 56. Platform/MPX Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1066, 1333 MHz			
	Min	Max		
Platform/MPX bus clock speed	333	533	MHz	1, 2

Note:
1. **Caution:** The MPX clock to SYSCLK ratio and e600 core to MPX clock ratio settings must be chosen such that the resulting SYSCLK frequency, e600 (core) frequency, and MPX clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 3.1.2, "Platform/MPX to SYSCLK PLL Ratio."
2. For MPX clock frequencies at 400 MHz and below, cfg_net2_div must be pulled low.

3.1.2 Platform/MPX to SYSCLK PLL Ratio

The the clock that drives the internal MPX bus is called the platform clock. The frequency of the platform clock is set using the following reset signals, as shown in Table 57:

- SYSCLK input signal
- Binary value on DIU_LD[10], LA[28:31] (cfg_sys_pll[0:4] - reset config) at power up

These signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the platform frequency, since the platform frequency must equal the DDR data rate.

For specifications on the PCI_CLK, refer to the PCI 2.2 Specification.

Table 57. Platform/SYSCLK Clock Ratios

Binary Value of DIU_LD[10], LA[28:31] Signals	Platform:SYSCLK Ratio	Binary Value of DIU_LD[10], LA[28:31] Signals	Platform:SYSCLK Ratio
00010	2:1	01010	10:1
00011	3:1	01100	12:1
00100	4:1	01110	14:1
00101	5:1	01111	15:1
00110	6:1	10000	16:1
00111	7:1	10001	17:1
01000	8:1	10010	18:1
01001	9:1	All others	Reserved

3.1.3 e600 Core to MPX/Platform Clock PLL Ratio

The clock ratio between the e600 core and the platform clock is determined by the binary value of LBCTL, LALE, LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$, DIU_LD4 (cfg_core_pll[0:3]–reset config) signals at power up. Table 58 describes the supported ratios. Note that cfg_core_speed must be pulled low if the core frequency is 800 MHz or below.

Table 58. e600 Core/Platform Clock Ratios

Binary Value of LBCTL, LALE, LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$, DIU_LD4 Signals	e600 core: MPX/Platform Ratio
1000	2:1
1010	2.5:1
1100	3:1
1110	3.5:1
0000	4:1
0010	4.5:1
All Others	Reserved

3.1.4 Frequency Options

3.1.4.1 SYSCLK and Platform Frequency Options

Table 59 shows the expected frequency options for SYSCLK and platform frequencies.

Table 59. SYSCLK and Platform Frequency Options

Platform: SYSCLK Ratio	SYSCLK (MHz)					
	33.33	66.66	83.33	100.00	111.11	133.33
	Platform/MPX Frequency (MHz)[1]					
3:1					333	400
4:1			333	400		533
5:1		333		500		
6:1		400	500			
8:1		533				
10:1	333					
12:1	400					
16:1	533					

1 Platform/MPX Frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed)

3.2 Power Supply Design and Sequencing

3.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD}_Plat, AV_{DD}_Core, AV_{DD}_PCI, and SD*n*AV_{DD}, respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply, one to each of the AV_{DD} type pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} type pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} type pin, which is on the periphery of 783 FC-PBGA the footprint, without the inductance of vias.

Figure 48 shows the filter circuit for the platform PLL power supplies (AV_{DD}_PLAT).

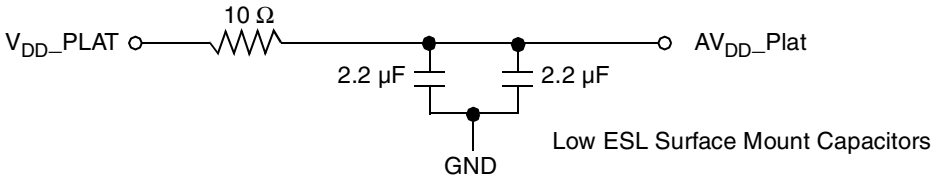


Figure 48. MPC8610 PLL Power Supply Filter Circuit (for Platform)

Figure 49 shows the filter circuit for the core PLL power supply (AV_{DD}_Core).

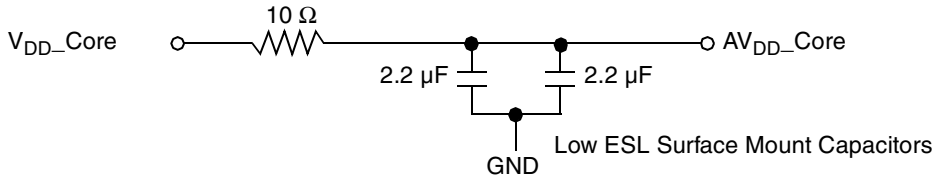
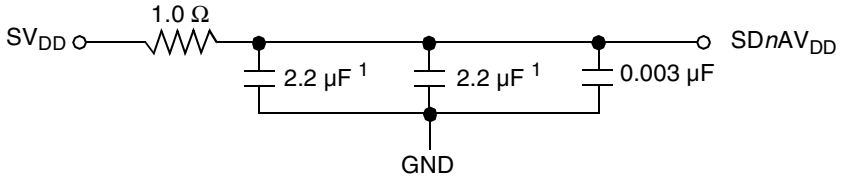


Figure 49. MPC8610 PLL Power Supply Filter Circuit (for Core)

The SD*n*AV_{DD} signals provide power for the analog portions of the SerDes PLLs. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in Figure 50. For maximum effectiveness, the filter circuit is placed as closely as possible to the SD*n*AV_{DD} balls to ensure it filters out as much noise as possible. The ground connection should be near the SD*n*AV_{DD} balls. The 0.003-µF capacitor is closest to the balls, followed by the two 2.2-µF capacitors, and finally the 1 ohm resistor to the board supply plane. The capacitors are connected from SD*n*AV_{DD} to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 50. SerDes PLL Power Supply Filter

Note the following:

- SD*n*AV$_{DD}$ should be a filtered version of SV$_{DD}$.
- Signals on the SerDes interface are fed from the SV$_{DD}$ power plane.

3.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8610 system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V$_{DD}$, BV$_{DD}$, OV$_{DD}$, GV$_{DD}$, V$_{DD}$_Core, and V$_{DD}$_PLAT pin of the device. These decoupling capacitors should receive their power from separate V$_{DD,}$ BV$_{DD}$, OV$_{DD}$, GV$_{DD}$, V$_{DD}$_Core, V$_{DD}$_PLAT, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V$_{DD}$, BV$_{DD}$, OV$_{DD}$, GV$_{DD}$, V$_{DD}$_Core, and V$_{DD}$_PLAT planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

3.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (S*n*V$_{DD}$ and X*n*V$_{DD}$) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

3.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to V$_{DD}$, BV$_{DD}$, OV$_{DD}$, GV$_{DD}$, V$_{DD}$_Core, V$_{DD}$_PLAT, X*n*V$_{DD}$, and S*n*V$_{DD}$ as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V$_{DD}$, BV$_{DD}$, OV$_{DD}$, GV$_{DD}$, V$_{DD}$_Core, V$_{DD}$_PLAT, X*n*V$_{DD}$, S*n*V$_{DD}$, and GND pins of the device.

Special cases:

- Local Bus—If parity is not used, tie LDP[0:3] to ground via a 4.7-kΩ resistor, tie LPBSE to OV$_{DD}$ via a 4.7-kΩ resistor (pull-up resistor). For systems which boot from local bus (GPCM)-controlled Flash, a pull up on LGPL4 is required.

- SerDes—Receiver lanes configured for PCI Express are allowed to be disconnected (as would occur when a PCI Express slot is connected but not populated). Directions for terminating the SerDes signals is discussed in Section 3.10, "Guidelines for High-Speed Interface Termination."

3.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8610 requires weak pull-up resistors (2–10 kΩ is recommended) on open drain type pins including I^2C pins and PIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 53. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

The following pins must not be pulled down during power-on reset: DIU_LD[5:6], MSRCID[1:2], $\overline{\text{HRESET_REQ}}$, and TRIG_OUT/READY.

The following are factory test pins and require strong pull up resistors (100 Ω – 1 kΩ) to OV_{DD}: $\overline{\text{LSSD_MODE}}$, TEST_MODE[0:3].

The following pins require weak pull-up resistors (2–10 kΩ) to their specific power supplies: $\overline{\text{LCS}}$[0:4], $\overline{\text{LCS}}$[5]/$\overline{\text{DMA_DREQ}}$2, $\overline{\text{LCS}}$[6]/$\overline{\text{DMA_DACK}}$[2], $\overline{\text{LCS}}$[7]/$\overline{\text{DMA_DDONE}}$[2], IRQ_OUT, IIC1_SDA, IIC1_SCL, IIC2_SDA, IIC2_SCL, and CKSTP_OUT.

The following pins should be pulled to ground with a 100-Ω resistor: SD1_IMP_CAL_TX, SD2_IMP_CAL_TX. The following pins should be pulled to ground with a 200-Ω resistor: SD1_IMP_CAL_RX, SD2_IMP_CAL_RX.

When the platform frequency is 400 MHz, cfg_platform_freq must be pulled down at reset. Also, cfg_dram_type[0 or 1] must be valid at power-up even before $\overline{\text{HRESET}}$ assertion.

For other pin pull-up or pull-down recommendations of signals, see Section 1, "Pin Assignments and Reset States."

3.7 Output Buffer DC Impedance

The MPC8610 drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 51). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and

R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

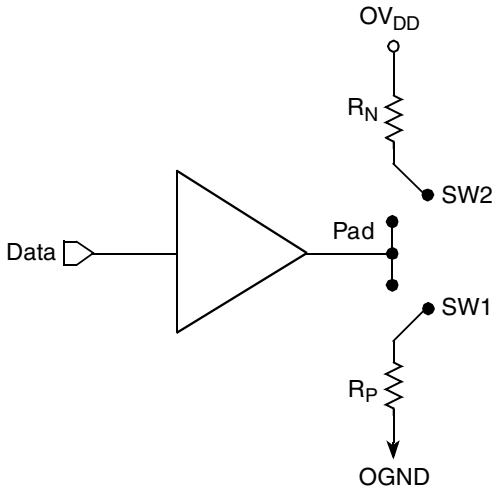


Figure 51. Driver Impedance Measurement

Table 60 summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD}, nominal OV_{DD}, 105°C.

Table 60. Impedance Characteristics

Impedance	Local Bus, DUART, Control, Configuration, Power Management	PCI Express	DDR DRAM	Symbol	Unit
R_N	43 Target	25 Target	20 Target	Z_0	W
R_P	43 Target	25 Target	20 Target	Z_0	W

Note: Nominal supply voltages. See Table 3, T_j = 105°C.

3.8 Configuration Pin Muxing

The MPC8610 provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e600 core PLL ratio configuration pins are not equipped with these default pull-up devices.

3.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 53. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP port connects primarily through the JTAG interface of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 52 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 52, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header shown in Figure 53; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 53 is common to all known emulators.

3.9.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 53. If this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- Tie TCK to OV_{DD} through a 10-kΩ resistor. This will prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

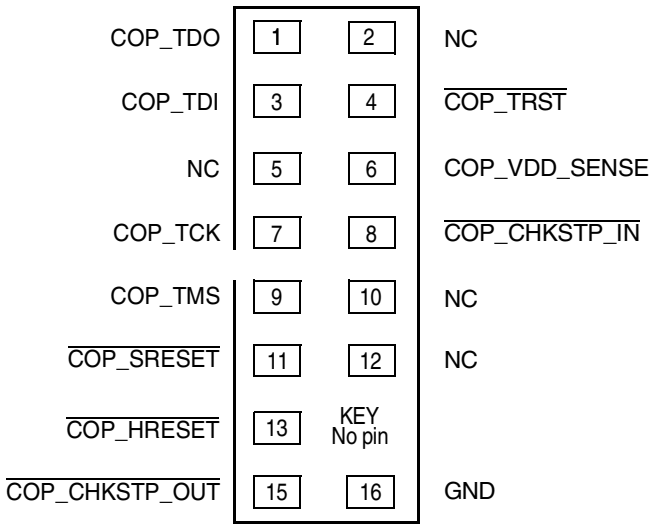
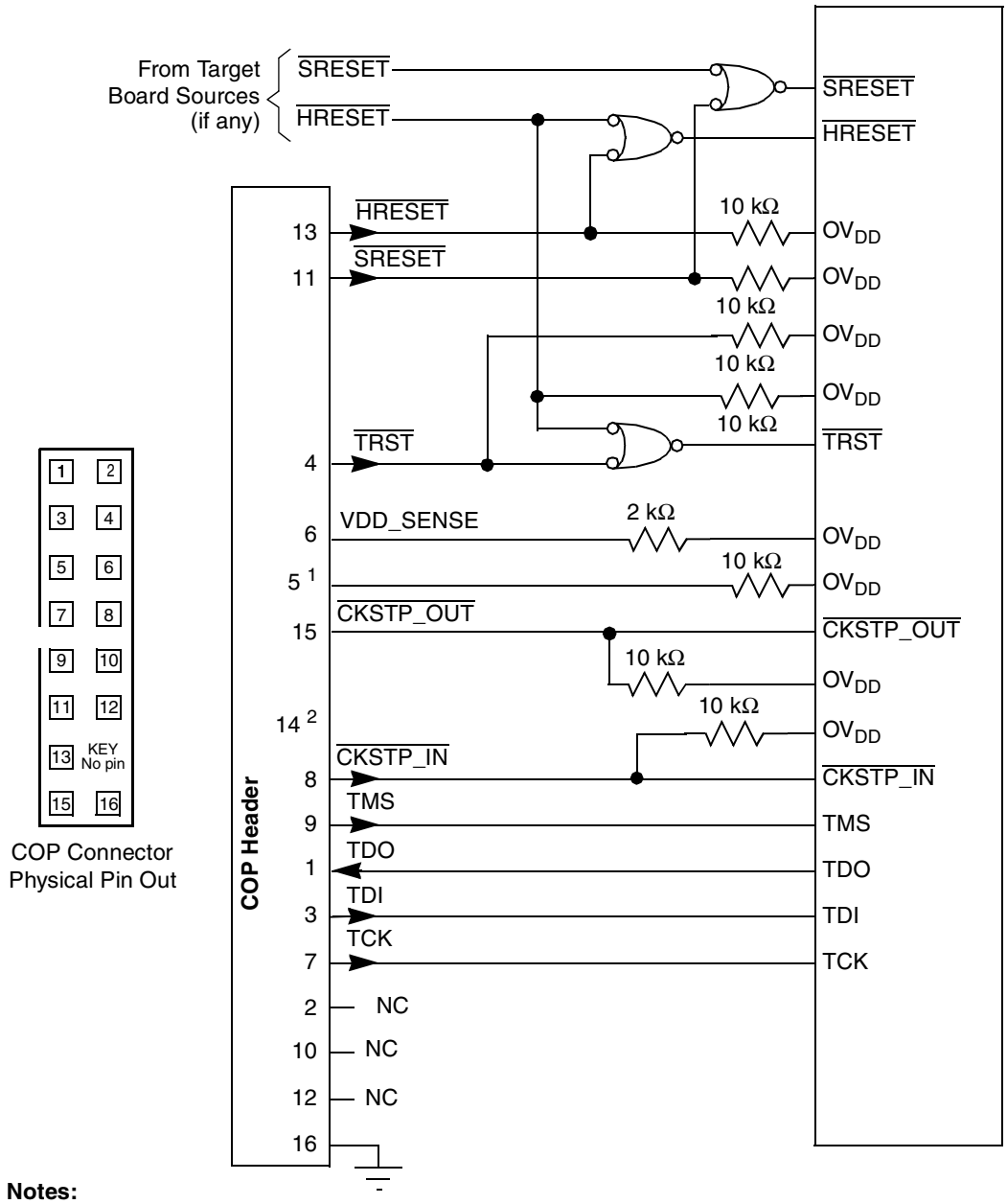


Figure 52. COP Connector Physical Pinout



Notes:

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.

Figure 53. JTAG Interface Connection

3.10 Guidelines for High-Speed Interface Termination

3.10.1 SerDes Interface

The high-speed SerDes interface can be disabled through the POR input cfg_io_ports[0:2] and through the DEVDISR register in software. If a SerDes port is disabled through the POR input the user can not enable it through the DEVDISR register in software. However, if a SerDes port is enabled through the POR input the user can disable it through the DEVDISR register in software. Disabling a SerDes port through software should be done on a temporary basis. Power is always required for the SerDes interface, even if the port is disabled through either mechanism. Table 61 describes the possible enabled/disabled scenarios for a SerDes port. The termination recommendations must be followed for each port.

Table 61. SerDes Port Enabled/Disabled Configurations

	Disabled through POR input	Enabled through POR input
Enabled through DEVDISR	SerDes port is disabled (and cannot be enabled through DEVDISR) Complete termination required (Reference clock not required	SerDes port is enabled Partial termination may be required[1] (Reference clock is required)
Disabled through DEVDISR	SerDes port is disabled (through POR input) Complete termination required (Reference clock not required)	SerDes port is disabled after software disables port Same termination requirements as when the port is enabled through POR input[2] (Reference clock is required)

1 Partial termination when a SerDes port is enabled through both POR input and DEVDISR is determined by the SerDes port mode. If port 1 is in x4 PCI Express mode, no termination is required because all pins are being used. If port 1 is in x1/x2 PCI Express mode, termination is required on the unused pins. If port 2 is in x8 PCI Express mode, no termination is required because all pins are being used. If port 1 is in x1/x2/x4 PCI Express mode, termination is required on the unused pins.

2 If a SerDes port is enabled through the POR input and then disabled through DEVDISR, no hardware changes are required. Termination of the SerDes port should follow what is required when the port is enabled through both POR input and DEVDISR. See Note 1 for more information.

If the high-speed SerDes port requires complete or partial termination, the unused pins should be terminated as described in this section.

The following pins must be left unconnected (floating):

- SD*n*_TX[7:0]
- $\overline{\text{SD}n\text{_TX}}$[7:0]

The following pins must be connected to GND:

- SD*n*_RX[7:0]
- $\overline{\text{SD}n\text{_RX}}$[7:0]
- SD*n*_REF_CLK
- $\overline{\text{SD}n\text{_REF_CLK}}$

For other directions on reserved or no-connects pins, see Section 1, “Pin Assignments and Reset States.”

3.11 Guidelines for PCI Interface Termination

PCI termination if PCI is not used at all.

Option 1

- If PCI arbiter is enabled during POR,
  - All AD pins will be driven to the stable states after POR. Therefore, all ADs pins can be floating. This includes PCI_AD[31:0], PCI_C/$\overline{BE}$[3:0], and PCI_PAR signals.
  - All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-kΩ resistor.
  - It is optional to disable PCI block through DEVDISR register after POR reset.

Option 2

- If PCI arbiter is disabled during POR,
  - All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to OV_{DD} through a single (or multiple) 10-kΩ resistor(s)
  - All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-kΩ resistor
  - It is optional to disable PCI block through DEVDISR register after POR reset.

3.12 Thermal

This section describes the thermal specifications of the MPC8610.

3.12.1 Thermal Characteristics

Table 62 provides the package thermal characteristics for the MPC8610.

Table 62. Package Thermal Characteristics[1]

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient thermal resistance, natural convection, single-layer (1s) board	$R_{\theta JA}$	24	°C/W	1
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JA}$	18	°C/W	1
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	18	°C/W	1
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	15	°C/W	1
Junction-to-board thermal resistance	$R_{\theta JB}$	10	°C/W	2
Junction-to-case thermal resistance	$R_{\theta JC}$	<0.1	°C/W	3

Notes:
1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case resistance is less than 0.1°C/W because the silicon die is the top of the packaging case..

3.12.2 Thermal Management Information

This section provides thermal management information for the flip-chip, plastic ball-grid array (FC_PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC8610 implements several features designed to assist with thermal management, including the temperature diode. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 3.12.2.5, “Temperature Diode,” for more information.

To reduce the die-junction temperature, heat sinks are required; due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. In any implementation of a heat sink solution, the force on the die should not exceed ten pounds force (45 newtons). Figure 54 shows a spring clip through the board. Occasionally the spring clip is attached to soldered hooks or to a plastic backing structure. Screw and spring arrangements are also frequently used.

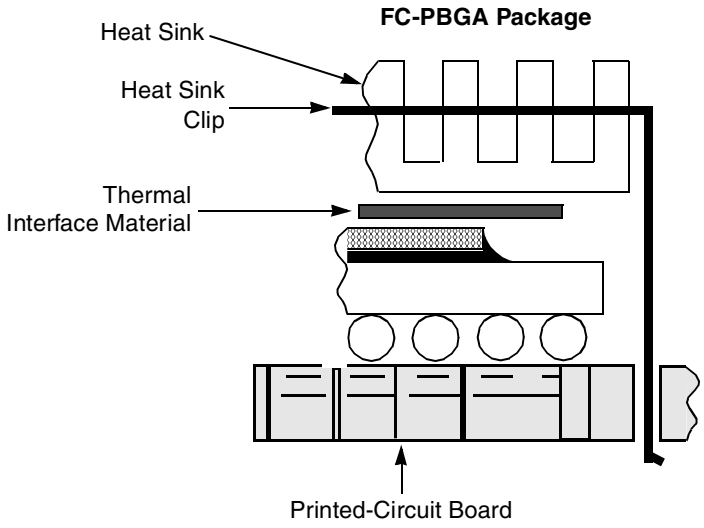


Figure 54. FC-PBGA Package Exploded Cross-Sectional View with Several Heat Sink Options

Suitable heat sinks are commercially available from the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Advanced Thermal Solutions 89 Access Road #27. Norwood, MA02062 Internet: www.qats.com	781-769-2800
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
Calgreg Thermal Solutions 60 Alhambra Road, Suite 1 Warwick, RI 02886 Internet: www.calgreg.com	888-732-6100
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770

Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

3.12.2.1 Internal Package Conduction Resistance

For the exposed-die packaging technology described in Table 62, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Figure 55 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

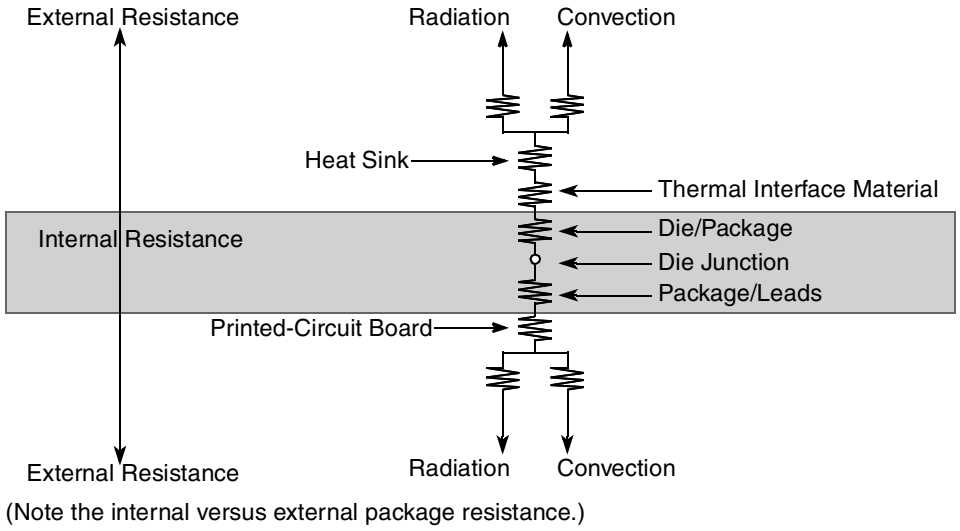


Figure 55. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

3.12.2.2 Thermal Interface Materials

A thermal interface material is recommended at the package-to-heat sink interface to minimize the thermal contact resistance. Figure 56 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, fluoroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. In contrast, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Often, heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 54). Therefore, synthetic grease offers the best thermal performance, considering the low interface pressure, and is recommended. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so on.

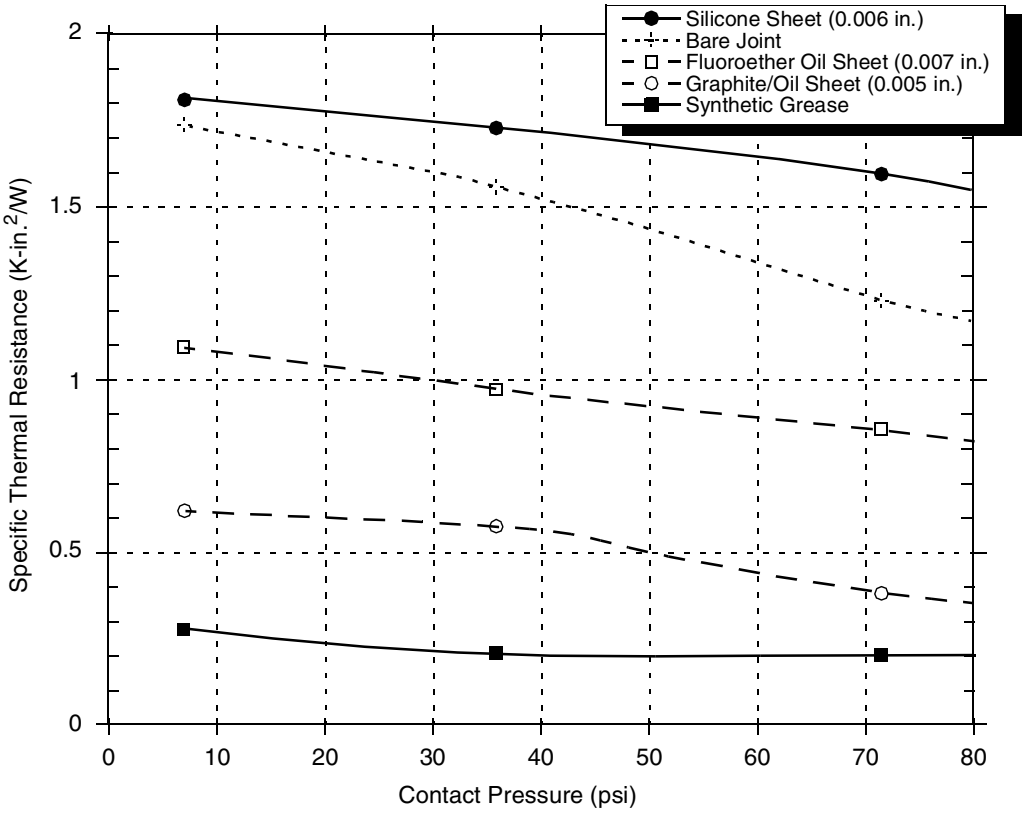


Figure 56. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity and mechanical strength to meet equipment shock/vibration requirements. There are several commercially available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Corporate Center PO Box 994 Midland, MI 48686-0994 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

3.12.2.3 Heat Sink Selection Example

This section provides a heat sink selection example using one of the commercially available heat sinks.

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_i + T_r + (R_{\theta JC} + R_{\theta int} + R_{\theta sa}) \times P_d$$

where:

T_j is the die-junction temperature
T_i is the inlet cabinet ambient temperature
T_r is the air temperature rise within the computer cabinet
$R_{\theta JC}$ is the junction-to-case thermal resistance
$R_{\theta int}$ is the adhesive or interface material thermal resistance
$R_{\theta sa}$ is the heat sink base-to-ambient thermal resistance
P_d is the power dissipated by the device

During operation, the die-junction temperatures (T_j) should be maintained less than the value specified in Table 3. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_i) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material ($R_{\theta int}$) is typically about 0.2°C/W. For example, assuming a T_i of 30°C, a T_r of 5°C, a package $R_{\theta JC}$ = 0.1, and a typical power consumption (P_d) of 10 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 0.2°C/W + \theta_{sa}) \times 10\ W$

For this example, a $R_{\theta sa}$value of 6.7°C/W or less is required to maintain the die junction temperature below the maximum value of Table 3.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, and so on.

Due to the complexity and variety of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board as well as system-level designs.

3.12.2.4 Recommended Thermal Model

For system thermal modeling, the MPC8610 thermal model is shown in Figure 57. Four cuboids are used to represent this device. The die is modeled as 8.5 × 9.7 mm at a thickness of 0.86 mm. See Section 2.3, “Power Characteristics,” for power dissipation details. The substrate is modeled as a single block 29 × 29 × 1.18 mm with orthotropic conductivity of 23.3 W/(m • K) in the xy-plane and 0.95 W/(m • K) in the z-direction. The die is centered on the substrate. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate with a conductivity of 8.1 W/(m • K) in the thickness dimension of 0.07 mm. The C5 solder layer is modeled as a cuboid with dimensions 29 × 29 × 0.4 mm with orthotropic thermal conductivity of 0.034 W/(m • K) in the xy-plane and 12.1 W/(m • K) in the z-direction. An LGA solder layer would be

modeled as a collapsed thermal resistance with thermal conductivity of 12.1 W/(m • K) and an effective height of 0.1 mm. The thermal model uses median dimensions to reduce grid. Please refer to the case outline for actual dimensions.

The thermal model uses approximate dimensions to reduce grid. The approximations used do not impact thermal performance. Please refer to the case outline for exact dimensions.

Conductivity	Value	Unit
Die (8.5 x 9.7 x 0.86mm)		
Silicon	Temperature dependent	
Bump and Underfill (8.5 × 9.7 × 0.07 mm) Collapsed Resistance		
k_z	8.1	W/(m • K)
Substrate (29 × 29 × 1.18 mm)		
k_x	23.3	W/(m • K)
k_y	23.3	
k_z	0.95	
Solder and Air (29 × 29 × 0.4 mm)		
k_x	0.034	W/(m • K)
k_y	0.034	
k_z	12.1	

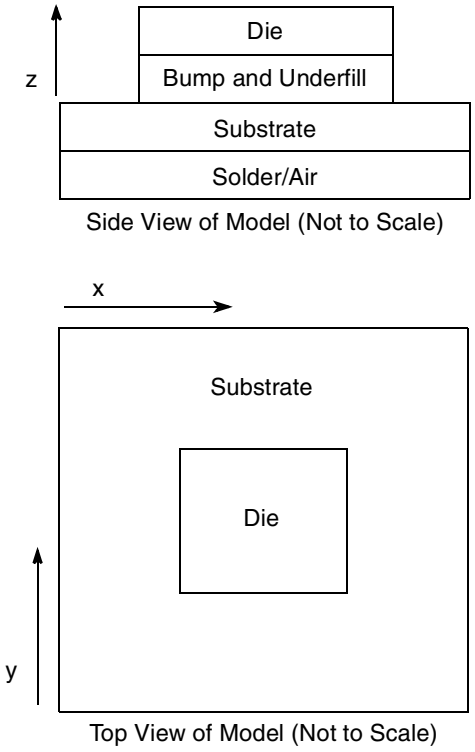


Figure 57. MPC8610 Thermal Model

3.12.2.5 Temperature Diode

The MPC8610 has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. For proper operation, the monitoring device used should auto-calibrate the device by canceling out the V_{BE} variation of each MPC8610's internal diode.

The following are the specifications of the MPC8610 on-board temperature diode:

$V_f > 0.40$ V
$V_f < 0.90$ V
Operating range 2–300 μA
Diode leakage < 10 nA @ 125°C

An approximate value of the ideality may be obtained by calibrating the device near the expected operating temperature.

Ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = I_s \left[e^{\frac{qV_f}{nKT}} - 1 \right]$$

Another useful equation is:

$$V_H - V_L = n\frac{KT}{q}\left[ln\frac{I_H}{I_L} \right]$$

Where:

I_{fw} = Forward current
I_s = Saturation current
V_d = Voltage at diode
V_f = Voltage forward biased
V_H = Diode voltage while I_H is flowing
V_L = Diode voltage while I_L is flowing
I_H = Larger diode bias current
I_L = Smaller diode bias current
q = Charge of electron (1.6×10^{-19} C)
n = Ideality factor (normally 1.0)
K = Boltzman's constant (1.38×10^{-23} Joules/K)
T = Temperature (Kelvins)

The ratio of I_H to I_L is usually selected to be 10:1. The above simplifies to the following:

$$V_H - V_L = 1.986 \times 10^{-4} \times nT$$

Solving for T, the equation becomes:

$$nT = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

4 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 4.1, "Part Numbers Fully Addressed by This Document."

4.1 Part Numbers Fully Addressed by This Document

Table 63 provides the Freescale part numbering nomenclature for the MPC8610. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 63. Part Numbering Nomenclature

MC	nnnn	w	xx	yyyy	M	z

Product Code	Part Identifier	Temp [3]	Package [1]	Core Processor Frequency[2] (MHz)	DDR Speed (MHz)	Product Revision Level
MC	8610	T = –40° to 105°C	PX = Leaded sphere FC-PBGA VT = RoHS lead free FC-PBGA	1066, 800	J = 533 MHz G = 400 MHz	Revision B = 1.1 System Version Register Value for Rev B: 0x80A0_0011—MPC8610
		Blank = 0 to 105°C		1333, 1066, 800		

Notes:
1. See Section 5, “Package Information,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. Extended temperature range devices are offered only with core frequencies of 1066 and 800 MHz.

Table 64 shows the parts that are available for ordering and their operating conditions.

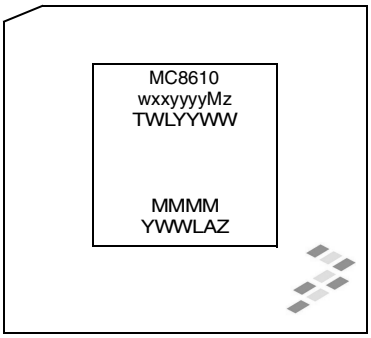
Table 64. Part Offerings and Operating Conditions

Part Offerings[1]	Operating Conditions
MC8610xx1333Jz	Max CPU speed = 1333 MHz, Max DDR = 533 MHz
MC8610xx1066Jz	Max CPU speed = 1066 MHz, Max DDR = 533 MHz
MC8610Txx1066Jz	Max CPU speed = 1066 MHz, Max DDR = 533 MHz extended Temperature Rating
MC8610xx800Gz	Max CPU speed = 800 MHz, Max DDR = 400 MHz
MC8610Txx800Gz	Max CPU speed = 800 MHz, Max DDR = 400 MHz Extended temperature rating

Note:
[1] The xx in the part marking represents the package option.The ‘T’ represents the extended temperature rating. The ‘z’ represents the revision letter. For more information see Table 63.

4.2 Part Marking

Parts are marked as the example shown in Figure 58.



Note:
TWLYYWW is the test code.
MMMM is the M00 (mask) number.
YWWLAZ is the assembly traceability code.

Figure 58. Part Marking for FC-PBGA Device

5 Package Information

This section details package parameters and dimensions.

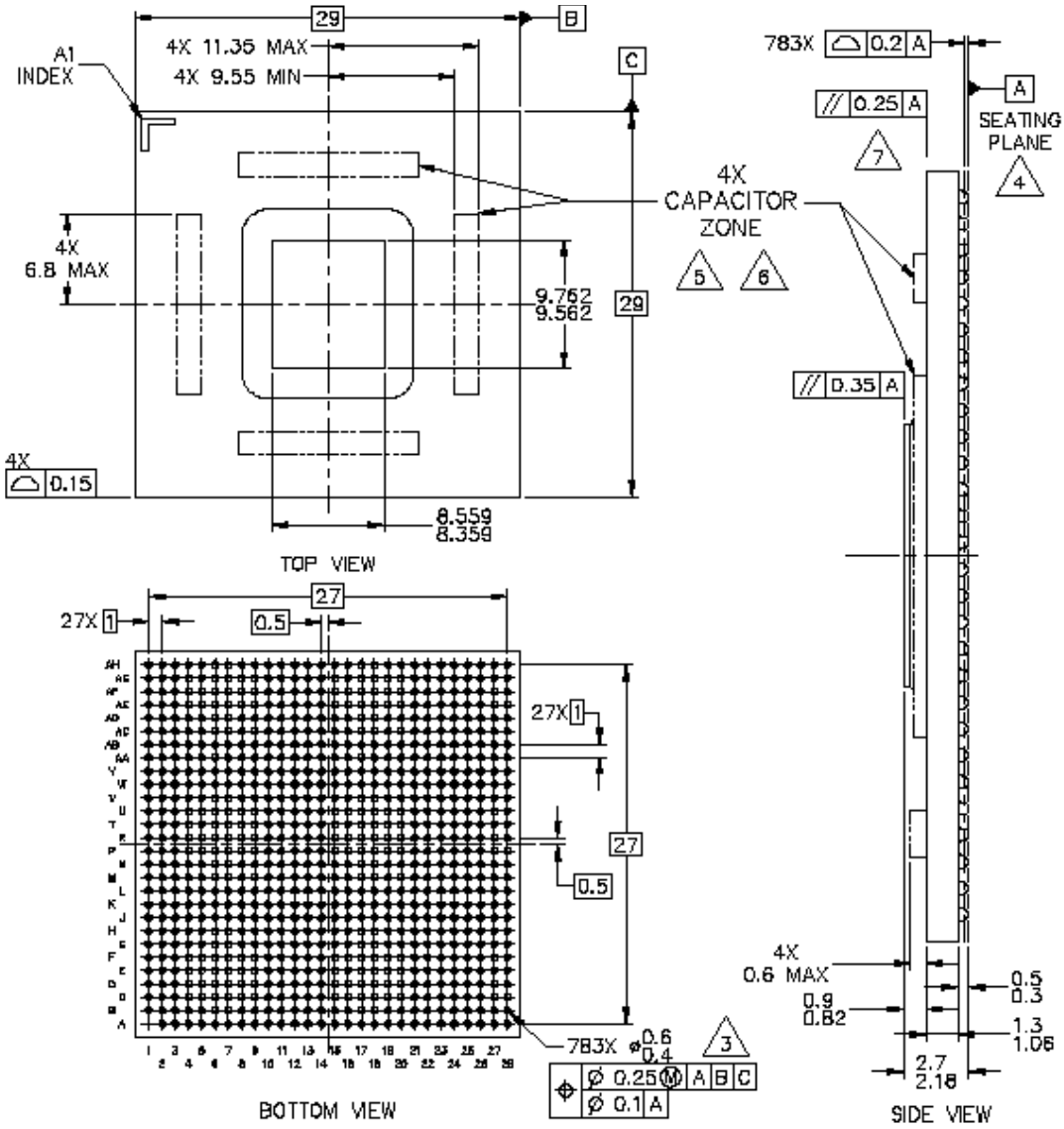
5.1 Package Parameters for the MPC8610

The package parameters are as provided in the following list. The package type is 29 mm × 29 mm, 783 pins. There are two package options: leaded flip chip-plastic ball grid array (FC-PBGA) and RoHS lead-free (FC-PBGA).

Die size	8.5 mm × 9.7 mm
Package outline	29 mm × 29 mm
Interconnects	783
Pitch	1 mm
Minimum module height	2.18 mm
Maximum module height	2.7 mm
Total capacitor count	23 caps; 100 nF each
For leaded FC-PBGA (package option: PX)	
Solder balls	63% Sn 37% Pb
Ball diameter (typical)	0.50 mm
For RoHS lead-free FC-PBGA (package option: VT)	
Solder balls	96.5% Sn, 3.5% Ag
Ball diameter (typical)	0.50 mm

5.2 Mechanical Dimensions of the MPC8610 FC-PBGA

Figure 59 shows the mechanical dimensions and bottom surface nomenclature of the MPC8610 lead-free FC-PBGA.



Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short capacitors or expose metal capacitor pads on package top.
7. All dimensions symmetrical about centerlines unless otherwise specified.

Figure 59. MPC8610 FC-PBGA Dimensions

6 Product Documentation

The following documents are required for a complete description of the device and are needed to design properly with the part.

- *MPC8610 Integrated Host Processor Reference Manual* (document number: MPC8610RM)
- *e600 PowerPC Core Reference Manual* (document number: E600CORERM)

7 Revision History

Table 65 summarizes revisions to this document.

Table 65. Revision History

Rev. No.	Date	Substantive Change(s)
2	1/2009	• Updated Table of Contents • Removed subheading Section 1.1. pin assignments. • Promoted section 4.3, “Ordering Information,” and associated subsections to Section 4, “Ordering Information.” Renumbered subsequent sections and subsections accordingly.
1	01/2009	• Updated Table of Contents • Removed Serial Rapid IO from Section 2.4.4, “Platform Frequency Requirements for PCI-Express” because SRIO is not available on MPC8610. • Removed note in Table 21 and Table 22 that states “Minimum DDR2 frequency is 400 MHz.” • In Table 31, removed rows for t_{i2cr} and t_{i2CF}. Added row for Cb. • Replaced 1067 with 1066 in Table 63. • Replaced CBGA with PBGA in Section 5.1, “Package Parameters for the MPC8610.”
0	10/2008	Initial release.

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