HM10G001

256CH TFT-LCD GATE DRIVER

SPECIFICATION

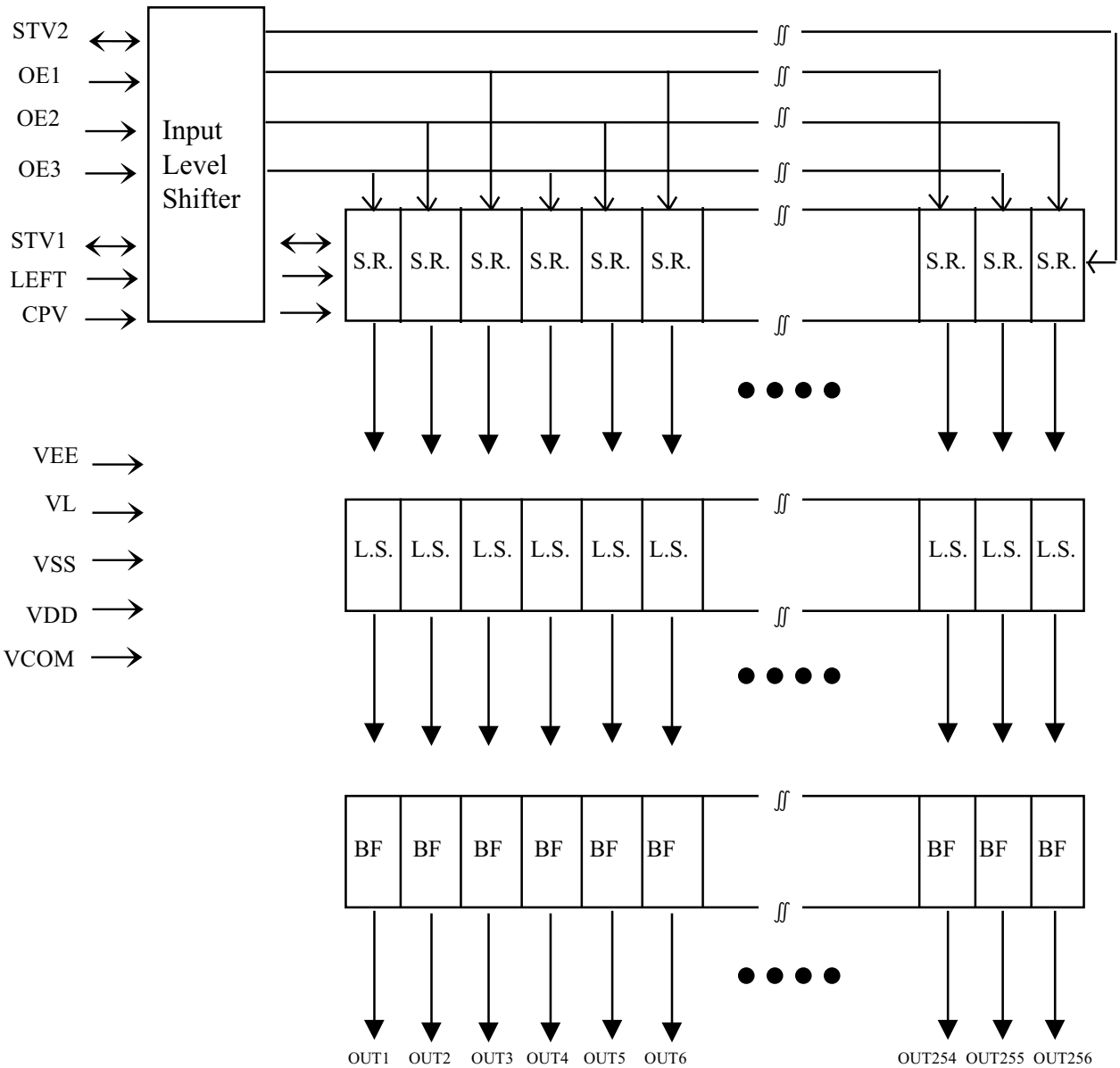
• General Description

HM10G001 is a gate driver for XGA TFT-LCD panels. With many attractive features such as low power consumption, high voltage operation, bi-directional shift register, negative voltage output etc., HM10G001 provides excellent TFT-LCD driving solution.

• Features

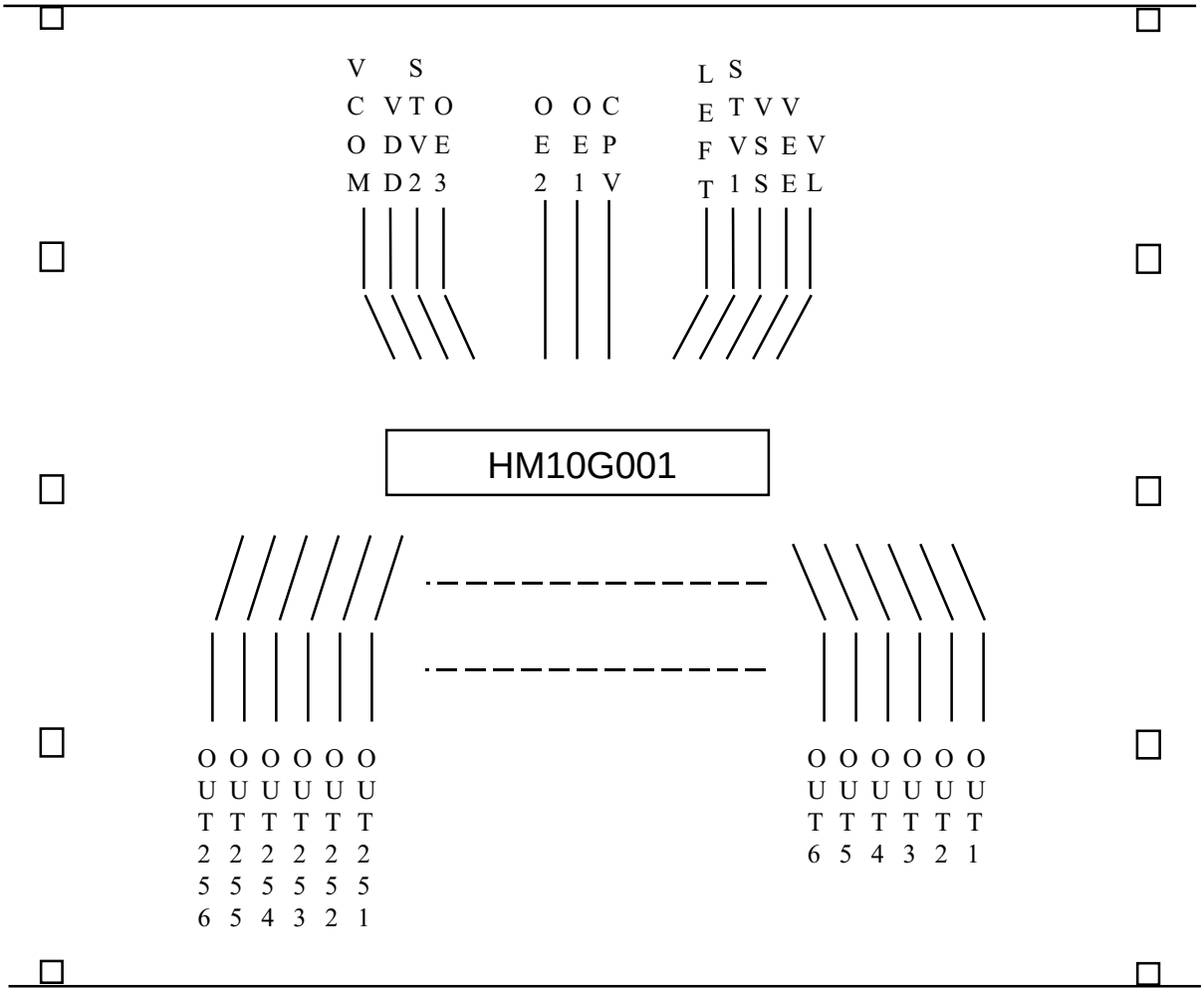
- Gate driver LSI for an Active Matrix LCD.
- The number of LCD driving outputs is 256
- High voltage operation : MAX. VL+35V
- Negative output voltage : VL-VSS = -5 ~ -15V
- Supply voltage for Input Signal : +3.0 ~ +3.6 V
- Selective shift direction.
- Slim TCP (Tape Carrier Package).
- CMOS LSI Construction.

• Block Diagram



BF : Output Buffer
L.S. : Level Shifter
S.R. : Shift Register

• **Pin Configuration**



Input signal : 12EA
Output signal : 256EA

Notice : - This diagram is seen from the top of chip pattern.
- NC pin is not included.
- TCP pin configuration could be different from this diagram according to TCP type.

• PIN Description

PIN NAME	INPUT / OUTPUT	FUNCTION
CPV	Input	Vertical shift clock input It is used as shift clock of shift register. Data is synchronized with the rising edge of this signal.
OE1 OE2 OE3	Input	Output enable control pins When OEn pin is ` H`, the associate LCD panel control outputs are fixed at `VL`, with shift register not cleared. OE signals are asynchronous with CPV. Output pin assignment OE1: OUT1, OUT4, OUT7 ------ OUT253, OUT256 OE2 : OUT2, OUT5, OUT8 ------ OUT254 OE3 : OUT3, OUT6, OUT9 ------ OUT255
LEFT	Input	Data shift direction control pin. Data shift direction; LEFT = High : STV1 → OUT1 → OUT2 …… OUT255 → OUT256 → STV2 LEFT = Low : STV2 → OUT256 → OUT255 …… OUT2 → OUT1 → STV1
STV1 STV2	In_Out	Input /Output pin for vertical synchronous signal. According to the status of LEFT input, these pins can be used as input pin for vertical synchronous signal or output pin for carry signal to the next cascaded gate driver IC. The carry signal is used as vertical synchronous signal of next cascaded gate driver and synchronized with falling edge of CPV. Pin assignment LEFT = L STV1 is output pin for carry signal. STV2 is input pin for vertical synchronous signal. LEFT = H : STV1 is input pin for vertical synchronous signal. STV2 is output pin for carry signal.
OUT1 ~ OUT256	Output	Output pins for LCD panel driving.

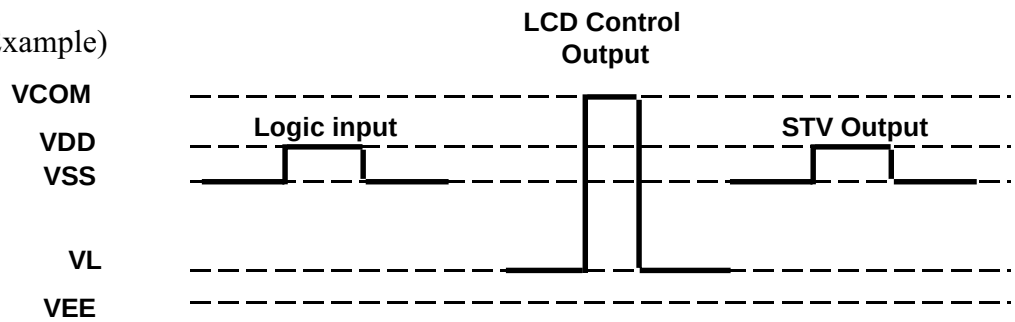
• Pin Description(continued)

PIN NAME	INPUT / OUTPUT	FUNCTION
VCOM	Input	Voltage source for LCD panel control output (High)
VDD	Input	Voltage source for input signal
VSS	Input	GND for input signal
VEE	Input	GND for internal chip operation
VL	Input	Voltage source for LCD panel control output(Low)

• Operation Description

1) Voltage Level of Input And Output Signals.

Example)



- The voltage levels of input signals (CPV, OE1, OE2, OE3, LEFT, STV1, STV2) are as follows:
  `H` level = VDD
  `L` level = VSS
- The voltage levels of carry output signal (STV1, 2) are as follows:
  `H` level = VDD
  `L` level = VSS
- The voltage levels of LCD control outputs are as follows:
  `H` level = VCOM
  `L` level = VL

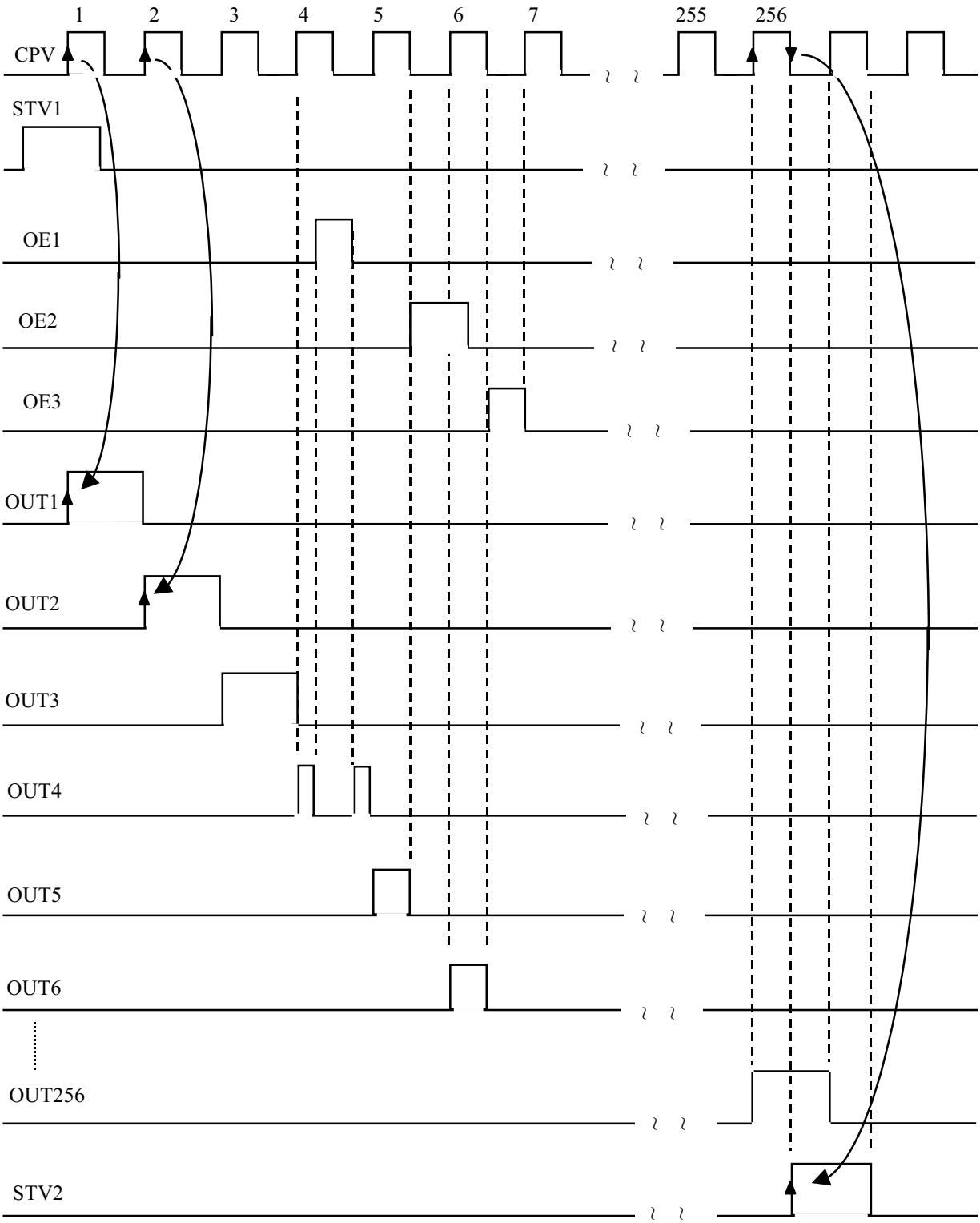
2) Function Description

According to input signals(STV1, STV2, CPV, LEFT, OE1, OE2, OE3), HM10G001 sets the LCD control outputs to `selection signal(H)` or `non-selection signal(L)`. Detail description of the chip operation is as follows.

The data shift direction(Left shift:OUT1 to OUT256, Right shift:OUT256 to OUT1) is selected according to LEFT input. If LEFT is `H`, the vertical shift data from controller is put into the STV1 pin and latched into the left first shift register and then output to LCD control output OUT1 at the associate rising edge of CPV for one CPV period. At the next rising edge of CPV, the data latched at the left first shift register is shifted to the next shift register and then output to OUT2. In this manner, the data is shifted to rightward direction and output to LCD control output pin from OUT1 to OUT256 one by one at the associate rising edge of CPV for one CPV period. The data contained in the 256th shift register is also output to STV2 pin at the associate falling edge of CPV and used as carry signal to the next cascaded gate driver. If LEFT is `L`, the vertical shift data from controller is put into the STV2 pin and latched into the right first shift register and then output to LCD control output OUT256 at the associate rising edge of CPV for one CPV period. At the next rising edge of CPV, the data latched at the right first shift register is shifted to the next shift register and then output to OUT255. In this manner, the data is shifted to leftward direction and outputted to LCD control output pin from OUT256 to OUT1 one by one at the associate rising edge of CPV for one CPV period. The data contained in the 256th shift register is also output to STV1 pin at the associate falling edge of CPV and used as carry signal to the next cascaded gate driver.

If the OEn signal is `H`, the associated outputs are set to VL level, but the internal data contained in the shift register is not changed and when the OEn signal return to `L` the information contained in the shift register is outputted to the display. Refer to output pin description for the assignment of output pins to OEn.

• **Timing Diagram (When LEFT = H)**



• Absolute maximum ratings(VSS Refferenced)

Reference Voltage : VSS

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage(1)	VDD	-0.3		7.0	V
Supply voltage(2)	VEE	-20		0.3	V
Voltage difference(1)	VL-VEE	-0.3		7.0	V
Voltage difference(2)	VCOM-VEE	-0.3		40	V
Voltage difference(3)	VCOM-VL	-0.3		40	V
Input voltage	Vin	-0.3		VDD+0.3	V
Operating frequency	f_{CPV}			100	kHz
Storage temperature range	TSTG	-55		125	℃

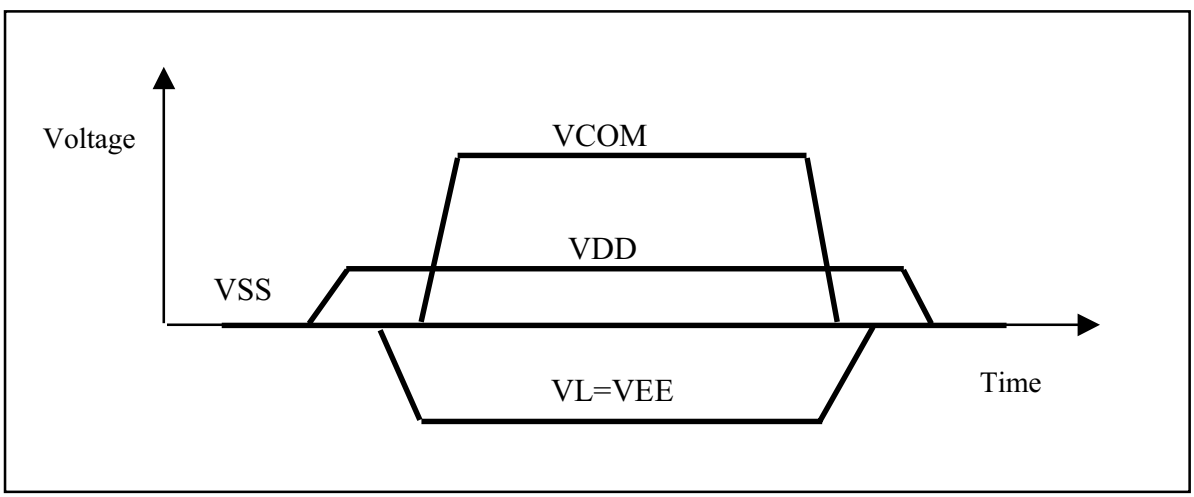
Each voltage should be kept to satisfy absolute maximum ratings.
If the applied voltage go beyond absolute maximum ratings, the chip may be broken eternally.
Exposure to absolute maximum ratings condition for long periods may affect badly to the reliability .

• Recommended Operating Conditions (VSS=0)

Reference Voltage : VSS

ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage(1)	VDD	3.0	3.3	3.6	V
Supply voltage(2)	VCOM	10		25	V
Supply voltage(3)	VEE	-15		-5	V
Voltage difference(1)	VL-VEE	0		6.0	V
Voltage difference(2)	VCOM-VEE	17		35	V
Voltage difference(3)	VCOM-VL	17		35	V
Input voltage	Vin	VSS-0.3		VDD+0.3	V
Operating frequency	f_{CPV}			100	kHz
Operating free-air temperature range	TA	-20		75	℃

• Power ON/OFF Sequence



Power ON/OFF Sequence

• Electrical characteristics under recommended operating conditions

ITEM	SYMBOL	CONDITIONS	RATINGS			UNIT	PINS
			MIN.	TYP.	MAX.		
`0` input voltage	VIL		VSS		0.2×VDD	V	All inputs
`1` input voltage	VIH		0.8×VDD		VDD	V	All inputs
`0` output voltage(1)	VOL	IOL=40㎂	VSS		VSS+0.4	V	STV1,2
`1` output voltage(2)	VOH	IOH= 40㎂	VDD-0.4		VDD	V	STV1,2
`0` output resistance	ROL	VOUT= VL+0.5V			1000	Ω	OUT1~ OUT256
`1` output resistance	ROH	VOUT= VCOM-0.5V			1000	Ω	OUT1~ OUT256
input current	Iin		-5.0		+5.0	㎂	All inputs
current consumption(1)	IDD	(Note1)			500	㎂	VDD
current consumption(2)	ICOM	(Note1)			100	㎂	VCOM

Note1: Current consumption of VDD, VDL, VCOM pin respectively under test conditions of;

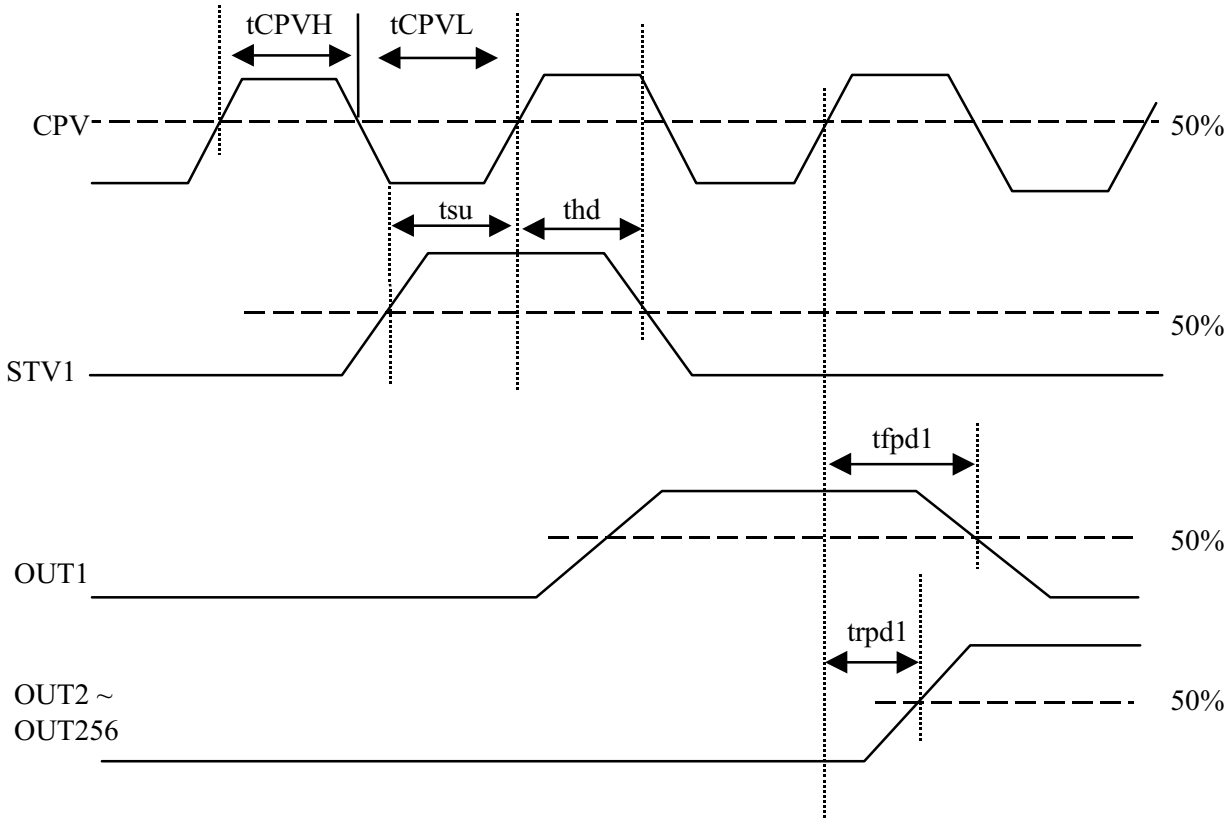
- Output : No load
- Input : VIH= VDD, VIL= VSS, f_{CPV}= 50KHz, f_{STV}= 83Hz, OE1~3= VIL.

•AC Characteristics under recommended operating conditions

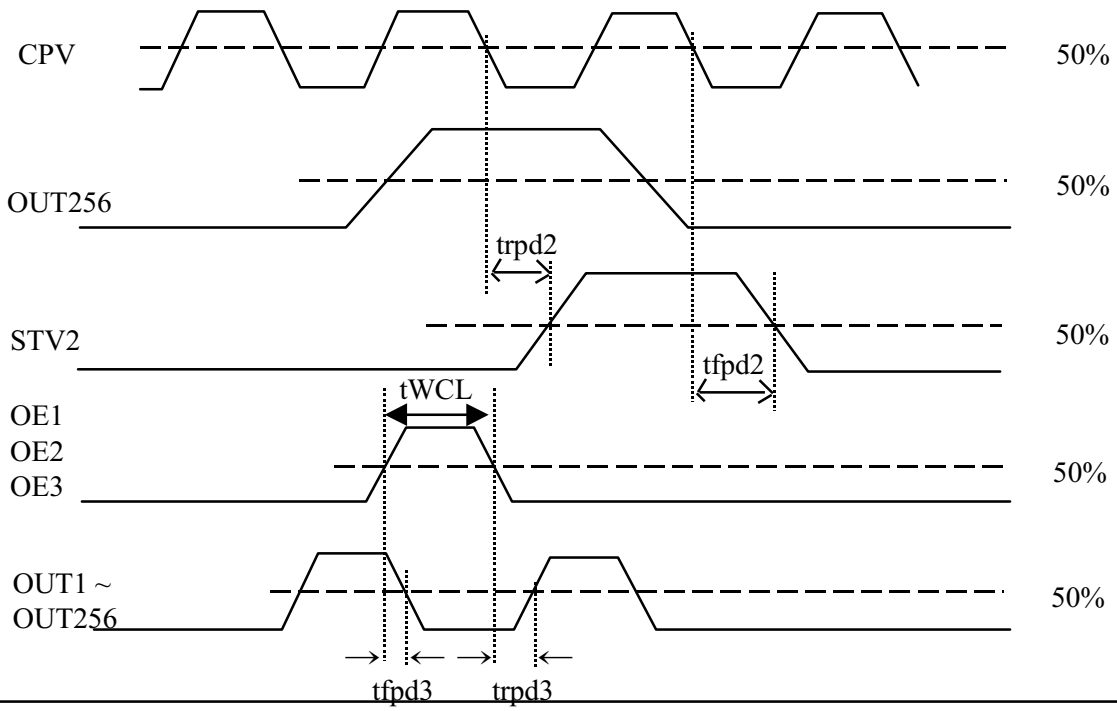
ITEM	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Clock frequency	fcpv			100	kHz
CPV clock pulse width	tCPVH,tCPVL	Duty=50%	5.0		us
OE signal pulse width	tWCL		1.0		us
Data setup time	tsu		700		ns
Data hold time	thd		700		ns
Output delay time1	trpd1	C_L=300pF		1000	ns
Output delay time2	tfpd1	C_L=300pF		1000	ns
Output delay time3	trpd2	C_L=30pF		800	ns
Output delay time4	tfpd2	C_L=30pF		800	ns
Output delay time5	trpd3	C_L=300pF		800	ns
Output delay time6	tfpd3	C_L=300pF		800	ns
Input signal rising time	t_{r_in}			100	ns
Input signal falling time	t_{f_in}			100	ns
Output signal rising time	tr_out1	C_L=300pF		350	ns
Output signal falling time	tf_out1	C_L=300pF,VL=VSS		350	ns
Output signal rising time	tr_out2	C_L=30pF		100	ns
Output signal falling time	tf_out2	C_L=30pF		100	ns

Refer to the following figure for the symbol.

•AC Characteristic Timing Diagram(1) (When LEFT=H)

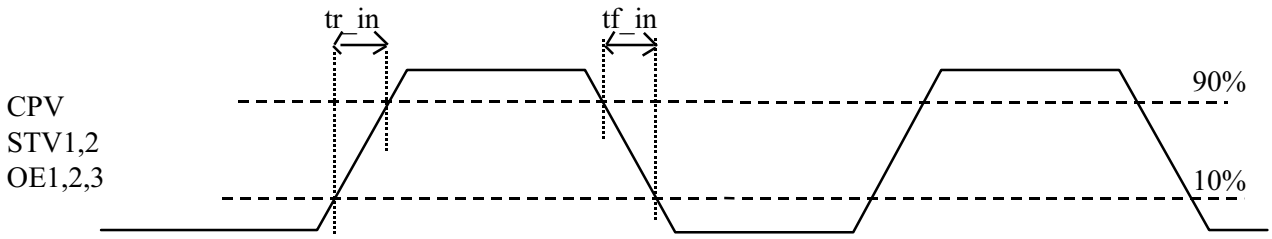


•AC Characteristic Timing Diagram(2) (Where LEFT=H)

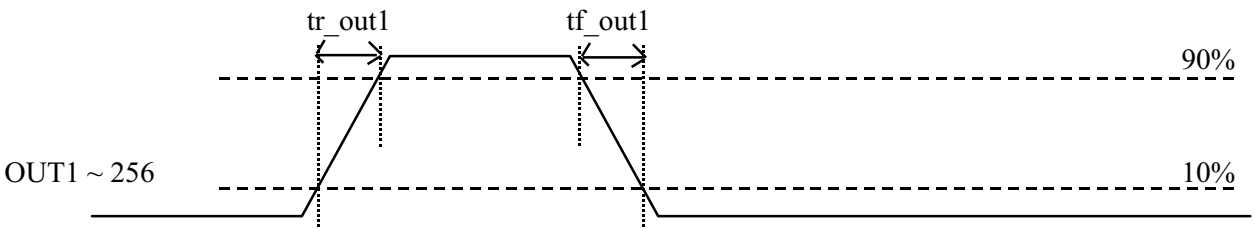


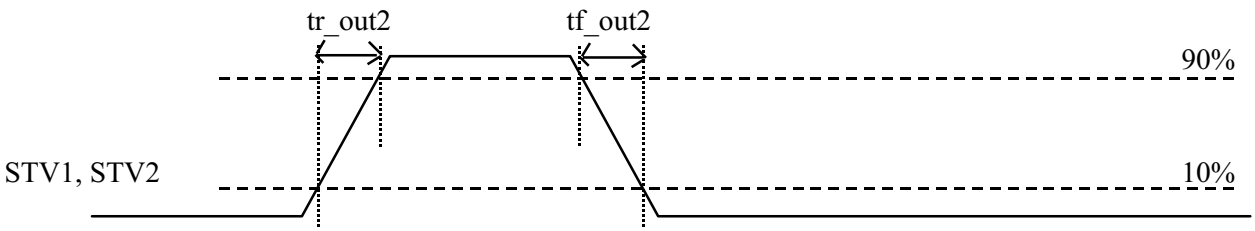
•AC Characteristics Timing Diagram(3)

Rising/falling time of input signal



Rising/falling time of output signal





Revision History

Date	Version	Revised Items
1999.4.1	Preliminary	——
1999.5.6	1.0	——
1999.12.3	1.1	- Power ON/OFF Sequence - Device Name - VHI : 0.7VDD -> 0.8VDD