



SPN4546

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN4546 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

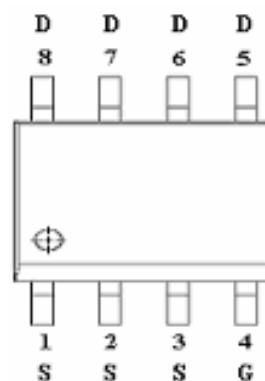
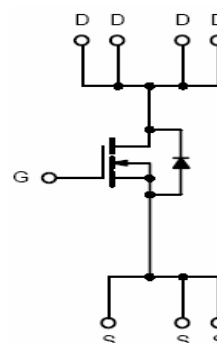
FEATURES

- ◆ 40V/6.0A, $R_{DS(ON)} = 48 \text{ m}\Omega @ V_{GS} = 10\text{V}$
- ◆ 40V/5.0A, $R_{DS(ON)} = 55 \text{ m}\Omega @ V_{GS} = 4.5\text{V}$
- ◆ 40V/4.5A, $R_{DS(ON)} = 80 \text{ m}\Omega @ V_{GS} = 2.5\text{V}$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP – 8P package design

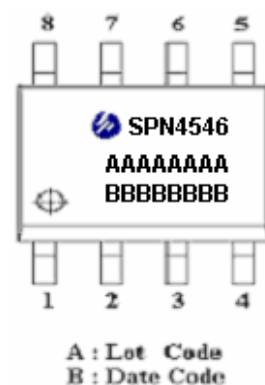
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOP – 8P)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4546S8RGB	SOP- 8P	SPN4546

※ SPN4546S8RGB 13" Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	40	V
Gate –Source Voltage	V _{GSS}	±12	V
Continuous Drain Current(T _J =150°C)	I _D	6.0	A
		5.0	
Pulsed Drain Current	I _{DM}	30	A
Continuous Source Current(Diode Conduction)	I _S	2.3	A
Power Dissipation	P _D	2.5	W
		1.6	
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	80	°C/W



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

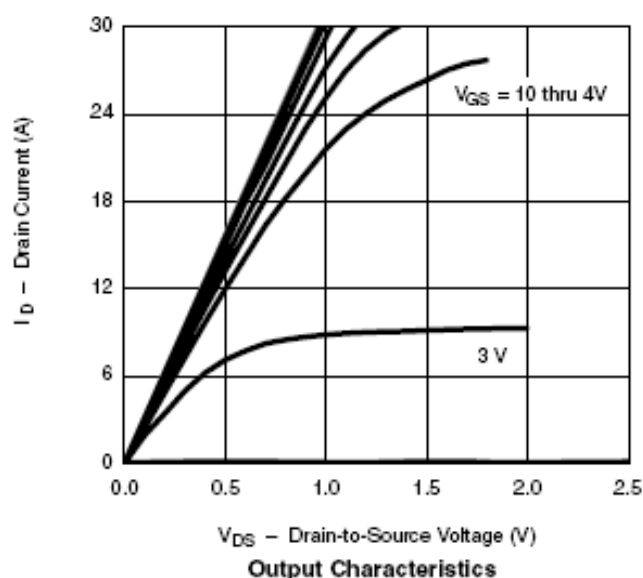
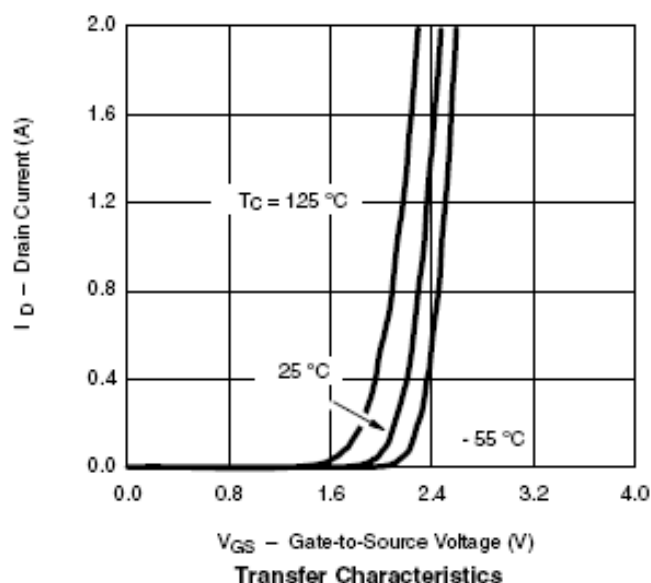
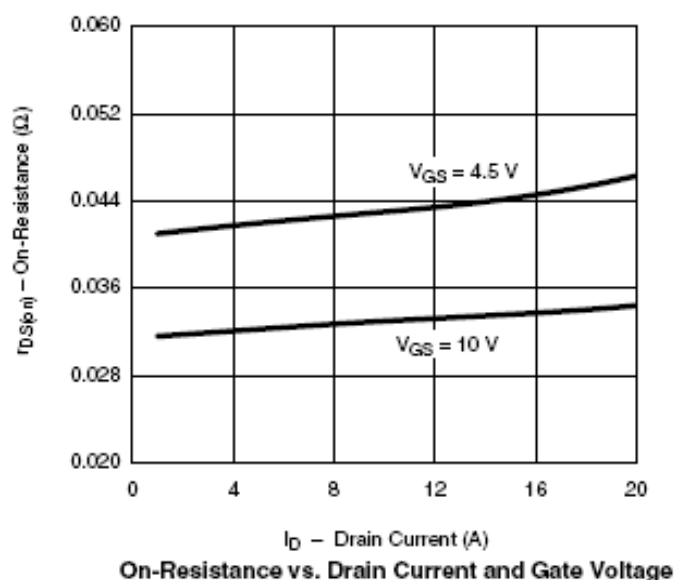
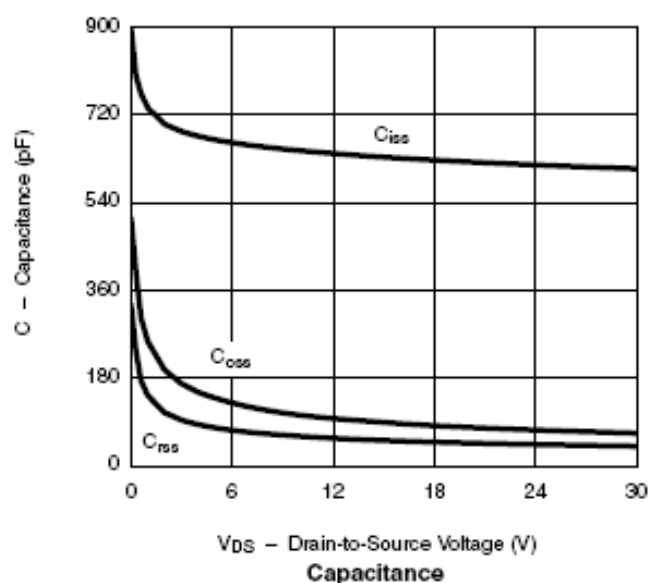
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250μA	40			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.5		1.2	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V			1	μA
		V _{DS} =40V, V _{GS} =0V T _J =85°C			5	
On-State Drain Current	I _{D(on)}	V _{DS} = 5V, V _{GS} =4.5V	10			A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D =6.0A		0.040	0.048	Ω
		V _{GS} =4.5V, I _D =5.0A		0.047	0.055	
		V _{GS} =2.5V, I _D =4.5A		0.072	0.080	
Forward Transconductance	g _{fs}	V _{DS} =15V, I _D =6.2A		13		S
Diode Forward Voltage	V _{SD}	I _S =2.3A, V _{GS} =0V		0.8	1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =15V, V _{GS} =10V I _D = 2A		16	24	nC
Gate-Source Charge	Q _{gs}			3		
Gate-Drain Charge	Q _{gd}			2.5		
Turn-On Time	t _{d(on)}	V _{DD} =15V, R _L =15Ω I _D =1.0A, V _{GEN} =10V R _G =6Ω		15	20	nS
	t _r			6	12	
Turn-Off Time	t _{d(off)}			10	20	
	t _f			40	80	



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TYPICAL CHARACTERISTICS

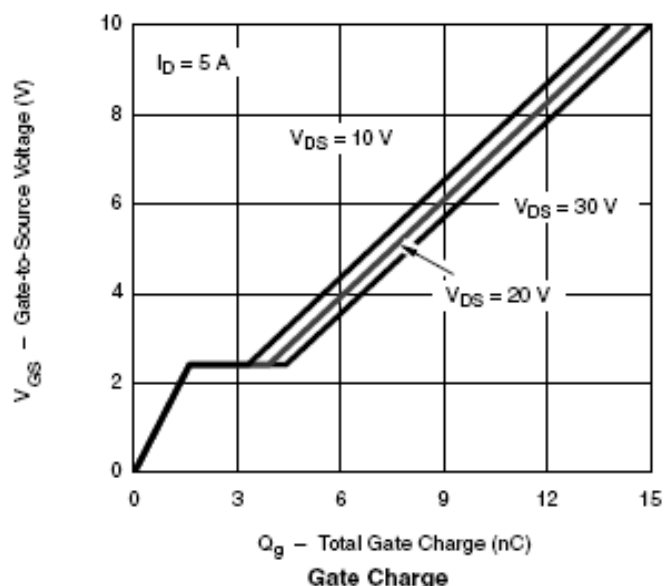
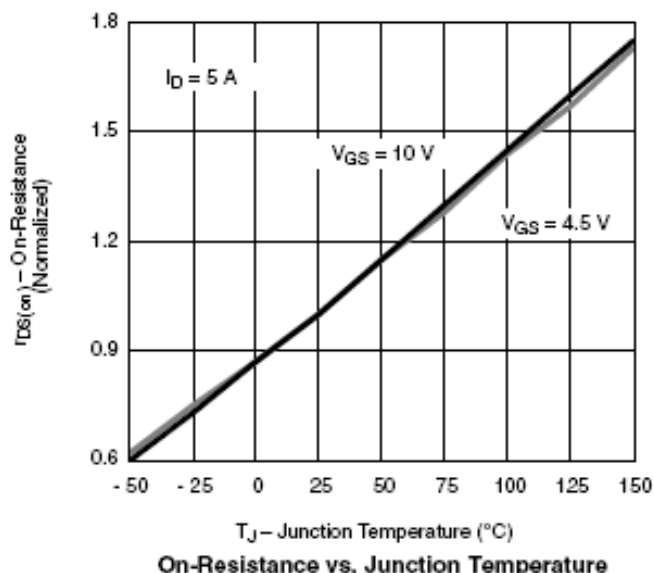
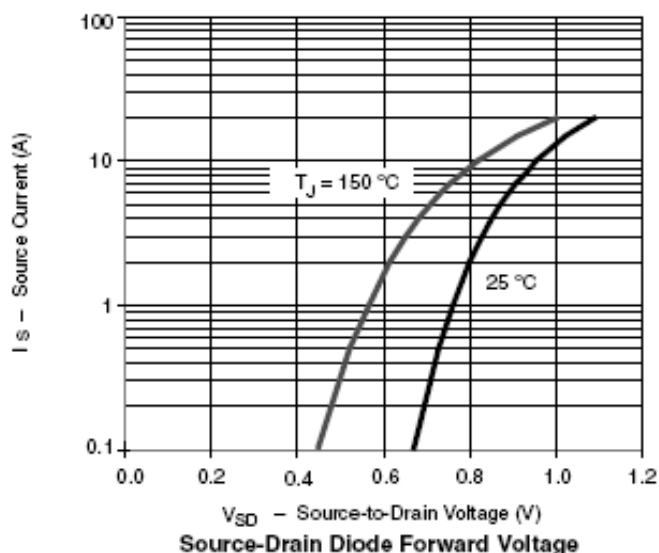
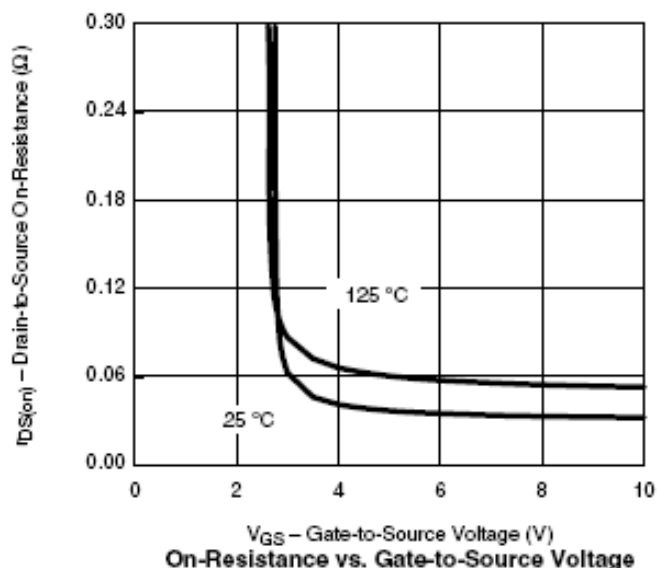




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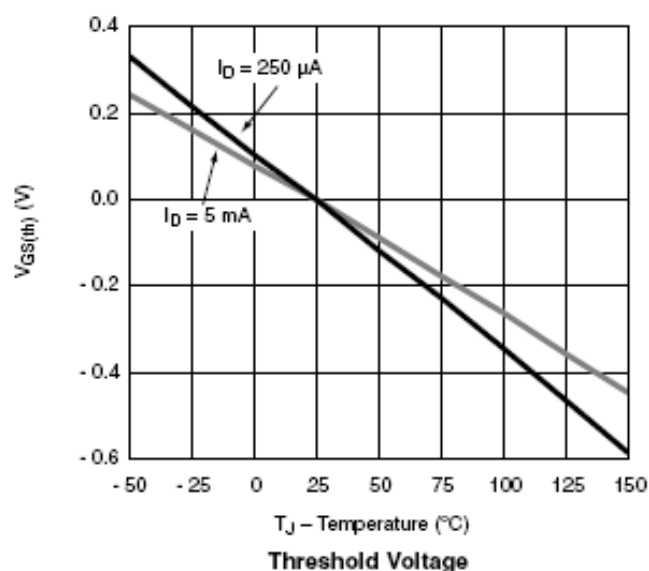
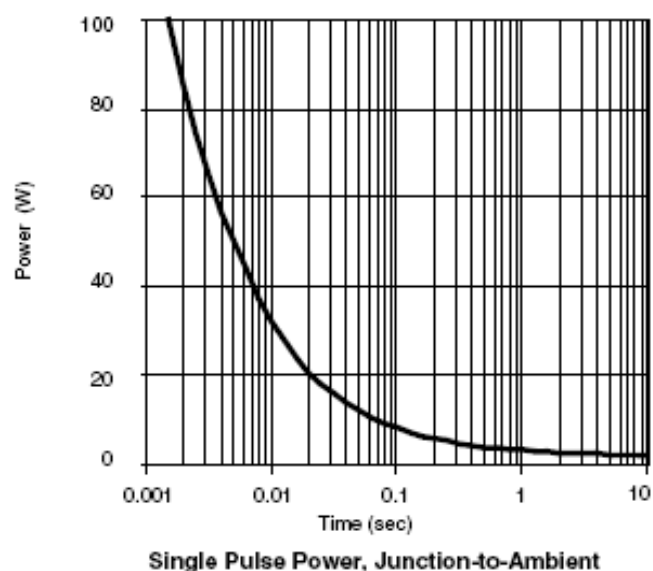
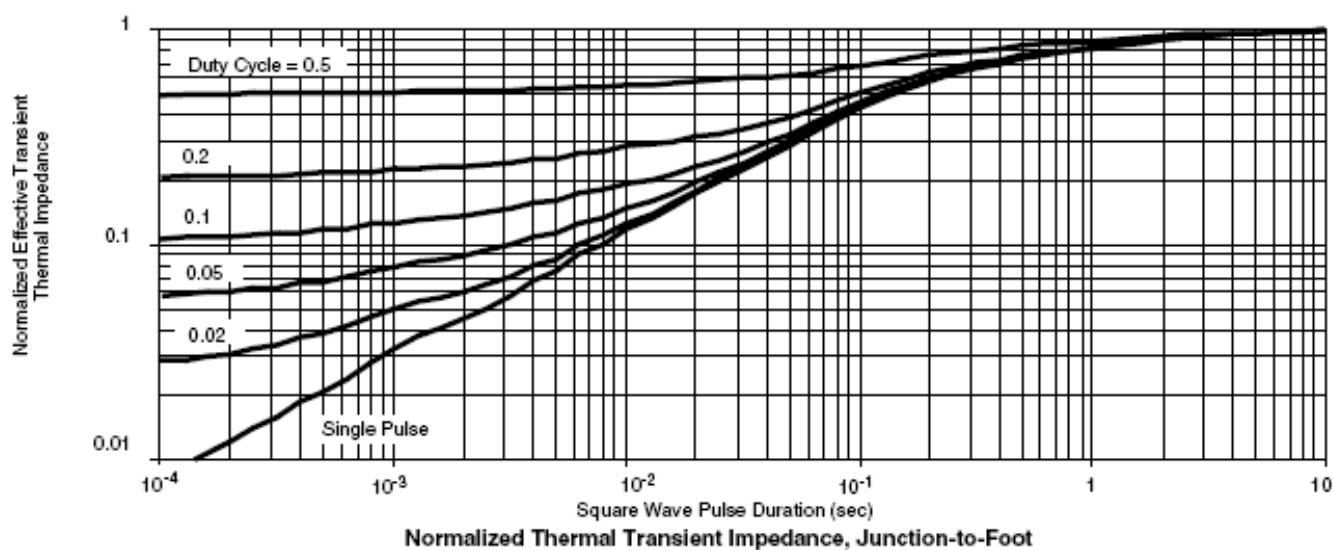




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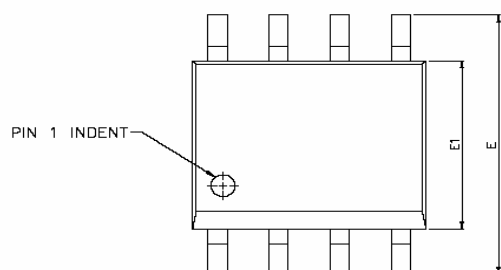
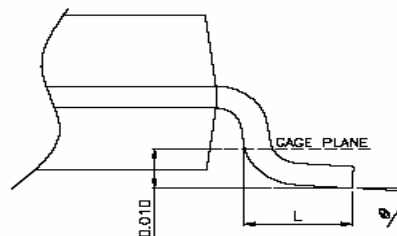




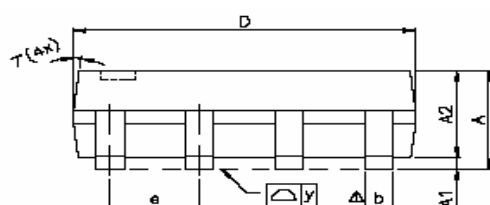
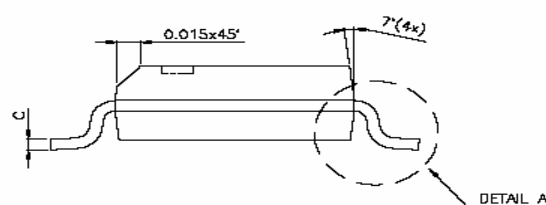
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SOP- 8 PACKAGE OUTLINE



DETAIL A



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
Δy	—	—	0.076	—	—	0.003
θ	0°	—	8°	0°	—	8°



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