# W86L388D
# Winbond Host Interface
# SD/MMC Memory Card
# Bridge

# W86L388D Data Sheet Revision History

| | Pages | Dates | Version | Version on Web | Main Contents |
|---|---|---|---|---|---|
| 1 | | 08/2001 | 0.50 | | First published. |
| 2 | | | | | |
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Winbond Electronics Corp.

Preliminary

# Table of Content

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PRELIMINARY

## 1. GENERAL DESCRIPTION

The W86L388D is a SD/MMC host interface bridge used between host microprocessor and SD/MMC. The data width of host microprocessor can be 8-bit or 16-bit. W86L388D can support synchronous or asynchronous type of host interface. It also supports DMA or Interrupt type of transfer mode to improve data transfer performance between host microprocessor and SD/MMC. W86L388D is fit for most of IA devices, such as PDA, Cellular Phone, DSC, and MP3 player.

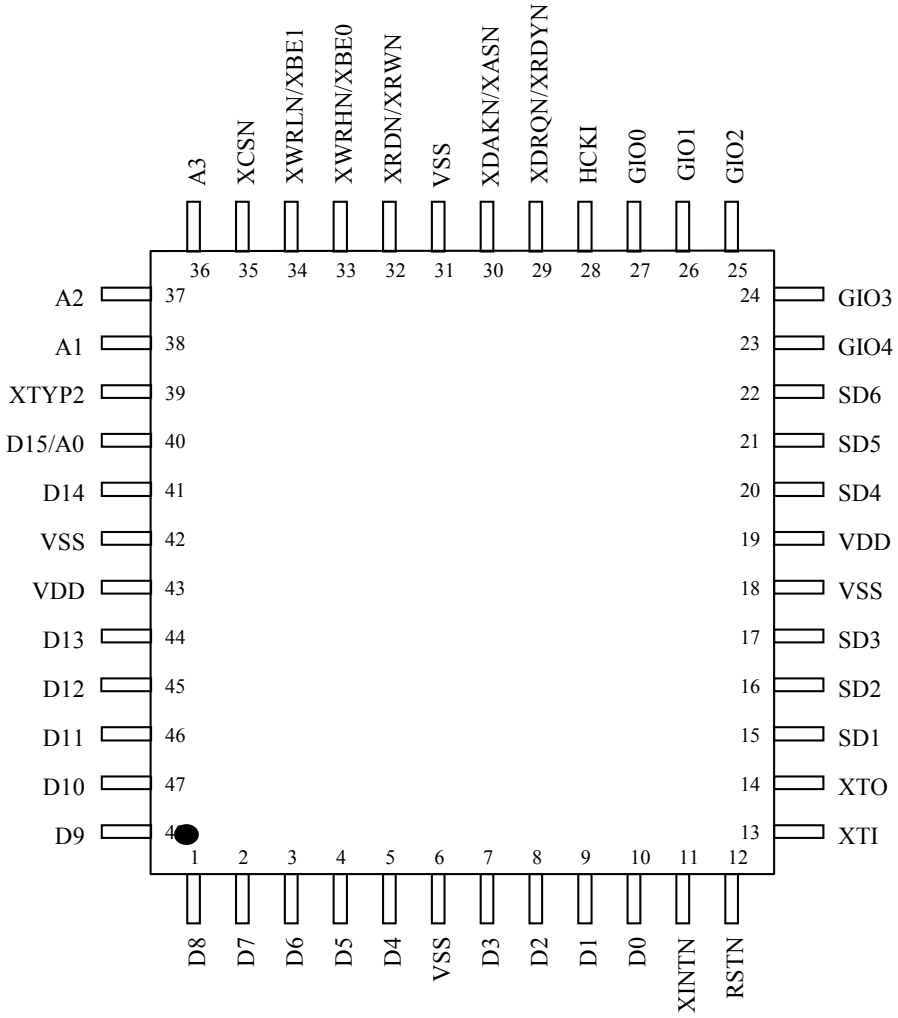
## 2. FEATURES

- Compliant with SD spec. Version 1.0
- Compliant with MMC spec. Version 2.2
- Support two types of host microprocessor interface access--synchronous and asynchronous mode
- DMA and Interrupt transfer mode supported
- Host microprocessor 8/16 bit data bus
- Built-in crystal driver circuit, support external oscillator or crystal clock
- Extra 5 programmable GPIO supported
- Wide range of clock input from 3.58MHz up to 25MHz
- 3.3V opereation
- 48-pin LQFP package

## Ordering Information

| Part Number | Package Type | Production Flow |
|---|---|---|
| W86L388D | 48-PIN LQFP | Commercial, 0°C to +70°C |

## 3. PIN CONFIGURATION



## 4. PIN DESCRIPTIONS

| Pin | Name | Type | Description |
|---|---|---|---|
| **SD Interface:** | | | |
| 21 | SD5 | DO/DI | SD connection #5 |
| 22 | SD6 | DO/DI | SD connection #6 |
| 15 | SD1 | DO/DI | SD connection #1 |
| 16 | SD2 | DO/DI | SD connection #2 |
| 17 | SD3 | DO | SD connection #3 |
| 20 | SD4 | DO | SD connection #4 |
| **Crystal Driver:** | | | |
| 13 | XTI | DI | Clock driver input signal, may be used as external clock input. |
| 14 | XTO | DO | Clock driver output signal. |
| **Host Interface Signal:** | | | |
| 28 | HCKI | DI | Host clock input. |
| 35 | XCSN | DI | Chip select input pin, active low. |
| 36:38 | A[3:1] | DI | Address input pins. |
| 40 | D15/A0 | DI/DO | Data bus D15 pin, D[15:8] is the high byte of the data bus, D15 also used as A0 when 8-bit CPU data size. In 8-bit mode, internal register high byte (D15:8) will accessed at data bus [7:0] when A0 = 1, low byte (D7:0) will accessed at data bus [7:0] when A0 = 0. |
| 41 | D14 | DI/DO | Data bus D14 pin. |
| 44:48 | D[13:9] | DI/DO | Data bus [13:9] pins. |
| 1:5 | D[8:4] | DI/DO | Data bus [8:4] pins, D[7:0] is the low byte of the data bus. |
| 7:10 | D[3:0] | DI/DO | Data bus [3:0] pins. |
| 33 | XWRHN/<br>XBE0 | DI | Type 1:<br>High byte (D15 to D8) write control pin, active low.<br>Type 2:<br>High byte (D15 to D8) data valid pin, active low. |
| 34 | XWRLN/<br>XBE1 | DI | Type 1:<br>Low byte (D7 to D0) write control pin, active low.<br>Type 2:<br>Low byte (D7 to D0) data valid pin, active low. |

4. PIN DESCRIPTIONS, CONTINUED

| Pin | Name | Type | Description |
|---|---|---|---|
| 32 | XRDN/<br>XRWN | DI | Type 1:<br>Read control pin, active low.<br>Type 2:<br>Read write control pin,<br>1: read<br>0: write |
| 11 | XINTN | DO | Interrupt request pin,active low. |
| 30 | XDAKN/<br>XASN | DI | Type 1:<br>DMA transfer acknowledge pin, active low.<br>Type 2:<br>Bus access cycle start pin, active low. |
| 29 | XDRQN/<br>XRDYN | DO | Type 1:<br>DMA transfer request pin, active low.<br>Type 2:<br>Bus cycle complete pin, active low. |
| 39 | XTYP2 | DI | Host interface type 2 select pin,<br>0 : type 1 mode.<br>1 : type 2 mode. |
| **General I/O Port Signal (SD I/F):** | | | |
| 27:23 | GIO[0:4] | DI/DO | 5-bit general input output port signals. GIO0 pin can be used as dedicate card detecttion. |
| **Other Signal:** | | | |
| 12 | RSTN | DI | Reset input, hardware reset input, active low. |
| **Power:** | | | |
| 19,43 | VDD | DP | Power supply 3.3V |
| 6,18,<br>31,42 | VSS | DP | Ground |

Type: DP is Power, DI is Digital Input, DO is Digital Output.

## 5. BLOCK DIAGRAM

### 5.1 Block Diagram

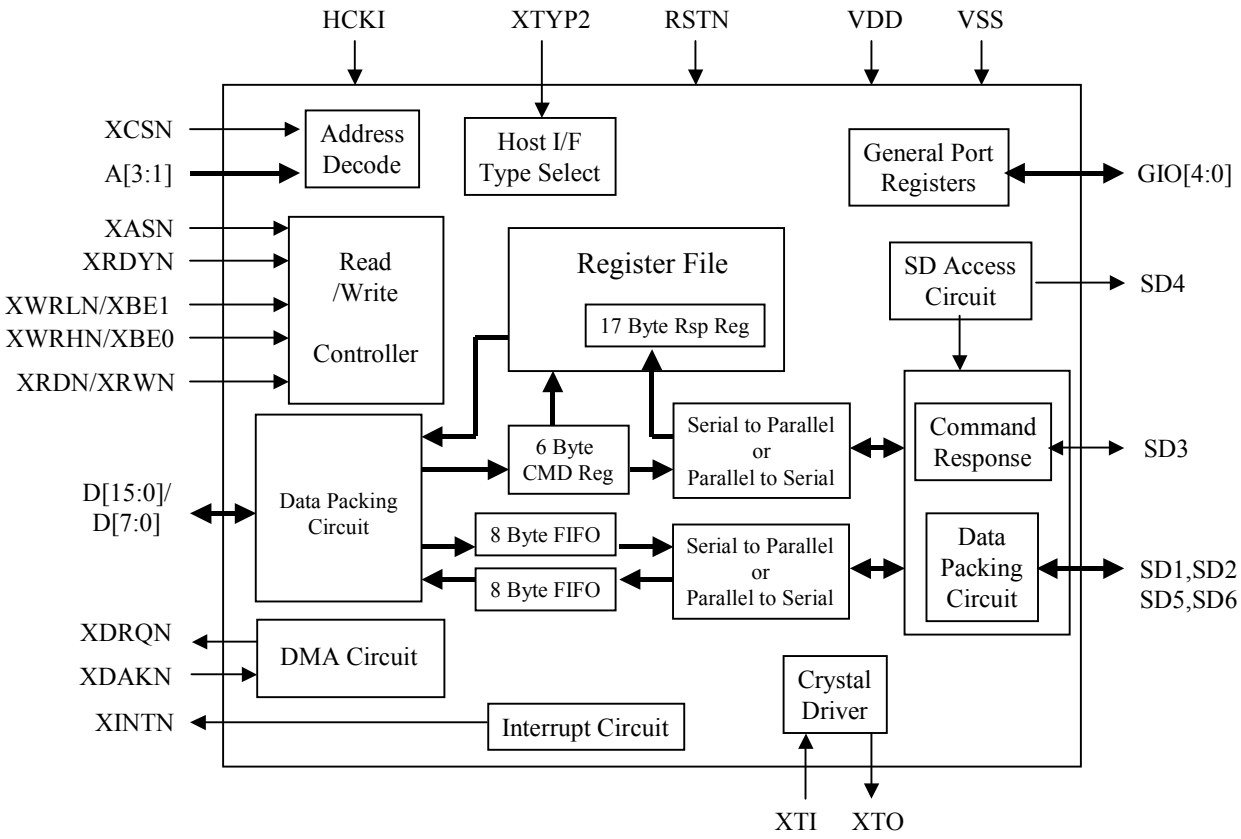



Fig. 5-1 Block Diagram of W86L388

## 6. REGISTER

The registers in the W86L388 are direct access registers and indirect access registers. The direct access registers and indirect access registers are listed as follows:

| Addr A[3:1] | Register Name (note 1) | Content (note 2) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | B 15 | B 14 | B 13 | B 12 | B 11 | B 10 | B 9 | B 8 | B 7 | B 6 | B 5 | B 4 | B 3 | B 2 | B 1 | B 0 |
| Direct Access Registers: | | | | | | | | | | | | | | | | | |
| 000 | Command Pipe Reg. (WO) Response Reg. (RO) | Command pipe registers / Response registers | | | | | | | | | | | | | | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 001 | Status Reg. (RO) | Status | | | | | | | | - | - | - | - | - | - | - | - |
| | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | | | | | | | | |
| 001 | Control Reg. (R/W) | - | - | - | - | - | - | - | - | Control | | | | | | | |
| | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 010 | Receive Data Buffer (R/O) | Receive data buffer | | | | | | | | | | | | | | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 010 | Transmit Data Buffer (WO) | Transmit data buffer | | | | | | | | | | | | | | | |
| | | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| 011 | Interrupt Status Reg. (RC) | Interrupt status | | | | | | | | - | - | - | - | - | - | - | - |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | |
| 011 | Interrupt Enable Reg. (R/W) | - | - | - | - | - | - | - | - | Interrupt enable | | | | | | | |
| | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 100 | General I/O Port Data Reg. (R/W) | GIO data | | | | | | | | - | - | - | - | - | - | - | - |
| | | 0 | 0 | 0 | X | X | X | X | X | | | | | | | | |
| 100 | General I/O Port Control Reg. (R/W) | - | - | - | - | - | - | - | - | GIO control | | | | | | | |
| | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 101 | General IP Interrupt Status Reg. (RC) | GIO interrupt status | | | | | | | | - | - | - | - | - | - | - | - |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | |
| 101 | General IP Interrupt Enable Reg. (R/W) | - | - | - | - | - | - | - | - | GIO interrupt enable | | | | | | | |
| | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 110 | Index Address Reg. (R/W) | - | - | - | - | - | - | - | - | Index address | | | | | | | |
| | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 111 | Index Data Register | Index data register | | | | | | | | | | | | | | | |
| | | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |

continued

| Addr A[3:1] | Register Name (note 1) | Content (note 2) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | B 15 | B 14 | B 13 | B 12 | B 11 | B 10 | B 9 | B 8 | B 7 | B 6 | B 5 | B 4 | B 3 | B 2 | B 1 | B 0 |
| Indirect Access Registers: | | | | | | | | | | | | | | | | | |
| 000 | Extend Status Reg. (RO) | Extend status | | | | | | | | - | - | - | - | - | - | - | - |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | |
| 000 | Setting Reg. (R/W) | - | - | - | - | - | - | - | - | Setting register | | | | | | | |
| | | | | | | | | | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 001 | Data Format Register (R/W) | W | - | - | - | Data length | | | | | | | | | | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 010 | Nac Time-out Register (R/W) | Nac time out register | | | | | | | | | | | | | | | |
| | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 011 | Error Status Reg. (RO) | Status | | | | | | | | - | - | - | - | - | - | - | - |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | |
| 100 | Ready & Data Size Register (R/W) | F | - | - | - | - | - | - | 8- | Test | | | | | | | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note 1: R/W means the register can be read and write.

RO means the register is read only.

RC means the register is read only and read clear.

WO means the register is write only.

Note 2: The data bit in the content is the initial value during hardware reset.

0: the bit value is 0.

1: the bit value is 1.

X: the bit value is unknow.

-: Undefined bit in the register and the value will read 0.

# 7. FUCNTIONAL DESCRIPTION

## 7.1 Host Interface

The Host interface type may be type 1 or type. The read cycle always 16-bit access and the write cycle may be 16-bit access or high byte or low byte access.

**Host Interface Type 1:**

The Host interface type 1 is selected when XTYP2 pin is low. Figure 7-1 shows the timing of CPU read and write in type 1. Figure 7-2 is the timing of CPU write high byte and write low byte.

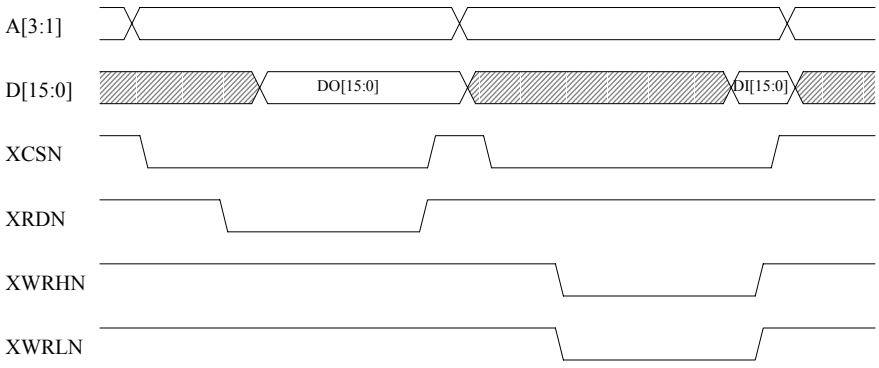



Fig. 7-1 16-bit Read and Write Access in Host I/F Type 1.

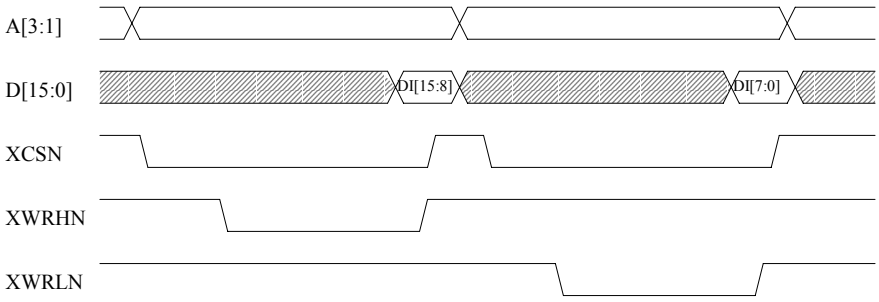



Fig. 7-2 High Byte and Low Byte Write Access in Host I/F Type 1.

**Host Interface Type 2:**

The Host interface type 2 is selected when XTYP2 pin is high. Figure 7-3 shows the timing of CPU read write in type 2 and the access cycle is 3-cycle access, figure 7-4 shows the timing of CPU read write in type 2 and the access cycle is 2-cycle access.

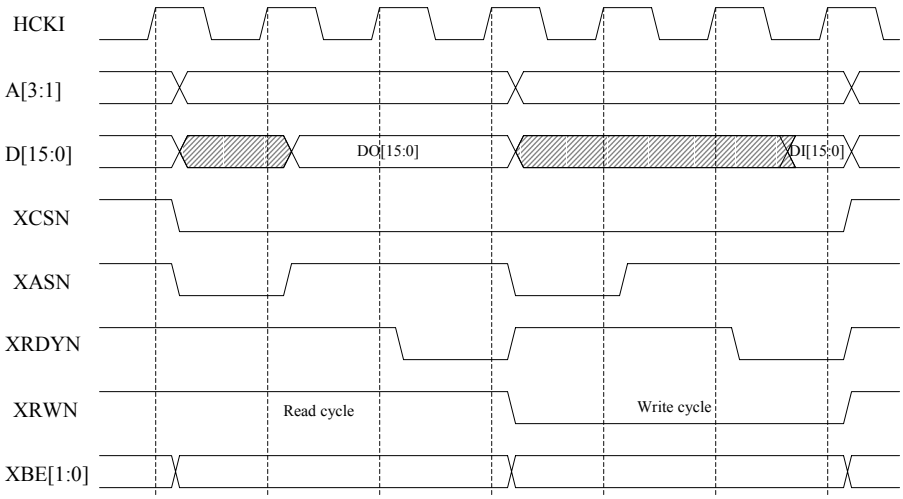



Fig. 7-3 Read and Write Timing in Host I/F Type 2, 3-Cycle Access.

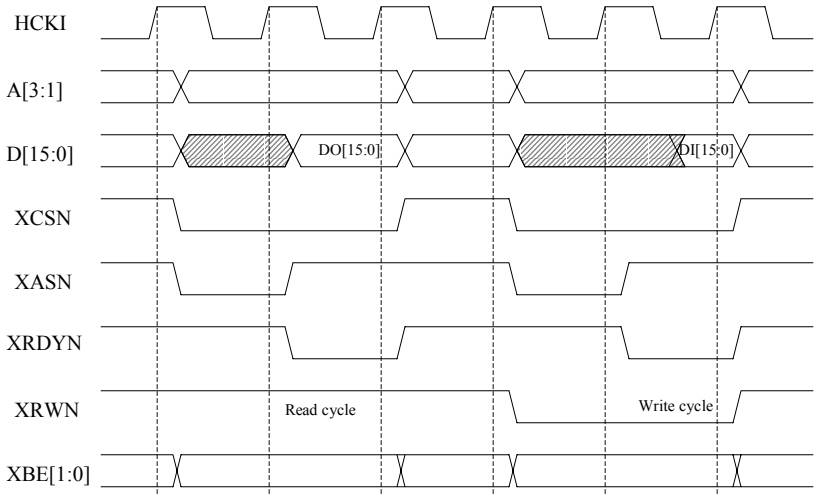



Fig. 7-4 Read and Write Timing in Host I/F Type 2, 2-Cycle Access.

**DMA Access:**

DMA request XDRQN is used to notify the Host that the Host should write data to the transmit data buffer or read data from the receive data buffer in data write to the card or data read from the card.

During data transmit to the card, the XDRQN will active if the data write command has been transfer to the card and the transmit data buffer have not enough data to transmit to the card. The XDRQN will not active if the transmit data buffer have enough data to transmit to the card.

During data receive from the card, the XDRQN will active if the data read command has been transfer to the card and the data have been received in the receive data buffer. The XDRQN will not active if the data read command has been executed completedly and the receive data buffer is read out.

There are two types of DMA acknowledge waveform, the first type is configured if DAKEN = low, XDAKN is ignore and XDRQN will inactive after each access receive or transmit data buffer, the XDRQN will re-active after four clock later. Figure 7-5 shows the waveform of DMA access receive data buffer in DAKEN = low. The second type is configured if DAKEN = high, XDAKN is used to count the transfer count of the data buffer, XDRQN will hold at active state until the data has been transferred completedly. Figure 7-6 is the waveform of DMA access transmit data buffer in DAKN = high.

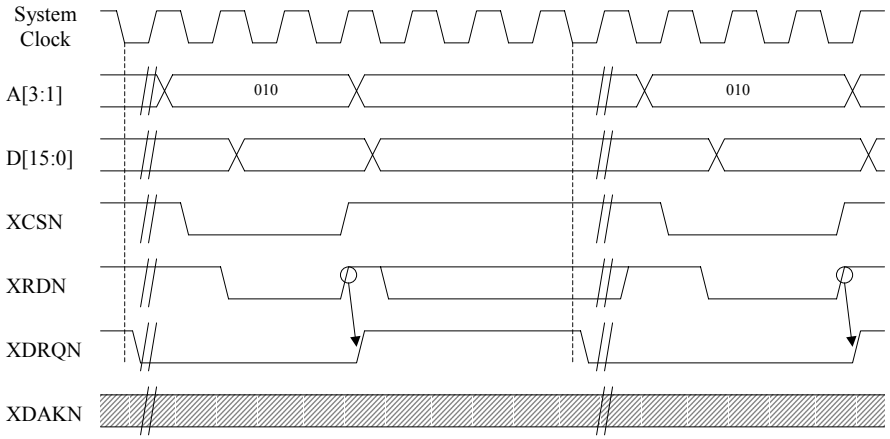



Fig. 7-5 DMA Access Receive Data Buffer (DAKEN = low).

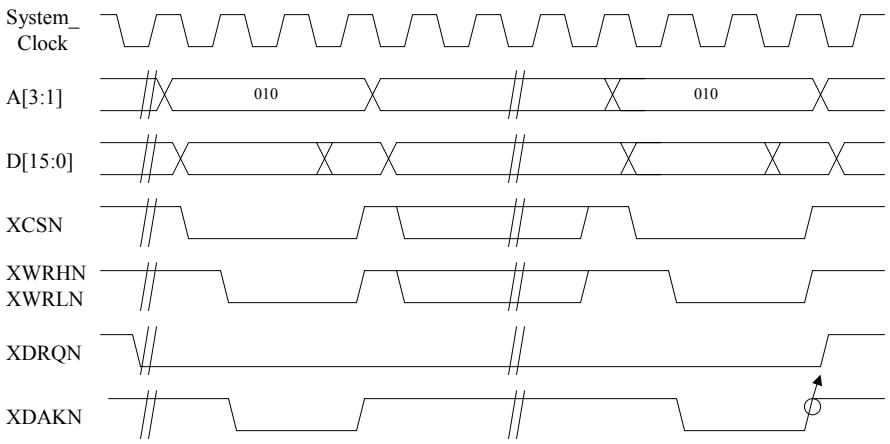



Fig. 7-6 DMA Access Transmit Data Buffer (DAKEN = high).

**Interrupt:**

Interrupt pin XINTN will active (low) at the falling edge of system clock if any bit in the interrupt register is high, the XINTN pin will return to high when read the interrupt register and if the interrupt source is not existed. Figure 7-7 is the timing of interrupt.

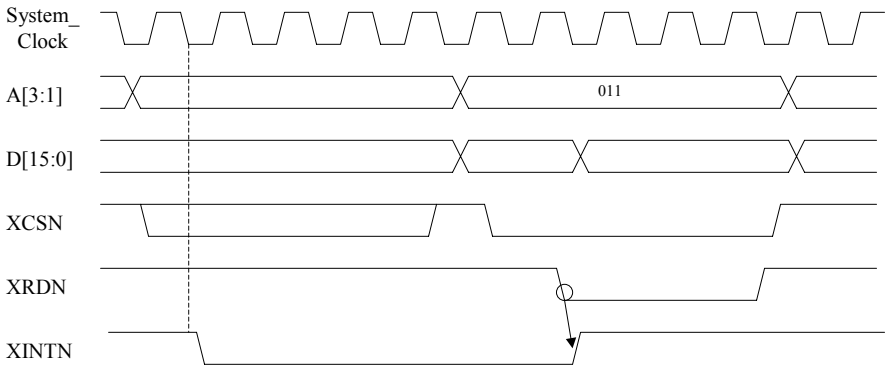



Fig. 7-7 Timing of Interrupt in.

## 7.2 Card Inserting and Removing

There are two method for Host to detect SD/MMC card inserting or removing through W86L388, the first method is detected by CD/DAT3 pin, the second method is a dedicate switch on the SD/MMC slot can be connected to the GIO0 pin and set GIO0 to input direction. These two methods can be performed even if the W86L388 is in power down state.

**Method 1, CD/DAT3 as card detection:**

The CD/DAT3 of SD bus can be used as card detection if no data transfer on the DAT3, if SIEN bit on the control register is low and INS_IE and INT_E on the interrupt enable register are all high, card inserting or removing will generate interrupt. Host must read the interrupt status register and re-check the card state by read the CD bit on the extend status register. This detection method will not effective when wide bus on the SD bus is transfer. MMC card may not support this detection method.

**Method 2, GIO0 as card detection:**

Some SD/MMC slot support external switch for card existing detection, the switch will on when SD or MMC is exist. GIO0 with a pull high resister can be used as card detection, the Host can disable the GOEN0 bit on the general I/O port control register and enable the GIT_EN0 bit on the general I/O port interrupt enable register and enable GIT_IE and INT_E bits on the interrupt enable register. SD or MMC card inserting or removing will change the switch state then change the state of GIO0 pin and then general interrupt to the Host. Host may re-check the card state by read the GIN0 bit on the general I/O port data register.

## 7.3 Reset Action

**Hardware Reset:**

Hardware reset is performed by setting RSTN pin to low state for at least 1 mS. The CPU data size will set to 16-bit default, all the registers will set to default value. The receive and transmit data buffer will be cleared; all the internal logic will be reset to initial state.

**Software Reset:**

Software reset is executed by write the RST bit of the control register to 1, all the internal logic will be reset to initial state and receive and transmit data buffer will be cleared, but the content of registers are not affected.

**Data Buffer Reset:**

Data buffer reset is used to reset the receive data buffer and transmit data buffer simutaneously, the serial interface command will affected if the data receive or transmit command is progressing. Internal logic state and the content of registers are not affected.

### 7.4 Clock Source

The clock source of W86L388 is the waveform of XTO pin, if crystal is connected, the frequency may be from 3.58MHz to 25MHz, if the clock source is from external clock, XTI may be used as clock input and the maximum frequency is 25MHz.

# 8. ELECTRICAL CHARACTERISTICS

## 8.1 Maximum Ratings*

| | Parameter | Symbol | Rating | Units |
|---|---|---|---|---|
| 1 | Supply Voltage with respect to $V_{VSS}$ | $V_{VDD}$ | -0.3 to 6 | V |
| 2 | Current at any pin other than supplies | | 0 to 10 | mA |
| 3 | Storage Temperature | $T_{st}$ | -65 to 150 | ℃ |

* Exceeding these values may cause permanent damage.

## 8.2 Recommended Operating Conditions

| | Characteristics | Symbol | Rating | Unit |
|---|---|---|---|---|
| 1 | Operation Voltage (referenced to VSS pin). | $V_{VDD}$ | 3.0 to 3.6 | V |
| 2 | Operation Voltage (referenced to VSS pin) (Note) | $V_{VDD}$ | 2.7to 3.0 | V |
| 3 | Clock Frequency at XTI pin | $f_{XTL}$ | 25 | MHz |
| 4 | Operation Temperature | $T_{op}$ | 0 to 70 | ℃ |

Note: Clock frequency not guaranteed up to 25MHz.

## 8.3 Power Supply Characteristics

| | Parameter | Condition | Symbol | Min | Typ‡ | Max | Units | Test |
|---|---|---|---|---|---|---|---|---|
| 1 | Standby Supply Current | Power Supply | $I_Q$ | | 2 | 20 | uA | Test 1 |
| 2 | Operating Supply Current | ($V_{VDD}$ = 3.3V) | $I_{VDD}$ | | TBD | TBD | mA | Test 2 |
| 3 | Operating Supply Current | | $I_{VDD}$ | | TBD | | mA | Test 3 |

‡: Typical figure are at $V_{DIVDD}$ = 3.3V and temperature = 25 ℃ and are for design aid only, not guaranteed and not subject to production testing.

Test 1: All input pins are $V_{VDD}$ or $V_{VSS}$, configured as power down mode, output without loading and no clock input on the XTI and HCKI pins.

Test 2: 20 MHz external clock input on the XTI pin, output without loading.

Test 3: 20 MHz crystal connected at XTI and XTO pins, output without loading.

### 8.4. Digital Characteristics

| | Parameter | Condition | Symbol | Min | Typ‡ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| 1 | Output High Voltage | 2mA load | $V_{OH}$ | 0.9 | | | VDD | 1 |
| 2 | Output Low Voltage | 2mA sink | $V_{OL}$ | | | 0.1 | VDD | 1 |
| 3 | Output High Voltage at SD4 output | 3mA load | $V_{OH}$ | 0.9 | | | VDD | |
| 4 | Output Low Voltage at SD4 output | 3mA sink | $V_{OL}$ | | | 0.1 | VDD | |
| 5 | High Level Input Voltage | | $V_{IH}$ | 0.7 | | | VDD | |
| 6 | Low Level Input Voltage | | $V_{IL}$ | | | 0.3 | VDD | |
| 7 | Input Current | | Iin | | | 1 | uA | |
| 8 | Input Capacitance | | Cin | | 10 | | pF | |

‡: Typical figure are at $V_{DVDD}$ = 3.3V and temperature = 25 ℃ and are for design aid only, not guaranteed and not subject to production testing.

Notes:

1: All output pins except SD4 output.

### 8.5. Timing Characteristics

| | Parameter | Symbol | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| **Clock (figure 8-1)** | | | | | | | |
| 1 | XTI | fXTI | 1 | - | 20 | MHz | 1 |
| 2 | XTI high pulse width | $tXTI_{wh}$ | 10 | - | - | nS | 1 |
| 3 | XTI low pulse width | $tXTI_{wl}$ | 10 | - | - | nS | 1 |
| 4 | XTI rise time | $tXTI_{r}$ | - | - | 5 | nS | 1 |
| 5 | XTI fall time | $tXTI_{f}$ | - | - | 5 | nS | 1 |
| 5 | XTO delay time | $tXTO_{d}$ | - | - | 5 | nS | 2 |
| 6 | XTI crystal driver | fXTI | 3.58 | - | 25 | MHz | 3 |
| 7 | HCLK frequency | fHCLK | 1 | - | 40 | MHz | |
| 8 | HCLK high pulse width | $tHCLK_{wh}$ | 10 | - | - | nS | |
| 9 | HCLK low pulse width | $tHCLK_{wl}$ | 10 | - | - | nS | |
| 10 | HCLK rise time | $tHCLK_{l}$ | - | - | 5 | nS | |
| 11 | HCLK fall time | $tHCLK_{f}$ | - | - | 5 | nS | |

8.5. Timing Characteristics , continued

| | Parameter | Symbol | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| **Reset** | | | | | | | |
| 1 | RSTN | tRST | 4 | - | - | cycle | |
| **Host Interface at Type 1 (figure 8-2, 8-3)** | | | | | | | |
| 1 | Access time | $t_{acc}$ | 100 | - | - | nS | 4 |
| 2 | Address setup time | $tA_{su}$ | 10 | - | - | nS | |
| 3 | Address hold time | $tA_{h}$ | 5 | - | - | nS | |
| 4 | D[15:0] output delay time | $tD_{od}$ | - | - | 30 | nS | 5,6 |
| 5 | D[15:0] output hold time | $tD_{oh}$ | 10 | - | - | nS | 5,7 |
| 6 | D[15:0] input setup time | $tD_{su}$ | 10 | - | - | nS | 8 |
| 7 | D[15:0] input hold time | $tD_{h}$ | 5 | - | - | nS | 9 |
| 8 | DMA request delay time | $tDRQ_{d}$ | - | - | 20 | nS | 2 |
| 9 | DMA request hold time | $tDRQ_{h}$ | 5 | - | 20 | nS | 2 |
| **Host Interface at Type 2 (figure 8-5)** | | | | | | | |
| 1 | Input signals setup time | $tIF2_{su}$ | 10 | - | - | nS | 10 |
| 2 | Input signals hold time | $tIF2_{h}$ | 5 | - | - | nS | 10 |
| 3 | Address setup time | $tA2_{su}$ | 10 | - | - | nS | |
| 4 | Address hold time | $tA2_{h}$ | 5 | - | - | nS | |
| 5 | XRDYN delay time | $tRDY_{d}$ | - | - | 20 | nS | 2 |
| 6 | XRDYN hold time | $tRDY_{h}$ | 5 | - | - | nS | 2 |
| 7 | D[15:0] output delay time | $tD_{od}$ | - | - | 30 | nS | 5 |
| 8 | D[15:0] output hold time | $tD_{oh}$ | 10 | - | - | nS | 5 |
| 9 | D[15:0] input setup time | $tD_{su}$ | 10 | - | - | nS | |
| 10 | D[15:0] input hold time | $tD_{h}$ | 5 | - | - | nS | |
| **Interrupt (figure 8-4)** | | | | | | | |
| 1 | Interrupt delay time | $tINT_{d}$ | - | - | 20 | nS | |
| 2 | Interrupt hold time | $TINT_{h}$ | 5 | - | 20 | nS | |

8.5. Timing Characteristics , continued

| | Parameter | Symbol | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| **Serial Interface Signals (figure 8-6, 8-7, 8-8, 8-9)** | | | | | | | |
| 1 | SD3 output delay | $tSD3_d$ | 5 | - | 15 | nS | 2 |
| 3 | SD3 input setup time | $tSD3D_{su}$ | 10 | - | - | nS | |
| 4 | SD3 input hold time | $tSD3_h$ | 5 | - | - | nS | |
| 2 | SD1,SD2,SD5,SD6 output delay time | $tSDn_d^*$ | - | - | 30 | nS | 2 |
| 3 | SD1,SD2,SD5,SD6 input setup time | $tSDn_{su}$ | 10 | - | - | nS | |
| 4 | SD1,SD2,SD5,SD6 input hold time | $tSDn_h$ | 5 | - | - | nS | |

Note 1: External clock input.

Note 2: 20 pF output loading.

Note 3: Crystal driver.

Note 4: Minimum active pulse width of (XCSN and XRDN) or (XCSN and XWRHN and XWRLN).

Note 5: 40 pF output loading.

Note 6: From the last active signal of XCSN or XRDN.

Note 7: From the first in-active signal of XCSN or XRDN.

Note 8: To the first in-active signal of XCSN, XWRHN or XWRLN, XWRHN or XWRLN related to the D[15:8] or D[7:0].

Note 9: From the first in-active signal of XCSN, XWRHN or XWRLN, XWRHN or XWRLN related to the D[15:8] or D[7:0].

Note 10: XCSN, XASN, XRWN and XBE[1:0] signals.

Note 11: SDn: SD1, SD2, SD5, SD6

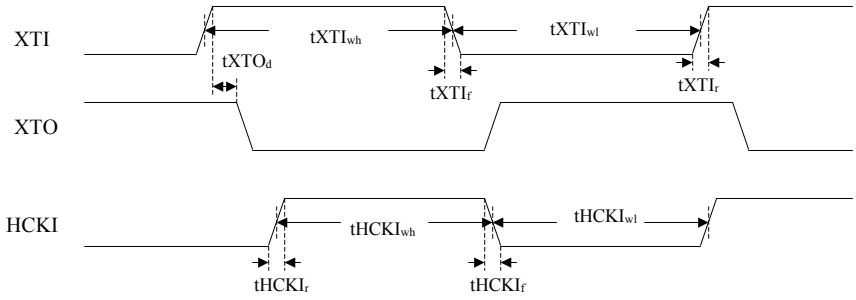



Fig. 8-1 Timing Characteristic of XTI, XTO and HCKI.

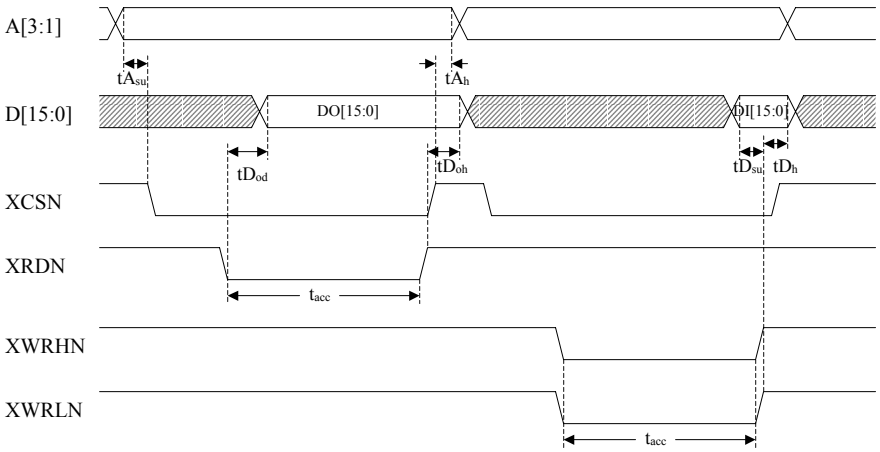



Fig. 8-2 Host Access Timing Characteristic in Host I/F Type 1.

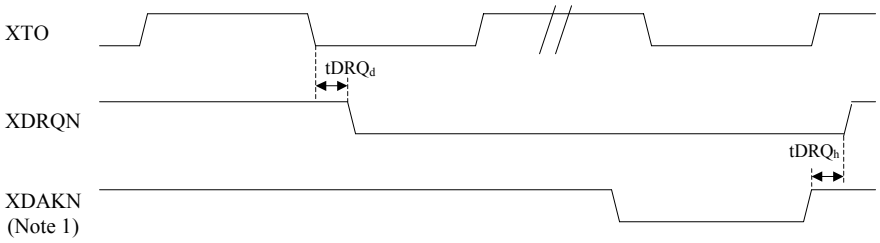



Fig. 8-3 DMA Timing Characteristic.

Note 1: May be XRDN or XWRHN or XWRLN signals when XDAKEN = low.

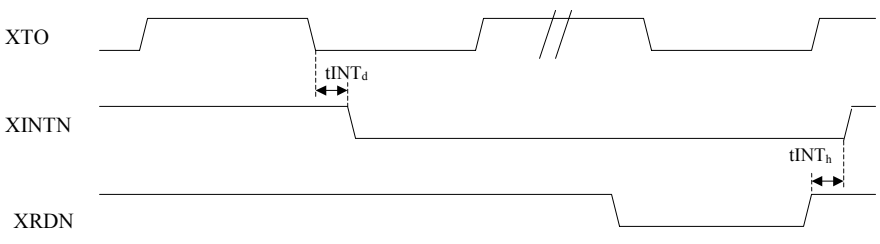



Fig. 8-4 Interrupt Timing Characteristic.

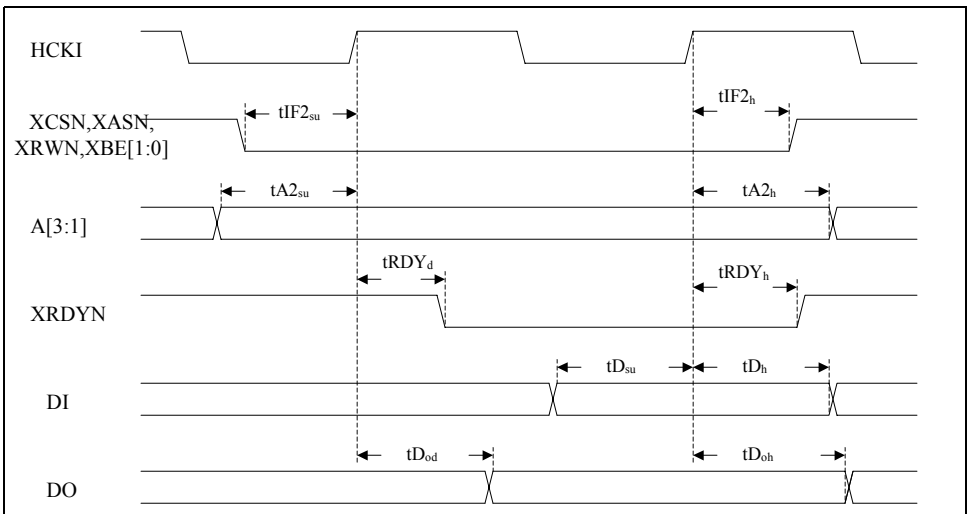



Fig. 8-5 Host Interface Type 2 Timing Characteristic.

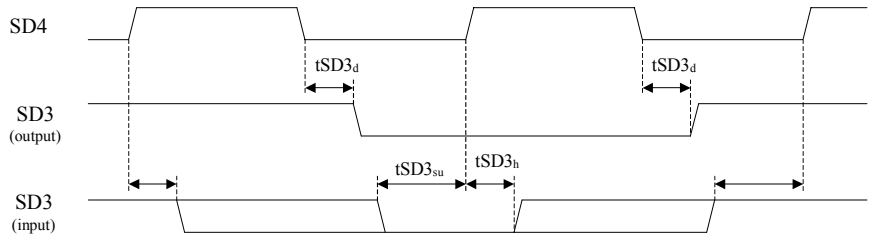



Fig. 8-6 Serial Interface SD3 Timing Characteristic (SD Mode).

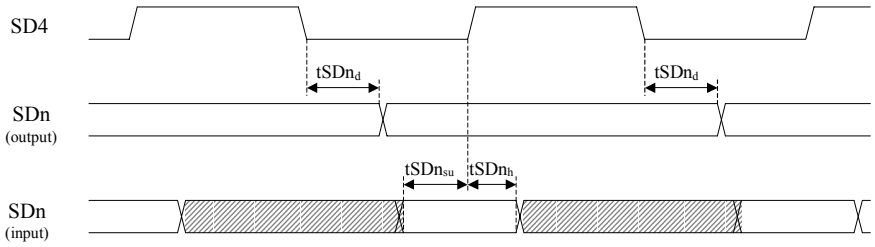



Fig. 8-7 Serial Interface SDn Timing Characteristic (SD Mode).

SDn: SD1, SD2, SD5, SD6

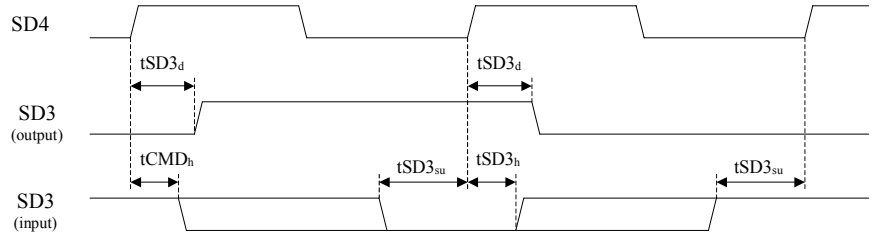



Fig. 8-8 Serial Interface SD3 Timing Characteristic (MMC Mode).

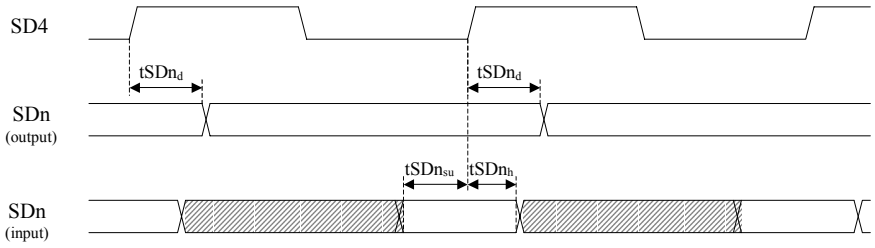
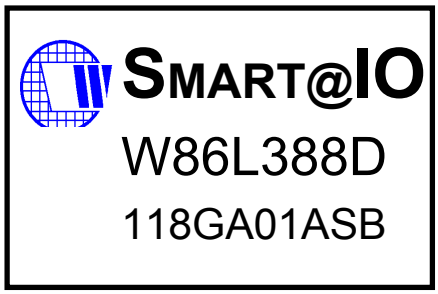



Fig. 8-9 Serial Interface SDn Timing Characteristic (MMC Mode).

SDn: SD1, SD2, SD5, SD6

## 9. HOW TO READ THE TOP MARKING

The top marking of W86L388D




1st line: Winbond logo and SMART@IO Mark

2nd line: Part number of W86L388D

3rd line: Tracking code 118 G A 01A SB

**118**: packages made in '01, week 18

**G**: assembly house ID; A means ASE, O means OSE, G means GR

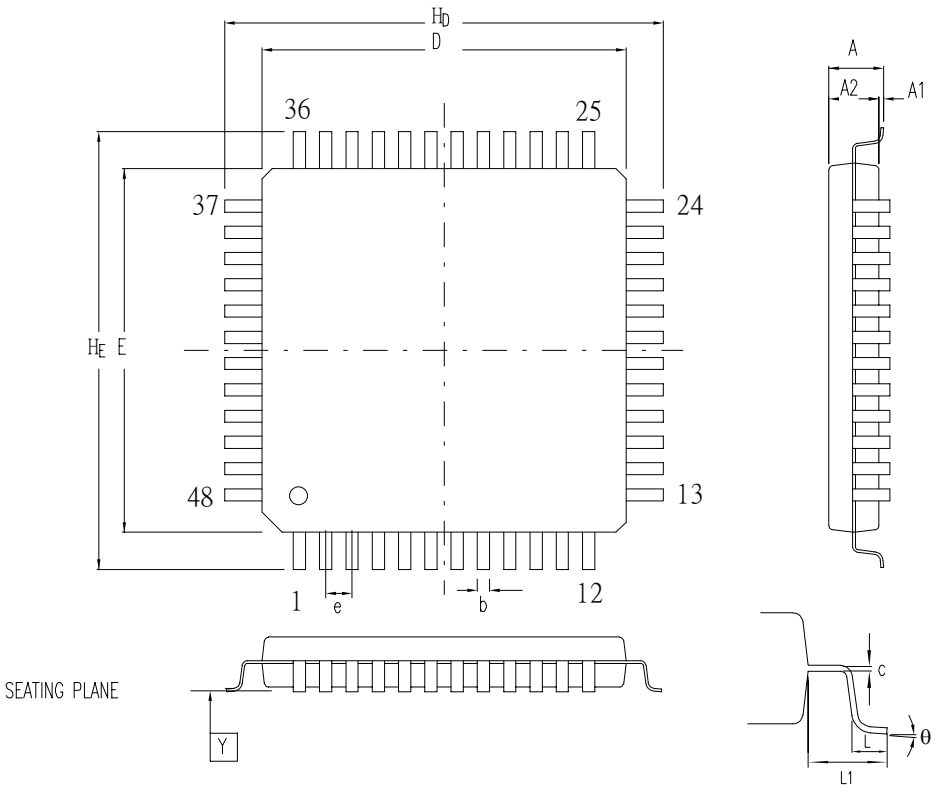
**A**: IC revision; A means version A, B means version B

**01A**: for internal use

**SB**: for internal use

## 10.PACKAGE DIMENSIONS

### 48-LQFP(7x7x1.4mm footprint 2.0mm)

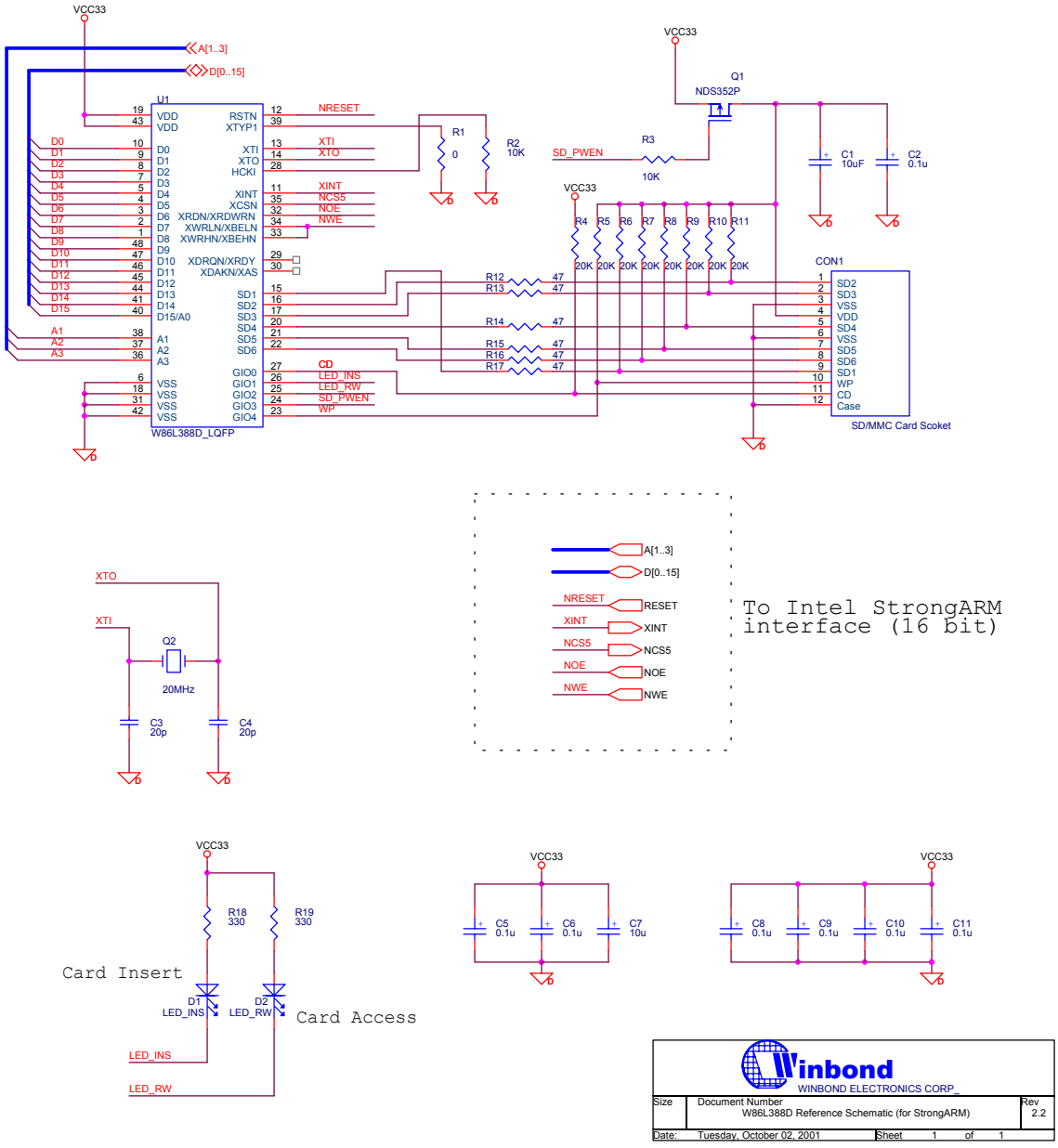



Controlling dimension : Millimeters

| Symbol | Dimension in inch | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | — | — | — | — | — | — |
| $A_1$ | 0.002 | 0.004 | 0.006 | 0.05 | 0.10 | 0.15 |
| $A_2$ | 0.053 | 0.055 | 0.057 | 1.35 | 1.40 | 1.45 |
| b | 0.006 | 0.008 | 0.010 | 0.15 | 0.20 | 0.25 |
| c | 0.004 | 0.006 | 0.008 | 0.10 | 0.15 | 0.20 |
| D | 0.272 | 0.276 | 0.280 | 6.90 | 7.00 | 7.10 |
| E | 0.272 | 0.276 | 0.280 | 6.90 | 7.00 | 7.10 |
| e | 0.014 | 0.020 | 0.026 | 0.35 | 0.50 | 0.65 |
| $H_D$ | 0.350 | 0.354 | 0.358 | 8.90 | 9.00 | 9.10 |
| $H_E$ | 0.350 | 0.354 | 0.358 | 8.90 | 9.00 | 9.10 |
| L | 0.018 | 0.024 | 0.030 | 0.45 | 0.60 | 0.75 |
| $L_1$ | — | 0.039 | — | — | 1.00 | — |
| Y | — | — | 0.004 | — | — | 0.10 |
| θ | 0° | — | 7 ° | 0° | — | 7 ° |

## 11. REFERENCE SCHEMATIC

W86L388D Reference Circuit



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Preliminary

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