MK2704
PLL Audio Clock Synthesizer

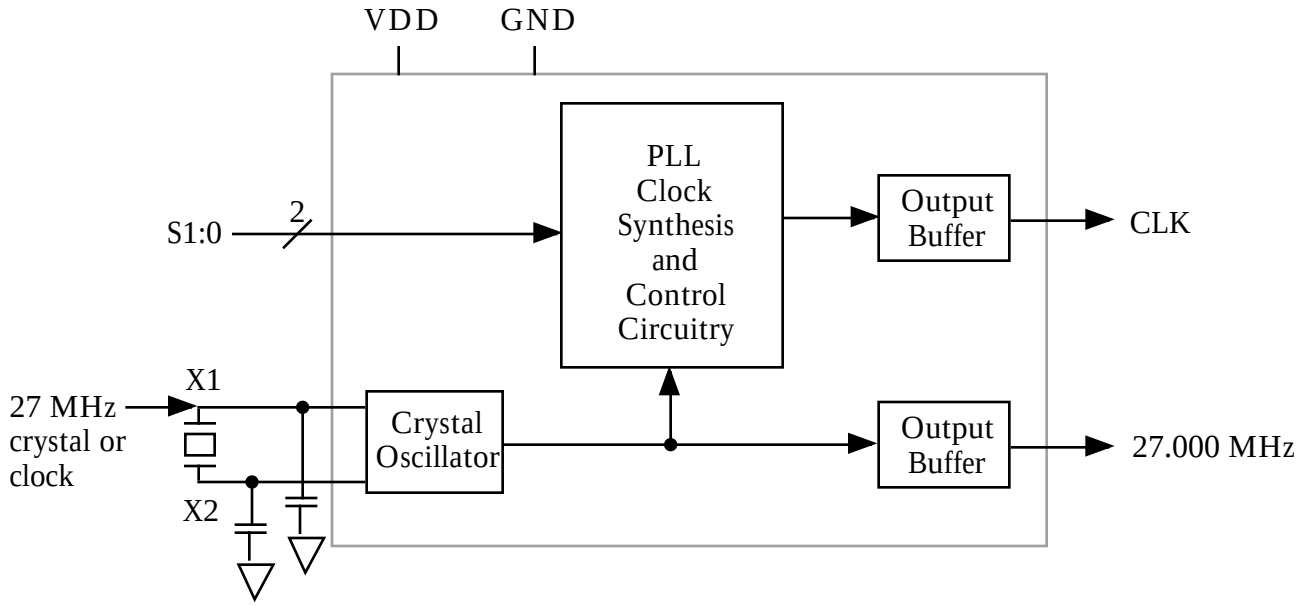
Description

The MK2704 is a low cost, low jitter, high performance PLL clock synthesizer designed to replace oscillators and PLL circuits in set-top box and multimedia systems. Using our patented analog Phase-Locked Loop (PLL) techniques, the device uses a fundamental 27 MHz crystal or clock input to produce a buffered reference clock and a selectable audio clock. The audio clock is frequency locked to the 27 MHz clock, assuring that the audio with zero ppm error and video will always track perfectly.

Features

- Packaged in 8 pin SOIC
- Uses an inexpensive fundamental crystal, or clock
- Output clocks of 16.9344 MHz, 18.432 MHz, and 36.864 MHz
- Supports 384x MPEG sampling rates of 44.1 kHz, 48 kHz and 96 kHz
- Patented zero ppm synthesis error in all clocks
- All frequencies are frequency locked
- Advanced, low power, sub-micron CMOS process
- 3.3 V or 5 V operating voltage

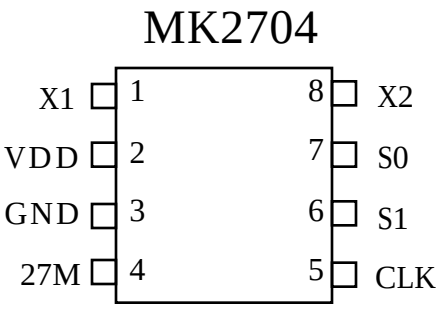
Block Diagram



(Capacitors are required for crystal tuning)

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Pin Assignment



8 pin SOIC

Audio Clock Output Select Table (MHz)

S1	S0	CLK
0	0	36.864
0	1	Test
1	0	16.9344
1	1	18.432

Key: 0 = connect pin directly to ground
1 = connect pin directly to VDD

Pin Descriptions

Number	Name	Type	Description
1	X1	XI	Crystal Connection. Connect to a 27.0 MHz fundamental crystal or clock.
2	VDD	P	Connect to +3.3V or +5V.
3	GND	P	Connect to ground.
4	27M	O	27.00 MHz buffered reference clock output.
5	CLK	O	Audio Clock Output per table above.
6	S1	I(PU)	Audio Clock Frequency Select Input #1. Determines CLK output per table above.
7	S0	I(PU)	Audio Clock Frequency Select Input #0. Determines CLK output per table above.
8	X2	XO	Crystal Connection to a 27.0 MHz crystal, or leave unconnected for clock input.

Key: XI, XO = Crystal connections; I(PU) = Input with internal pull-up resistor; O = output;
P = power supply connection

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Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature	MK2704S	0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3V unless noted)					
Operating Voltage, VDD		3.13		5.50	V
Input High Voltage, VIH, X1 pin only	Note 2	(VDD/2)+1			V
Input Low Voltage, VIL, X1 pin only	Note 2			(VDD/2)-1	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Output High Voltage, VOH	IOH=-12mA	2.4			V
Output Low Voltage, VOL	IOL=12mA			0.4	V
Output High Voltage, VOH, CMOS level	IOH=-4mA	VDD-0.4			V
Operating Supply Current, IDD	No Load		10		mA
Short Circuit Current	Each output		±50		mA
Input Capacitance	S1, S0		5		pF
Frequency synthesis error	All clocks			0	ppm
AC CHARACTERISTICS (VDD = 3.3V unless noted)					
Input Crystal Frequency			27.00		MHz
Input Crystal Accuracy				±30	ppm
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	At 1.4V	40		60	%
Maximum Absolute Jitter, short term			±190		ps

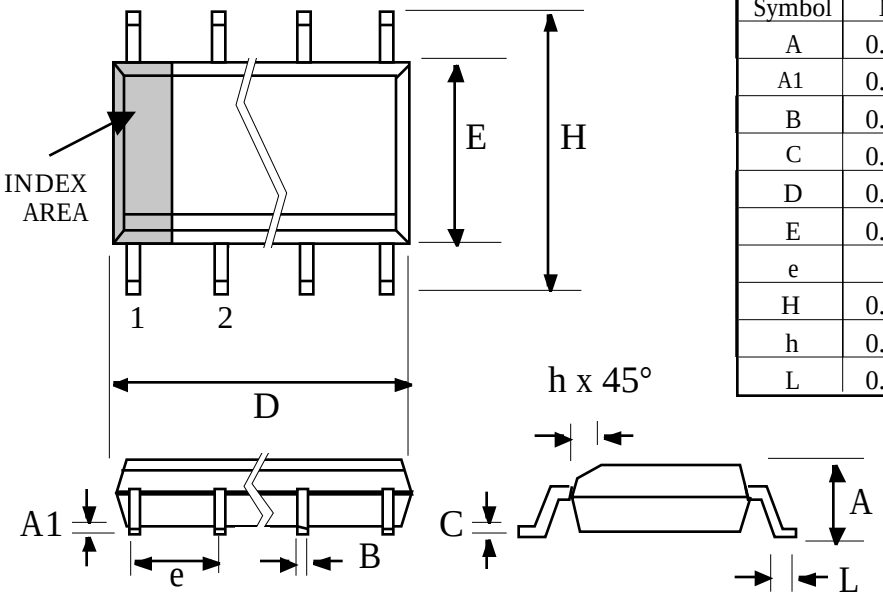
Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. CMOS level input. Nominal trip point is VDD/2 for 3.3 V or 5 V operation.

External Components

The MK2704 requires a minimum number of external components for proper operation. For a crystal input, one load capacitor should be connected from each of the X1 and X2 pins to ground. The value (in pF) of each crystal load capacitor should equal $(C_L-16)\cdot 2$, where C_L is the crystal's load (correlation) capacitance in pF. The input crystal must be connected as close to the chip as possible. The input crystal should be a parallel resonant, fundamental, AT cut 27 MHz. For a clock input, connect to X1 and leave X2 unconnected. Decoupling capacitors of 0.01µF should be connected between VDD and GND on pins 2 and 3, as close to the MK2704 as possible. A series termination resistor of 33 Ω may be used for the clock output.

Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)



8 pin SOIC

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.24
B	0.0130	0.0200	0.33	0.51
C	0.0075	0.0098	0.19	0.24
D	0.1890	0.1968	4.80	5.00
E	0.1497	0.1574	3.80	4.00
e	.050 BSC		1.27 BSC	
H	0.2284	0.2440	5.80	6.20
h	0.0099	0.0195	0.25	0.50
L	0.0160	0.0500	0.41	1.27

Ordering Information

Part/Order Number	Marking	Shipping packaging	Package	Temperature
MK2704S	MK2704S	tubes	8 pin SOIC	0 to 70 °C
MK2704STR	MK2704S	tape and reel	8 pin SOIC	0 to 70 °C

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