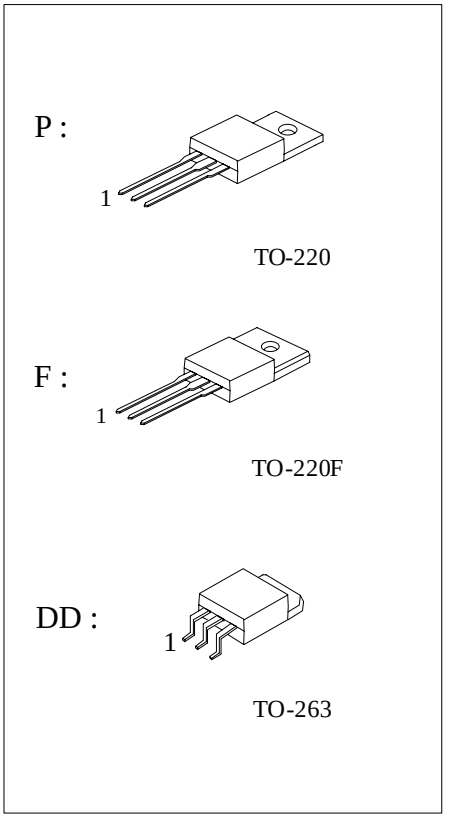
# 8.0 Amps, 650 Volts
# N-CHANNEL MOSFET




## ■ DESCRIPTION

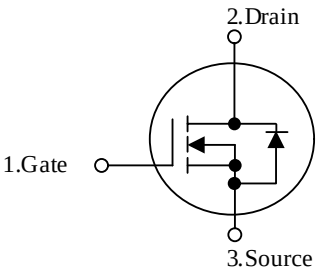
**These N-Channel enhancement mode power field effect Transistors are produced using planar stripe, DMOS technology.**

**This advanced technology has been especially tailored to minimize on - state resistance , provide superior switching performance,and Withstand high energy pulse in the avalanche and commutaion mode .These devices are well suited for high efficiency switch mode power supply，electronic lamp ballasts based on half bridge topology.**

## ■ FEATURES

* $R_{DS(ON)}$ = 1.4Ω@$V_{GS}$ = 10V
* Low gate and reverse transfer Capacitance ( C: 12 pF typical )
* Fast switching capability
* Avalanche energy tested
* Improved dv/dt capability, high ruggedness

## ■ SYMBOL




## ■ ORDERING INFORMATION

| Order Number | Package | Pin Assignment | | | Packing |
|---|---|---|---|---|---|
| | | 1 | 2 | 3 | |
| FTK8N65P | TO-220 | G | D | S | Tube |
| FTK8N65F | TO-220F | G | D | S | Tube |
| FTK8N65DD | TO-263 | G | D | S | Reel & Taping |

Note: Pin Assignment: G: Gate D: Drain S: Source

## ■ ABSOLUTE MAXIMUM RATINGS ($T_C$ = 25˚C, unless otherwise specified)

| PARAMET | | SYMBOL | RATINGS | UNIT |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DSS}$ | 650 | V |
| Gate-Source Voltage | | $V_{GSS}$ | ±30 | V |
| Avalanche Current (Note 1) | | $I_{AR}$ | 7.5 | A |
| Continuous Drain Current | $T_C$ = 25°C | $I_D$ | 7.5 | A |
| | $T_C$ = 100°C | | 4.2 | |
| Pulsed Drain Current (Note 1) | | $I_{DM}$ | 28 | A |
| Avalanche Energy | Single Pulse(Note 2) | $E_{AS}$ | 230 | mJ |
| | Repetitive Limited by $T_{J(MAX)}$ | $E_{AR}$ | 14.7 | mJ |
| Peak Diode Recovery dv/dt (Note 3) | | dv/dt | 4.5 | V/ns |
| Power Dissipation (TO-220,TO-263/ TO-220F) | $T_C$ = 25°C | $P_D$ | 142 / 48 | W |
| | Derate above 25°C | | 1.14 / 0.38 | W / ˚C |
| Junction Temperature | | $T_J$ | +150 | ˚C |
| Operating and Storage Temperature | | $T_{STG}$ | -55 ~ +150 | ˚C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ THERMAL DATA

| PARAMETER | | SYMBOL | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Junction-to-Ambient | | $\theta_{JA}$ | | | 62.5 | ˚C / W |
| Junction-to-Case | TO-220, TO-263 | $\theta_{Jc}$ | | | 0.88 | |
| | TO-220F | $\theta_{Jc}$ | | | 2.6 | |

## ■ ELECTRICAL CHARACTERISTICS ($T_C$ = 25˚C , unless Otherwise specified.)

| PARAMETER | | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain-Source Breakdown Voltage | | $BV_{DSS}$ | $V_{GS}$ = 0V, $I_D$ = 250μA | 650 | | | V |
| Drain-Source Leakage Current | | $I_{DSS}$ | $V_{DS}$ = 650V, $V_{GS}$ = 0V | | | 10 | μA |
| Gate-Body Leakage Current | Forward | $I_{GSSF}$ | $V_{GS}$ = 30V, $V_{DS}$ = 0V | | | 100 | nA |
| | Reverse | $I_{GSSR}$ | $V_{GS}$ = -30V, $V_{DS}$ = 0V | | | -100 | nA |
| Breakdown Voltage Temperature Coefficient | | $\Delta BV_{DSS}$ / $\Delta T_J$ | $I_D$ = 250μA, Referenced to 25°C | | 0.7 | | V / ˚C |
| **ON CHARACTERISTICS** | | | | | | | |
| Gate Threshold Voltage | | $V_{GS(TH)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA | 2.0 | | 4.0 | V |
| Static Drain-Source On-Resistance | | $R_{DS(ON)}$ | $V_{GS}$ = 10V, $I_D$ = 3.75A | | | 1.4 | Ω |
| Forward Transconductance | | $g_{FS}$ | $V_{DS}$ = 40V, $I_D$ = 3.5A (Note 4) | | 8.7 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Input Capacitance | | $C_{ISS}$ | $V_{DS}$ = 25V, $V_{GS}$ = 0V, f = 1.0MHz | | 965 | | pF |
| Output Capacitance | | $C_{OSS}$ | | | 105 | | pF |
| Reverse Transfer Capacitance | | $C_{RSS}$ | | | 12 | | pF |
| **SWITCHING CHARACTERISTICS** | | | | | | | |
| Turn-On Delay Time | | $t_{D(ON)}$ | $V_{DD}$ = 300V, $I_D$ = 7A, $R_G$ = 25Ω (Note 4,5) | | 16 | | ns |
| Turn-On Rise Time | | $t_R$ | | | 60 | | ns |
| Turn-Off Delay Time | | $t_{D(OFF)}$ | | | 81 | | ns |
| Turn-Off Fall Time | | $t_F$ | | | 65 | | ns |
| Total Gate Charge | | $Q_G$ | $V_{DS}$ = 480V,$I_D$ = 7A, $V_{GS}$ = 10V (Note 4,5) | | 28 | | nC |
| Gate-Source Charge | | $Q_{GS}$ | | | 5 | | nC |
| Gate-Drain Charge | | $Q_{GD}$ | | | 12 | | nC |

## ■ ELECTRICAL CHARACTERISTICS ($T_J$ = 25˚C , unless Otherwise specified.)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | |
| Drain-Source Diode Forward Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = 7.0 A | | | 1.5 | V |
| Maximum Continuous Drain-Source Diode Forward Current | $I_S$ | | | | 7.5 | A |
| Maximum Pulsed Drain-Source Diode Forward Current | $I_{SM}$ | | | | 28 | A |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, $I_S$ = 7.0A, | | 400 | | ns |
| Reverse Recovery Charge | $Q_{RR}$ | $d_{IF}/dt$ =100 A/$\mu$s (Note 4) | | 4.0 | | $\mu$C |

Note:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 19.5mH, $I_{AS}$ = 7.5A, $V_{DD}$ = 50V, $R_G$ = 25 Ω, Starting $T_J$ = 25°C
3. $I_{SD} \leq$ 7.5A, di/dt ≤ 300A/$\mu$s, $V_{DD} \leq BV_{DSS}$, Starting $T_J$ = 25°C
4. Pulse Test: Pulse width ≤ 300$\mu$s, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

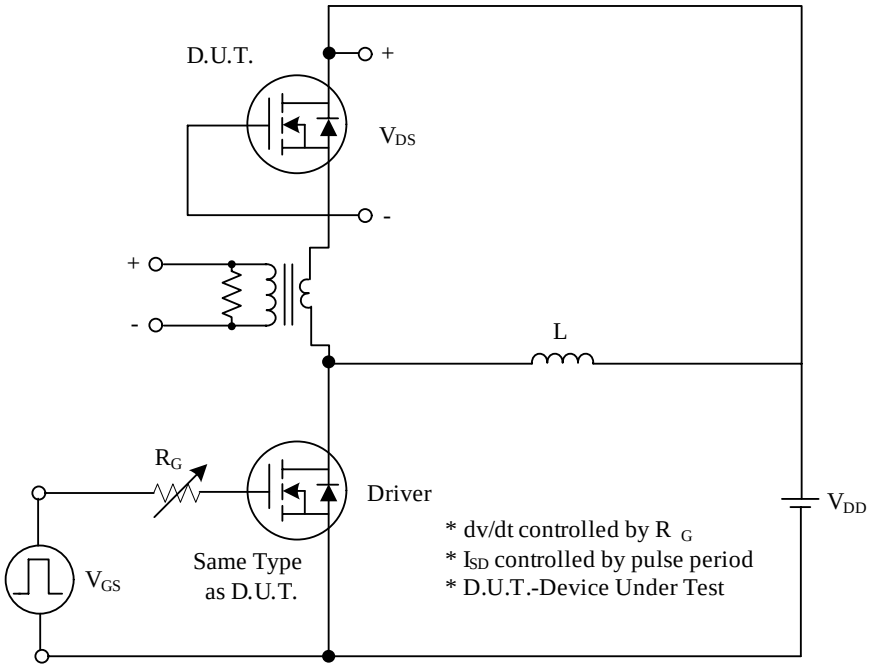



Fig. 1A Peak Diode Recovery dv/dt Test Circuit

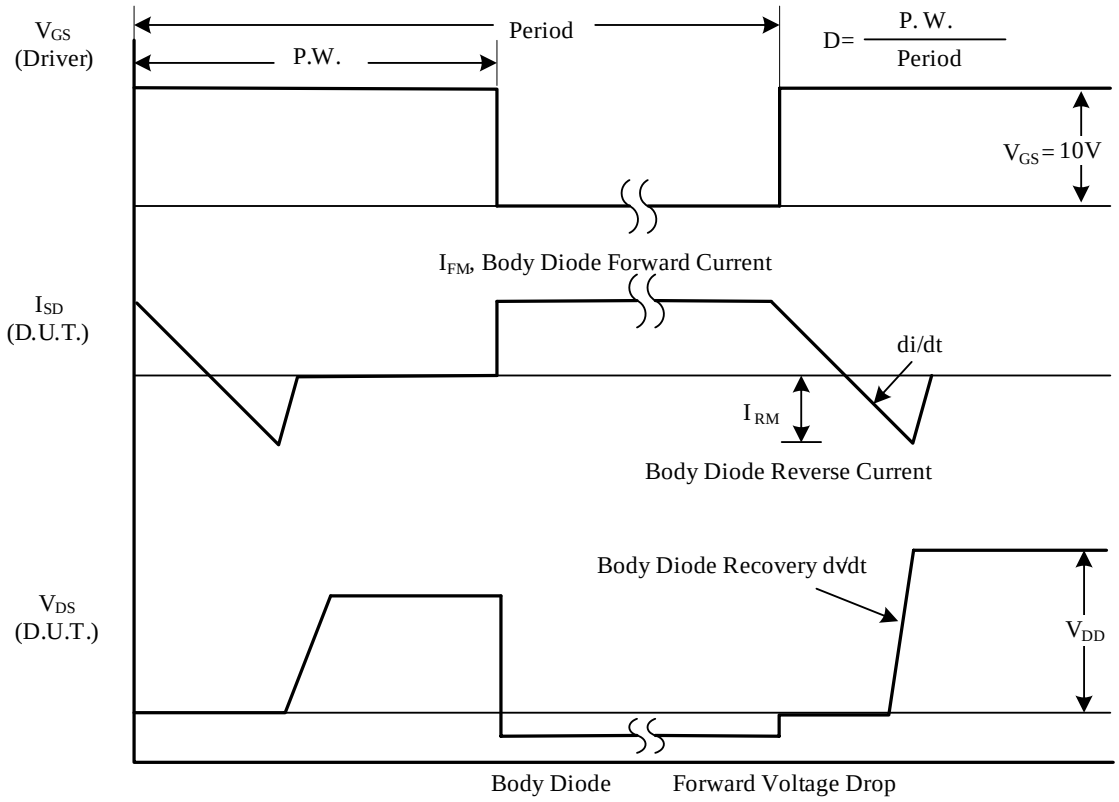



Fig. 1B Peak Diode Recovery dv/dt Waveforms

## ■ TEST CIRCUITS AND WAVEFORMS (Cont.)

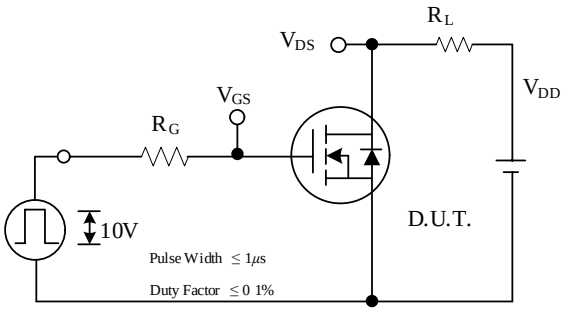



Fig. 2A Switching Test Circuit

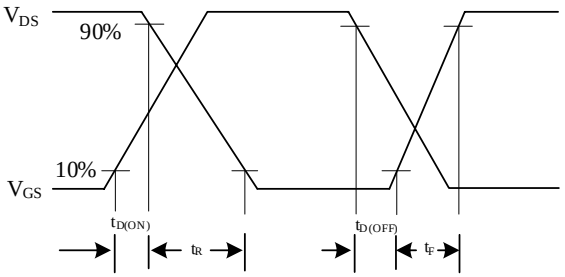



Fig. 2B Switching Waveforms

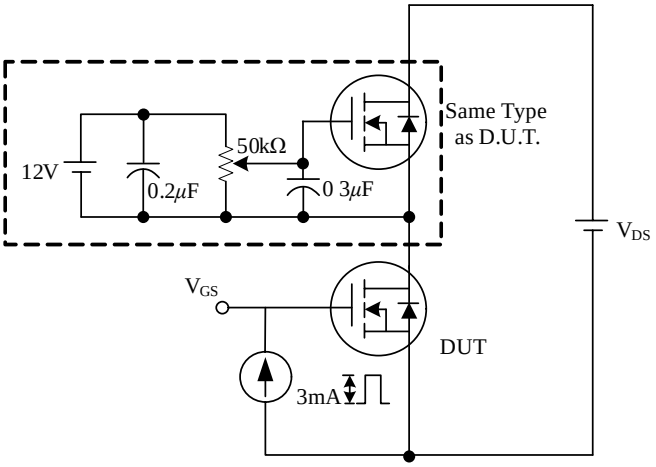



Fig. 3A Gate Charge Test Circuit

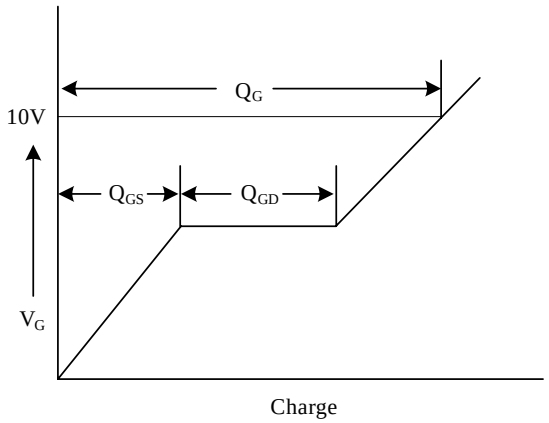



Fig. 3B Gate Charge Waveform

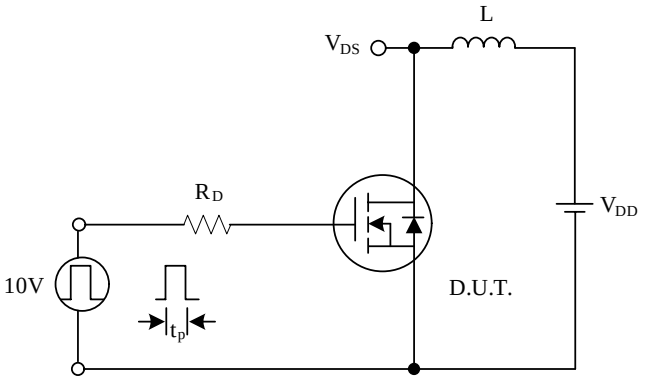



Fig. 4A Unclamped Inductive Switching Test Circuit

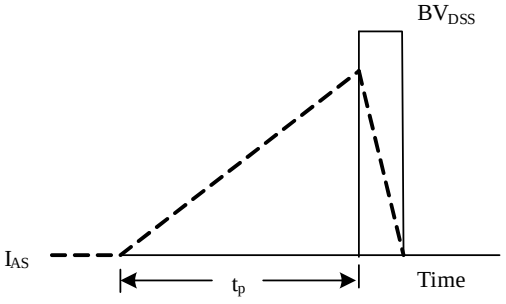



Fig. 4B Unclamped Inductive Switching Waveforms

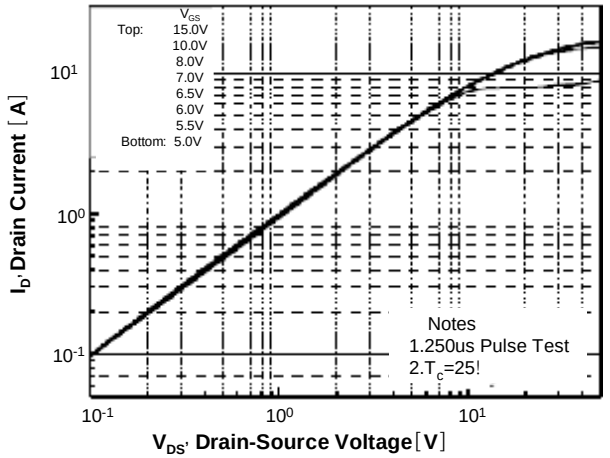



Figure 1.On-Region Characteristics

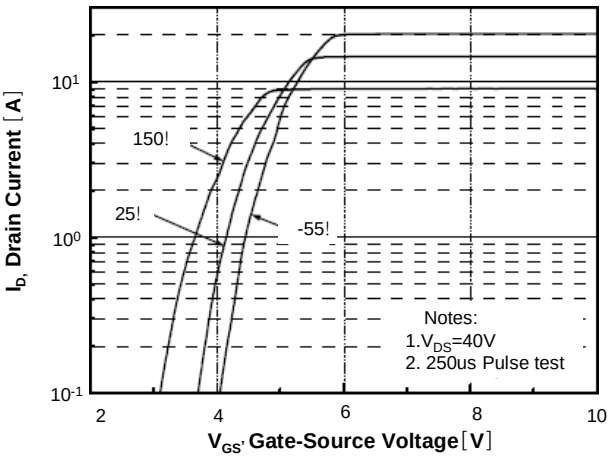



Figure 2.Transfet Characteristics

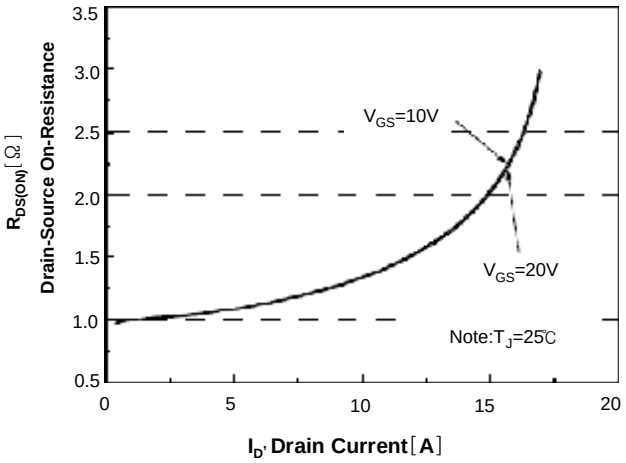



Figure 3.On-Resistance Variation vs Drain Current and Gate Voltage

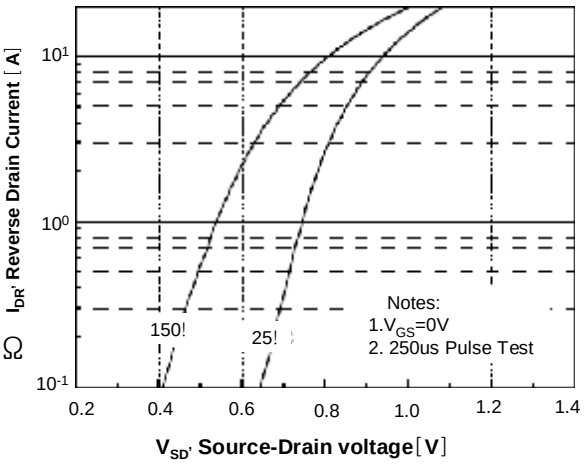



Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

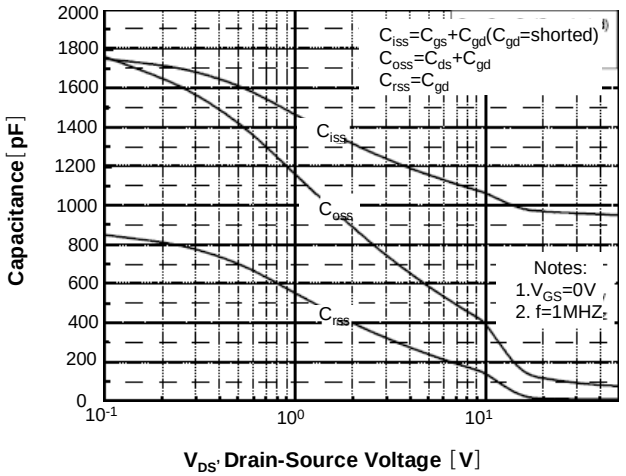



Figure 5.Capacitance Characteristics

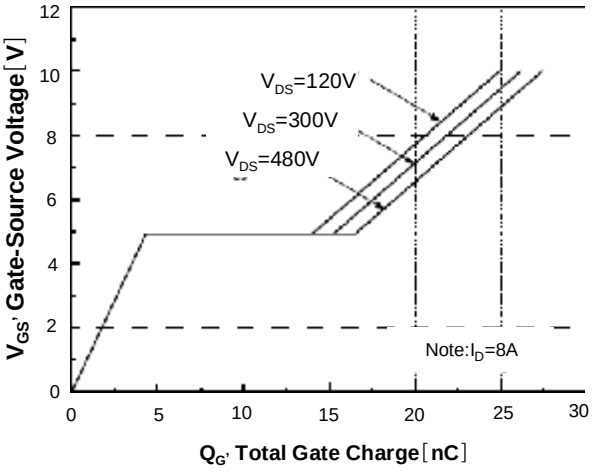



Figure 6. Gate Charge Characteristics

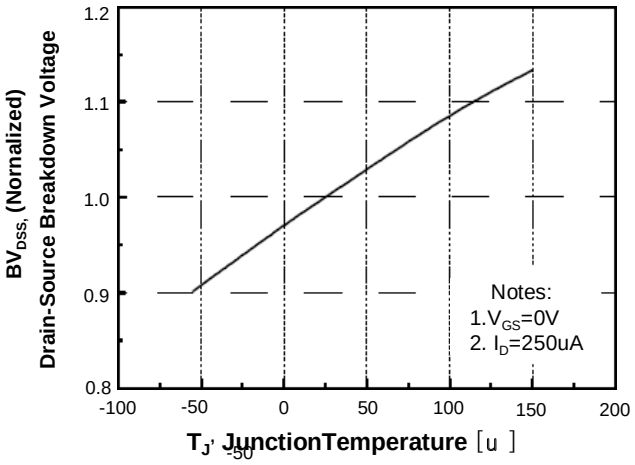



**Figure 7. Breakdown Voltage Variation vs Temperature**

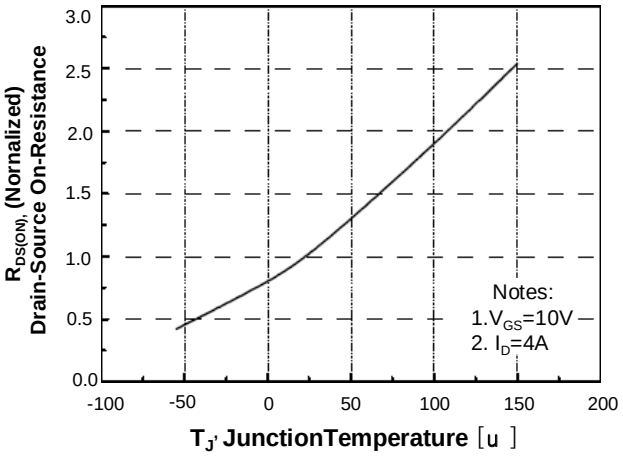



**Figure 8. On-Resistance Variation vs Temperature**

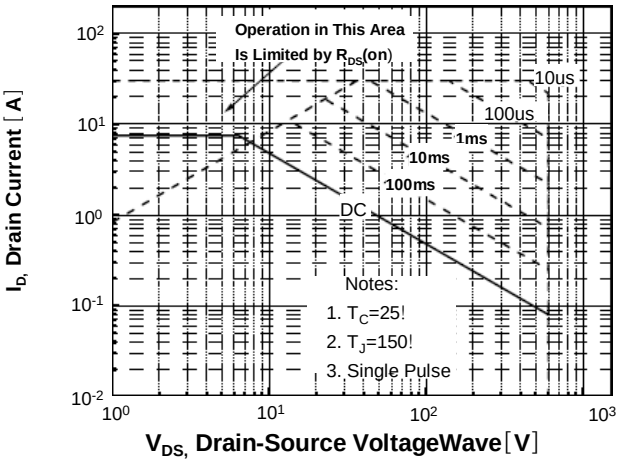



**Figure 9. Maximum Safe Operating Area**

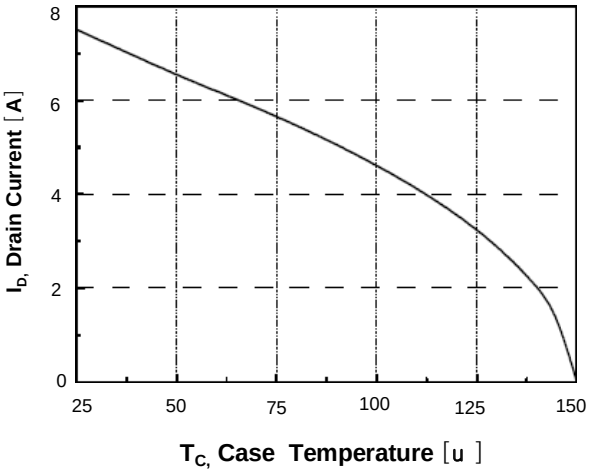



**Figure 10. Maximum Drain Current vs. Case Temperature**

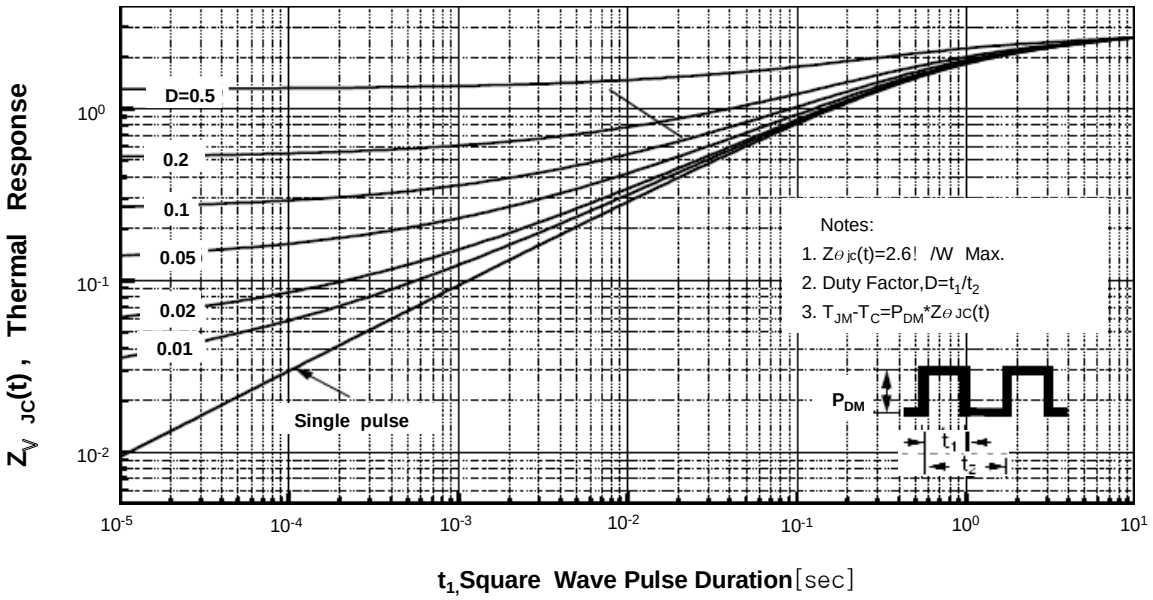



**Figure 11. Transient Thermal Response Curve**