NCP5006

Compact Backlight LED Boost Driver

The NCP5006 is a high efficiency boost converter operating in current loop, based on a PFM mode, to drive White LED. The current mode regulation allows a uniform brightness of the LEDs. The chip has been optimized for small ceramic capacitors, capable to supply up to 1.0 W output power.

Features

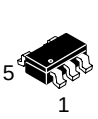
- 2.7 to 5.5 V Input Voltage Range
- V_{out} to 24 V Output Compliance Allows up to 5 LEDs Drive in Series
- Built−in Overvoltage Protection
- Inductor Based Converter brings up to 90% Efficiency
- Constant Output Current Regulation
- 0.3 μA Standby Quiescent Current
- Includes Dimming Function (PWM)
- Enable Function Driven Directly from Low Battery Voltage Source
- Automatic LEDs Current Matching
- Thermal Shutdown Protection
- All Pins are Fully ESD Protected
- Low EMI Radiation
- Pb−Free Package is Available

Typical Applications

- LED Display Back Light Control
- Keyboard Back Light
- High Efficiency Step Up Converter

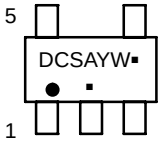
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TSOP−5
SN SUFFIX
CASE 483

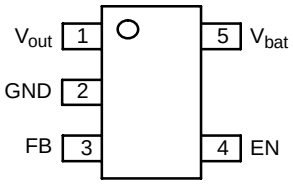
MARKING DIAGRAM



DCS = Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP5006SNT1	TSOP−5	3000 Tape & Reel
NCP5006SNT1G	TSOP−5 (Pb−Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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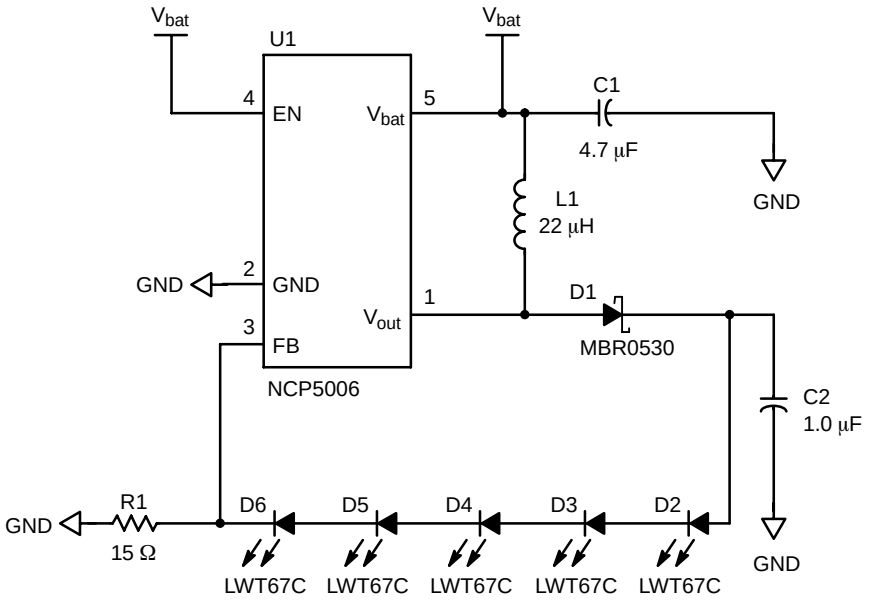


Figure 1. Typical Application

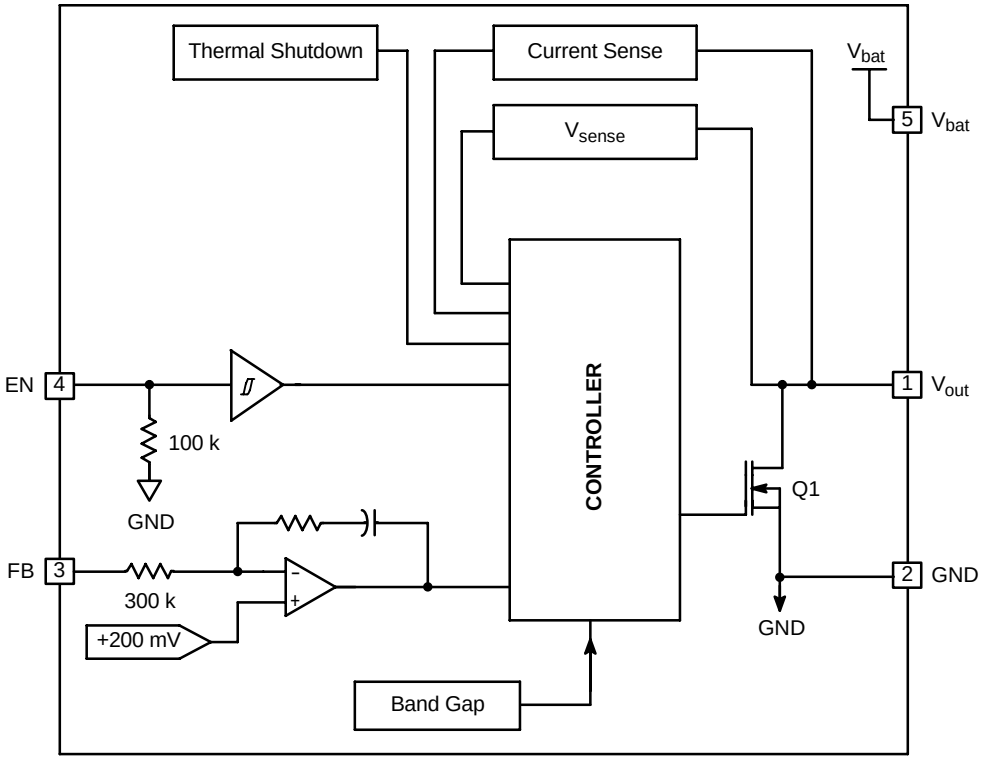


Figure 2. Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Type	Description
1	V_{out}	POWER	This pin is the power side of the external inductor and must be connected to the external Schottky diode. It provides the output current to the load. Since the boost converter operates in a current loop mode, the output voltage can range up to +24 V but shall not extend this limit. However, if the voltage on this pin is higher than the Over Voltage Protection threshold (OVP) the device comes back to shutdown mode. To restart the chip, one must either send a Low to High sequence on Pin EN, or switch off the V_{bat} supply. A capacitor must be used on the output voltage to avoid false triggering of the OVP circuit. This capacitor should be 1.0 μF minimum. Ceramic type, (ESR <100 mΩ), is mandatory to achieve the high end efficiency. This capacitor limits the noise created by the fast transients present in this circuitry. In order to limit the inrush current and to operate with an acceptable start−up time, it is recommended to use any value between 1.0 μF and 8.2 μF capacitor maximum. Care must be observed to avoid EMI through the PCB copper tracks connected to this pin.
2	GND	POWER	This pin is the system ground for the NCP5006 and carries both the power and the analog signals. High quality ground must be provided to avoid spikes and/or uncontrolled operation. Care must be observed to avoid high−density current flow in a limited PCB copper track. Ground plane technique is recommended.
3	FB	ANALOG INPUT	This pin provides the output current range adjustment by means of a sense resistor connected to the analog control or with a PWM control. The dimming function can be achieved by applying a PWM voltage technique to this pin (see Figure 29). The current output tolerance depends upon the accuracy of this resistor. Using a ±5% metal film resistor or better, yields a good enough output current accuracy. Note: A built−in comparator switch OFF the DC/DC converter if the voltage sensed across this pin and ground is higher than 700 mV (typical).
4	EN	DIGITAL INPUT	This is an Active−High logic input which enables the boost converter. The built−in pull down resistor disables the device when the EN pin is left open. The LED brightness can be controlled by applying a pulse width modulated signal to the enable pin (see Figure 31).
5	V_{bat}	POWER	The external voltage supply is connected to this pin. A high quality reservoir capacitor must be connected across Pin 1 and Ground to achieve the specified output voltage parameters. A 4.7 μF/6.3 V, low ESR capacitor must be connected as close as possible across Pin 5 and ground Pin 2. The X5R or X7R ceramic MURATA types are recommended. The return side of the external inductor shall be connected to this pin. Typical application will use a 22 μH, size 1008, to handle the 1.0 to 100 mA max output current range. On the other hand, when the desired output current is above 20 mA, the inductor shall have an ESR < 1.5 Ω to achieve a good efficiency over the V_{bat} range.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply	V_{bat}	6.0	V
Output Power Supply Voltage Compliance	V_{out}	28	V
Digital Input Voltage Digital Input Current	EN	$-0.3 < V_{in} < V_{bat} + 0.3$ 1.0	V mA
ESD Capability (Note 1) Human Body Model (HBM) Machine Model (MM)	V_{ESD}	 2.0 200	 kV V
TSOP−5 Package Power Dissipation @ T_A = +85°C (Note 2) Thermal Resistance, Junction−to−Air	 P_D $R_{\theta JA}$	 160 250	 mW °C/W
Operating Ambient Temperature Range	T_A	−25 to +85	°C
Operating Junction Temperature Range	T_J	−25 to +125	°C
Maximum Junction Temperature	T_{Jmax}	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115
2. The maximum package power dissipation limit must not be exceeded.
3. Latch−up current maximum rating: ±100 mA per JEDEC standard: JESD78.
4. Moisture Sensivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

POWER SUPPLY SECTION (Typical values are referenced to T_A = +25°C, Min & Max values are referenced −25°C to +85°C ambient temperature, unless otherwise noted.)

Rating	Pin	Symbol	Min	Typ	Max	Unit
Power Supply	4	V_{bat}	2.7	−	5.5	V
Output Load Voltage Compliance	5	V_{out}	21	24	−	V
Continuous DC Current in the Load @ V_{out} = 3xLED, L = 22 μH, ESR < 1.5 Ω, V_{bat} = 3.60 V	5	I_{out}	50	−	−	mA
Stand By Current, @ I_{out} = 0 mA, EN = L, V_{bat} = 3.6 V	4	I_{stdb}	−	0.3	−	μA
Stand By Current, @ I_{out} = 0 mA, EN = L, V_{bat} = 5.5 V	4	I_{stdb}	−	0.8	3.0	μA
Inductor Discharging Time @ V_{bat} = 3.6 V, L = 22 μH, 3xLED, I_{out} = 10 mA	4	Toffmax	−	320	−	ns
Thermal Shutdown Protection	−	T_{SD}	−	160	−	°C
Thermal Shutdown Protection Hysteresis	−	T_{SDH}	−	30	−	°C

ANALOG SECTION (Typical values are referenced to T_A = +25°C, Min & Max values are referenced −25°C to +85°C ambient temperature, unless otherwise noted.)

Rating	Pin	Symbol	Min	Typ	Max	Unit
High Level Input Voltage Low Level Input Voltage	4	EN	1.3 −	− −	− 0.4	V V
EN Pull Down Resistor	4	R_{EN}	−	100	−	kΩ
Feedback Voltage Threshold	3	FB	185	200	225	mV
Output Current Stabilization Time Delay following a DC/DC Start−up, @ V_{bat} = 3.60 V, L = 22 μH, I_{out} = 20 mA	1	I_{outdly}	−	100	−	μs
Internal Switch ON Resistor @ Tamb = +25°C	1	QR_{DSON}	−	1.7	−	Ω

5. The overall tolerance depends upon the accuracy of the external resistor.

ESD PROTECTION

The NCP5006 includes silicon devices to protect the pins against the ESD spikes voltages. To cope with the different ESD voltages developed in the applications, the built−in structures have been designed to handle ± 2.0 kV_{in} Human Body Model (HBM) and ± 200 V in Machine Model (MM) on each pin.

DC/DC OPERATION

The DC/DC converter is designed to supply a constant current to the external load, the circuit being powered from a standard battery supply. Since the regulation is made by means of a current loop, the output voltage will varies depending upon the dynamic impedance presented by the load.

Considering high intensity LED, the output voltage can range from a low 6.40 V (two LED in series biased with a low current), up to 21 V, the voltage compliance the chip can sustain continuously.

The basic DC/DC structure is depicted in Figure 3. With a 28 V maximum rating voltage capability, the power device can accommodate high voltage source without any leakage current downgrading.

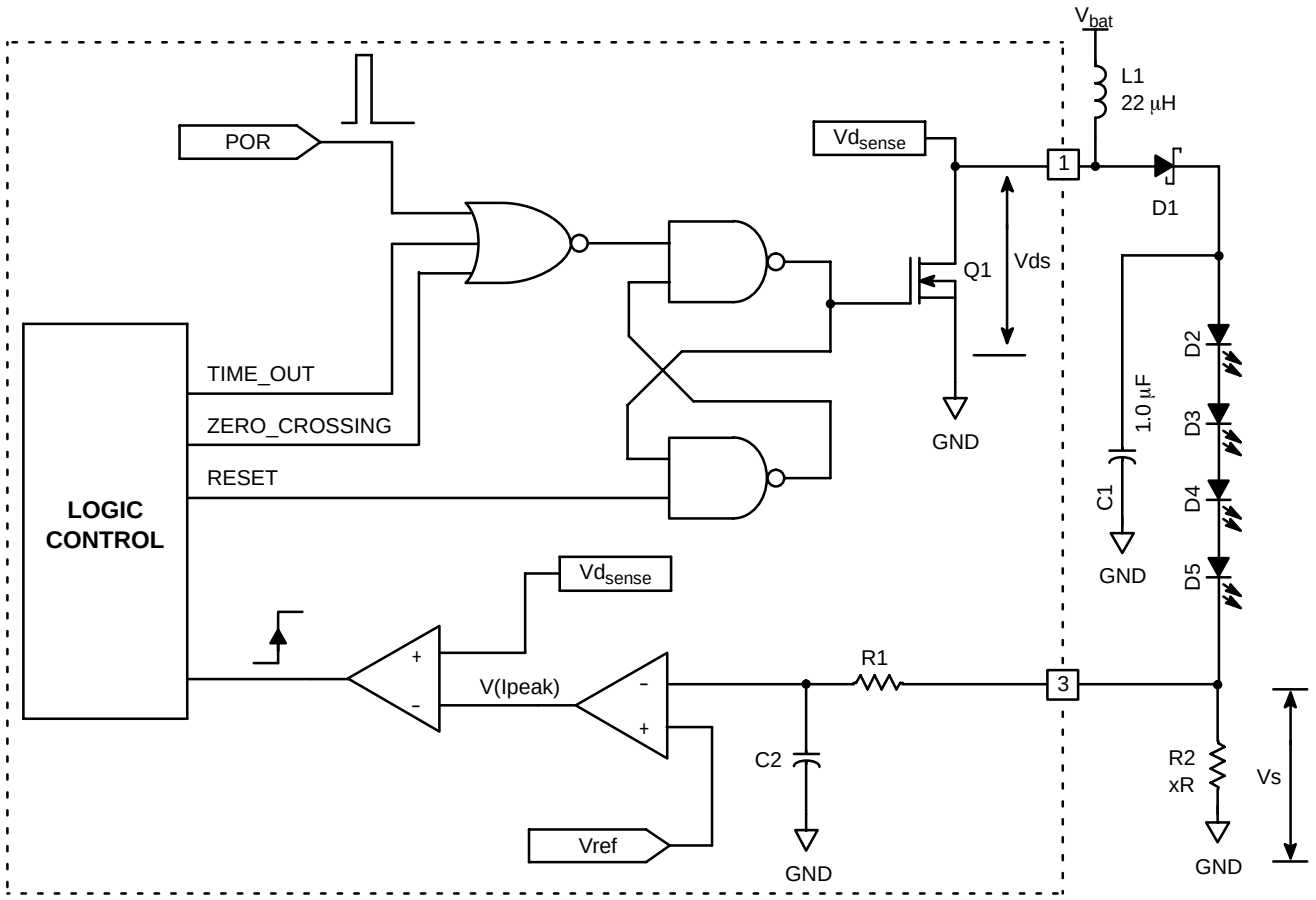


Figure 3. Basic DC/DC Converter Structure

Basically, the chip operates with two cycles:

Cycle #1: time t1, the energy is stored into the inductor

Cycle #2: time t2, the energy is dumped to the load

The POR signal sets the flip−flop and the first cycle takes place. When the current hits the peak value, defined by the error amplifier associated to the loop regulation, the flip−flop resets, the NMOS is deactivated and the current is dumped into the load. Since the timings depend on the environment, the internal timer limits the toff cycle to 320 ns (typical), making sure the system operates in a continuous mode to maximize the energy transfer.

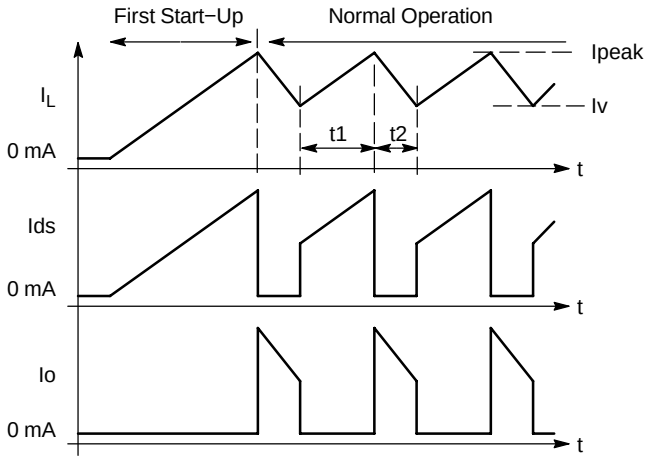


Figure 4. Basic DC−DC Operation

Based on the data sheet, the current flowing into the inductor is bounded by two limits:

- Ipeak Value: Internally fixed to 350 mA typical
- Iv Value: Limited by the fixed Toff time built in the chip (320 ns typical)

The system operates in a continuous mode as depicted in Figure 4 and t_1 and t_2 times can be derived from basic equations. (Note: The equations are for theoretical analysis only, they do not include the losses.)

$$L = E * \frac{dI}{dt} \quad \text{(eq. 1)}$$

Let V_{bat} = E, then:

$$t1 = \frac{(Ip - Iv) * L}{V_{bat}} \quad \text{(eq. 2)}$$

$$t2 = \frac{(Ip - Iv) * L}{Vo - V_{bat}} \quad \text{(eq. 3)}$$

Since t_2 = 320 ns typical and Vo = 21 V maximum, then (assuming a typical V_{bat} = 3.0 V):

$$\Delta I = \frac{t2 * (Vo - V_{bat})}{L} \quad \text{(eq. 4)}$$

$$\Delta Imax = \frac{320\ ns * (21-3.0)}{22\ \mu H} = 261\ mA$$

Of course, from a practical stand point, the inductor must be sized to cope with the peak current present in the circuit to avoid saturation of the core. On top of that, the ferrite material shall be capable to operate at high frequency (1.0 MHz) to minimize the Foucault's losses developed during the cycles.

The operating frequency can be derived from the electrical parameters. Let V = Vo − V_{bat}, rearranging Equation 1:

$$ton = \frac{dI * L}{E} \quad \text{(eq. 5)}$$

Since toff is nearly constant (according to the 320 ns typical time), the dI is constant for a given load and inductance value. Rearranging Equation 5 yields:

$$ton = \frac{\frac{V*dt}{L} * L}{E} \quad \text{(eq. 6)}$$

Let E = V_{bat}, and Vopk = output peak voltage, then:

$$ton = \frac{(Vopk - V_{bat}) * dt}{V_{bat}} \quad \text{(eq. 7)}$$

Finally, the operating frequency is:

$$f = \frac{1}{ton + toff} \quad \text{(eq. 8)}$$

The output power supplied by the NCP5006 is limited to one watt: Figure 5 shows the maximum power that can be delivered by the chip as a function of the output voltage.

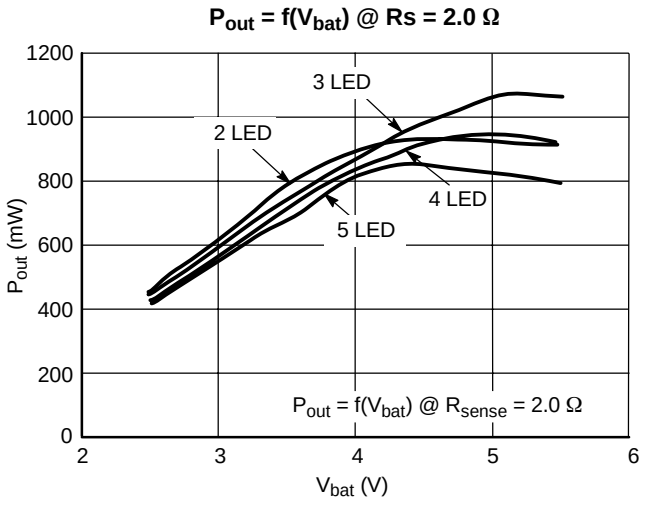
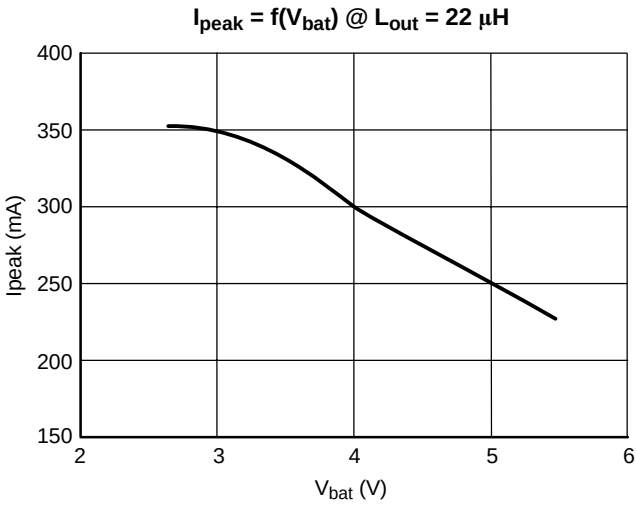
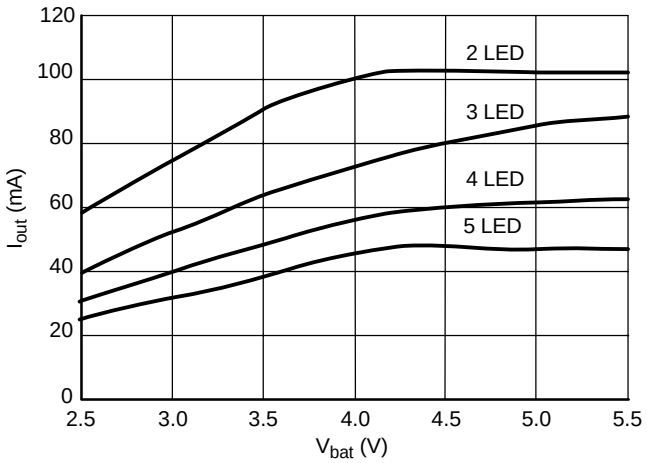


Figure 5. Maximum Output Power as a Function of the Battery Supply Voltage



Test conditions: L = 22 μH, R_{sense} = 10 Ω, Tamb = +20°C

Figure 6. Typical Inductor Peak Current as a Function of V_{bat} Voltage



Test conditions: L = 22 μH, R_{sense} = 2.0 Ω, Tamb = +25°C

Figure 7. Maximum Output Current as a Function of V_{bat}

Output Current Range Set−Up

The current regulation is achieved by means of an external sense resistor connected in series with the LED string.

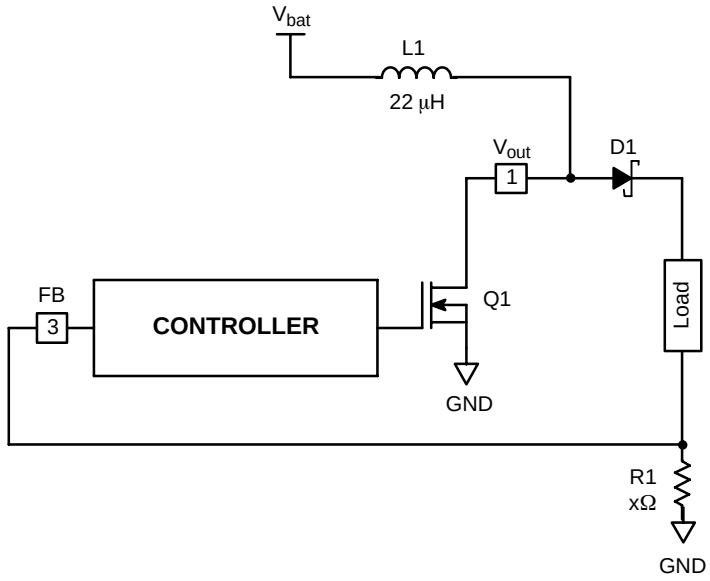


Figure 8. Output Current Feedback

The current flowing through the LED creates a voltage drop across the sense resistor R1. The voltage drop is constantly monitored internally, and maximum peak current allowed in the inductor is set accordingly in order to keep constant this voltage drop (and thus the current flowing through the LED). For example, should one need a 10 mA output current, the sense resistor should be sized according to the following equation:

$$R_1 = \frac{\text{Feedback Threshold}}{I_{out}} = \frac{200\ \text{mV}}{10\ \text{mA}} = 20\ \Omega \qquad \text{(eq. 9)}$$

A standard 5% tolerance resistor, 22 Ω SMD device, yields 9.09 mA, good enough to fulfill the back light demand. The typical application schematic diagram is provided in Figure 9.

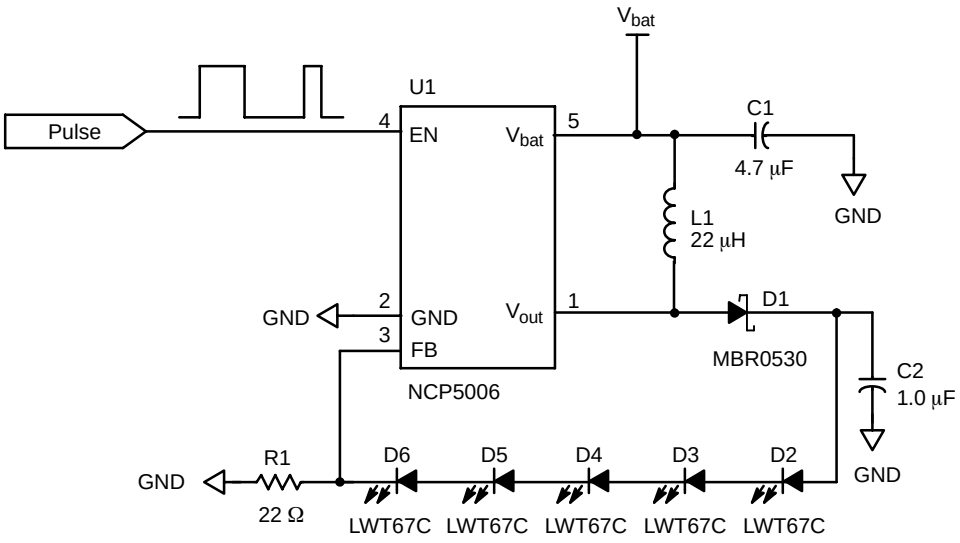


Figure 9. Basic Schematic Diagram

Output Load Drive

In order to optimize the built−in Boost capabilities, one shall operate the NCP5006 in the continuous output current mode. Such a mode is achieved by using and external reservoir capacitor (see Table 1) across the LED.

At this point, the peak current flowing into the LED diodes shall be within the maximum ratings specified for these devices. Of course, pulsed operation can be achieved, due to the EN signal Pin 4, to force high current into the LED when necessary.

The Schottky diode D1, associated with capacitor C2 (see Figure 9), provides a rectification and filtering function.

When a pulse−operating mode is acceptable:

- A PWM mode control can be used to adjust the output current range by means of a resistor and a capacitor connected across FB pin. On the other hand, the Schottky diode can be removed and replaced by at least one LED diode, keeping in mind such LED shall sustain the large pulsed peak current during the operation.

TYPICAL OPERATING CHARACTERISTICS

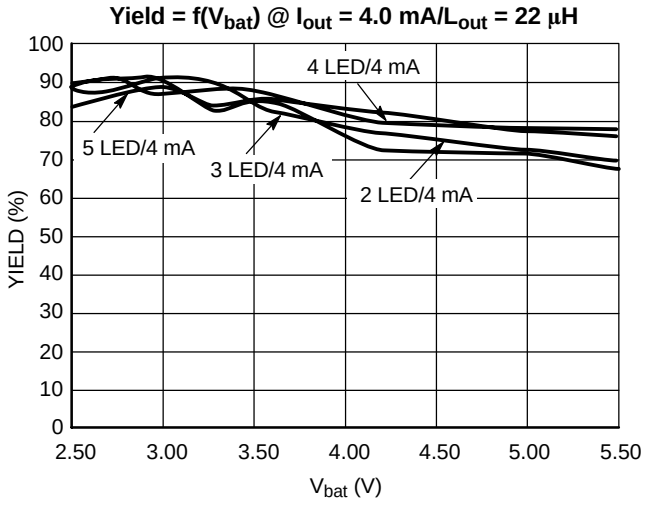


Figure 10. Overall Efficiency vs. Power Supply @ I_{out} = 4.0 mA, L = 22 μH

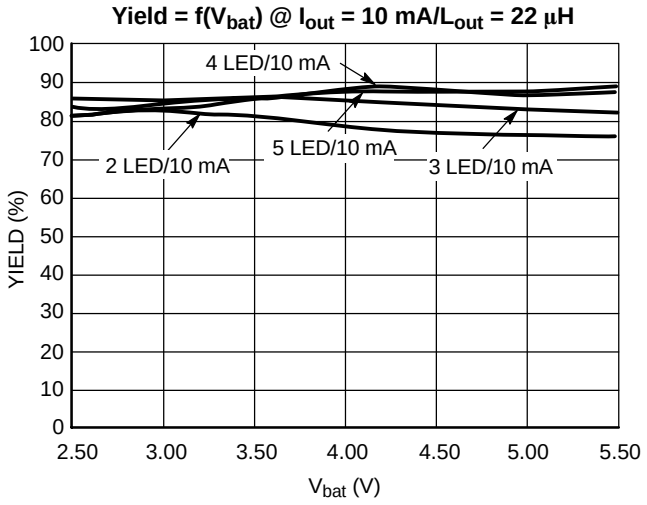


Figure 11. Overall Efficiency vs. Power Supply @ I_{out} = 10 mA, L = 22 μH

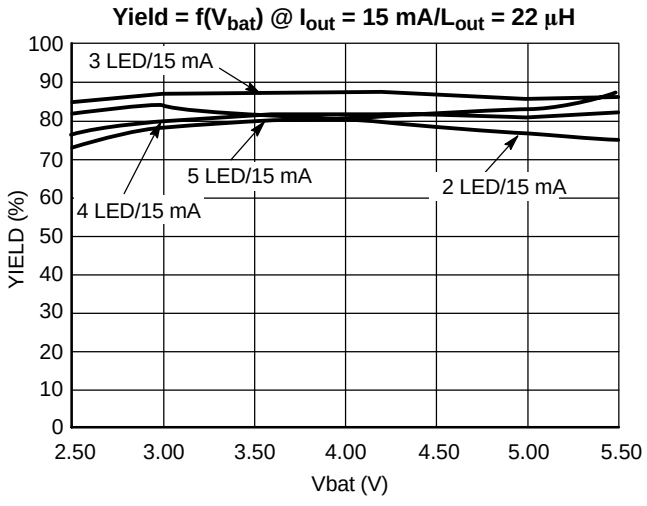


Figure 12. Overall Efficiency vs. Power Supply @ I_{out} = 15 mA, L = 22 μH

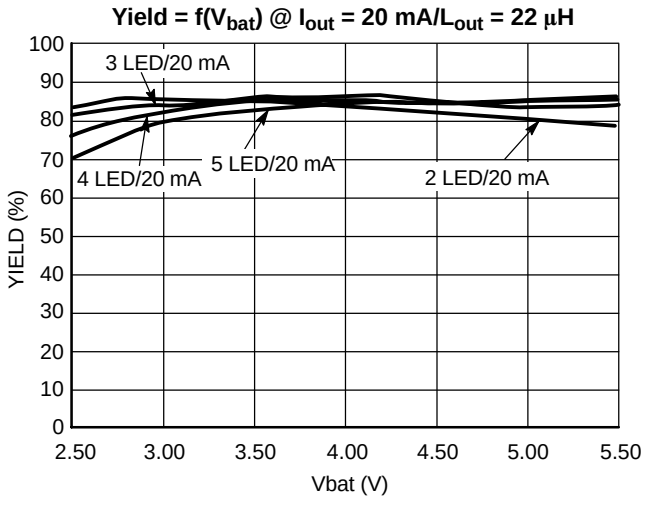


Figure 13. Overall Efficiency vs. Power Supply @ I_{out} = 20 mA, L = 22 μH

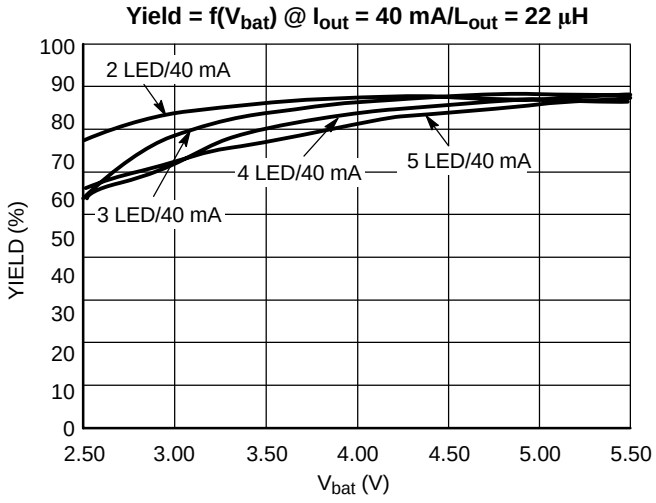


Figure 14. Overall Efficiency vs. Power Supply @ I_{out} = 40 mA, L = 22 μH

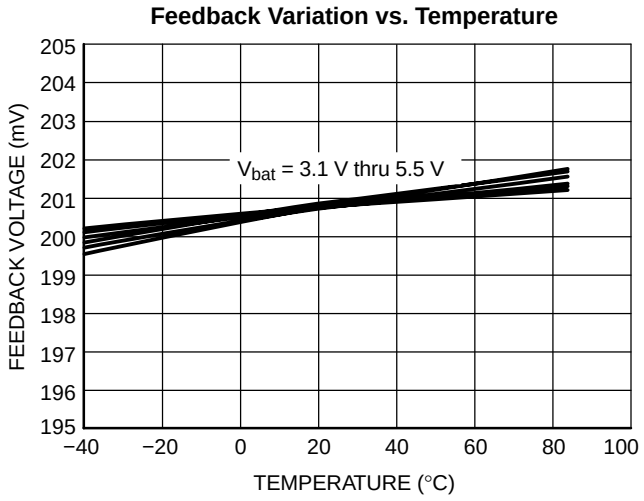


Figure 15. Feedback Voltage Stability

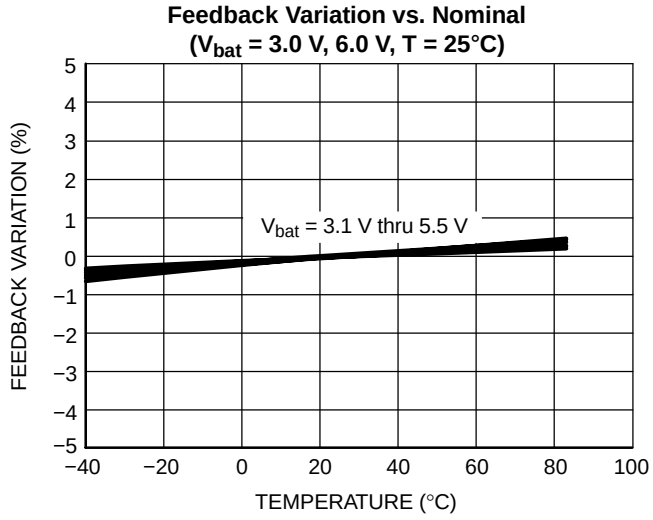


Figure 16. Feedback Voltage Variation

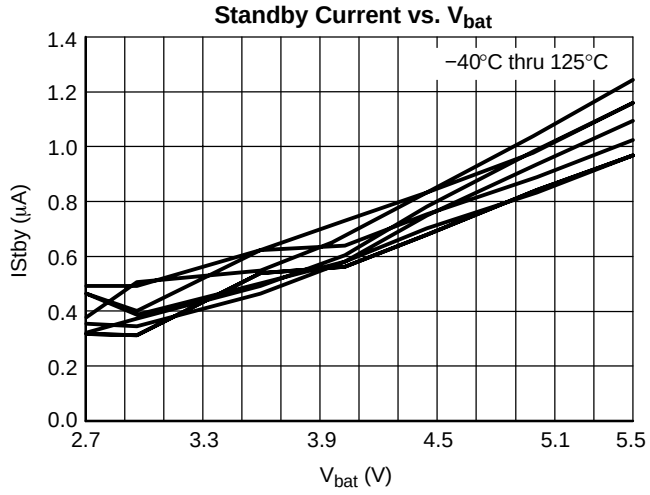


Figure 17. Standby Current

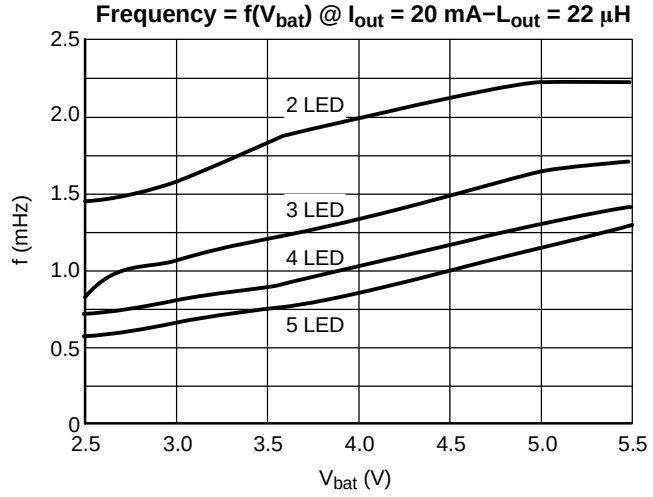


Figure 18. Typical Operating Frequency

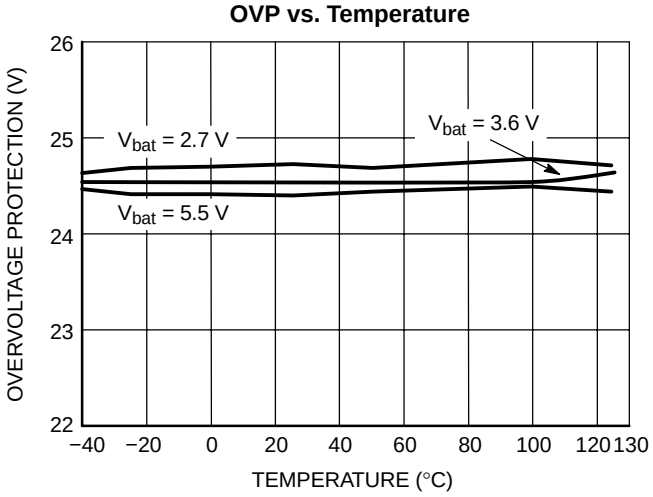
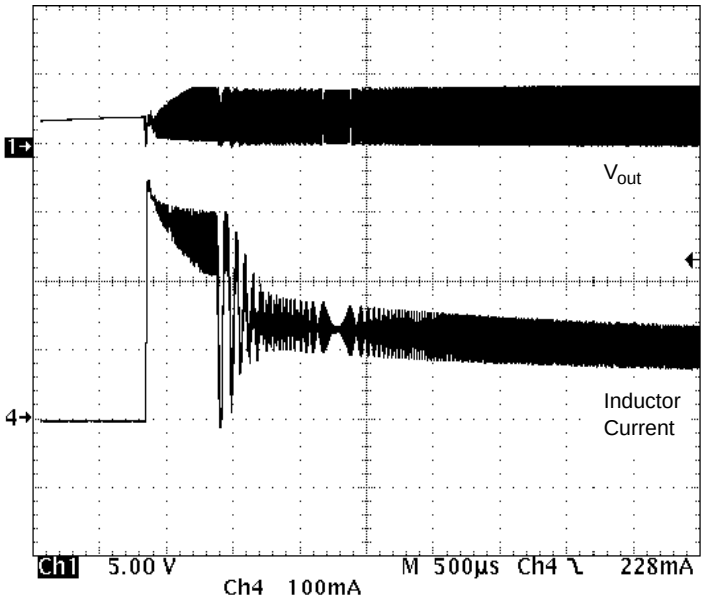


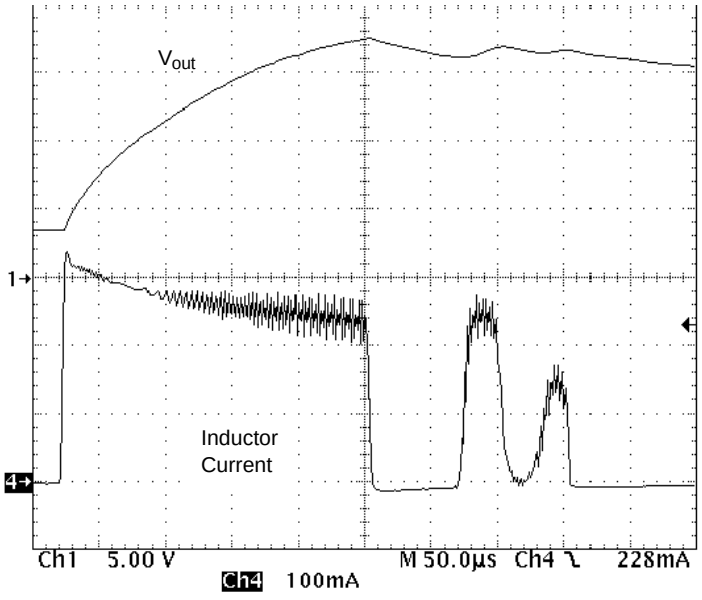
Figure 19. Overvoltage Protection

TYPICAL OPERATING WAVEFORMS



Conditions: V_{bat} = 3.6 V, L_{out} = 22 µH, 5 LED, I_{out} = 15 mA

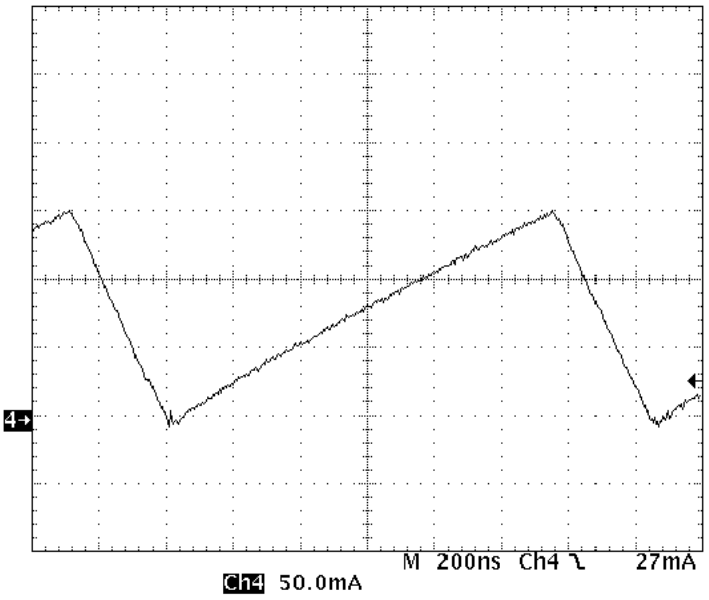
Figure 20. Typical Power Up Response



Conditions: V_{bat} = 3.6 V, L_{out} = 22 µH, 5 LED, I_{out} = 15 mA

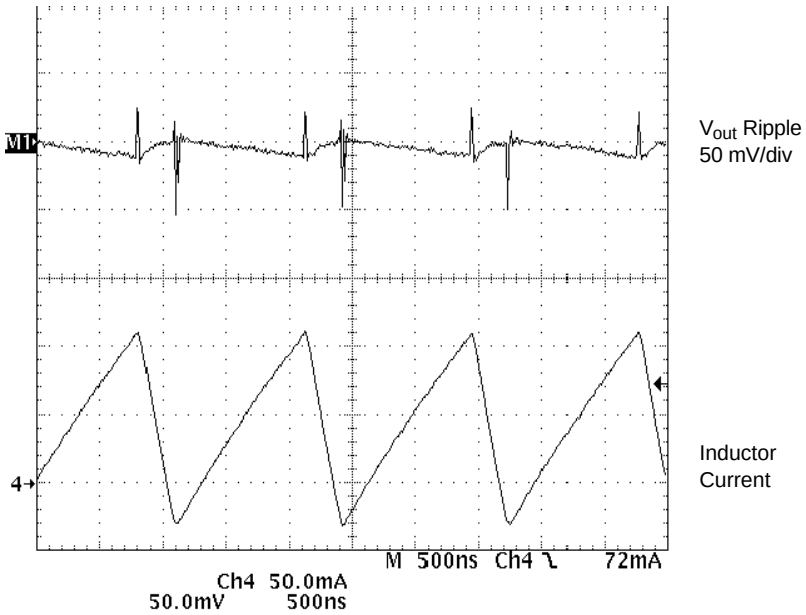
Figure 21. Typical Start−Up Inductor Current and Output Voltage

TYPICAL OPERATING WAVEFORMS



Conditions: V_{bat} = 3.6 V, L_{out} = 22 μH, 5 LED, I_{out} = 15 mA

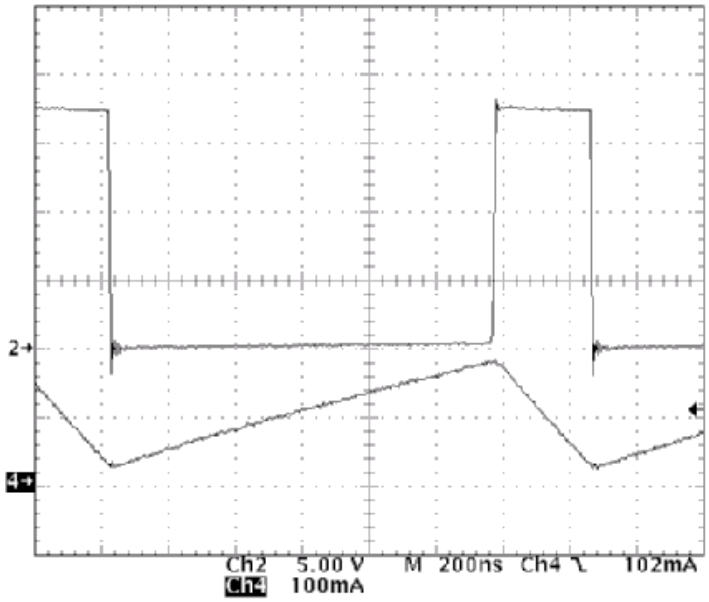
Figure 22. Typical Inductor Current



Conditions: V_{bat} = 3.6 V, L_{out} = 22 μH, 5 LED, I_{out} = 15 mA

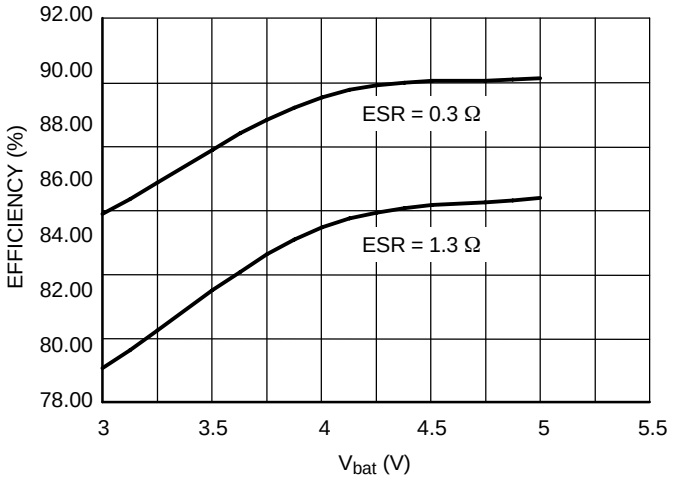
Figure 23. Typical Output Voltage Ripple

TYPICAL OPERATING WAVEFORMS



Test Conditions: L = 22 μH, I_{out} = 15 mA, V_{bat} = 3.6 V, Ambient Temperature

Figure 24. Typical Output Peak Voltage



NCP5006: Efficiency = f(ESR) @ 5 LED, ILed = 20 mA

Figure 25. Efficiency as a Function of V_{bat} and Inductor ESR

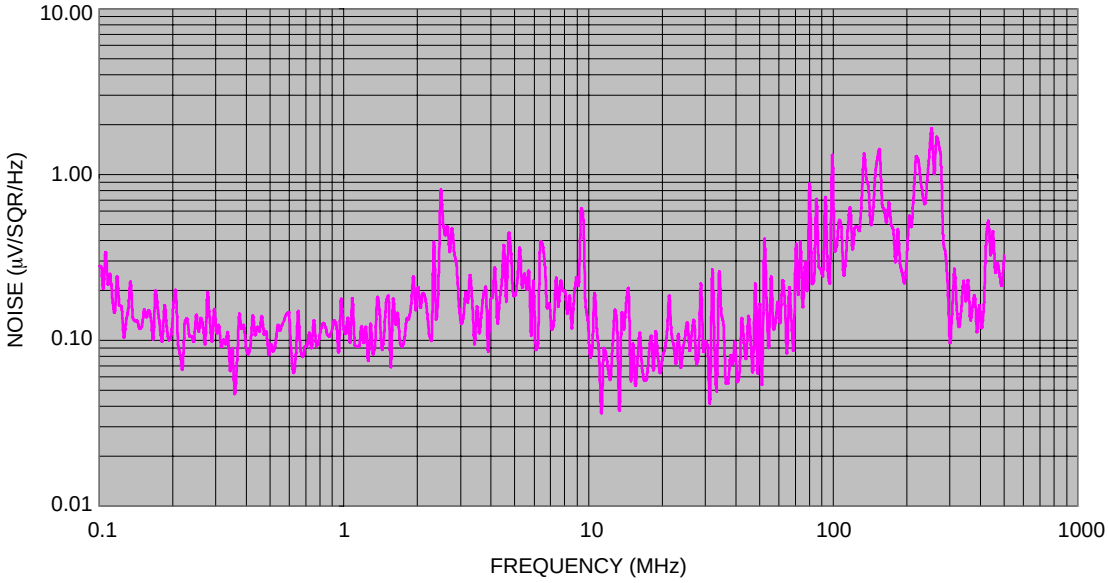
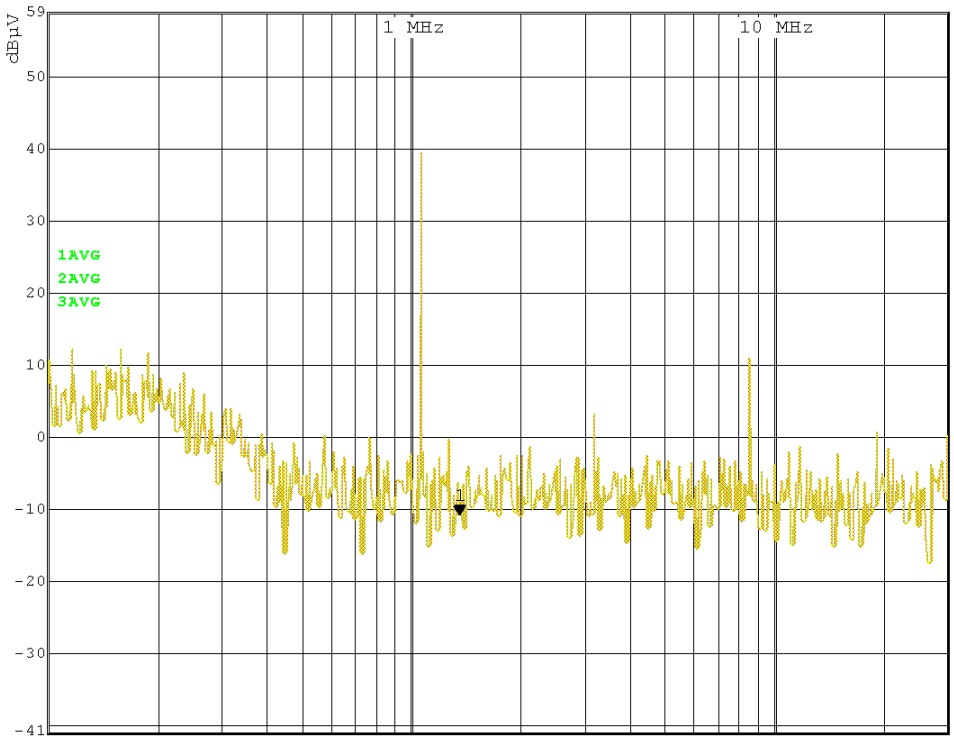


Figure 26. Noise Returned to the Battery



Test Conditions: V_{bat} = 3.6 V, I_{out} = 20 mA, string of 3 LED (OSRAM LWT67C)

Figure 27. Relative EMI Over 100 kHz − 30 MHz Bandwidth

TYPICAL APPLICATIONS CIRCUITS

Standard Feedback

The standard feedback provides a constant current to the LED, independently of the V_{bat} supply and number of LED associated in series. Figure 28 depicts a typical application to supply 13 mA to the load.

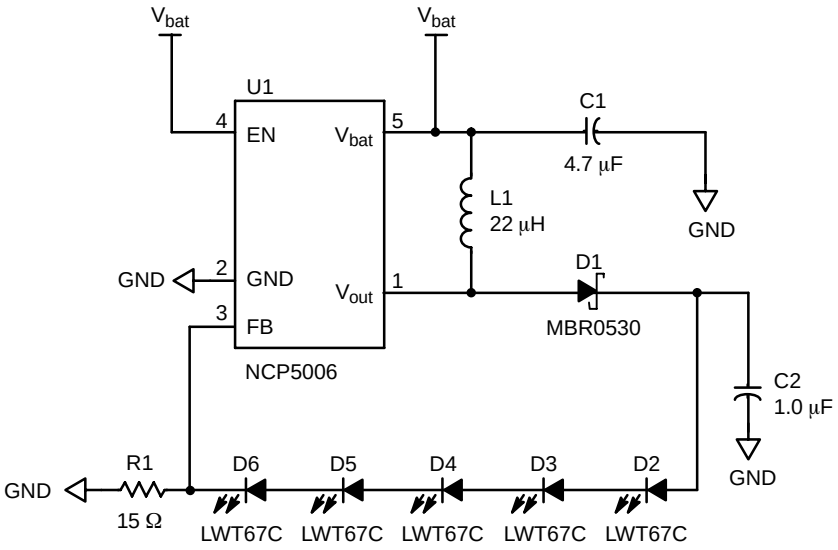


Figure 28. Basic DC Current Mode Operation with Analog Feedback

PWM Operation

The analog feedback Pin 3 provides a way to dim the LED by means of an external PWM signal as depicted in Figure 29. By optimizing the internal high impedance presented by the FB pin, one can set up a simple R/C network to accommodate such a dimming function. Two modes of operation can be considered:

- Pulsed mode, with no filtering
- Averaged mode with filtering capacitor

Although the pulsed mode will provide a good dimming function, from a human eye standpoint, it will continuously start and stop the converter, yielding high transients . These transients might generate spikes difficult to filter out in the rest of the application, a situation not recommended. The output current depends upon the duty cycle of the signal presented to the node Pin 3: this is very similar to the digital control discussed in Figure 31.

The average mode yields a noise free operation since the converter operates continuously, together with a very good dimming function. The cost is an extra resistor and one extra capacitor, both being low cost parts.

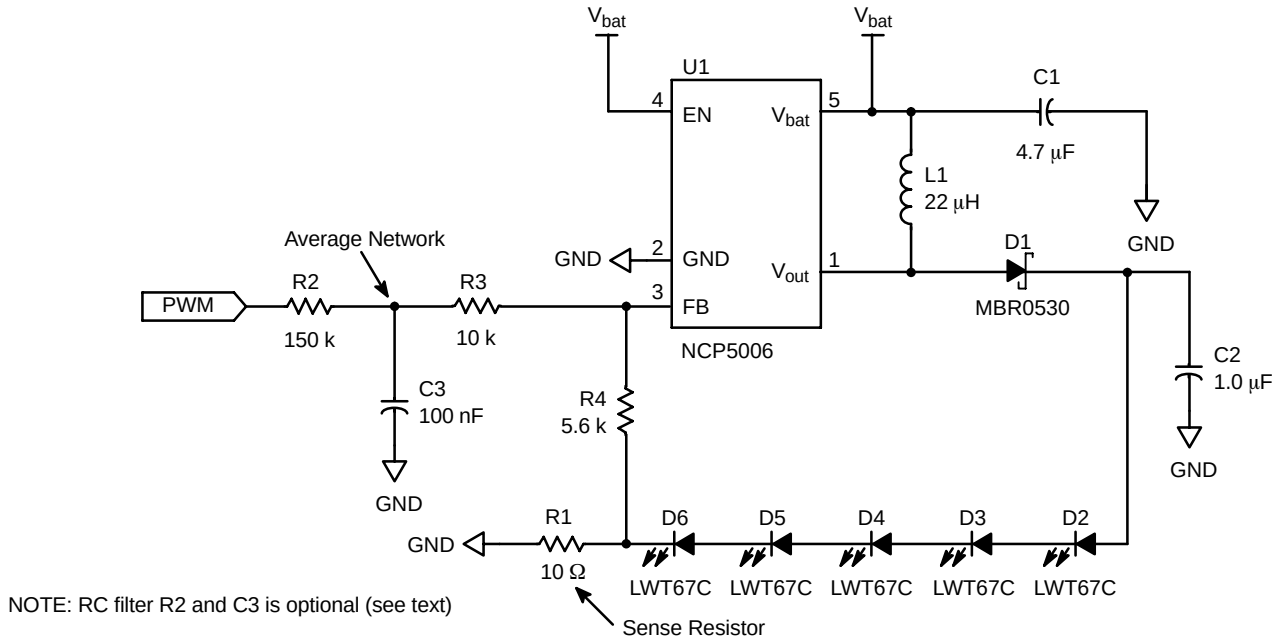


Figure 29. Basic DC Current Mode Operation with PWM Control

To implement such a function, let consider the feedback input as an operational amplifier with a high impedance input (reference schematic Figure 29). The analog loop will keep going to balance the current flowing through the sense resistor R1 until the feedback voltage is 200 mV. An extra resistor (R4) isolates the FB node from low resistance to ground, making possible to add an external voltage to this pin.

The time constant R2/C3 generates the voltage across C3, added to the node Pin 1, while R2/R3/R4/R1/C3 create the discharge time constant. In order to minimize the pick up noise at FB node, the resistors shall have relative medium value, preferably well below 1.0 MΩ. Consequently, let R2 = 150 k, R3 = 10 k and R4 = 5.6 k. On the other hand, the feedback delay to control the luminosity of the LED shall be acceptable by the user, 10 ms or less being a good compromise. The time constant can now be calculated based on a 400 mV offset voltage at the C3/R2/R3 node to force zero current to the LED. Assuming the PWM signal comes from a standard gate powered by a 3.0 V supply, running at 10 kHz, then a full dimming of the LED can be achieved with a 95% span of the Duty Cycle signal. Figure 30 depicts the behavior under such PWM analog mode.

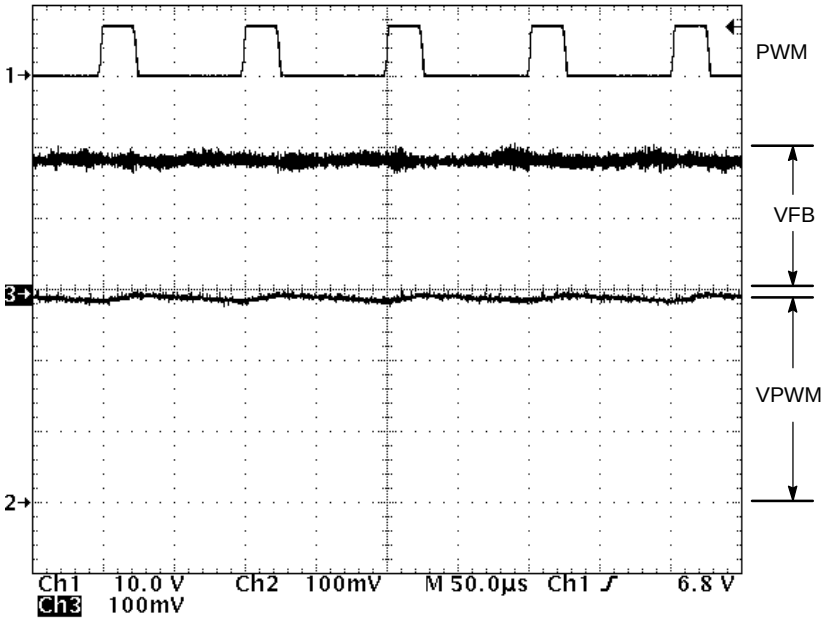
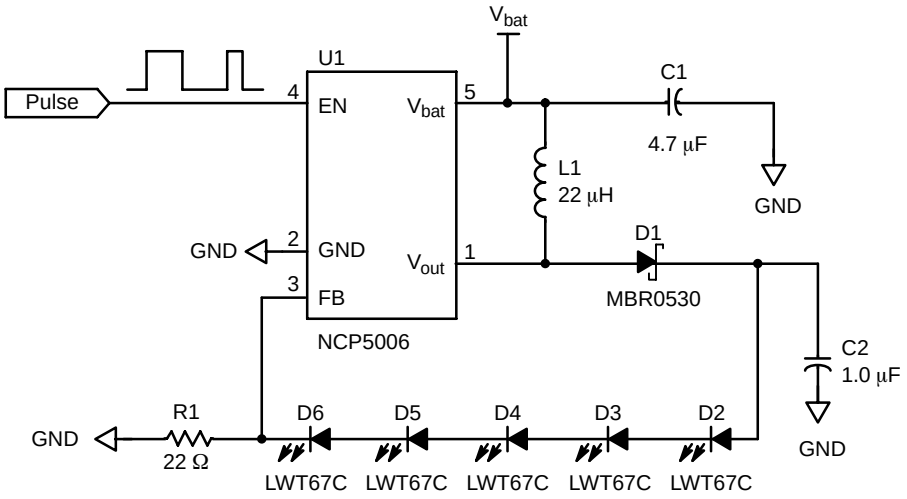


Figure 30. Operation with Analog PWM, f = 10 kHz, DC = 25%

Digital Control

Due to the EN pin, a digitally controlled luminosity can be implemented by providing a PWM signal to this pin (see Figure 31). The output current depends upon the Duty Cycle, but care must be observed as the DC/DC converter is continuously pulsed ON/OFF and noise are likely to be generated.



NOTE: Pulse width and frequency depends upon the application constraints.

Figure 31. Typical Semi−Pulsed Mode of Operation

The PWM operation, using the EN pin as a digital control, is depicted in Figures 32 and 33. The tests have been carried out at room temperature with V_{bat} = 3.60 V, L = 22 μH, five LEDs in series, RFB = 22 Ω.

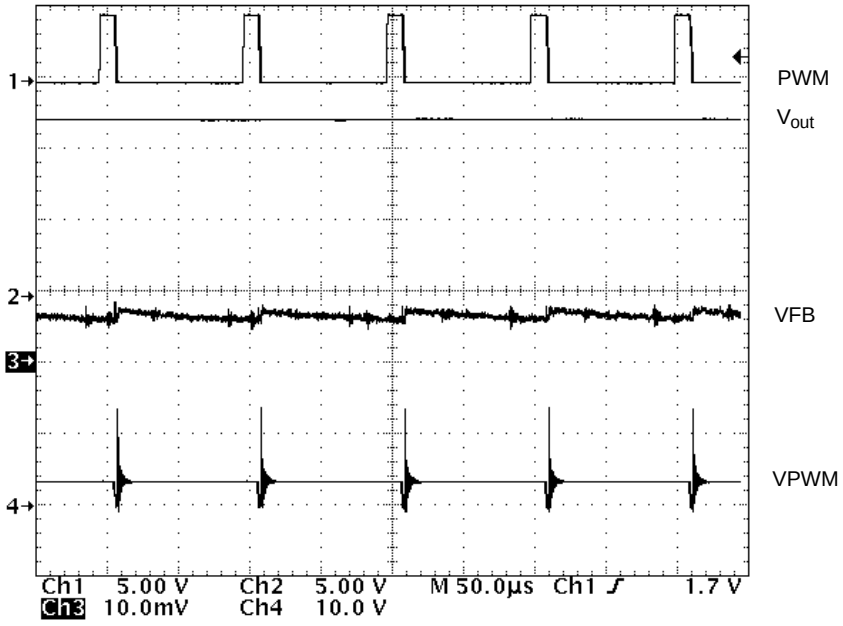


Figure 32. Operation @ PWM = 10 kHz, DC = 10%

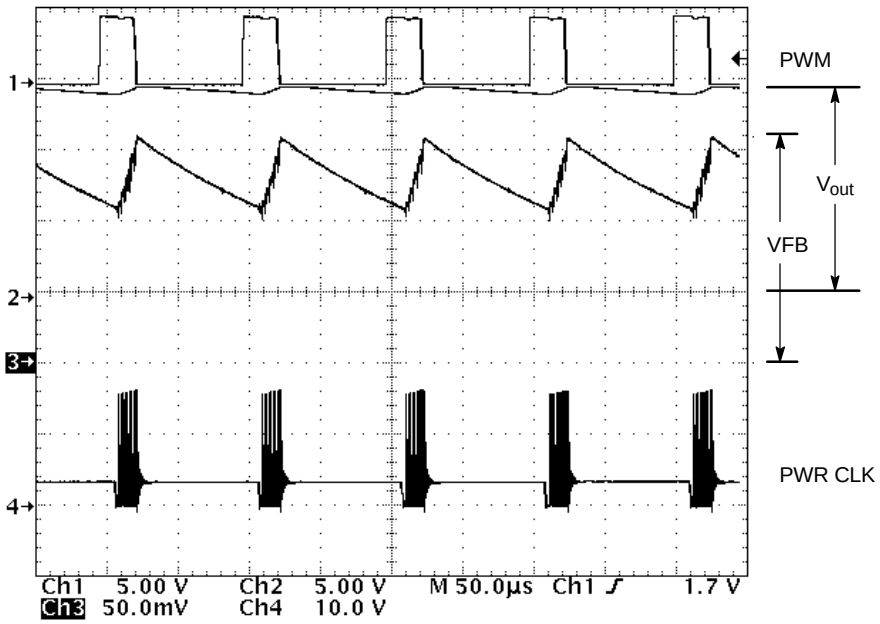


Figure 33. Operation @ PWM = 10 kHz, DC = 25%

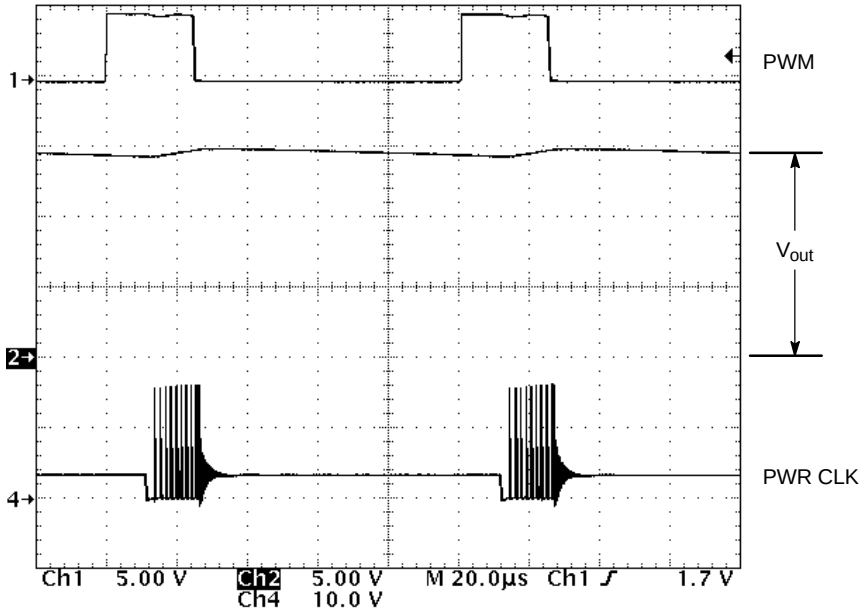


Figure 34. Magnified View of Operation @ PWM = 10 kHz, DC = 25%

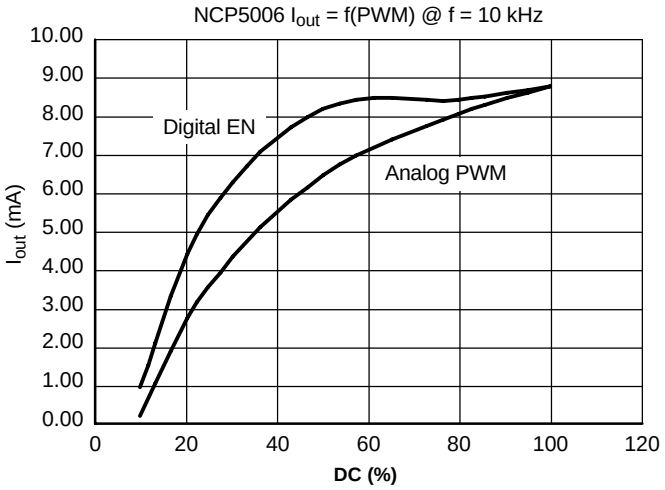


Figure 35. Output Current as a Function of the Operating Condition

Table 1. Recommended Passive Parts

Part	Manufacturer	Description	Part Number
Ceramic Capacitor 1.0 μF/16 V	MURATA	GRM42 − X7R	GRM42−6X7R−105K16
Ceramic Capacitor 1.0 μF/25 V	MURATA	GRM42 – X5R	GRM
Ceramic Capacitor 4.7 μF/6.3 V	MURATA	GRM40 – X5R	GRM40−X5R−475K6.3
Inductor 22 μH	CoilCraft	1008PS − Shielded	1008PS−223MC
Inductor 22 μH	CoilCraft	Power Wafer	LPQ4812−223KXC
Inductor 22 μH	WURTH	Power Choke	744031220
Inductor 22 μH	TDK	Power Inductor	VLP4614T−220MR40

Typical LEDs Load Mapping

Since the output power is voltage battery limited (see Figure 5), one shall arrange the LED to cope with a specific need. In particular, since the power cannot extend 600 mW under realistic battery supply, powering ten LED can be achieved by a series/parallel combination as depicted in Figure 36.

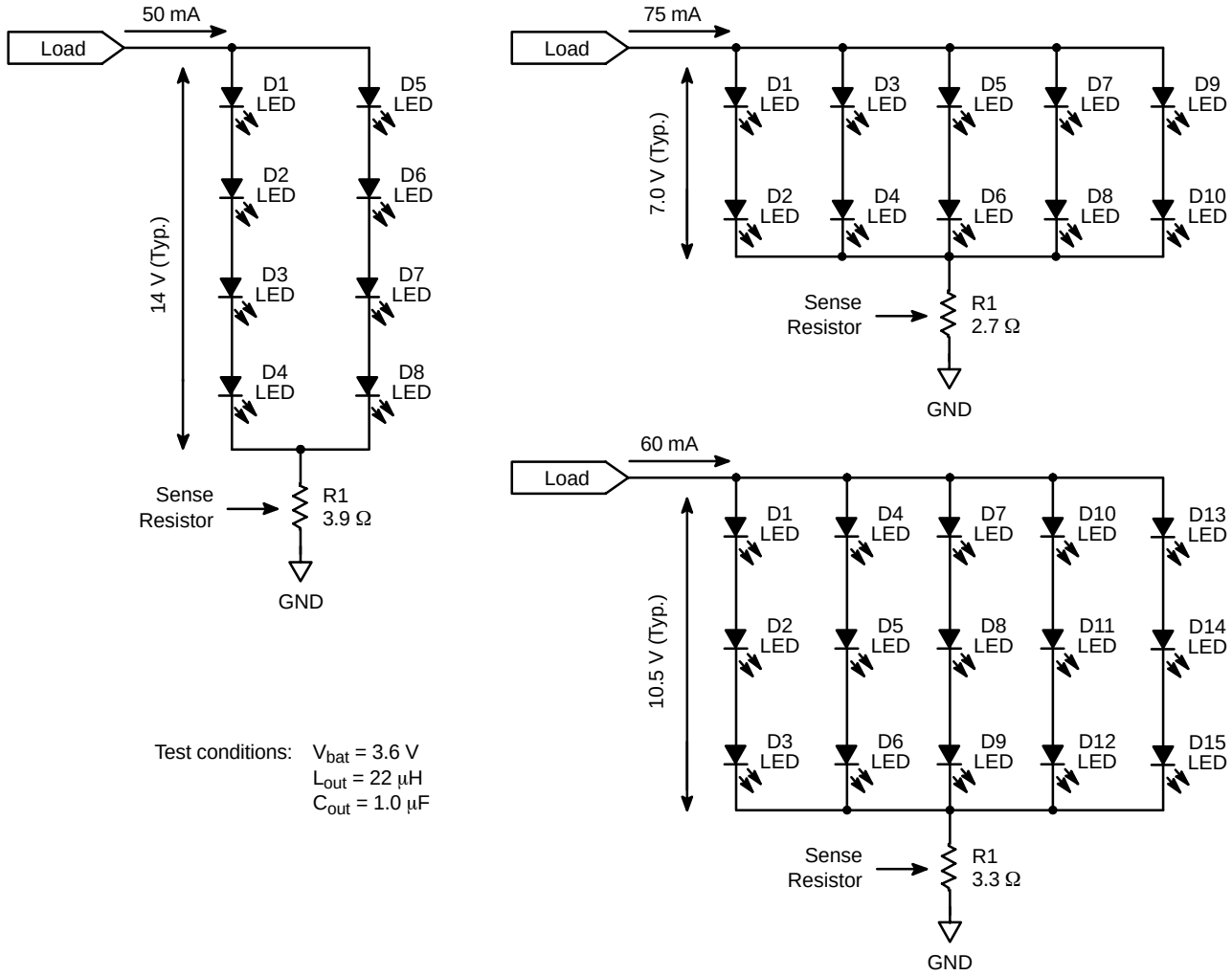


Figure 36. Examples of Possible LED Arrangements

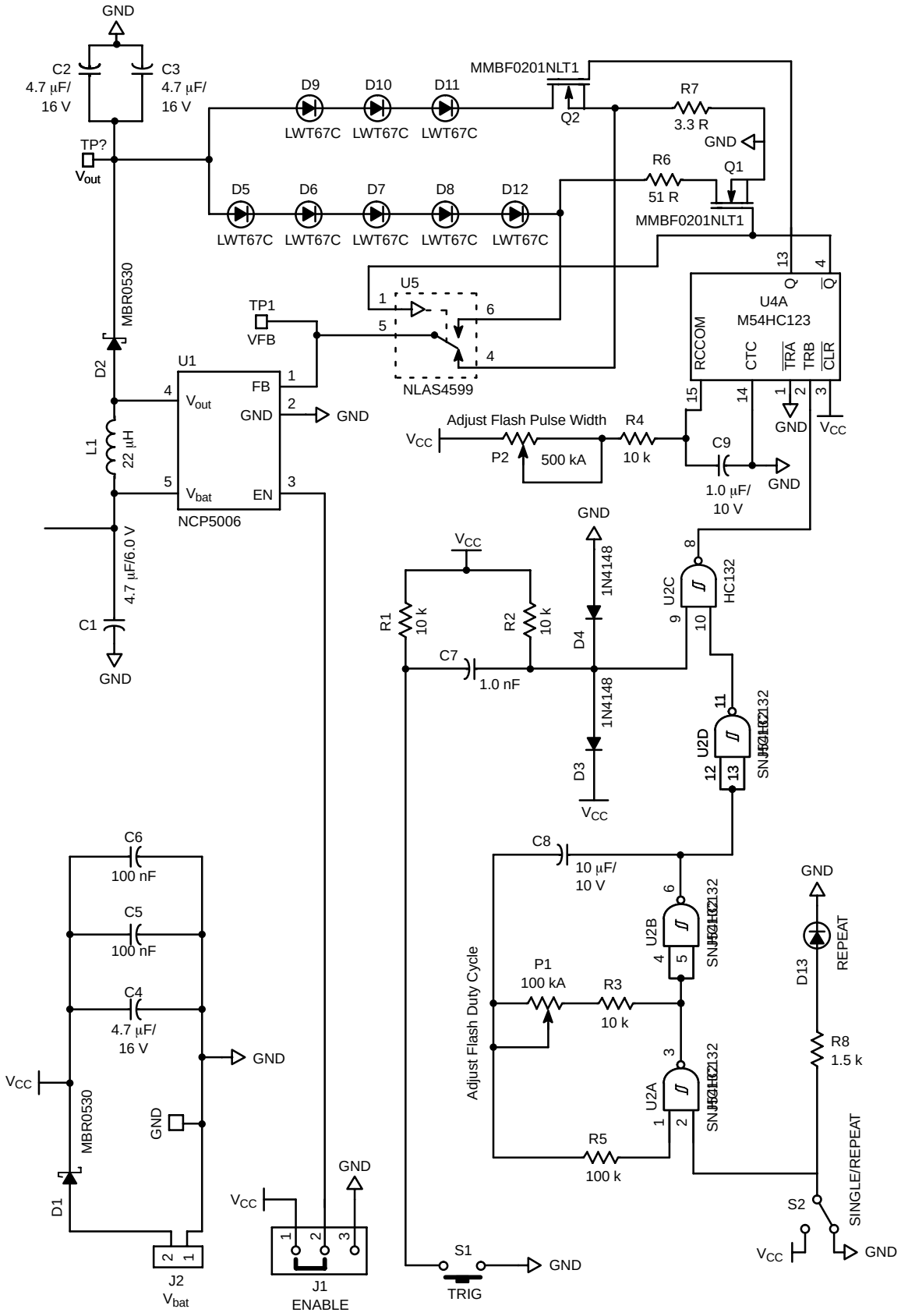


Figure 37. NCP5006 Demo Board Schematic Diagram

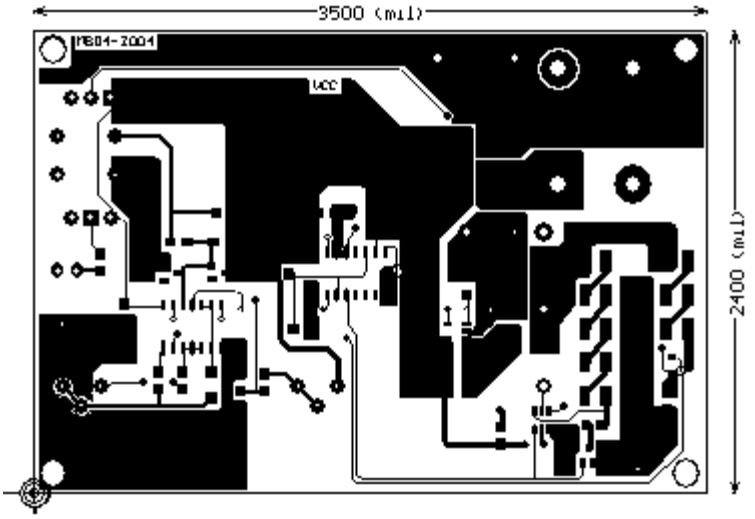


Figure 38. NCP5006 Demo Board PCB: Top Layer

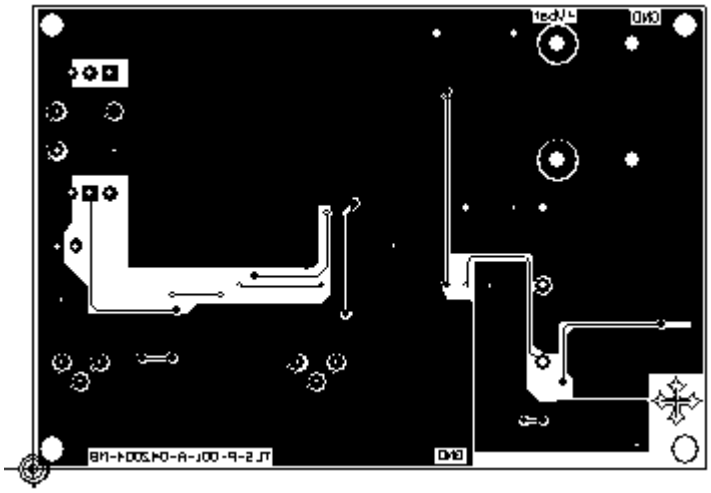


Figure 39. NCP5006 Demo Board PCB: Bottom Layer

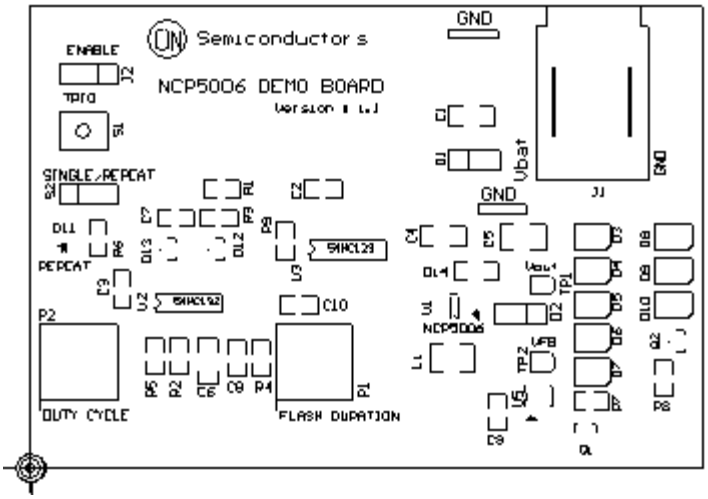


Figure 40. NCP5006 Demo Board Top Silkscreen

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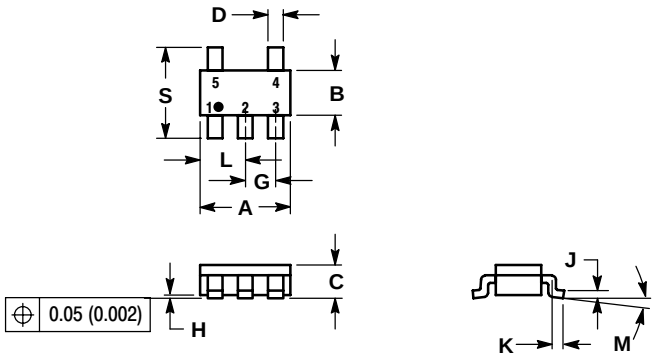
Note 1: This device series contains ESD protection and exceeds the following tests 4
Note 2: The maximum package power dissipation limit must not be exceeded 4
Note 3: Latch−up current maximum rating: ± 100 mA per JEDEC standard: JESD78 4
Note 4: Moisture Sensivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A 4
Note 5: The overall tolerance depends upon the accuracy of the external resistor 5

ABBREVIATIONS

EN Enable
FB Feed Back
POR Power On Reset: Internal pulse to reset the chip when the power supply is applied

PACKAGE DIMENSIONS

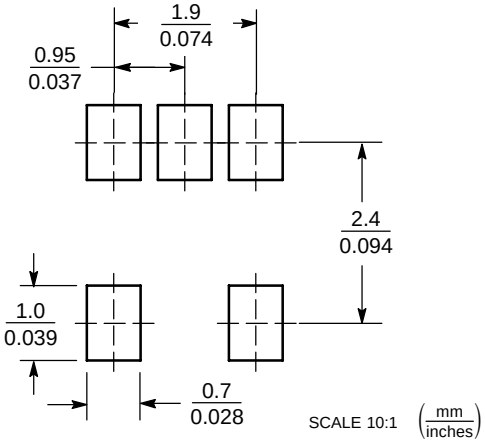
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CASE 483−02
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3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. A AND B DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0	10	0	10
S	2.50	3.00	0.0985	0.1181

SOLDERING FOOTPRINT*



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