Standard Products

UT699 32-bit Fault-Tolerant SPARC™ V8/LEON 3FT Processor

Data Sheet
July, 2013

FEATURES

- Implemented on a 0.25µm CMOS technology
- Flexible static design allows up to 66MHz clock rate
- 89 DMIPS throughput via 66MHz base clock frequency
- Internally configured clock network
- On-board programmable timers and interrupt controllers
- High-performance fully pipelined IEEE-754 FPU
- Power saving 2.5V core power supply
- 3.3V I/O compatibility
- Hardened-by-design flip-flops and memory cells
- Separate instruction and data cache architecture
- 10/100 Base-T Ethernet port for VxWorks development
- Integrated PCI 2.2 compatible core
- Four integrated multi-protocol SpaceWire nodes with two supporting the RMAP protocol
- Two CAN-compliant 2.0 bus interfaces
- Multifunctional memory controller
- -40°C to +105°C operating case temperature range
- Operational environment:
  - Intrinsic total-dose: 100 krad(Si) and 300 krad(Si)
  - SEL Immune >108 MeV-cm^2/mg
- Packaging options:
  - 352-pin Ceramic Quad Flatpack, weight 31.5 grams
  - 484-pin Ceramic Land Grid, Column Grid and Ball Grid Array packages
- Standard Microcircuit Drawing 5962-08228
  - QML Q and V
- Applications
  - Nuclear power plant controls
  - Critical transportation systems
  - High-altitude avionics
  - Medical electronics
  - X-Ray cargo scanning

INTRODUCTION

The UT699 is a pipelined monolithic, high-performance, fault-tolerant SPARC™ V8/LEON 3FT Processor. The UT699 provides a 32-bit master/target PCI interface, including a 16 bit user I/O interface for off-chip peripherals. A compliant 2.0 AMBA bus interface integrates the on-chip LEON 3FT, SpaceWire, Ethernet, memory controller, cPCI, CAN bus, and programmable interrupt peripherals.

The UT699 is SPARC V8 compliant; compilers and kernels for SPARC V8 can therefore be used industry standard development tools. A full software development suite is available including a C/C++ cross-compiler system based on GCC and the Newlib embedded C-library.

BCC includes a small run-time kernel with interrupt support and Pthreads library. For multi-threaded applications, a SPARC™ compliant port of the eCos real-time kernel, RTEMS 4.6.5, and VxWorks 6.x is supported.

1.0 Introduction

The UT699 LEON 3FT processor is based upon the industry-standard SPARC V8 architecture. The system-on-chip incorporates the SPARC V8 core and the peripheral blocks indicated below. The core and peripherals communicate internally via the AMBA (Advanced Microcontroller Bus Architecture) backplane. This bus is comprised of the AHB (Advanced High-speed Bus) which is used for high-speed data transfer, and the APB (Advanced Peripheral Bus) which is used for low-speed data transfer.

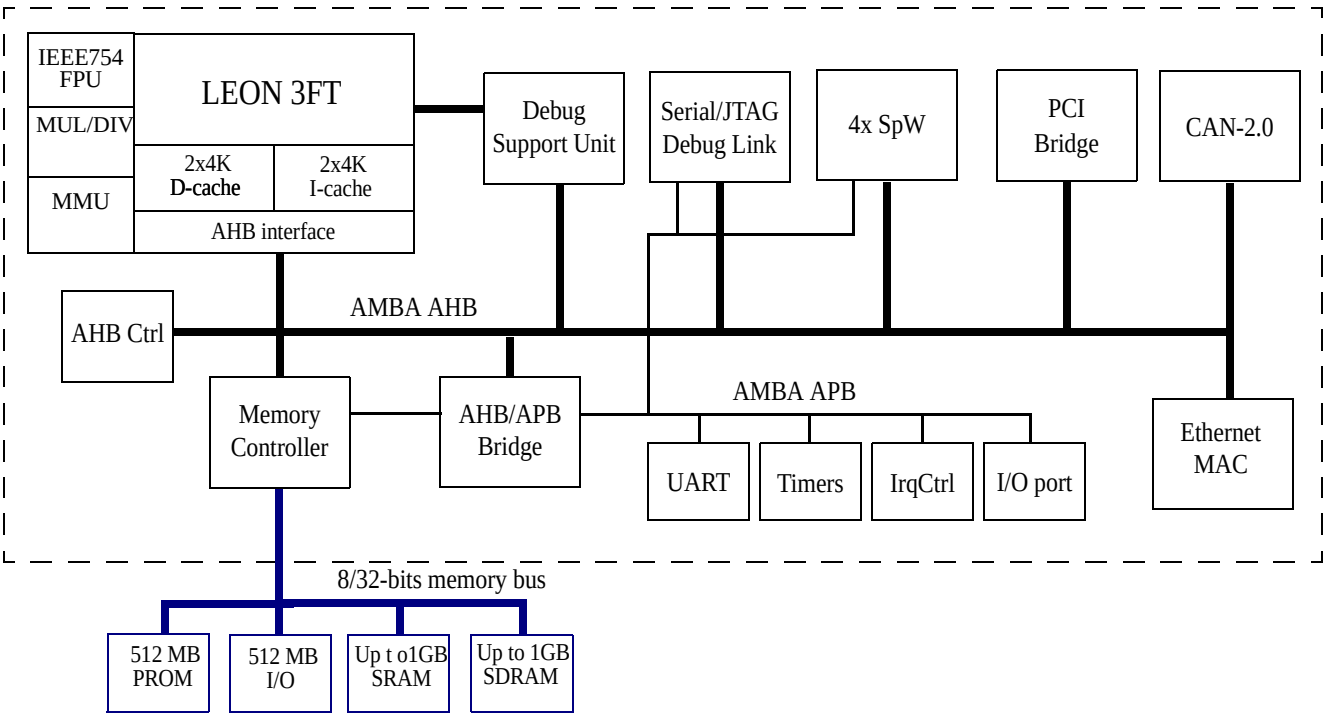


Figure 1. UT699 Functional Block Diagram

The LEON 3FT architecture includes the following peripheral blocks:

- LEON3 SPARC V8 integer unit with 8kB instruction cache and 8kB of data cache
- IEEE-754 floating point unit
- Debug support unit
- UART and JTAG debug links
- 8/16/32-bit memory controller with EDAC for external PROM and SRAM
- 32-bit SDRAM controller with EDAC for external SDRAM
- Timer unit with three 32-bit timers and watchdog
- Interrupt controller for 15 interrupts in two priority levels
- 16-bit general purpose I/O port (GPIO) which can be used as external interrupt sources
- AMBA AHB status register
- Up to four SpaceWire links with RMAP on channels 3and 4
- Up to two CAN controllers
- Ethernet with support for MII
- cPCI interface with 8-channel arbiter

2.0 Pin Identification and Description

Pin Function	Description
I	CMOS input
IS	CMOS input Schmitt
O	CMOS output
I/O	CMOS bi-direct
OD	CMOS open drain
PCI-I	PCI input
PCI-O	PCI output
PCI-I/O	PCI bi-direct
PCI-3	PCI three-state

2.1. System Signals

Pin Name	Function	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
SYSCLK	I	88	Y20	--	Main system clock
$\overline{\text{RESET}}$	IS	136	L19	--	System reset
$\overline{\text{ERROR}}$[1]	OD	142	K19	--	Processor error mode indicator. This is an active low output.
$\overline{\text{WDOG}}$[1]	OD	145	J19	--	Watchdog indicator. This is an active low output.

Notes:
1. This pin is actively driven low and must be tied to V_{DD} through a pull-up resistor.

2.2 Address Bus

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
ADDR[0]	O	1	W5	low	Bit 0 of the address bus
ADDR[1]	O	2	Y5	low	Bit 1 of the address bus
ADDR[2]	O	4	W6	low	Bit 2 of the address bus
ADDR[3]	O	5	AA5	low	Bit 3 of the address bus
ADDR[4]	O	6	Y6	low	Bit 4 of the address bus
ADDR[5]	O	7	AB5	low	Bit 5 of the address bus
ADDR[6]	O	9	W7	low	Bit 6 of the address bus
ADDR[7]	O	10	AA6	low	Bit 7 of the address bus
ADDR[8]	O	11	Y7	low	Bit 8 of the address bus
ADDR[9]	O	12	AA7	low	Bit 9 of the address bus

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
ADDR[10]	O	16	AB6	low	Bit 10 of the address bus
ADDR[11]	O	17	W8	low	Bit 11 of the address bus
ADDR[12]	O	18	AB7	low	Bit 12 of the address bus
ADDR[13]	O	19	Y8	low	Bit 13 of the address bus
ADDR[14]	O	21	AA8	low	Bit 14 of the address bus
ADDR[15]	O	22	W9	low	Bit 15 of the address bus
ADDR[16]	O	23	AB8	low	Bit 16 of the address bus
ADDR[17]	O	24	Y9	low	Bit 17 of the address bus
ADDR[18]	O	26	W10	low	Bit 18 of the address bus
ADDR[19]	O	27	AB9	low	Bit 19 of the address bus
ADDR[20]	O	28	Y10	low	Bit 20 of the address bus
ADDR[21]	O	29	AA9	low	Bit 21 of the address bus
ADDR[22]	O	31	W11	low	Bit 22 of the address bus
ADDR[23]	O	32	AA10	low	Bit 23 of the address bus
ADDR[24]	O	33	Y11	low	Bit 24 of the address bus
ADDR[25]	O	34	AB10	low	Bit 25 of the address bus
ADDR[26]	O	38	AB11	low	Bit 26 of the address bus
ADDR[27]	O	39	AA11	low	Bit 27 of the address bus

2.3 Data Bus

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
DATA[0]	I/O	43	W12	high-Z	Bit 0 of the data bus
DATA[1]	I/O	45	W13	high-Z	Bit 1 of the data bus
DATA[2]	I/O	46	Y12	high-Z	Bit 2 of the data bus
DATA[3]	I/O	47	AA13	high-Z	Bit 3 of the data bus
DATA[4]	I/O	48	AA12	high-Z	Bit 4 of the data bus
DATA[5]	I/O	50	AB13	high-Z	Bit 5 of the data bus
DATA[6]	I/O	51	W14	high-Z	Bit 6 of the data bus

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
DATA[7]	I/O	52	AA14	high-Z	Bit 7 of the data bus
DATA[8]	I/O	53	Y13	high-Z	Bit 8 of the data bus
DATA[9]	I/O	57	W15	high-Z	Bit 9 of the data bus
DATA[10]	I/O	58	AB15	high-Z	Bit 10 of the data bus
DATA[11]	I/O	59	Y14	high-Z	Bit 11 of the data bus
DATA[12]	I/O	60	AB14	high-Z	Bit 12 of the data bus
DATA[13]	I/O	62	W16	high-Z	Bit 13 of the data bus
DATA[14]	I/O	63	AA18	high-Z	Bit 14 of the data bus
DATA[15]	I/O	64	Y15	high-Z	Bit 15 of the data bus
DATA[16]	I/O	66	AB16	high-Z	Bit 16 of the data bus
DATA[17]	I/O	67	AA15	high-Z	Bit 17 of the data bus
DATA[18]	I/O	68	AB17	high-Z	Bit 18 of the data bus
DATA[19]	I/O	69	AA16	high-Z	Bit 19 of the data bus
DATA[20]	I/O	71	AA19	high-Z	Bit 20 of the data bus
DATA[21]	I/O	72	W17	high-Z	Bit 21 of the data bus
DATA[22]	I/O	73	AB18	high-Z	Bit 22 of the data bus
DATA[23]	I/O	74	Y16	high-Z	Bit 23 of the data bus
DATA[24]	I/O	78	Y17	high-Z	Bit 24 of the data bus
DATA[25]	I/O	79	AA17	high-Z	Bit 25 of the data bus
DATA[26]	I/O	80	W18	high-Z	Bit 26 of the data bus
DATA[27]	I/O	81	AB19	high-Z	Bit 27 of the data bus
DATA[28]	I/O	83	Y19	high-Z	Bit 28 of the data bus
DATA[29]	I/O	84	AB20	high-Z	Bit 29 of the data bus
DATA[30]	I/O	85	Y18	high-Z	Bit 30 of the data bus
DATA[31]	I/O	86	AA20	high-Z	Bit 31 of the data bus

2.4 Check Bits

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
CB[0]	I/O	89	V19	high-Z	Bit 0 of EDAC checkbits
CB[1]	I/O	90	AA21	high-Z	Bit 1 of EDAC checkbits
CB[2]	I/O	91	Y21	high-Z	Bit 2 of EDAC checkbits
CB[3]	I/O	92	W19	high-Z	Bit 3 of EDAC checkbits
CB[4]	I/O	93	Y22	high-Z	Bit 4 of EDAC checkbits
CB[5]	I/O	94	W20	high-Z	Bit 5 of EDAC checkbits
CB[6]	I/O	96	W22	high-Z	Bit 6 of EDAC checkbits
CB[7]	I/O	97	W21	high-Z	Bit 7 of EDAC checkbits

2.5 Memory Control Signals

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
$\overline{\text{WRITE}}$	O	98	V21	high	PROM and I/O write enable strobe
$\overline{\text{OE}}$	O	99	U19	high	PROM and I/O output enable
$\overline{\text{IOS}}$	O	102	T20	high	I/O area chip select
$\overline{\text{ROMS[0]}}$	O	103	V22	high	PROM chip select
$\overline{\text{ROMS[1]}}$	O	104	U20	high	PROM chip select
$\overline{\text{RWE[0]}}$	O	105	U22	high	SRAM write enable strobe
$\overline{\text{RWE[1]}}$	O	108	T19	high	SRAM write enable strobe
$\overline{\text{RWE[2]}}$	O	109	T22	high	SRAM write enable strobe
$\overline{\text{RWE[3]}}$	O	110	T21	high	SRAM write enable strobe
$\overline{\text{RAMOE[0]}}$	O	111	V20	high	SRAM output enable
$\overline{\text{RAMOE[1]}}$	O	112	R21	high	SRAM output enable
$\overline{\text{RAMOE[2]}}$	O	113	R20	high	SRAM output enable
$\overline{\text{RAMOE[3]}}$	O	114	R22	high	SRAM output enable
$\overline{\text{RAMOE[4]}}$	O	115	R19	high	SRAM output enable
$\overline{\text{RAMS[0]}}$	O	117	P22	high	SRAM chip select
$\overline{\text{RAMS[1]}}$	O	118	P20	high	SRAM chip select

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
$\overline{\text{RAMS[2]}}$	O	119	P21	high	SRAM chip select
$\overline{\text{RAMS[3]}}$	O	120	P19	high	SRAM chip select
$\overline{\text{RAMS[4]}}$	O	123	N19	high	SRAM chip select
READ	O	139	K20	high	SRAM, PROM, and I/O read indicator
$\overline{\text{BEXC}}$	I	140	K22	--	Bus exception
$\overline{\text{BRDY}}$	I	141	K21	--	Bus ready

2.6 SDRAM

Pin Name Direction		Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
SDCLK	O	41	AB12	high	SDRAM clock
$\overline{\text{SDRAS}}$	O	124	N22	high	SDRAM row address strobe
$\overline{\text{SDCAS}}$	O	125	N20	high	SDRAM column address strobe
$\overline{\text{SDWE}}$	O	126	N21	high	SDRAM write enable
$\overline{\text{SDCS[0]}}$	O	128	M21	high	SDRAM chip select
$\overline{\text{SDCS[1]}}$	O	129	M22	high	SDRAM chip select
SDDQM[0]	O	131	L21	high	SDRAM data mask
SDDQM[1]	O	132	M20	high	SDRAM data mask
SDDQM[2]	O	133	L20	high	SDRAM data mask
SDDQM[3]	O	134	L22	high	SDRAM data mask

2.7 CAN 2.0 Interface

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
CAN_RXD[0]	I	146	J20	--	CAN receive data
CAN_TXD[0]	O	147	J22	high	CAN transmit data
CAN_RXD[1]	I	148	J21	--	CAN receive data
CAN_TXD[1]	O	150	H22	high	CAN transmit data

2.8 Debug Support Unit (DSU)

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
DSUACT	O	151	H19	low	DSUmode indicator
DSUBRE	I	152	H20	--	DSU break
DSUEN	I	153	G19	--	DSU enable
DSURX	I	154	G20	--	DSU UART receive data
DSUTX	O	155	G21	high	DSU UART transmit data

2.9 JTAG Interface

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
$\overline{\text{TRST}}$	I	156	F20	--	JTAG reset
$\overline{\text{TMS}}$	I	157	F21	--	JTAG test mode select
TCK	I	160	G22	--	JTAG clock
TDI	I	161	F22	--	JTAG test data input
TDO	O	162	F19	undef	JTAG test data output

2.10 Ethernet Interface

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
EMDC	O	163	E22	low	Ethernet media interface clock
ERX_CLK	I	166	D22	--	Ethernet RX clock
EMDIO	I/O	167	D20	high-Z	Ethernet media interface data
ERX_COL	I	168	E21	--	Ethernet collision error
ERX_CRS	I	169	E20	--	Ethernet carrier sense detect
ERX_DV	I	171	D21	--	Ethernet receiver data valid
ERX_ER	I	172	C21	--	Ethernet reception error
ERXD[0]	I	173	C22	--	Ethernet receive data
ERXD[1]	I	174	B21	--	Ethernet receive data
ERXD[2]	I	175	C20	--	Ethernet receive data

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
ERXD[3]	I	176	B20	--	Ethernet receive data
ETXD[0]	O	177	C19	low	Ethernet transmit data
ETXD[1]	O	178	C18	high	Ethernet transmit data
ETXD[2]	O	179	B18	low	Ethernet transmit data
ETXD[3]	O	180	B19	high	Ethernet transmit data
ETX_CLK	I	182	A19	--	Ethernet TX clock
ETX_EN	O	184	A18	low	Ethernet transmit enable
ETX_ER	O	185	A20	low	Ethernet transmit error. Always driven low.

2.11 General Purpose I/O

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
GPIO[0]	I/O	191	B17	high-Z	Bit 0 of general purpose I/O
GPIO[1]	I/O	192	C17	high-Z	Bit 1 of general purpose I/O
GPIO[2]	I/O	193	A17	high-Z	Bit 2 of general purpose I/O
GPIO[3]	I/O	194	D17	high-Z	Bit 3 of general purpose I/O
GPIO[4]	I/O	196	C16	high-Z	Bit 4 of general purpose I/O
GPIO[5]	I/O	197	D16	high-Z	Bit 5 of general purpose I/O
GPIO[6]	I/O	198	C15	high-Z	Bit 6 of general purpose I/O
GPIO[7]	I/O	199	D15	high-Z	Bit 7 of general purpose I/O
GPIO[8]	I/O	254	C7	high-Z	Bit 8 of general purpose I/O
GPIO[9]	I/O	255	B5	high-Z	Bit 9 of general purpose I/O
GPIO[10]	I/O	256	D7	high-Z	Bit 10 of general purpose I/O
GPIO[11]	I/O	257	A5	high-Z	Bit 11 of general purpose I/O
GPIO[12]	I/O	259	D6	high-Z	Bit 12 of general purpose I/O
GPIO[13]	I/O	260	C5	high-Z	Bit 13 of general purpose I/O
GPIO[14]	I/O	261	C6	high-Z	Bit 14 of general purpose I/O
GPIO[15]	I/O	262	D5	high-Z	Bit 15 of general purpose I/O

2.12 SpaceWire Interface

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
SPW_CLK	I	221	A11	--	SpaceWire clock
SPW_RXS[0]	I	205	A16	--	SpaceWire receive strobe
SPW_RXD[0]	I	206	A15	--	SpaceWire receive data
SPW_TXS[0]	O	207	B16	low	SpaceWire transmit strobe
SPW_TXD[0]	O	208	B15	low	SpaceWire transmit data
SPW_RXS[1]	I	212	A14	--	SpaceWire receive strobe
SPW_RXD[1]	I	213	A13	--	SpaceWire receive data
SPW_TXS[1]	O	214	B14	low	SpaceWire transmit strobe
SPW_TXD[1]	O	215	B13	low	SpaceWire transmit data
SPW_RXS[2]	I	234	A9	--	SpaceWire receive strobe
SPW_RXD[2]	I	235	A8	--	SpaceWire receive data
SPW_TXS[2]	O	236	B9	low	SpaceWire transmit strobe
SPW_TXD[2]	O	237	B8	low	SpaceWire transmit data
SPW_RXS[3]	I	242	A7	--	SpaceWire receive strobe
SPW_RXD[3]	I	243	A6	--	SpaceWire receive data
SPW_TXS[3]	O	244	B7	low	SpaceWire transmit strobe
SPW_TXD[3]	O	245	B6	low	SpaceWire transmit data

2.13 UART Interface

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
RXD	I	223	C12	--	UART receive data
TXD	O	224	C11	high	UART transmit data

2.14 PCI Address and Data Bus

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
PCI_AD[0]	PCI-I/O	266	AA2	high-Z	Bit 0 of PCI address and data bus

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
PCI_AD[1]	PCI-I/O	267	AA3	high-Z	Bit 1 of PCI address and data bus
PCI_AD[2]	PCI-I/O	268	Y1	high-Z	Bit 2 of PCI address and data bus
PCI_AD[3]	PCI-I/O	269	Y2	high-Z	Bit 3 of PCI address and data bus
PCI_AD[4]	PCI-I/O	270	Y3	high-Z	Bit 4 of PCI address and data bus
PCI_AD[5]	PCI-I/O	272	W1	high-Z	Bit 5 of PCI address and data bus
PCI_AD[6]	PCI-I/O	273	W2	high-Z	Bit 6 of PCI address and data bus
PCI_AD[7]	PCI-I/O	274	W3	high-Z	Bit 7 of PCI address and data bus
PCI_AD[8]	PCI-I/O	279	V2	high-Z	Bit 8 of PCI address and data bus
PCI_AD[9]	PCI-I/O	280	V3	high-Z	Bit 9 of PCI address and data bus
PCI_AD[10]	PCI-I/O	281	U1	high-Z	Bit 10 of PCI address and data bus
PCI_AD[11]	PCI-I/O	284	U2	high-Z	Bit 11 of PCI address and data bus
PCI_AD[12]	PCI-I/O	285	U3	high-Z	Bit 12 of PCI address and data bus
PCI_AD[13]	PCI-I/O	286	T1	high-Z	Bit 13 of PCI address and data bus
PCI_AD[14]	PCI-I/O	287	R2	high-Z	Bit 14 of PCI address and data bus
PCI_AD[15]	PCI-I/O	288	R1	high-Z	Bit 15 of PCI address and data bus
PCI_AD[16]	PCI-I/O	305	J1	high-Z	Bit 16 of PCI address and data bus
PCI_AD[17]	PCI-I/O	306	K2	high-Z	Bit 17 of PCI address and data bus
PCI_AD[18]	PCI-I/O	307	K1	high-Z	Bit 18 of PCI address and data bus
PCI_AD[19]	PCI-I/O	308	G1	high-Z	Bit 19 of PCI address and data bus
PCI_AD[20]	PCI-I/O	309	H3	high-Z	Bit 20 of PCI address and data bus
PCI_AD[21]	PCI-I/O	310	H2	high-Z	Bit 21 of PCI address and data bus
PCI_AD[22]	PCI-I/O	312	F1	high-Z	Bit 22 of PCI address and data bus
PCI_AD[23]	PCI-I/O	313	F2	high-Z	Bit 23 of PCI address and data bus
PCI_AD[24]	PCI-I/O	317	E1	high-Z	Bit 24 of PCI address and data bus
PCI_AD[25]	PCI-I/O	318	E2	high-Z	Bit 25 of PCI address and data bus
PCI_AD[26]	PCI-I/O	321	F3	high-Z	Bit 26 of PCI address and data bus
PCI_AD[27]	PCI-I/O	322	D1	high-Z	Bit 27 of PCI address and data bus
PCI_AD[28]	PCI-I/O	323	D2	high-Z	Bit 28 of PCI address and data bus
PCI_AD[29]	PCI-I/O	324	E3	high-Z	Bit 29 of PCI address and data bus
PCI_AD[30]	PCI-I/O	326	D3	high-Z	Bit 30 of PCI address and data bus

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
PCI_AD[31]	PCI-I/O	327	C1	high-Z	Bit 31 of PCI address and data bus

2.15 PCI Control Signals

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
$\overline{\text{PCI_RST}}$	PCI-I	265	C3	--	PCI reset input
PCI_CLK	PCI-I	293	C2	--	PCI clock input
PCI_C/$\overline{\text{BE}}$[0]	PCI-I/O	275	V1	high-Z	PCI bus command and byte enable
PCI_C/$\overline{\text{BE}}$[1]	PCI-I/O	289	P2	high-Z	PCI bus command and byte enable
PCI_C/$\overline{\text{BE}}$[2]	PCI-I/O	302	H1	high-Z	PCI bus command and byte enable
PCI_C/$\overline{\text{BE}}$[3]	PCI-I/O	316	G2	high-Z	PCI bus command and byte enable
PCI_PAR	PCI-I/O	290	P1	high-Z	PCI parity checkbit
$\overline{\text{PCI_FRAME}}$[1]	PCI-3	301	L1	high-Z	PCI cycle frame indicator
$\overline{\text{PCI_IRDY}}$[1]	PCI-3	300	L2	high-Z	PCI initiator ready indicator
$\overline{\text{PCI_TRDY}}$[1]	PCI-3	299	M1	high-Z	PCI target ready indicator
$\overline{\text{PCI_STOP}}$[1]	PCI-3	295	N1	high-Z	PCI target stop request
$\overline{\text{PCI_DEVSEL}}$[1]	PCI-3	296	M2	high-Z	PCI device select
PCI_IDSEL	PCI-I	315	G3	--	PCI initialization device select
$\overline{\text{PCI_REQ}}$	PCI-O	329	A4	high-Z	PCI request to arbiter in point to point configuration
$\overline{\text{PCI_GNT}}$	PCI-I	328	B2	--	PCI bus access indicator in point to point configuration
$\overline{\text{PCI_HOST}}$	PCI-I	330	AB3	--	PCI host enable input (Connect to $\overline{\text{SYSEN}}$ in PCI bus)

Notes:
1. This pin must be tied to V_{DD} through a pull-up resistor as specified in the PCI Local Bus Specification Revision 2.1 Section 4.3.3.

2.16 PCI Arbiter

Pin Name	Direction	Pin Number		Reset Value	Description
		352 CQFP	484 CLGA		
$\overline{\text{PCI_ARB_REQ[0]}}$	PCI-I	331	B4	--	PCI arbiter bus request
$\overline{\text{PCI_ARB_REQ[1]}}$	PCI-I	332	AB4	--	PCI arbiter bus request
$\overline{\text{PCI_ARB_REQ[2]}}$	PCI-I	337	Y4	--	PCI arbiter bus request
$\overline{\text{PCI_ARB_REQ[3]}}$	PCI-I	339	T3	--	PCI arbiter bus request
$\overline{\text{PCI_ARB_REQ[4]}}$	PCI-I	343	P3	--	PCI arbiter bus request
$\overline{\text{PCI_ARB_REQ[5]}}$	PCI-I	344	M3	--	PCI arbiter bus request
$\overline{\text{PCI_ARB_REQ[6]}}$	PCI-I	348	K3	--	PCI arbiter bus request
$\overline{\text{PCI_ARB_REQ[7]}}$	PCI-I	350	C4	--	PCI arbiter bus request
$\overline{\text{PCI_ARB_GNT[0]}}$	PCI-O	333	B3	high-Z	PCI arbiter bus grant
$\overline{\text{PCI_ARB_GNT[1]}}$	PCI-O	336	AA4	high-Z	PCI arbiter bus grant
$\overline{\text{PCI_ARB_GNT[2]}}$	PCI-O	338	W4	high-Z	PCI arbiter bus grant
$\overline{\text{PCI_ARB_GNT[3]}}$	PCI-O	342	R3	high-Z	PCI arbiter bus grant
$\overline{\text{PCI_ARB_GNT[4]}}$	PCI-O	345	N3	high-Z	PCI arbiter bus grant
$\overline{\text{PCI_ARB_GNT[5]}}$	PCI-O	347	L3	high-Z	PCI arbiter bus grant
$\overline{\text{PCI_ARB_GNT[6]}}$	PCI-O	349	J3	high-Z	PCI arbiter bus grant
$\overline{\text{PCI_ARB_GNT[7]}}$	PCI-O	351	A3	high-Z	PCI arbiter bus grant

2.17 Power and Ground Pins (352 CQFP)

Pin Name	Pin Number		Description
	352 CQFP	484 CLGA	
V_{DD}	3, 15, 25, 35, 40, 44, 54, 65, 75, 87, 95, 106, 116, 127, 135, 137, 149, 158, 170, 181, 190, 200, 203, 211, 217, 222, 226, 229, 233, 241, 247, 251, 263, 271, 283, 292, 294, 304, 314, 325, 335, 346	B1, B10, B12, B22, E7, E9, E14, E16, F6, F10, F13, F17, G5, G9, G14, H6, H8, H10, H13, H15, J7, J16, J18, K5, K8, K15, K17, L6, M6, N5, N8, N15, N17, P7, P16, P18, R6, R8, R10, R13, R15, T5, T9, T14, U6, U9, U11, U12, U14, U17, V10, V13, AA1, AA22	I/O supply voltage

Pin Name	Pin Number		Description
	352 CQFP	484 CLGA	
V_{SS}	8, 20, 30, 42, 49, 61, 70, 82, 107, 130, 138, 159, 183, 187, 195, 204, 216, 219, 225, 230, 238, 246, 250, 258, 264, 278, 282, 303, 311, 334, 352	A1, A12, A22, B11, C8, C10, C13, D4, D9, D14, D18, D19, E4, E6, E10, E13, E17, E19, F4, G4, G8, G11, G12, G15, G17, H4, H7, H16, H18, J2, J4, J9, J14, K4, K10, K13, L7, L11, L12, L17, M7, M11, M12, M17, N4, N10, N13, P4, P9, P14, R4, R7, R16, R18, T2, T4, T8, T15, T17, U4, U10, U13, V4, V5, V8, V11, V12, V15, V18, AB1, AB22	I/O supply ground (pins 187/D19 and 264/D4 must be tied to V_{SS})
V_{DDC}	14, 37, 56, 77, 101, 122, 144, 165, 186, 188, 201, 209, 220, 227, 232, 239, 249, 252, 276, 297, 319, 340	A2, A21, D10, D13, E5, E11, E12, E18, F8, F15, G7, G10, G13, G16, G18, H5, H9, H11, H12, H14, H17, J6, J8, J15, K7, K16, L4, L8, L15, L18, M4, M8, M15, M18, N7, N16, P6, P8, P15, R5, R9, R11, R12, R14, R17, T7, T10, T13, T16, T18, U8, U15, V6, V17, AB2, AB21	Core supply voltage
V_{SSC}	13, 36, 55, 76, 100, 121, 143, 164, 189, 202, 210, 218, 228, 231, 240, 253, 277, 298, 320, 341	A10, C9, C14, D11, D12, E8, E15, F5, F7, F9, F11, F12, F14, F16, F18, G6, H21, J5, J10, J11, J12, J13, J17, K6, K9, K11, K12, K14, K18, L5, L9, L10, L13, L14, L16, M5, M9, M10, M13, M14, M16, M19, N6, N9, N11, N12, N14, N18, P5, P10, P11, P12, P13, P17, T6, T11, T12, U5, U7, U16, U18, U21, V7, V9, V14, V16	Core supply ground
N/C	248	D8	This pin must be left floating
Unused	291	N2	This pin must be tied to V_{DD} through a 10k pull-up resistor

3.0 AC and DC Electrical Specifications

3.1 Absolute Maximum Ratings[1]

Symbol	Description		Min	Max	Units
V_{DDC}	Core supply voltage		-0.3	3.6	V
V_{DD}	I/O supply voltage		-0.3	4.3	V
V_{IN}	Input voltage any pin		V_{SS} - 0.3	V_{DD} + 0.3	V
P_D[2]	Maximum power dissipation permitted @ $T_C = 105^oC$		--	9	W
T_J[3]	Junction temperature		--	150	^oC
Θ_{JC}	Thermal resistance, junction to case	352 CQFP	--	5	$^oC/W$
		484 CLGA/CCGA/CBGA	--	5	
T_{STG}	Storage temperature		-65	150	^oC
ESD_{HBM}	ESD protection (human body model) Class 2		2000	--	V

Notes:

1. Stresses greater than those listed in the following table can result in permanent damage to the device. These parameters cannot be violated.
2. Per MIL-STD-883, Method 1012, Section 3.4.1, PD = $(T_J(max)-T_c(max))/\Theta_{JC}$
3. Maximum junction temperature may be increased to 175^oC during burn-in and steady-static life testing.

3.2 Recommended Operating Conditions

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V; T_C = -40°C to 105°C)

Symbol	Description	Min	Max	Units
V_{DDC}	Core supply voltage	2.3	2.7	V
V_{DD}	I/O supply voltage	3.0	3.6	V
V_{IN}	Input voltage any pin	0	V_{DD}	V
T_C	Case operating temperature	-40	105	°C
t_R	Rise time, all CMOS and PCI inputs	--	20	ns
t_F	Fall time, all CMOS and PCI inputs	--	20	ns

3.3 Power Supply Operating Characteristics (pre- and post-radiation)

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V; T_C = -40°C to 105°C)

Symbol	Description	Conditions		Max	Units
I_{DDC}[1,2]	Active core power supply current	V_{DDC} = 2.7V, V_{DD}= 3.6V For 25MHz ≤ f_{SYSCLK} ≤ 66MHz All other clock inputs running at f_{SYSCLK}		27	mA/MHz
I_{DD}[1,3]	Active I/O power supply current	V_{DDC} = 2.7, V_{DD} = 3.6V For 25MHz ≤ f_{SYSCLK} ≤ 66MHz All other clock inputs running at f_{SYSCLK}		0.75	mA/MHz
I_{DDCS}	Standby core power supply current	V_{DDC} = 2.7V, V_{DD}= 3.6V f_{SYSCLK} = 0MHz, f_{ETH_CLK} = 0MHz f_{PCI_CLK} = 0MHz, f_{SPW_CLK} = 0MHz	T_C = -40°C and 25°C	2	mA
			T_C = 105°C	20	
I_{DDS}	Standby I/O power supply quiescent current	V_{DDC} = 2.7V, V_{DD} = 3.6V f_{SYSCLK} = 0MHz, f_{ETH_CLK} = 0MHz, f_{PCI_CLK} = 0MHz, f_{SPW_CLK} = 0MHz		0.75	mA
I_{PDC}[4]	Core power supply current power-down mode	V_{DDC} = 2.7V, V_{DD} = 3.6V f_{SYSCLK} = 66MHz, f_{ETH_CLK} = 0MHz f_{PCI_CLK} = 0MHz, f_{SPW_CLK} = 0MHz		2.75	mA/MHz
			300k post rad	5	
I_{PD}[4]	I/O power supply current power-down mode	V_{DDC} = 2.7V, V_{DD} = 3.6V f_{SYSCLK} = 66MHz, f_{ETH_CLK} = 0MHz f_{PCI_CLK} = 0MHz, f_{SPW_CLK} = 0MHz		0.75	mA/MHz

Notes:

1. During this measurement the processor is executing the Dhrystone benchmark.
2. This measurement includes the contribution due to I_{DDCS}.
3. This measurement includes the contribution due to I_{DDS}.
4. Power-down mode is entered by performing a WRASR instruction wr %g0, %asr19.

3.4 DC Characteristics for LVCMOS3 Inputs (pre- and post-radiation)

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V; T_C = -40°C to 105°C)

Symbol	Description	Conditions		Min	Max	Units
V_{IH}	High-level input voltage			$0.7V_{DD}$	--	V
V_{IL}	Low-level input voltage			--	$0.3V_{DD}$	V
V_{T+}	Positive going threshold voltage for Schmitt inputs			--	$0.7V_{DD}$	V
V_{T-}	Negative going threshold voltage for Schmitt inputs			$0.3V_{DD}$	--	V
V_H	Hysteresis voltage for Schmitt inputs			0.4	--	V
I_{IN}	Input leakage current	$V_{IN} = V_{DD}$		--	1	µA
		$V_{IN} = V_{SS}$		-1	--	
C_{IN}[1]	Input pin capacitance	*f* = 1MHz; V_{DD} = 0V, V_{DDC} = 0V	352 CQFP	--	19	pF
			484 CLGA	--	16	

Notes:

1. Capacitance is measured for initial qualification and when design changes might affect the input/output capacitance.

3.5 DC Characteristics for LVCMOS3 Outputs (pre- and post-radiation)

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V; T_C = -40°C to 105°C)

Symbol	Description	Conditions		Min	Max	Units
V_{OH}[1]	High-level output voltage	I_{OH} = -100µA		V_{DD}-0.25	--	V
		I_{OH} = -12mA		2.4	--	
V_{OL}	Low-level output voltage	I_{OL} = 100µA		--	0.25	V
		I_{OL} = 12mA		--	0.4	
I_{OZ}	Three-state output current	$V_O = V_{DD}$		-10	10	µA
		$V_O = V_{SS}$		-10	10	
I_{OS}[2]	Short-circuit output current	$V_O = V_{DD}$; V_{DD} = 3.6V		--	130	mA
		$V_O = V_{SS}$; V_{DD} = 3.6V		-65	--	
C_{OUT}[3]	Output pin capacitance	*f* = 1MHz; V_{DD} = 0V, V_{DDC} = 0V	352 CQFP	--	16	pF
			484 CLGA	--	16	

Notes:
1. Except open-drain output.
2. Supplied as a design limit. Neither guaranteed nor tested.
3. Capacitance is measured for initial qualification and when design changes might affect the input/output capacitance.

3.6 AC Electrical Characteristics for LVCMOS3 Inputs and Outputs (pre- and post-radiation)

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V; T_C = -40°C to 105°C)

Symbol	Description	Conditions	Min	Max	Units
f_{CLK}	System clock frequency		--	66	MHz
t_{HIGH}	System clock high time		6.67	--	ns
t_{LOW}	System clock low time		6.67	--	ns
t_{DSD}[1]	System clock to SDRAM clock propagation delay		2	5	ns
t_{RSD}[2]	SDRAM clock rise time	f_{CLK} = 66MHz V_O transitioning between V_{OH} (min) and V_{OL} (max)	--	2	ns
t_{FSD}[2]	SDRAM clock fall time	f_{CLK} = 66MHz V_O transitioning between V_{OH} (min) and V_{OL} (max)	--	2	ns
t_{JCCSD}[2]	SDRAM clock cycle-cycle jitter	f_{CLK} = 66MHz	--	500	ps

Notes:
1. Tested as shown in Figure 14.
2. Supplied as a design limit. Neither guaranteed nor tested.

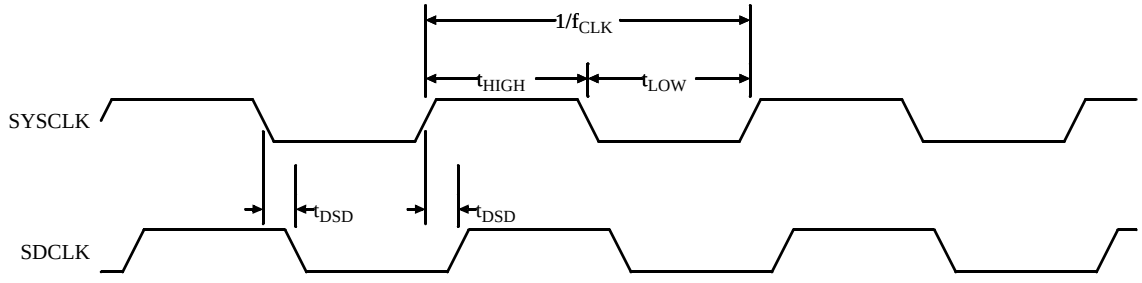


Figure 2. System Clock and SDCLK Timing Diagram

3.7 DC Electrical Characteristics for PCI Inputs (pre- and post-radiation)

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V; T_C = -40°C to 105°C)

Symbol	Description	Conditions		Min	Max	Units
V_{IH}	High-level input voltage			$0.5V_{DD}$	--	V
V_{IL}	Low-level input voltage			--	$0.3V_{DD}$	V
I_{IN}	Input leakage current	$V_{IN} = V_{DD}$		--	10	µA
		$V_{IN} = V_{SS}$		-10	--	
C_{IN}[1]	Input pin capacitance	*f* = 1MHz; V_{DD} = 0V, V_{DDC} = 0V	352 CQFP	--	19	pF
			484 CLGA	--	22	

Notes:
1. Capacitance is measured for initial qualification and when design changes might affect the input/output capacitance.

3.8 DC Electrical Characteristics for PCI Outputs (pre- and post-radiation)

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V; T_C = -40°C to 105°C)

Symbol	Description	Conditions		Min	Max	Units
V_{OH}	High-level output voltage	I_{OH} = -500µA		$0.9V_{DD}$	--	V
V_{OL}	Low-level output voltage	I_{OL} = 1500µA		--	$0.1V_{DD}$	V
I_{OZ}	Three-state output current	$V_O = V_{DD}$		-10	10	µA
		$V_O = V_{SS}$		-10	10	
I_{OS}[1]	Short-circuit output current	$V_O = V_{DD}$; V_{DD} = 3.6V		--	270	mA
		$V_O = V_{SS}$; V_{DD} = 3.6V		-130	--	
C_{OUT}[2]	Output pin capacitance	*f* = 1MHz; V_{DD} = 0V, V_{DDC} = 0V	352 CQFP	--	19	pF
			484 CLGA	--	22	

Notes:
1. Supplied as a design guideline. Neither guaranteed nor tested.
2. Capacitance is measured for initial qualification and when design changes might affect the input/output capacitance.

3.9 AC Electrical Characteristics for PCI Inputs (pre- and post-radiation)

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V; T_C = -40°C to 105°C)

Symbol	Description	Conditions	Min	Max	Units
f_{PCI_CLK}	PCI clock frequency		--	33	MHz
t_{HIGH}	PCI clock high time		11	--	ns
t_{LOW}	PCI clock low time		11	--	ns

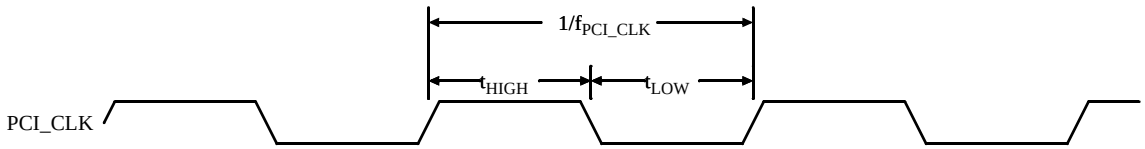


Figure 3. PCI Clock Timing Diagram

4.0 Timing Specifications

4.1 Power Sequencing and Reset

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V; T_C = -40°C to 105°C)

Symbol	Description	Conditions	Min	Max	Units
t_{VCD}[1]	V_{DD} valid to V_{DDC} delay	$V_{DD} \geq$ 3.0V; $V_{DDC} \geq$ 2.30V	0	--	ns
t_{VHBZ}[1]	V_{DD} valid to control signals high-Z ($\overline{WRITE}$, $\overline{OE}$, $\overline{IOS}$, $\overline{ROMS[1:0]}$, $\overline{RWE[3:0]}$, $\overline{RAMOE\ [4:0]}$, READ $\overline{SDWE}$, and $\overline{SDCS[1:0]}$) V_{DD} valid to outputs high-Z ([DATA[31:0], CB[7:0], and GPIO[15:0])	$V_{DD} \geq$ 1.5V; V_{DDC} = 0V	--	4	t_{CLK}
t_{CHBV}[1]	V_{DDC} valid to control signals valid-inactive ($\overline{WRITE}$, $\overline{OE}$, $\overline{IOS}$, $\overline{ROMS[1:0]}$, $\overline{RWE[3:0]}$, $\overline{RAMOE\ [4:0]}$, READ $\overline{SDWE}$, and $\overline{SDCS[1:0]}$)	$V_{DD} \geq$ 3.0V; $V_{DDC} \geq$ 2.30V	--	4	t_{CLK}
t_{RESET1}[1]	V_{DDC} valid to $\overline{RESET}$ deassert	$V_{DDC} \geq$ 2.30V	4	--	t_{CLK}
t_{RESET2}	$\overline{RESET}$ deasserted to outputs valid-active ($\overline{ROMS[0]}$ and $\overline{OE}$)		--	12	t_{CLK}
t_{RESET3}[2]	$\overline{RESET}$ asserted to control signals valid-inactive ($\overline{WRITE}$, $\overline{OE}$, $\overline{IOS}$, $\overline{ROMS[1:0]}$, $\overline{RWE[3:0]}$, $\overline{RAMOE\ [4:0]}$, READ $\overline{SDWE}$, and $\overline{SDCS[1:0]}$) $\overline{RESET}$ asserted to outputs high-Z (DATA[31:0], CB[7:0], and GPIO[15:0])		--	4	t_{CLK}

Notes:
1. Guaranteed by design.
2. Guaranteed by design for control signals.

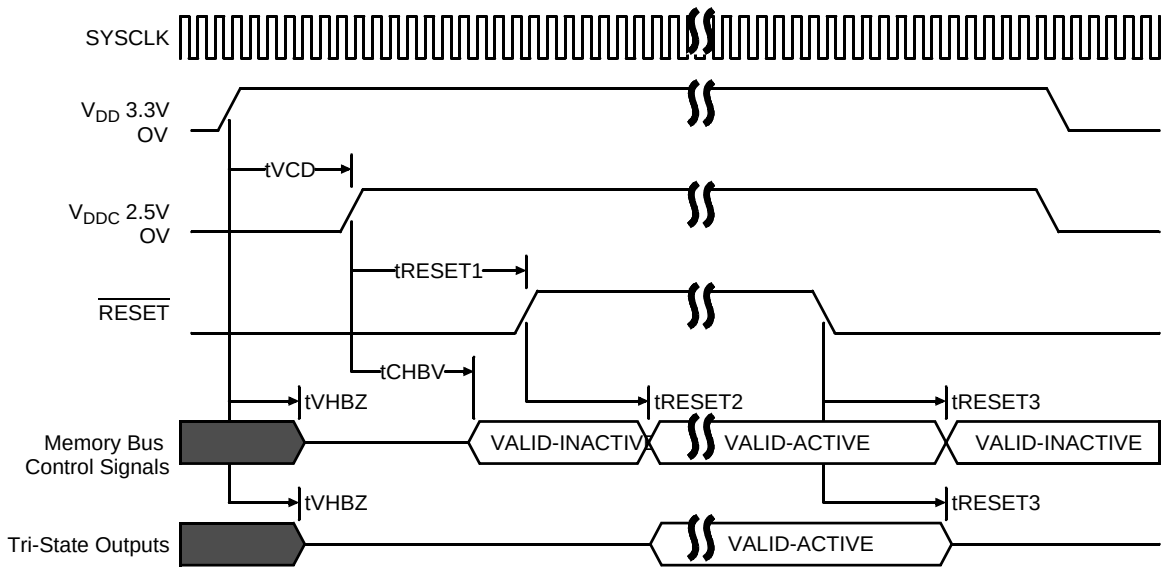


Figure 4. Power Sequencing and Reset Timing Diagram

4.1.1. Power Sequencing

Proper power sequencing of the UT699 is achieved by bringing up V_{DD} to its recommended minimum operating voltage of 3.0V, and then delaying t_{VCD} clock cycles before bringing up the V_{DDC} supply. **If power is applied to the V_{DDC} supply pins while V_{DD} is less than 3.0V, excessive current or damage to the device could occur**.

4.1.2 Bus Control and Bi-Direct Fail-Safe Circuitry

In order to prevent bus contention on the external memory interface while V_{DDC} is ramping up, the UT699 has functionality to ensure that the bi-direct and memory bus control signals described in Section 4.1 will be in a high-Z state t_{VHBZ} clock cycles after V_{DD} reaches 1.5V. The core logic will then put these signals into their valid-inactive states t_{CHBV} clock cycles after V_{DDC} reaches 2.3V.

It is recommended that users place pull-up resistors on the indicated output enable, write enable, and chip select pins, and a pull-down resistor on the READ pin, if there will be a significant delay between when V_{DD} and V_{DDC} reach their recommended operating voltages. This will prevent bus capacitance or transients from inadvertently placing these pins in an active state, which could result in external memory devices driving the address and data buses.

4.1.3 Reset Circuitry

The reset circuitry is controlled by the core logic; therefore, the circuitry is functional only after V_{DDC} reaches its minimum operating voltage of 2.3V. After V_{DDC} is stable, the system must continue to assert $\overline{\text{RESET}}$ for a minimum of t_{RESET1} clock cycles before it can be de-asserted. Asserting $\overline{\text{RESET}}$ for less time could result in the $\overline{\text{RESET}}$ signal not being recognized.

The UT699 will begin fetching code from external memory no more than t_{RESET2} clock cycles after $\overline{\text{RESET}}$ is de-asserted. Control signals $\overline{\text{ROMS[0]}}$ and $\overline{\text{OE}}$ will be driven to their valid-active states in order for the UT699 to begin fetching code from PROM. During normal operation, the indicated bus control signals will go to a valid-inactive state, and the bi-directs will go to a high-Z state, within t_{RESET3} clock cycles after the assertion of $\overline{\text{RESET}}$.

4.1.4 Programming Pins GPIO[2:0]

Data on pins GPIO[2:0] are latched on the rising edge of reset. The states of these pins determine the data width of the PROM area, and enable EDAC for the PROM area. Chapter 3 of the User's Manual describes the value of these inputs to achieve the required operation.

In order for the state of GPIO[2:0] to be properly latched, it is recommended to place pull-up or pull-down resistors on these pins to ensure that the setup and hold timing is met. The states of these pins should be statically set prior to the rising edge of $\overline{\text{RESET}}$.

4.2 Output Timing Characteristics for Memory Interface, $\overline{\text{ERROR}}$, and $\overline{\text{WDOG}}$

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V; T_C = -40°C to 105°C)

Symbol	Description	Min	Max	Units
t1[1]	SDCLK↑ to output valid (ADDR[27:0], $\overline{\text{WRITE}}$, $\overline{\text{OE}}$, $\overline{\text{IOS}}$, $\overline{\text{ROMS[1:0]}}$, $\overline{\text{RWE [3:0]}}$, $\overline{\text{RAMOE [4:0]}}$, $\overline{\text{RAMS[4:0]}}$, READ, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, $\overline{\text{SDCS[1:0]}}$, and SDDQM[3:0])	2	8	ns
t2[1]	SDCLK↑ to output valid (DATA[31:0] and CB[7:0])	2	8	ns
t3[1,2]	SDCLK↑ to output high-Z (DATA[31:0] and CB[7:0])	2	8	ns
t4[1]	SDCLK↑ to signal low ($\overline{\text{ERROR}}$ and $\overline{\text{WDOG}}$)	2	9	ns
t8[1,2]	$\overline{\text{WRITE}}$↑ or $\overline{\text{RWE[3:0]}}$↑ to output high-Z (DATA [31:0] and CB[7:0])	2.5	-	ns
t9[1]	Skew from first memory output signal transition to last memory output signal transition	-	2	ns

Notes:

1. All outputs are measured using the load conditions shown in Figure 15.
2. High-Z defined as +/-300mV change from steady state.

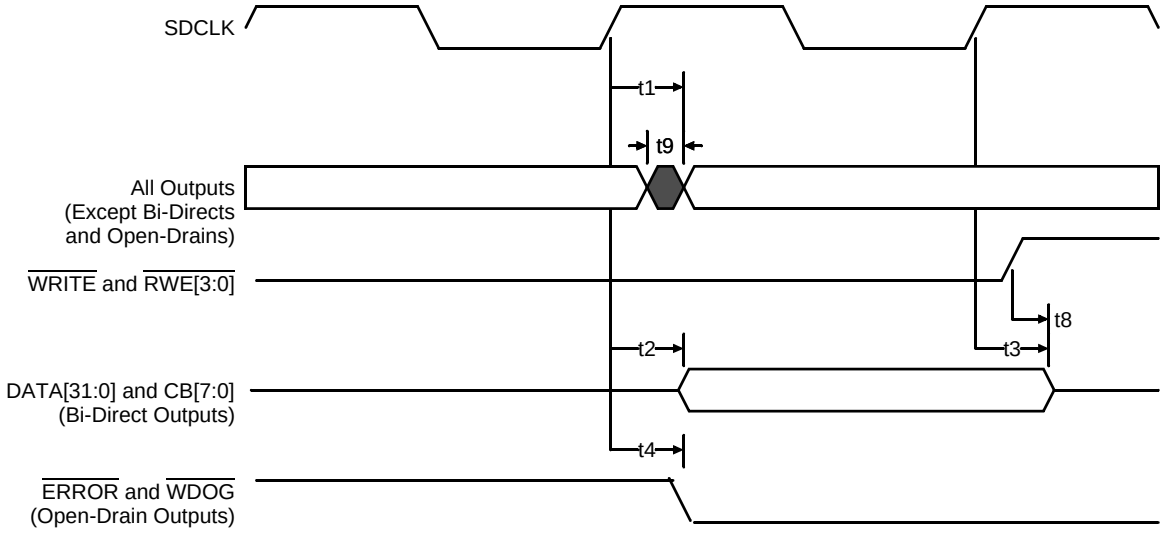


Figure 5. Memory Interface, $\overline{\text{ERROR}}$, and $\overline{\text{WDOG}}$ Output Timing Diagram

4.3 Input Timing Characteristics for Memory Interface

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V; T_C = -40°C to 105°C)

Symbol	Description	Min	Max	Units
t5[1]	Setup time to SDCLK↑ (DATA[31:0], CB[6:0], $\overline{\text{BEXC}}$, and synchronous $\overline{\text{BRDY}}$)	0	-	ns
t6[1]	Hold time from SDCLK↑ (DATA[31:0], CB[6:0], $\overline{\text{BEXC}}$, and synchronous $\overline{\text{BRDY}}$)	1	-	ns
t7[2]	Asynchronous $\overline{\text{BRDY}}$ pulse width	1.5	-	t_{CLK}

Notes:
1. CB[7] is not used for EDAC and is not tested
2. Guaranteed by design.
.

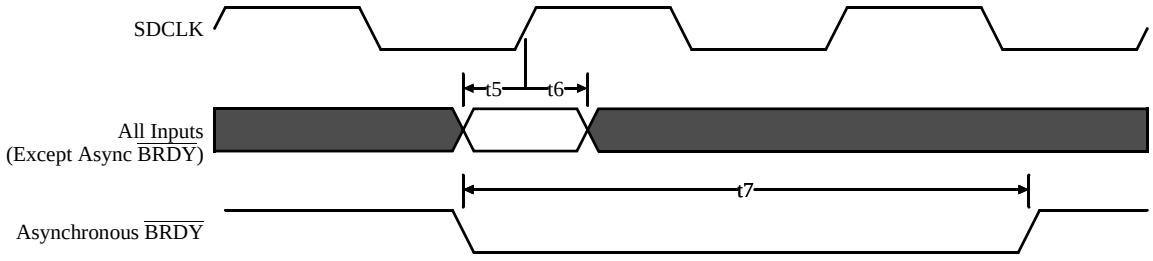


Figure 6. Memory Interface Input Timing Diagram

4.4 Timing Characteristics for General Purpose Input / Output (GPIO)

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V; T_C = -40°C to 105°C)

Symbol	Description	Min	Max	Units
t10[1]	SDCLK↑ to GPIO output valid (GPIO[15:0])	2	8	ns

Notes:
1. All outputs are measured using the load conditions shown in Figure 15.

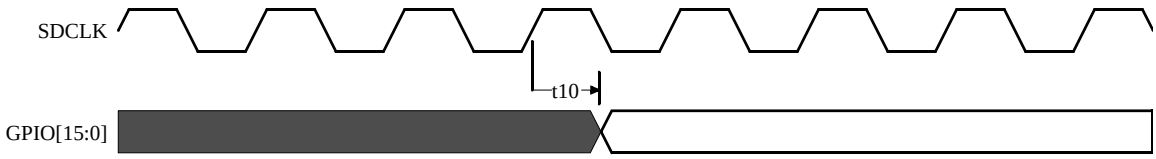


Figure 7. General Purpose I/O Timing Diagram

4.5 Timing Characteristics SpaceWire Interface

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V; T_C = -40°C to 105°C)

Symbol	Description	Min	Max	Units
t11[1]	SPW_CLK period	5	--	ns
t12[2]	SPW_CLK↑ to data delay (SPW_TXD[3:0])	3	7	ns
t13[2]	SPW_CLK↑ to strobe delay (SPW_TXS[3:0])	3	7	ns
t14[3]	Transmit data and strobe bit width variation (SPW_TXD[3:0] and SPW_TXS[3:0])	UI-600[4]	UI+600	ps
t15[3]	Receive data and strobe bit width (SPW_RXD[3:0] and SPW_RXS[3:0])	2.5	--	ns
t16	Receive data and strobe edge separation (SPW_RXD[3:0] and SPW_RXS[3:0])	2.5	--	ns

Notes:
1. The SPW_CLK frequency must be less than 4x the SYS_CLK frequency. For example, if SPW_CLK is running at 200MHz, the SYS_CLK frequency must be greater than 50MHz.
2. All outputs are measured using the load conditions shown in Figure 15.
3. Applies to both high pulse and low pulse.
4. A unit interval (UI) is defined as the nominal, or ideal, bit width.

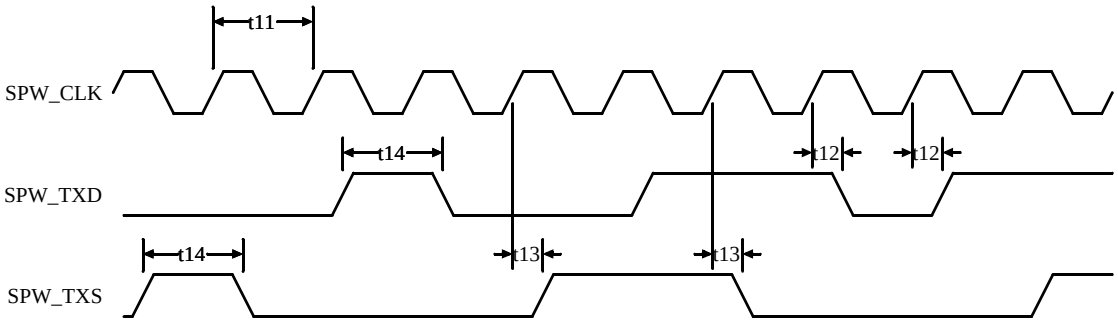


Figure 8. SpaceWire Transmit Timing Diagram

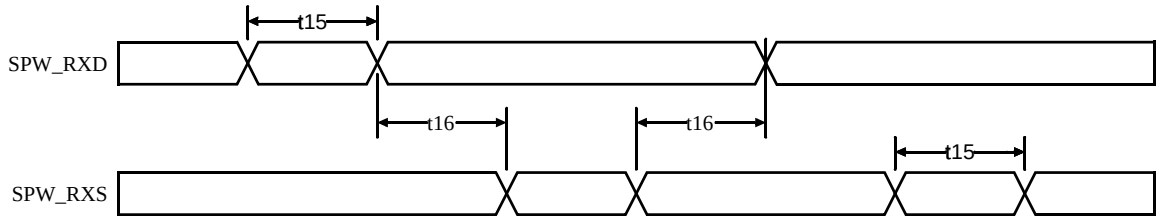


Figure 9. SpaceWire Receive Timing Diagram

4.6 Timing Characteristics for PCI Interface

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V; T_C = -40°C to 105°C)

Symbol	Description	Min	Max	Units
t17[1]	PCI_CLK↑ to output valid (PCI_AD[31:0], PCI_C/$\overline{BE}$[3:0], PCI_PAR, $\overline{PCI_FRAME}$, $\overline{PCI_IRDY}$, $\overline{PCI_TDRY}$, $\overline{PCI_STOP}$, $\overline{PCI_DEVSEL}$, $\overline{PCI_REQ}$, and $\overline{PCI_ARB_GNT[7:0]}$)	2	13	ns
t18[1,2]	PCI_CLK↑ to output valid from high-Z (PCI_AD[31:0], PCI_C/$\overline{BE}$[3:0], PCI_PAR, $\overline{PCI_FRAME}$, $\overline{PCI_IRDY}$, $\overline{PCI_TDRY}$, $\overline{PCI_STOP}$, and $\overline{PCI_DEVSEL}$)	2	13	ns
t19[1,2]	PCI_CLK↑ to output high-Z (PCI_AD[31:0], PCI_C/$\overline{BE}$[3:0], PCI_PAR, $\overline{PCI_FRAME}$, $\overline{PCI_IRDY}$, $\overline{PCI_TDRY}$, $\overline{PCI_STOP}$, and $\overline{PCI_DEVSEL}$)	--	14	ns
t20	Setup time to PCI_CLK↑ (PCI_AD[31:0], PCI_C/$\overline{BE}$[3:0], PCI_PAR, $\overline{PCI_FRAME}$, $\overline{PCI_IRDY}$, $\overline{PCI_TDRY}$, $\overline{PCI_STOP}$, $\overline{PCI_DEVSEL}$, PCI_IDSEL, $\overline{PCI_GNT}$, and $\overline{PCI_ARB_REQ[7:0]}$)	3	--	ns
t21	Hold time from PCI_CLK↑ (PCI_AD[31:0], PCI_C/$\overline{BE}$[3:0], PCI_PAR, $\overline{PCI_FRAME}$, $\overline{PCI_IRDY}$, $\overline{PCI_TDRY}$, $\overline{PCI_STOP}$, $\overline{PCI_DEVSEL}$, and PCI_IDSEL)	1	--	ns
t22[3]	PCI_CLK↑ to $\overline{RESET}$ deassertion	10	--	PCI Clocks
t23a[3]	PCI_CLK↑ to $\overline{PCI_RST}$ deassertion	10	--	PCI Clocks
t23b[3]	$\overline{PCI_RST}$ assertion to PCI_CLK idle	10	--	PCI Clocks
t24[3]	$\overline{PCI_RST}$ assertion to output high-Z (PCI_AD[31:0], PCI_C/$\overline{BE}$[3:0], PCI_PAR, $\overline{PCI_FRAME}$, $\overline{PCI_IRDY}$, $\overline{PCI_TDRY}$, $\overline{PCI_STOP}$, and $\overline{PCI_DEVSEL}$)	--	40	ns

Notes:

1. All outputs are measured using the load conditions shown in Figure 15.
2. High-Z defined as +/-300mV change from steady state.
3. Guaranteed by design.

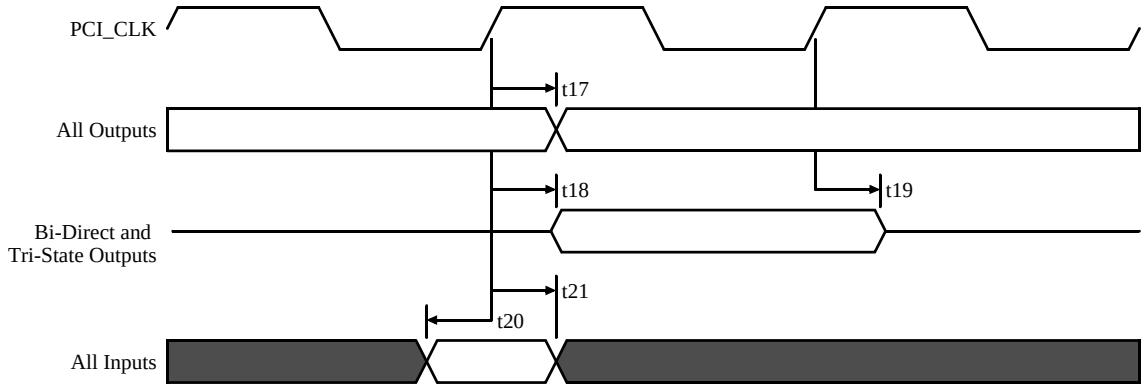


Figure 10. PCI Timing Diagram

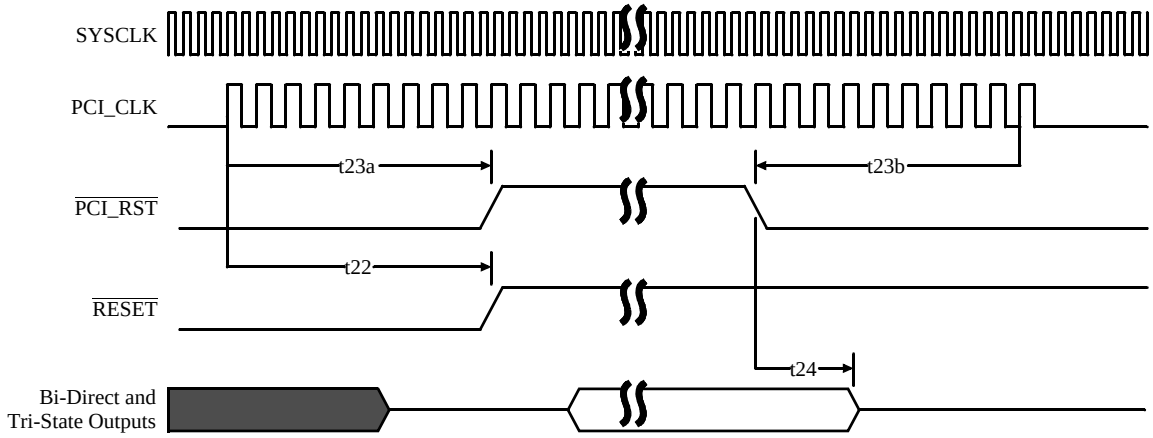


Figure 11. Timing Relationships of Clock and Reset for PCI Core Utilization

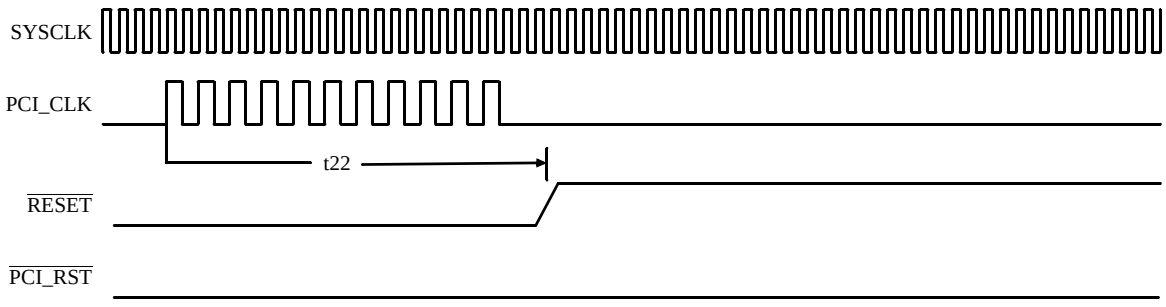


Figure 12. Timing Relationships of Clock and Reset for Unused PCI Core

4.7 Timing Characteristics for Ethernet Interface

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V; T_C = -40°C to 105°C)

Symbol	Description	Conditions	Min	Max	Units
t25[1]	ETX_CLK↑ to output valid (ETXD[3:0], and ETX_EN)		2	8	ns
t26[2]	Setup time to ERX_CLK↑ (ERX_DV[4]ERX_ER, and ERXD[3:0])		1	--	ns
t27[2]	Hold time from ERX_CLK↑ (ERX_DV[4]ERX_ER, and ERXD[3:0])		1	--	ns
t28[1]	EMDC↑ to output valid (EMDIO)	f_{EMDC}= 123KHz[3]; f_{SYSCLK} = 25MHz	2	11	ns
t29[4]	Setup time to EMDC↑ (EMDIO)		10	--	ns
t30[4]	Hold time from EMDC↑ (EMDIO)		5	--	ns

Notes:
1. All outputs are measured using the load conditions shown in Figure 15.
2. ERX_COL and ERX_CRS are asynchronous inputs and are not tested.
3. $f_{EMDC} = f_{SYSCLK} / 202$.
4. Guaranteed by design.

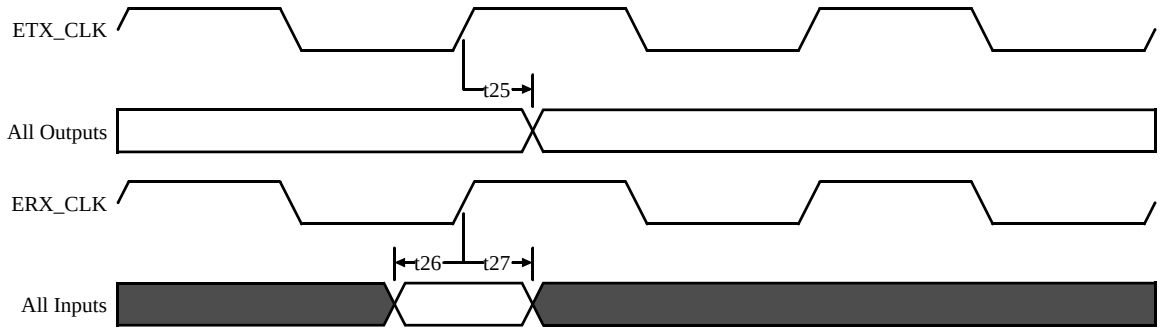


Figure 13. Ethernet Transmit and Receive Timing

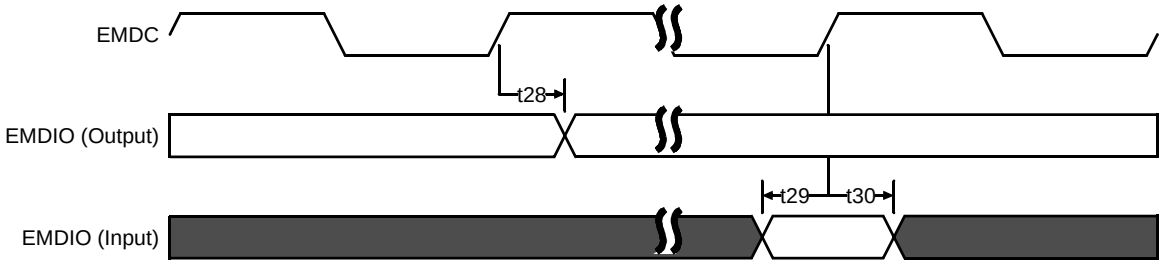


Figure 14. Ethernet MDIO Interface Timing

4.8 Test Conditions for Timing Specifications

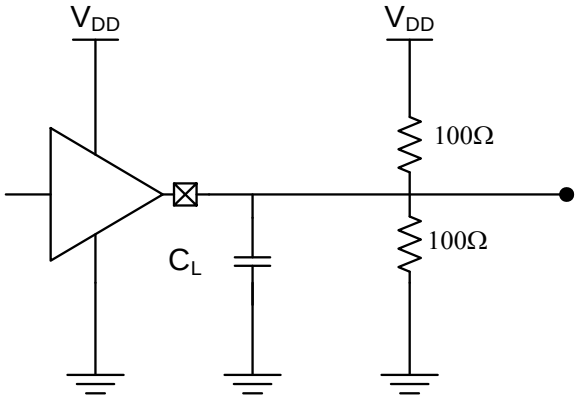


Figure 15. Equivalent Load Circuit for Timing Characteristics Tests
C_L = 50 pF for ATE test load
C_L =15 pF for benchtop test load

5.0 Operational Environment

The UT699 processor includes the following SEU mitigation features:

* Register file SEU error-correction of up to 1 error per 32-bit word
* Cache memory error-detection of up to 4 errors per tag or 32-bit word
* Autonomous and software transparent error handling
* No timing impact due to error detection or correction.

Table 1. Operational Environment

Parameter	Limit	Units
Total Ionizing Dose (TID)	3E5	rads(Si)
Single Event Latchup (SEL) [1, 2]	>108	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2

Notes:

1. The UT699 is latchup immune to particle LETs >108 MeV-cm^2/mg.
2. Worst case temperature and voltage of T_C = +105^{o}C, V_{DD} = 3.6V, V_{DDC} = 2.7V.
3. Contact factory for error rate information.

6.0 Packaging

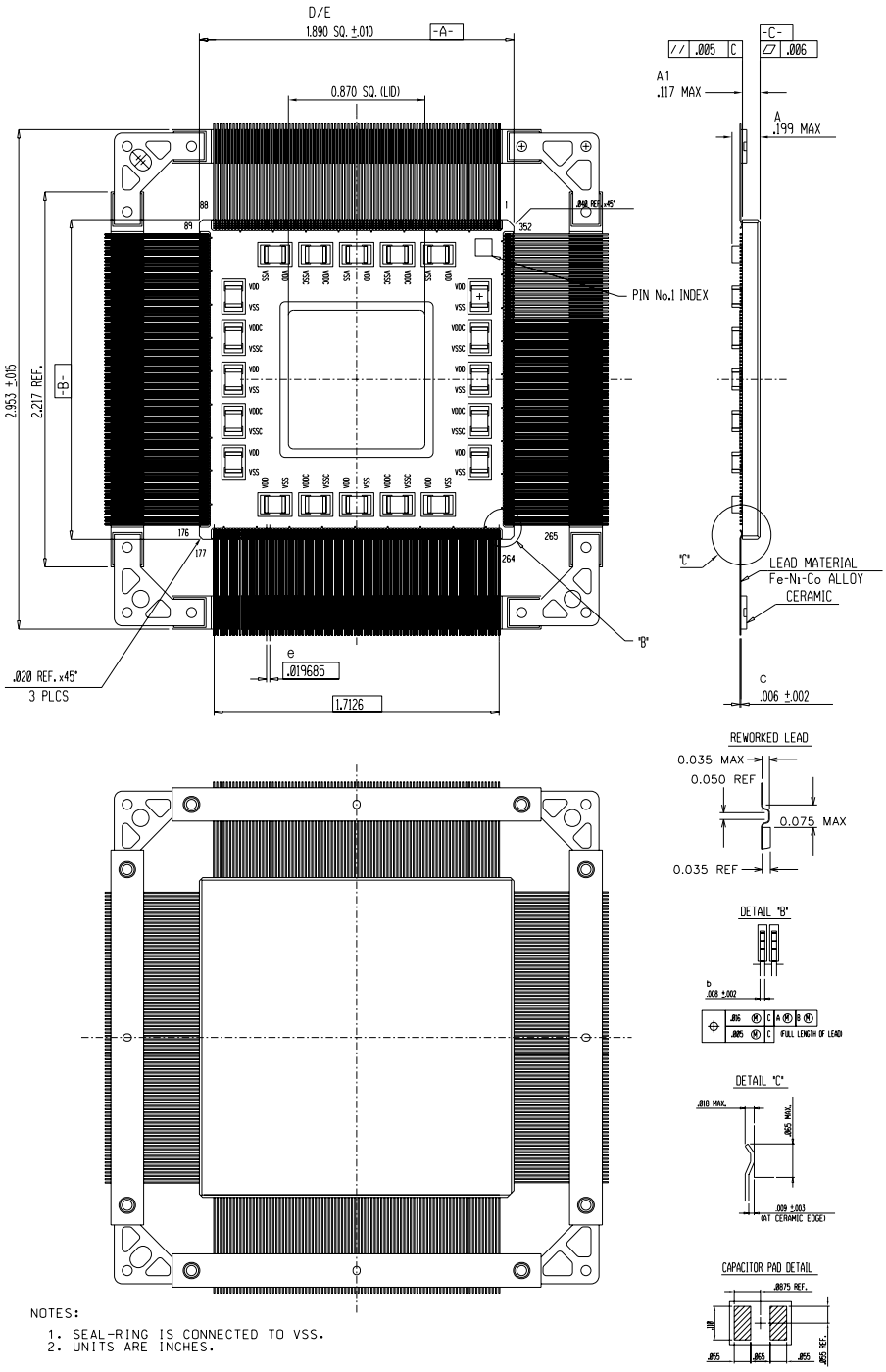


Figure 16. 352-lead Ceramic Quad Flatpack with Top-Brazed Leads

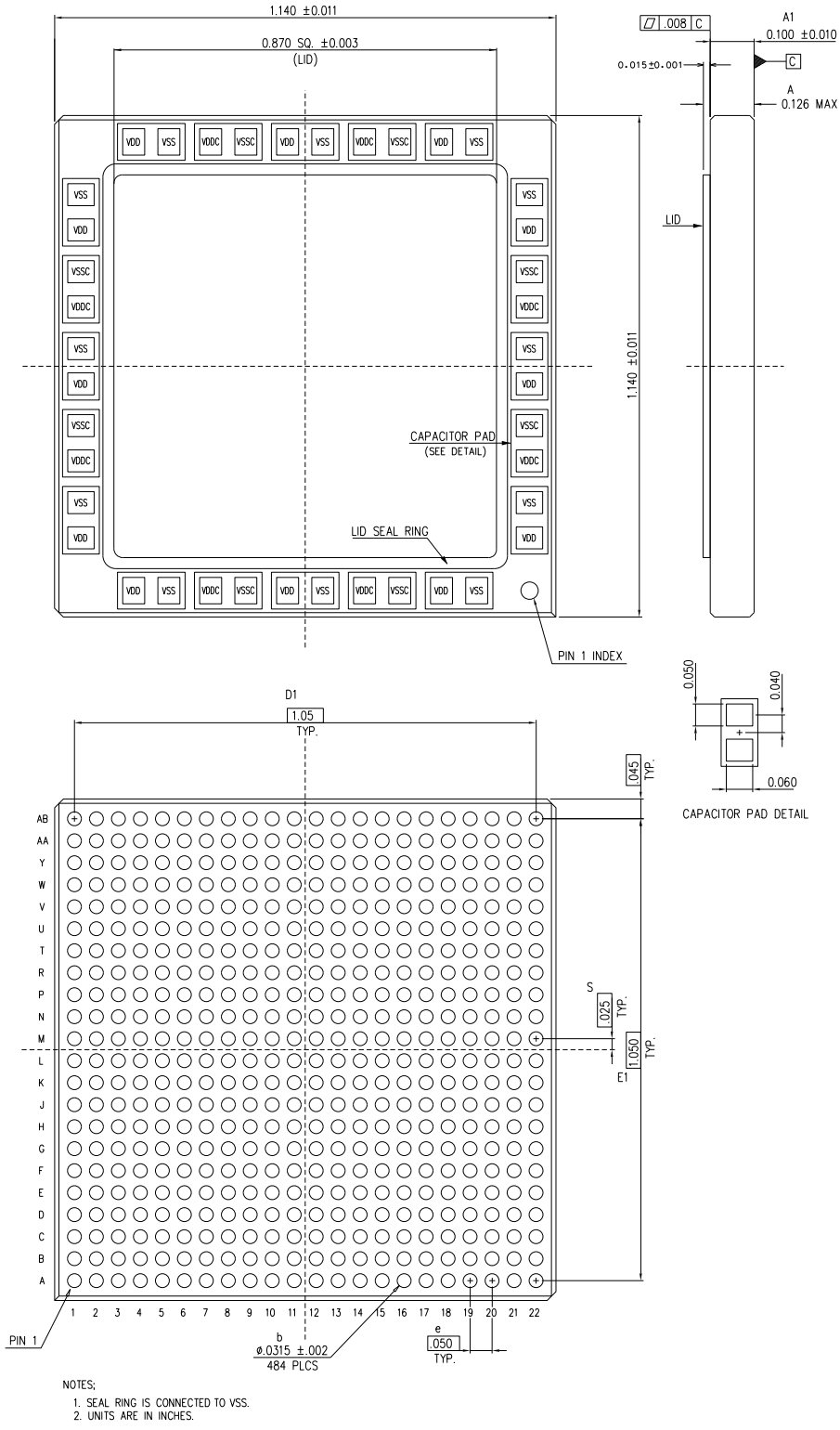


Figure 17. 484-lead Ceramic Land Grid Array

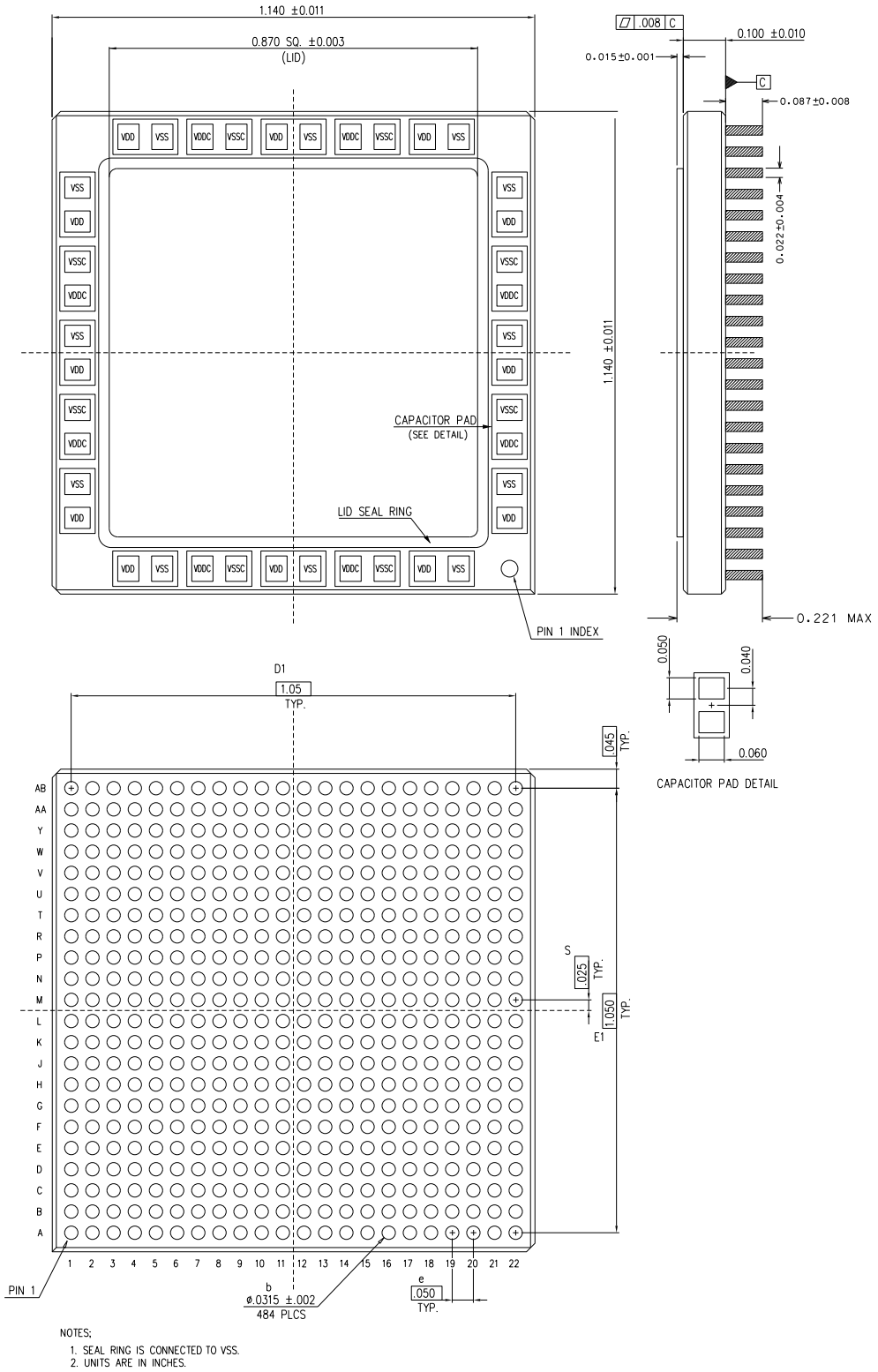


Figure 18. 484-lead Ceramic Column Grid Array

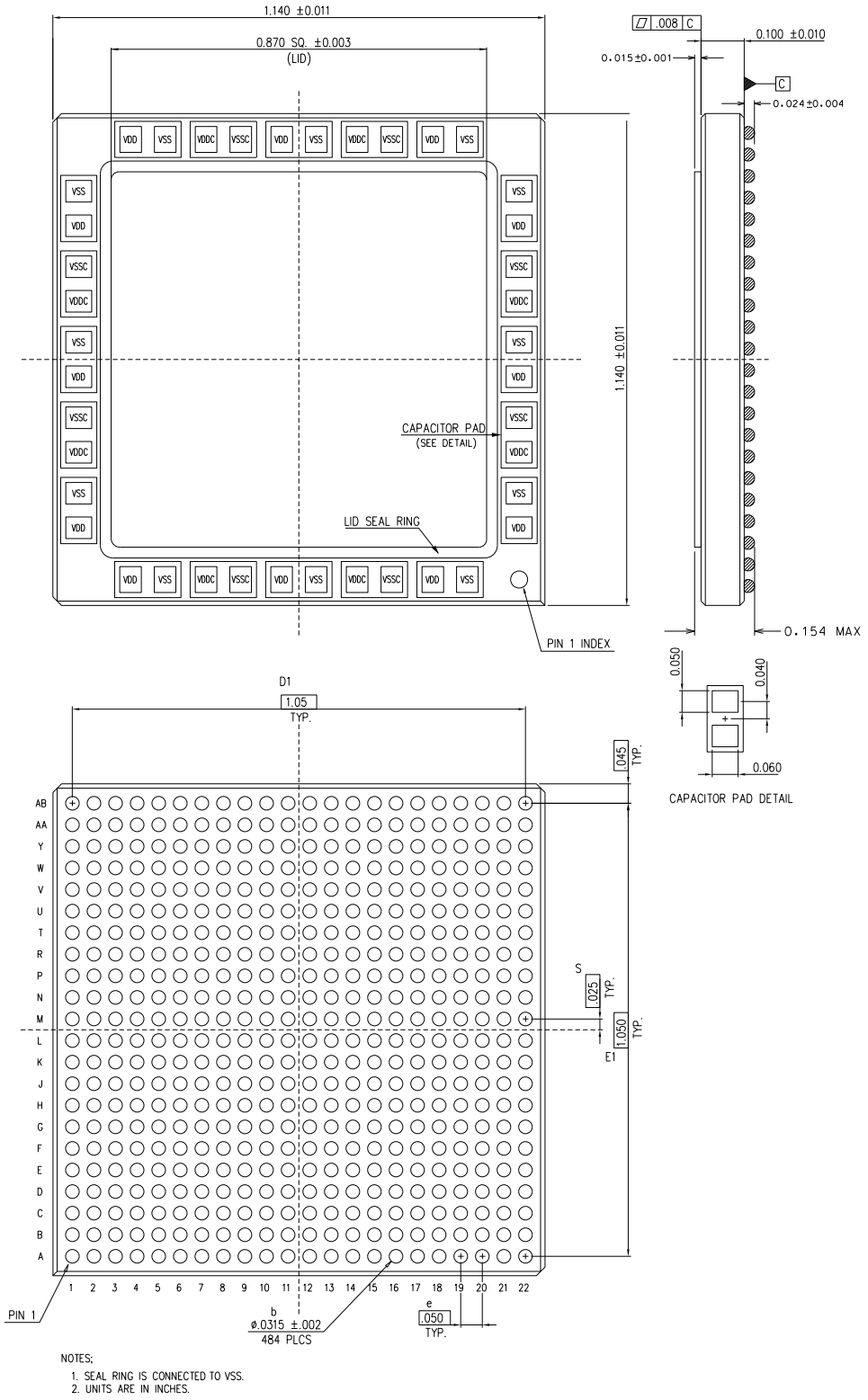
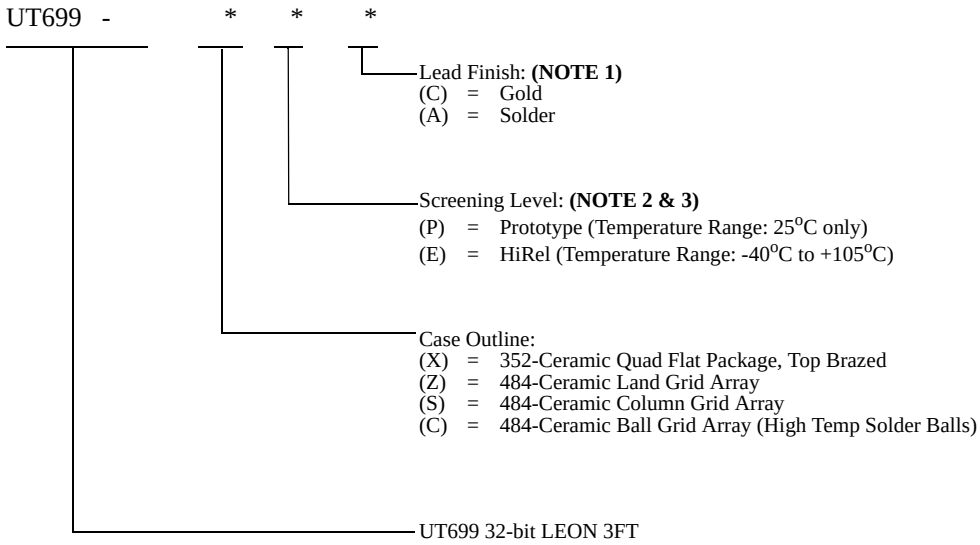


Figure 19. 484-lead Ceramic Ball Grid Array

7.0 Ordering Information

UT699 LEON 3FT

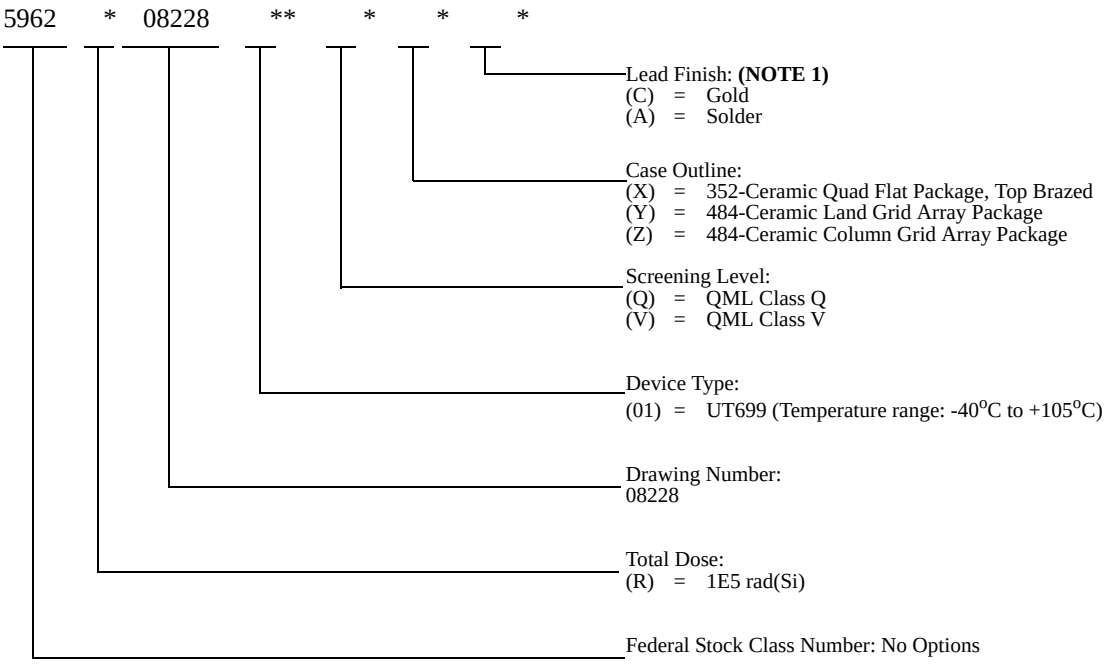


Notes:

1. Lead finish (A or C) must be specified.
2. Prototype Flow per Aeroflex Manufacturing Flows Document. Devices are tested at 25°C only. Radiation is neither tested nor guaranteed.
3. HiRel Flow per Aeroflex Manufacturing Flows Document. Radiation is neither tested nor guaranteed.

Package Option	Associated Lead Finish
(X) 352-CQFP	**(C) Gold**
(Z) 484-CLGA	**(C) Gold**
(S) 484-CCGA	**(A) Solder**
(C) 484-CBGA	**(A) Solder**

UT699 LEON 3FT: SMD



Notes:
1. Lead finish is “C” (gold) only for case outlines "X" and "Y". Lead finish is "A" (solder) only for case outline "Z".

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

COLORADO
Toll Free: 800-645-8862
Fax: 719-594-8468

INTERNATIONAL
Tel: 805-778-9229
Fax: 805-778-1980

NORTHEAST
Tel: 603-888-3975
Fax: 603-888-4585

SE AND MID-ATLANTIC
Tel: 321-951-4164
Fax: 321-951-4254

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Tel: 949-362-2260
Fax: 949-362-2266

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Tel: 719-594-8017
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www.aeroflex.com info-ams@aeroflex.com

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