TLV62568 采用 SOT 封装的 1A 高效同步降压转换器

1 特性

- 效率高达 95%
- 低 $R_{DS(ON)}$，可在 150mΩ 和 100mΩ 之间切换
- 输入电压范围：2.5V 至 5.5V
- 可调输出电压：0.6V 至 V_{IN}
- 针对轻载效率的省电模式
- 针对最低压降的 100% 占空比
- 35µA 静态工作电流
- 1.5MHz 开关频率
- 电源正常输出
- 过流保护
- 内部软启动
- 热关断保护
- 采用小外形尺寸晶体管 (SOT) 封装
- 与 TLV62569 引脚兼容

2 应用

- 通用负载点 (POL) 电源
- 网络视频摄像头
- 机顶盒
- 无线路由器

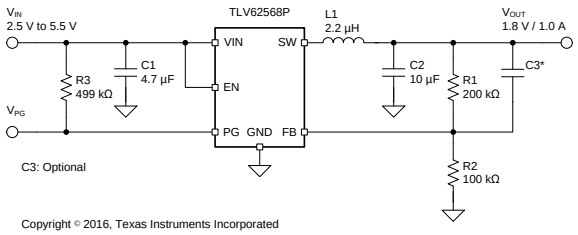
3 说明

TLV62568 器件是一款同步降压 DC-DC 转换器，专门针对高效和紧凑型解决方案进行了优化。该器件集成的开关能够提供高达 1A 的输出电流。

在中等负载或重载条件下，该器件运行在脉宽调制 (PWM) 模式下，开关频率为 1.5MHz。在轻载情况下，该器件自动进入节能模式 (PSM)，从而在整个负载电流范围内保持高效率。关断时，流耗减少至 2µA 以下。

TLV62568 的输出电压可通过一个外部电阻分压器进行调节。内部软启动电路可限制启动期间的浪涌电流。该器件 还内置了 诸如输出过流保护、热关断保护和电源正常输出等其他特性。该器件提供 SOT23 和 SOT563 两种封装。

简化电路原理图



器件信息(1)

器件型号	封装	封装尺寸（标称值）
TLV62568	SOT-23 (5)	2.90mm x 2.80mm
TLV62568P	SOT-23 (6)	
TLV62568	SOT563 (6)	1.60mm x 1.60mm
TLV62568P	SOT563 (6)	

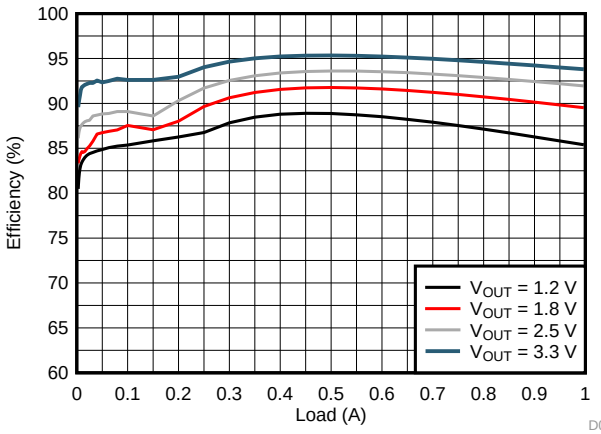
(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

器件比较

器件编号	功能	封装标记	封装
TLV62568DBV	-	14VF	SOT23-5
TLV62568PDDC(1)	电源正常		SOT23-6
TLV62568DRL	-	18L	SOT563-6
TLV62568PDRL	电源正常	18N	SOT563-6

(1) 产品预览

5V 输入电压下的效率



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目录

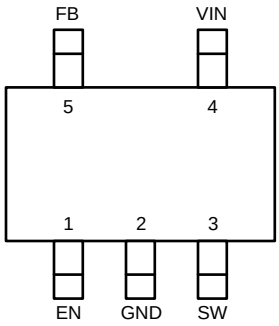
4 修订历史记录

Changes from Original (November 2016) to Revision A **Page**

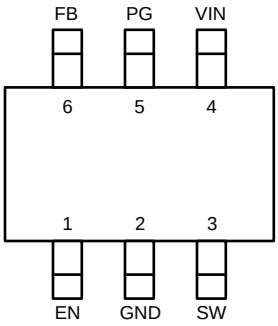
- 已更改 TLV62568DRL 和 TLV62568PDRL 更改为生产状态。 ... 1
- 将器件比较表移至第 1 页 ... 1
- Added DRL package thermal information ... 4
- Added startup time of TLV62568DRL, TLV62568PDRL ... 5
- 已添加 TLV62568PDRL layout. ... 14

5 Pin Configuration and Functions

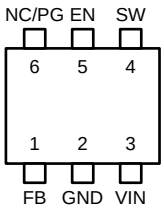
SOT23-5
DBV Package
(Top View)



SOT23-6
DDC Package
(Top View)



SOT563-6
DRL Package
(Top View)



Pin Functions

PIN NUMBER				I/O/PWR	DESCRIPTION
NAME	SOT23-5	SOT23-6	SOT563-6		
EN	1	1	5	I	Device enable logic input. Logic high enables the device, logic low disables the device and turns it into shutdown. Do not leave floating.
GND	2	2	2	PWR	Ground pin.
SW	3	3	4	PWR	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
VIN	4	4	3	PWR	Power supply voltage input.
PG	-	5	6	O	Power good open drain output pin for TLV62568P. The pull-up resistor should not be connected to any voltage higher than 5.5V. If it's not used, leave the pin floating.
FB	5	6	1	I	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
NC	-	-	6	O	No connection pin for TLV62568DRL. The pin can be connected to the output. Or leave it floating.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VIN, EN, PG	–0.3	6	V
	SW (DC)	–0.3	V_{IN}+0.3	V
	SW (AC, less than 10 ns)(3)	–3.0	9	V
	FB	–0.3	5.5	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) While switching.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions (1)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	2.5		5.5	V
V_{OUT}	Output voltage	0.6		V_{IN}	V
I_{OUT}	Output current			1	A
T_J	Operating junction temperature	–40		125	°C
I_{SINK_PG}	Sink current at PG pin			1	mA

(1) Refer to the *Application and Implementation* section for further information.

6.4 Thermal Information

THERMAL METRIC (1)		TLV62568	TLV62568x	UNIT
		DBV (5 Pins)	DRL (6 pins)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	191.6	149.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	141.4	45.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.5	31.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	34.5	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.9	31.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{IN} = 5.0 V, T_J = 25°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current into VIN pin	Not switching		35		uA
I_{SD}	Shutdown current into VIN pin	EN = 0 V		0.1	2	µA
V_{UVLO}	Under voltage lock out	V_{IN} falling		2.3	2.45	V
	Under voltage lock out hysteresis			100		mV
T_{JSD}	Thermal shutdown threshold	Junction temperature rising		150		°C
		Junction temperature falling		130		
LOGIC INTERFACE						
V_{IH}	High-level input voltage at EN pin	2.5 V ≤ V_{IN} ≤ 5.5 V	1.2	0.95		V
V_{IL}	Low-level input voltage at EN pin	2.5 V ≤ V_{IN} ≤ 5.5 V		0.85	0.4	V
t_{SS}	Soft startup time	TLV62568DBV		700		µs
		TLV62568DRL, TLV62568PDRL		900		
V_{PG}	Power good threshold, TLV62568P	V_{FB} rising, referenced to V_{FB} nominal		95%		
		V_{FB} falling, referenced to V_{FB} nominal		90%		
$V_{PG,OL}$	Power good low-level output voltage	I_{SINK} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5.0 V		0.01		µA
$t_{PG,DLY}$	Power good delay time	V_{FB} falling		40		µs
OUTPUT						
V_{FB}	Feedback regulation voltage		0.588	0.6	0.612	V
$R_{DS(on)}$	High-side FET on resistance			150		mΩ
	Low-side FET on resistance			100		
I_{LIM}	High-side FET current limit		1.5			A
f_{SW}	Switching frequency	V_{OUT} = 1.8 V		1.5		MHz

6.6 Typical Characteristics

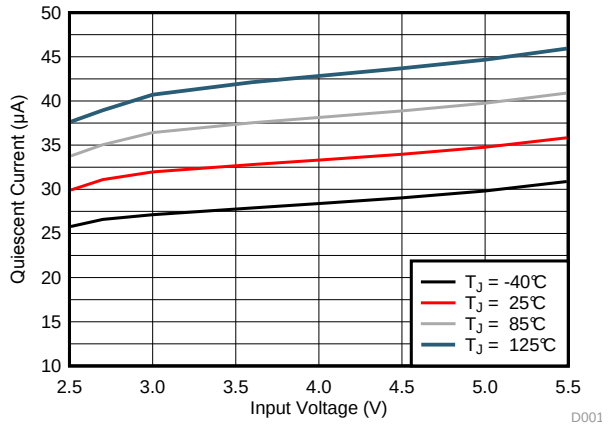


图 1. Quiescent Current vs Input Voltage

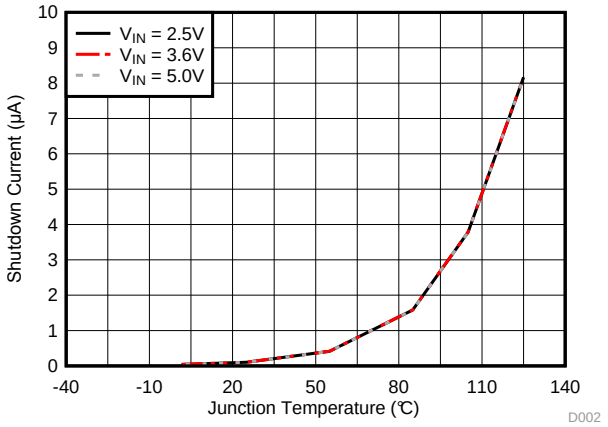


图 2. Shutdown Current vs Junction Temperature

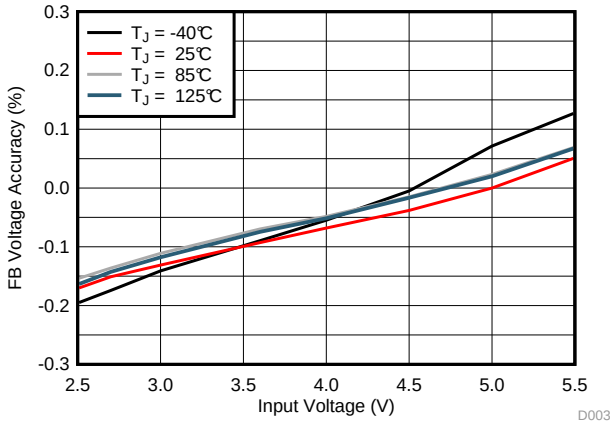


图 3. FB Voltage Accuracy

7 Detailed Description

7.1 Overview

The TLV62568 is a high-efficiency synchronous step-down converter. The device operates with an adaptive off-time with peak current control scheme. The device operates at typically 1.5-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the V_{IN}/V_{OUT} ratio, a simple circuit sets the required off time for the low-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current.

7.2 Functional Block Diagram

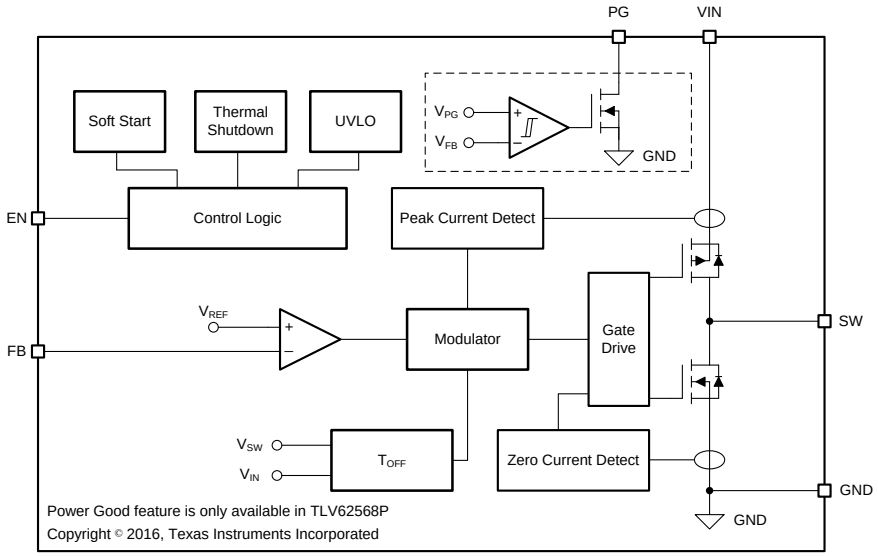


图 4. TLV62568 Functional Block Diagram

7.3 Feature Description

7.3.1 Power Save Mode

The device automatically enters Power Save Mode to improve efficiency at light load when the inductor current becomes discontinuous. In Power Save Mode, the converter reduces switching frequency and minimizes current consumption. In Power Save Mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor.

7.3.2 100% Duty Cycle Low Dropout Operation

The device offers a low input-to-output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times (R_{DS(ON)} + R_L) \quad (1)$$

where

- $R_{DS(ON)}$ = High side FET on-resistance
- R_L = Inductor ohmic resistance (DCR)

7.3.3 Soft Startup

After enabling the device, internal soft startup circuitry ramps up the output voltage which reaches nominal output voltage during a startup time. This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

Feature Description (接下页)

The TLV62568 is able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

7.3.4 Switch Current Limit

The switch current limit prevents the device from high inductor current and drawing excessive current from a battery or input voltage rail. Excessive current might occur with a heavy load or shorted output circuit condition. The TLV62568 adopts the peak current control by sensing the current of the high-side switch. Once the high-side switch current limit is reached, the high-side switch is turned off and low-side switch is turned on to ramp down the inductor current with an adaptive off-time.

7.3.5 Under Voltage Lockout

To avoid mis-operation of the device at low input voltages, under voltage lockout is implemented that shuts down the device at voltages lower than V_{UVLO} with V_{HYS_UVLO} hysteresis.

7.3.6 Thermal Shutdown

The device enters thermal shutdown once the junction temperature exceeds the thermal shutdown rising threshold, T_{JSD}. Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

7.4 Device Functional Modes

7.4.1 Enabling/Disabling the Device

The device is enabled by setting the EN input to a logic High. Accordingly, a logic Low disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and should not be left floating.

7.4.2 Power Good

The TLV62568P has a power good output. The PG pin goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

表 1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, $V_{FB} \geq V_{PG}$	√	
	EN = High, $V_{FB} \leq V_{PG}$		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	$1.4\ V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} \leq 1.4\ V$	√	

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

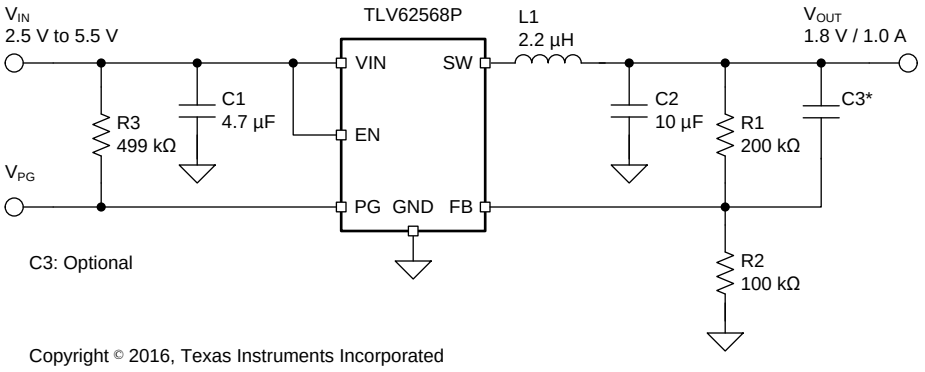


图 5. TLV62568 1.8-V Output Application

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 2 as the input parameters.

表 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.5 V to 5.5 V
Output voltage	1.8 V
Maximum output current	1.0 A

表 3 lists the components used for the example.

表 3. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER(1)
C1	4.7 µF, Ceramic Capacitor, 10 V, X7R, size 0805, GRM21BR71A475KA73L	Murata
C2	10 µF, Ceramic Capacitor, 10 V, X7R, size 0805, GRM21BR71A106KE51L	Murata
L1	2.2 µH, Power Inductor, SDER041H-2R2MS	Cyntec
R1,R2,R3	Chip resistor,1%,size 0603	Std.
C3	Optional, 6.8 pF if it is needed	Std.

(1) See *Third-party Products Disclaimer*

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Output Voltage

An external resistor divider is used to set output voltage according to 公式 2.

When sizing R2, in order to achieve low current consumption and acceptable noise sensitivity, use a maximum of 200 kΩ for R2. Larger currents through R2 improve noise sensitivity and output voltage accuracy but increase current consumption.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.6V \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

A feed forward capacitor, C3 improves the loop bandwidth to make a fast transient response (shown in 图 19). 6.8-pF capacitance is recommended for R2 of 100-kΩ resistance. A more detailed discussion on the optimization for stability vs. transient response can be found in SLVA289.

8.2.2.2 Output Filter Design

The inductor and output capacitor together provide a low-pass filter. To simplify this process, 表 4 outlines possible inductor and capacitor value combinations. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

表 4. Matrix of Output Capacitor and Inductor Combinations

V_{OUT} [V]	L [µH](1)	C_{OUT} [µF](2)				
		4.7	10	22	2x 22	100
0.6 ≤ V_{OUT} < 1.2	1				+	
	2.2				++(3)	
1.2 ≤ V_{OUT} < 1.8	1			+	+	
	2.2			++(3)	+	
1.8 ≤ V_{OUT}	1		+	+	+	
	2.2		++(3)	+	+	

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%.
(2) Capacitor tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and -50%.
(3) This LC combination is the standard value and recommended for most applications.

8.2.2.3 Inductor Selection

The main parameters for inductor selection is inductor value and then saturation current of the inductor. To calculate the maximum inductor current under static load conditions, 公式 3 is given:

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

where:

- $I_{OUT,MAX}$ is the maximum output current
- ΔI_L is the inductor current ripple
- f_{SW} is the switching frequency
- L is the inductor value (3)

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor.

8.2.2.4 Input and Output Capacitor Selection

The architecture of the TLV62568 allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep its resistance up to high frequencies and to achieve narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric.

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering. For most applications, 4.7-µF input capacitance is sufficient; a larger value reduces input voltage ripple.

The TLV62568 is designed to operate with an output capacitor of 10 µF to 47 µF, as outlined in 表 4.

8.2.3 Application Performance Curves

V_{IN} = 5 V, V_{OUT} = 1.8 V, L = 2.2 µH, T_A = 25 °C, unless otherwise noted.

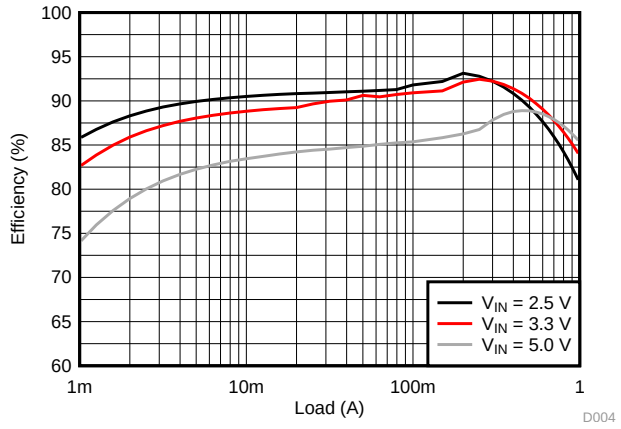


图 6. 1.2-V Output Efficiency

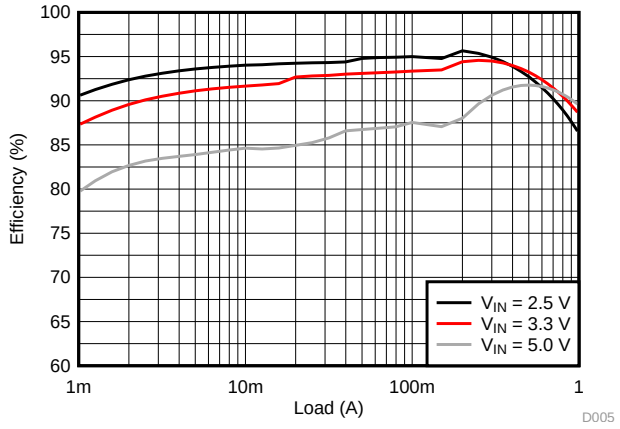


图 7. 1.8-V Output Efficiency

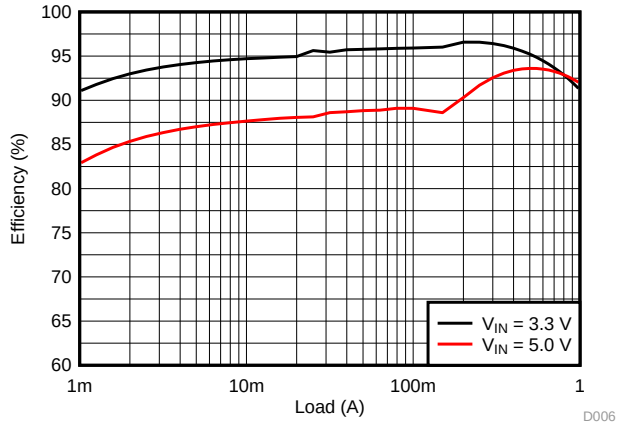


图 8. 2.5-V Output Efficiency

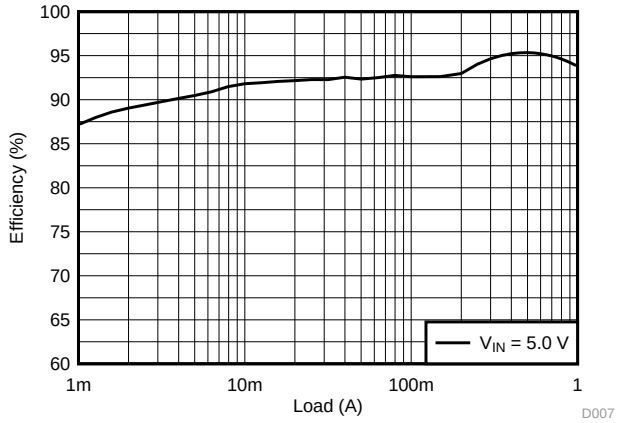
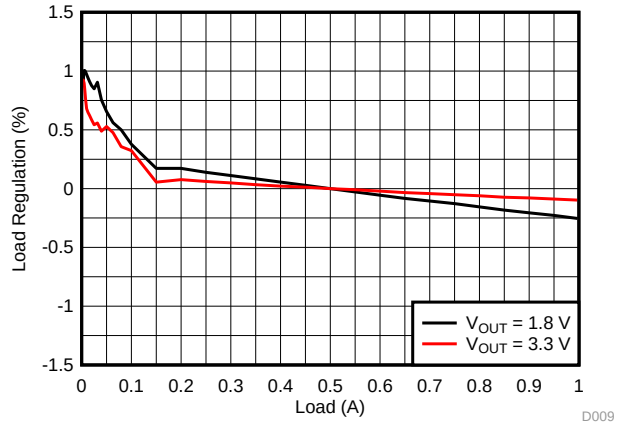
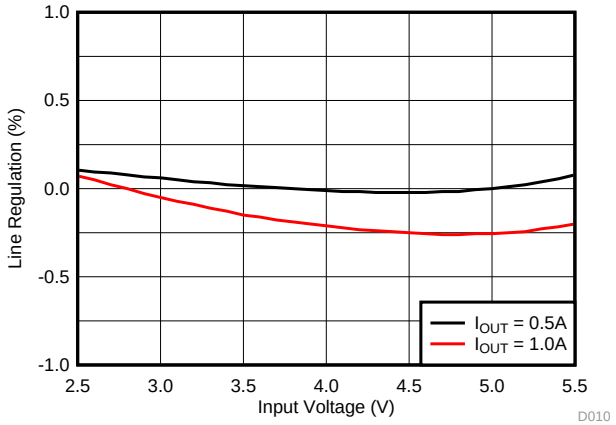


图 9. 3.3-V Output Efficiency



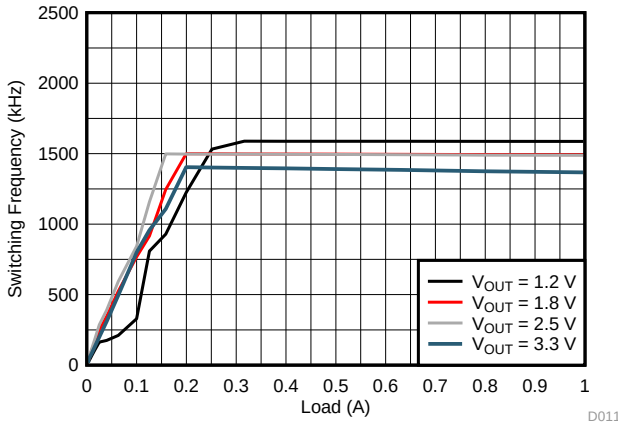
V_{IN} = 5 V

图 10. Load Regulation



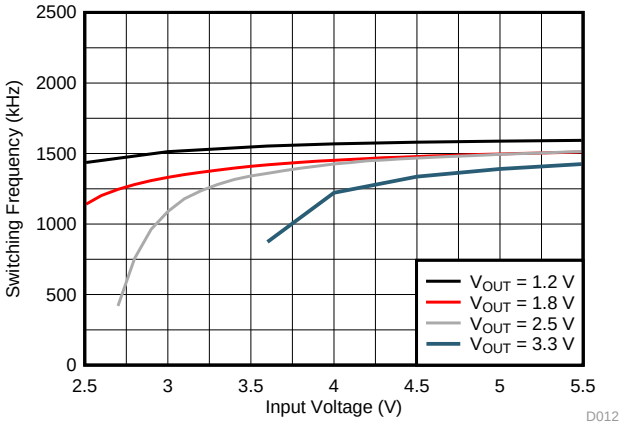
V_{OUT} = 1.8 V

图 11. Line Regulation



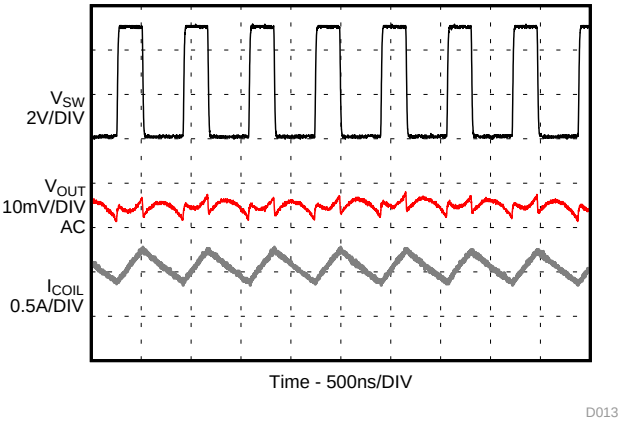
V_{IN} = 5 V

图 12. Switching Frequency vs Load



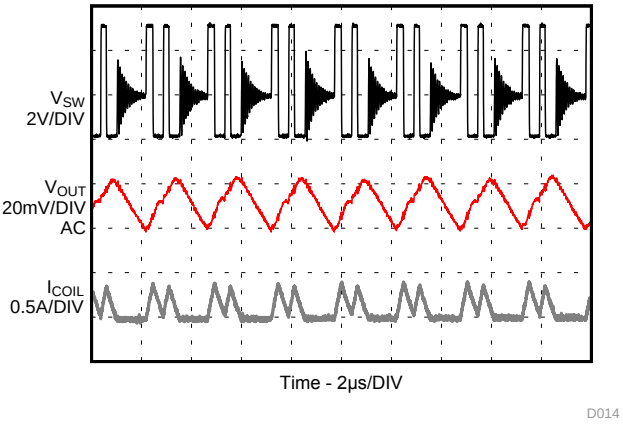
I_{OUT} = 0.5 A

图 13. Switching Frequency vs Input Voltage



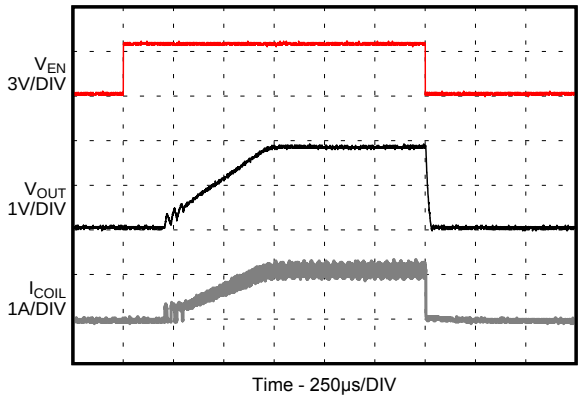
I_{OUT} = 0.5 A

图 14. PWM Operation



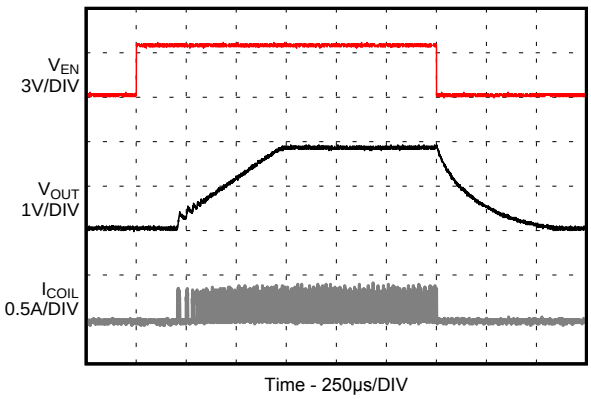
I_{OUT} = 0.1 A

图 15. Power Save Mode Operation



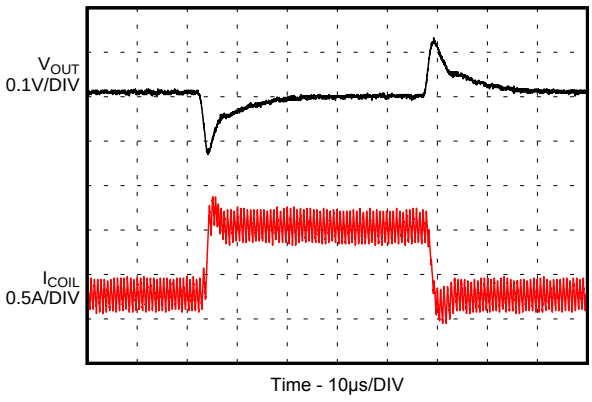
I_{OUT} = 1 A

图 16. Startup with Load



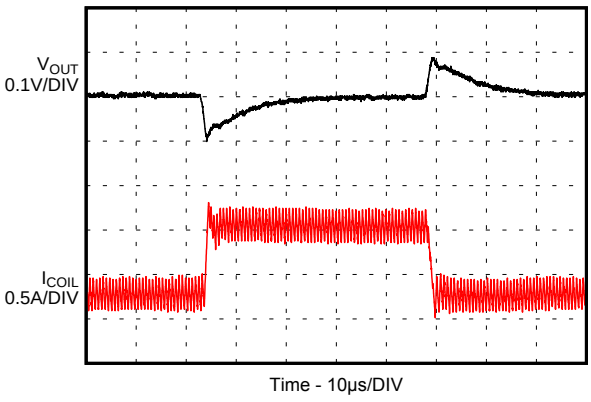
I_{OUT} = 0.1 A

图 17. Startup with Load



Load Step 0.3 A to 1 A, 1A/µs slew rate

图 18. Load Transient



Load Step 0.3 A to 1 A, 1A/µs slew rate C3 = 6.8 pF

图 19. Load Transient with a feed forward capacitor

9 Power Supply Recommendations

The power supply to the TLV62568 must have a current rating according to the supply voltage, output voltage and output current.

10 Layout

10.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TLV62568 device.

- The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the power GND to avoid a GND potential shift.
- The sense traces connected to FB are signal traces. Special care should be taken to avoid noise being induced. Keep these traces away from SW nodes.
- GND layers might be used for shielding.

10.2 Layout Example

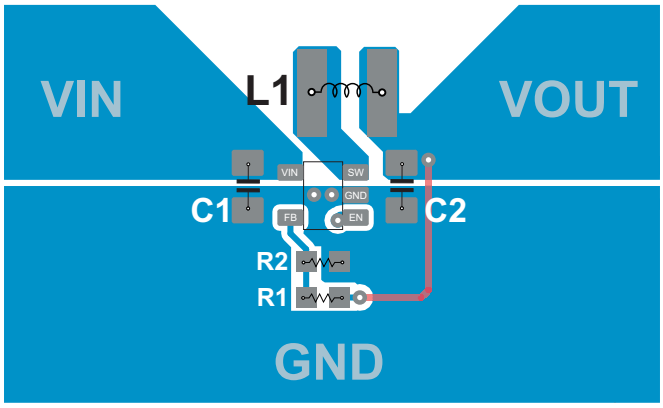


图 20. TLV62568DBV Layout

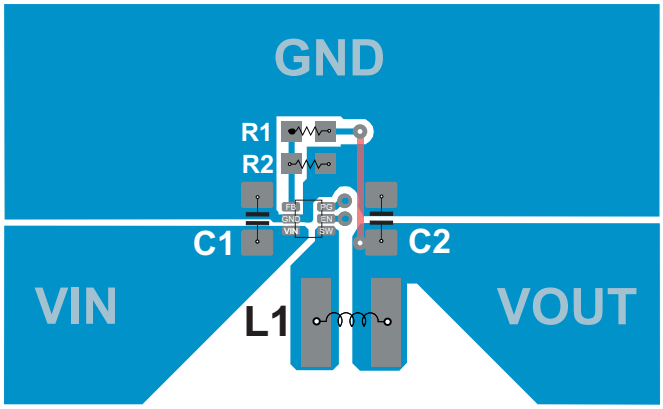


图 21. TLV62568PDRL Layout

10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Notes SZZA017 and SPRA953.

11 器件和文档支持

11.1 器件支持

11.1.1 Third-Party Products Disclaimer

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11.2 文档支持

11.2.1 相关文档

应用报告《半导体和 IC 封装热指标》（文件编号：SPRA953）

应用报告《采用 JEDEC PCB 设计的线性和逻辑封装散热特性》（文件编号：SZZA017）

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV62568DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	14VF	Samples
TLV62568DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	14VF	Samples
TLV62568DRLR	ACTIVE	SOT-5X3	DRL	6	3000	Green (RoHS & no Sb/Br)	CU | CU SN	Level-1-260C-UNLIM	-40 to 125	18L	Samples
TLV62568DRLT	ACTIVE	SOT-5X3	DRL	6	250	Green (RoHS & no Sb/Br)	CU | CU SN	Level-1-260C-UNLIM	-40 to 125	18L	Samples
TLV62568PDDCR	PREVIEW	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU	Level-1-260C-UNLIM	-40 to 125	9X9	
TLV62568PDDCT	PREVIEW	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU	Level-1-260C-UNLIM	-40 to 125	9X9	
TLV62568PDRLR	ACTIVE	SOT-5X3	DRL	6	3000	Green (RoHS & no Sb/Br)	CU | CU SN	Level-1-260C-UNLIM	-40 to 125	18N	Samples
TLV62568PDRLT	ACTIVE	SOT-5X3	DRL	6	250	Green (RoHS & no Sb/Br)	CU | CU SN	Level-1-260C-UNLIM	-40 to 125	18N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

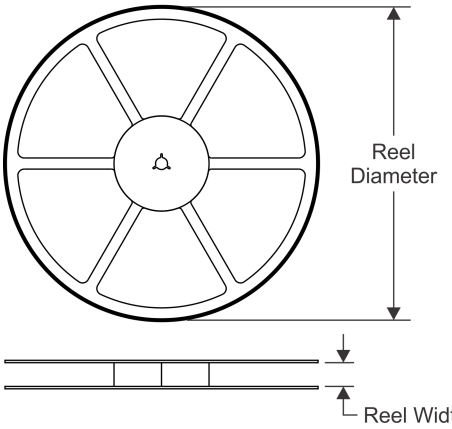
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

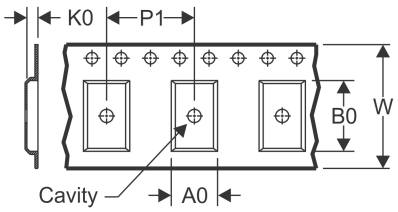
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

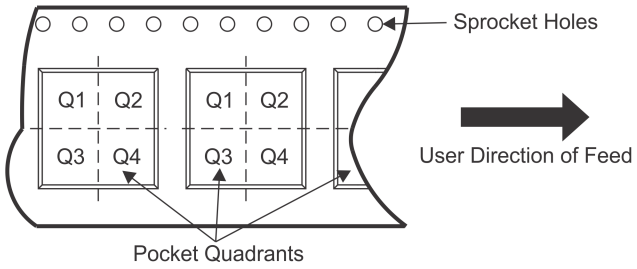


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

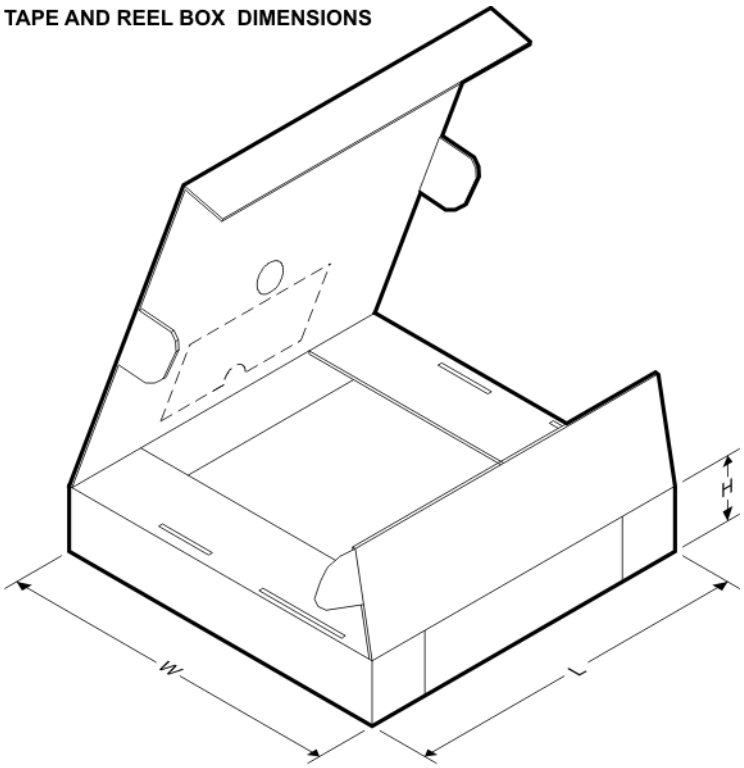
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62568DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62568DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV62568DRLR	SOT-5X3	DRL	6	3000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TLV62568DRLT	SOT-5X3	DRL	6	250	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TLV62568PDDCR	SOT-23-THIN	DDC	6	3000	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3
TLV62568PDDCT	SOT-23-THIN	DDC	6	250	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3
TLV62568PDRLR	SOT-5X3	DRL	6	3000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TLV62568PDRLT	SOT-5X3	DRL	6	250	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3

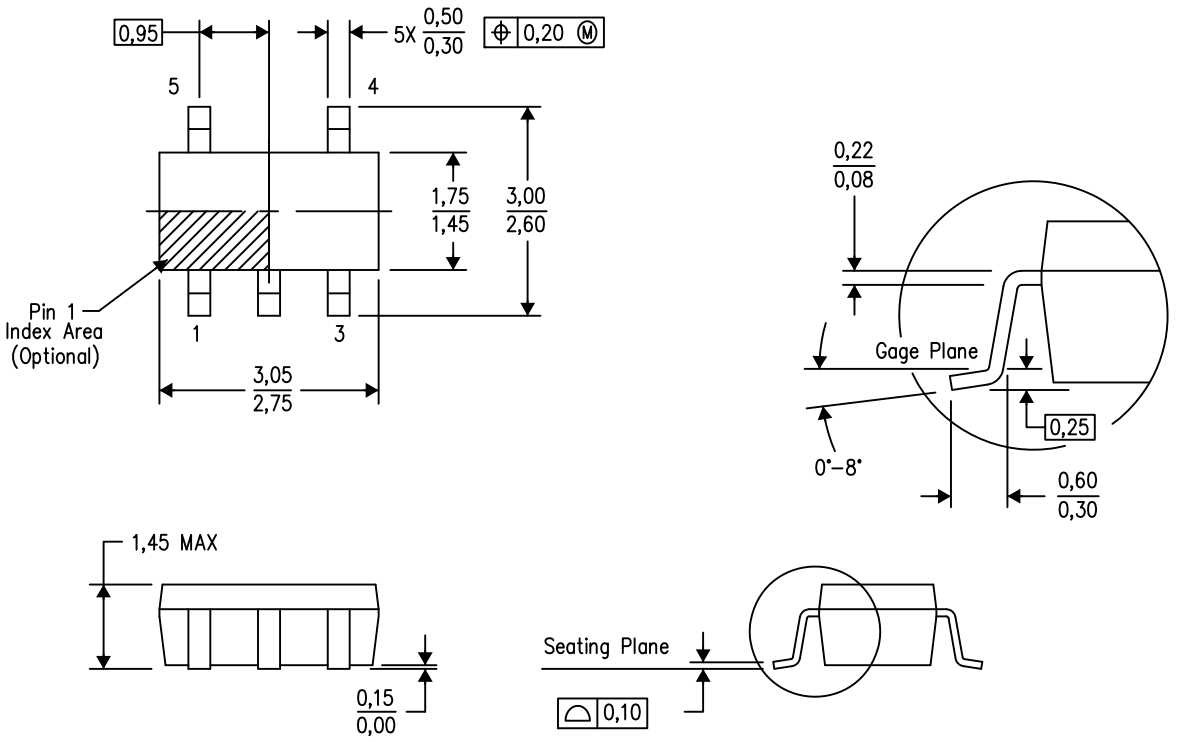
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62568DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV62568DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV62568DRLR	SOT-5X3	DRL	6	3000	184.0	184.0	19.0
TLV62568DRLT	SOT-5X3	DRL	6	250	184.0	184.0	19.0
TLV62568PDDCR	SOT-23-THIN	DDC	6	3000	184.0	184.0	19.0
TLV62568PDDCT	SOT-23-THIN	DDC	6	250	184.0	184.0	19.0
TLV62568PDRLR	SOT-5X3	DRL	6	3000	184.0	184.0	19.0
TLV62568PDRLT	SOT-5X3	DRL	6	250	184.0	184.0	19.0

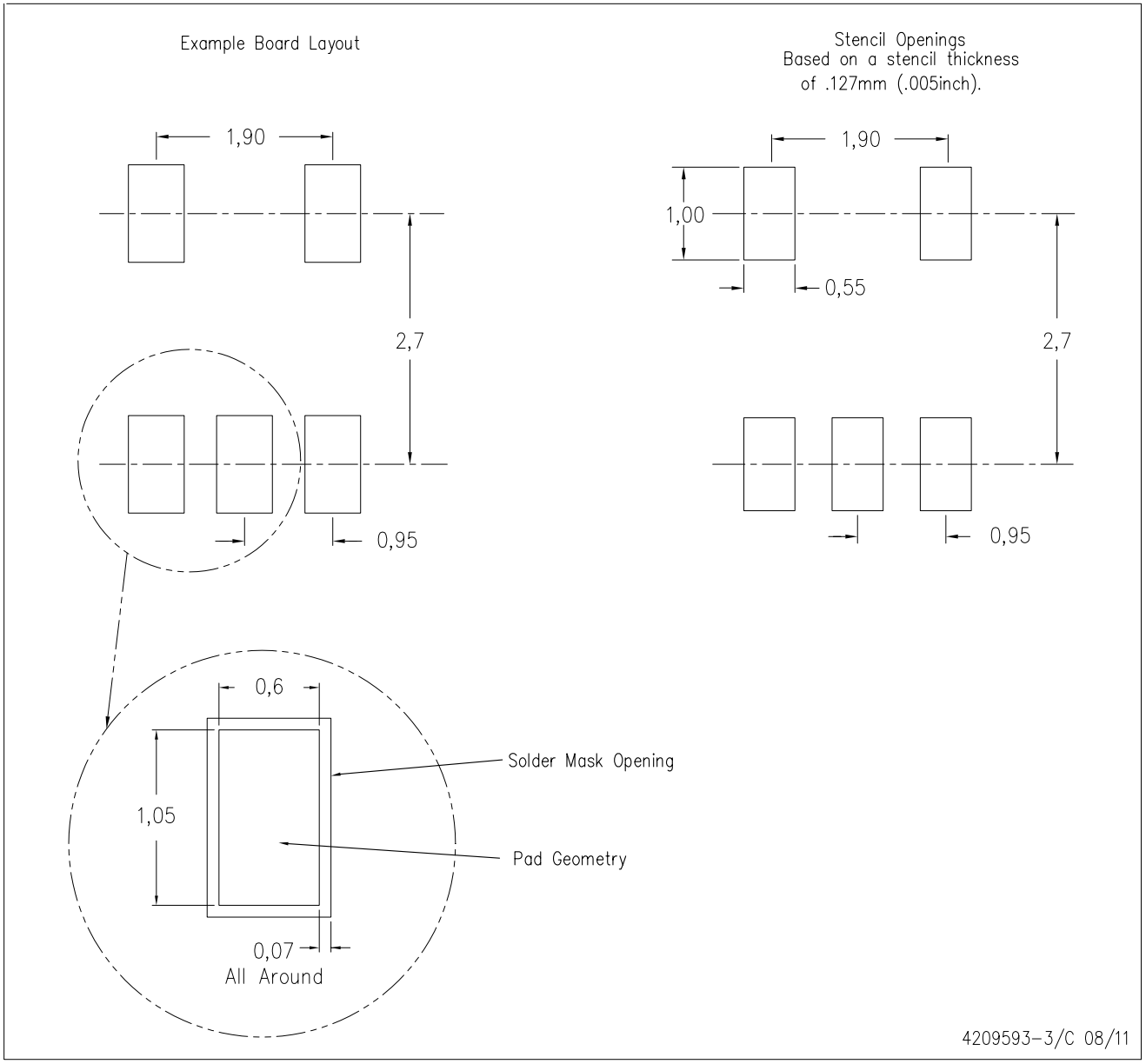
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



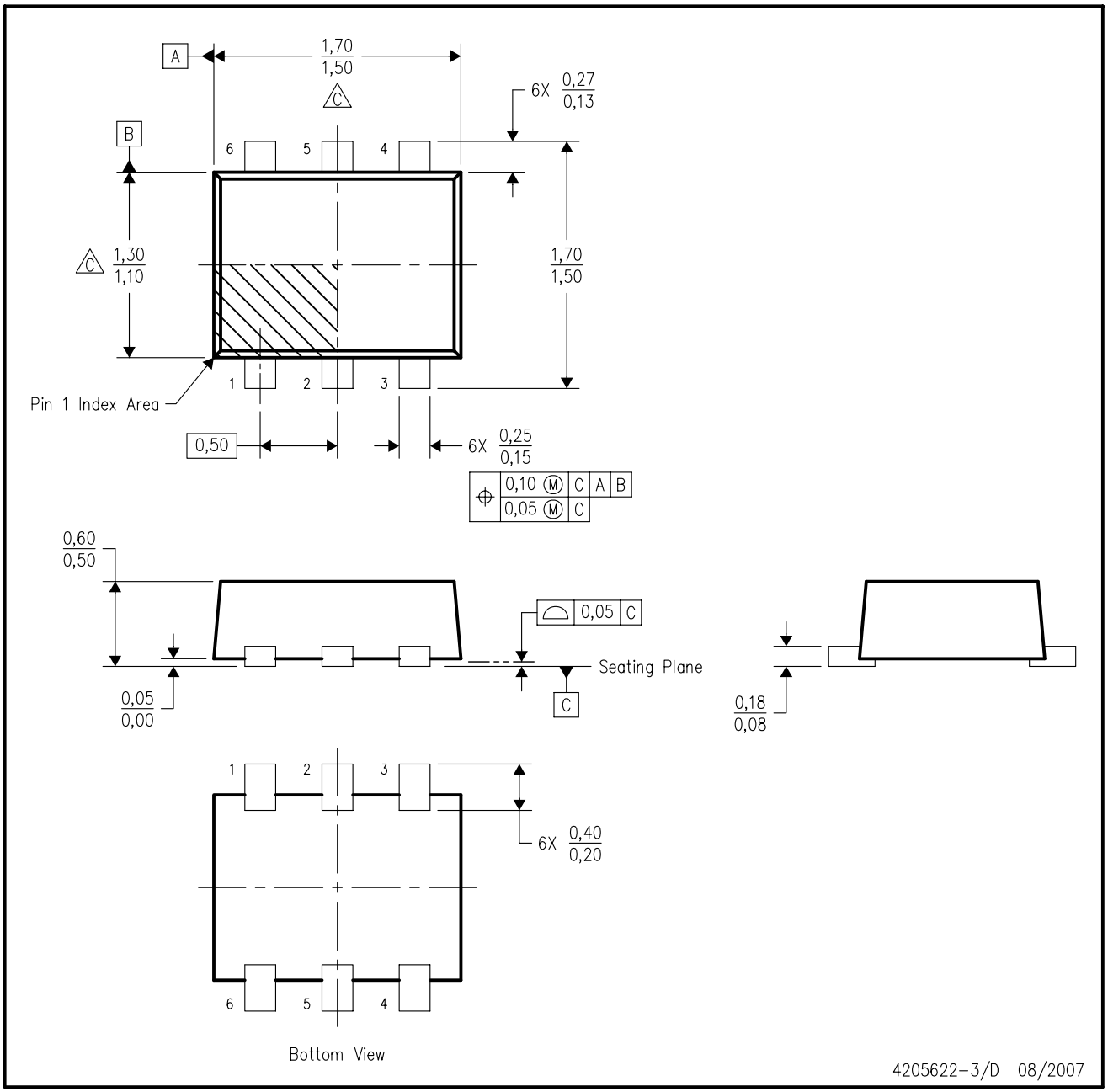
4073253–4/N 12/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE

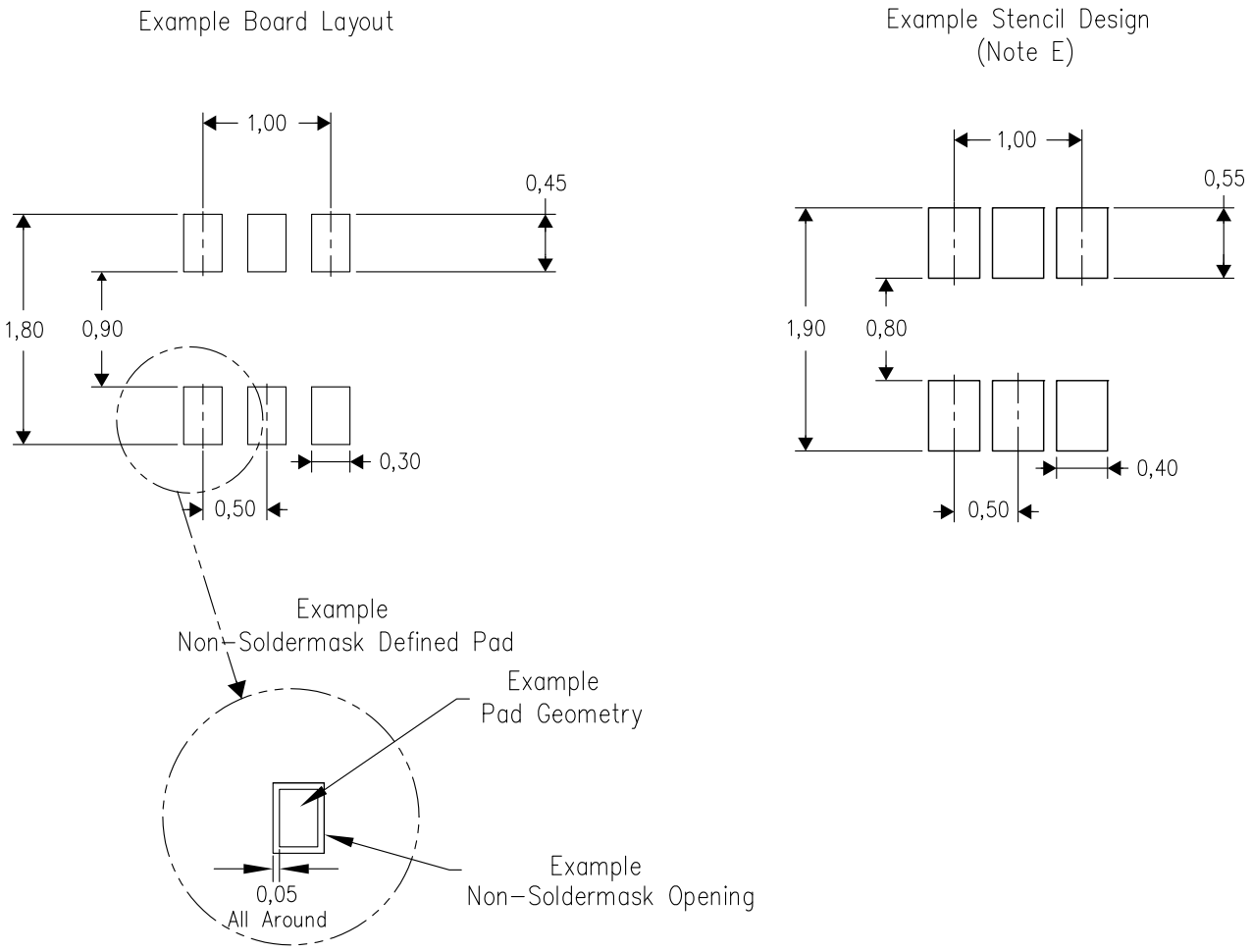


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

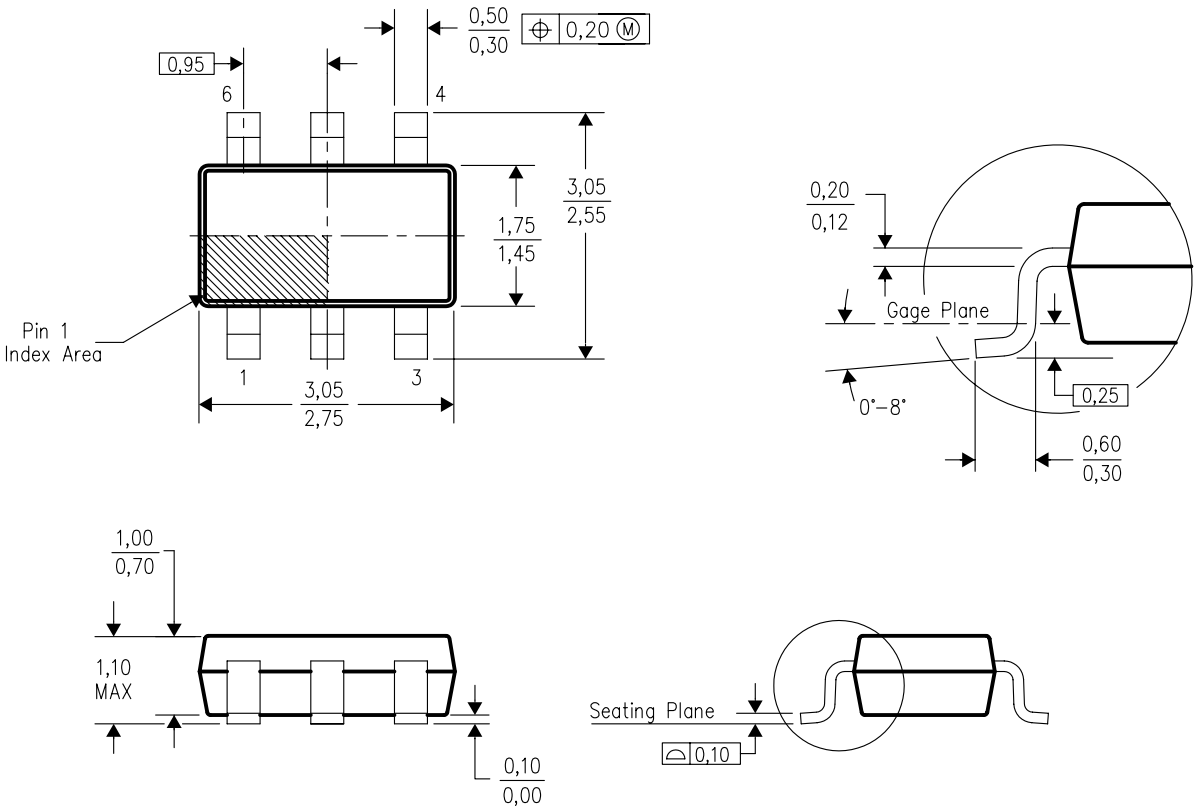
DRL (R–PDSO–N6) PLASTIC SMALL OUTLINE



4208207–3/E 06/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE



4204403–3/E 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AA (6 pin).

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