

Low Phase Noise CMOS XO (48MHz to 96MHz)

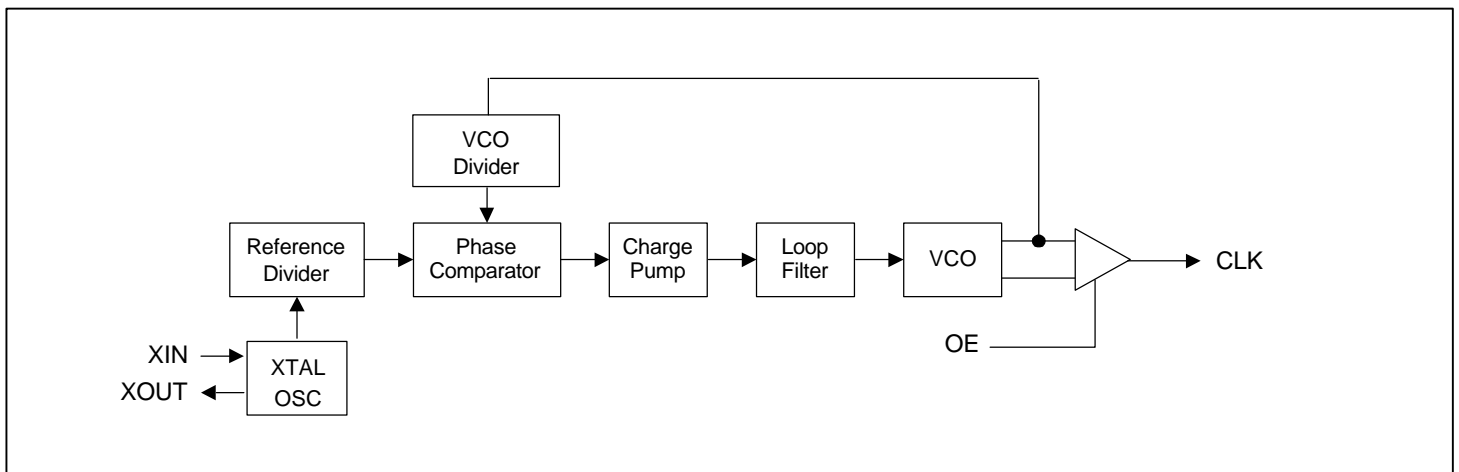
FEATURES

- Low phase noise XO output for the 48MHz to 96MHz range (-137 dBc at 10kHz offset).
- CMOS output.
- 12 to 24MHz crystal input.
- Integrated crystal load capacitor: no external load capacitor required.
- Low jitter (RMS): 3-6ps period, 7-10ps accum.
- 3.3V operation.
- Available in 8-Pin TSSOP or SOIC.

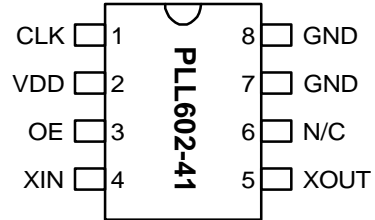
DESCRIPTIONS

The PLL602-41 is a low cost, high performance and low phase noise XO, providing less than -137dBc at 10kHz offset in the 48MHz to 96MHz operating range. The very low jitter (3 to 6 ps RMS period jitter and 7 to 10 ps RMS accumulated jitter) makes this chip ideal for applications requiring reference frequency sources. Input crystal can range from 12 to 24MHz (fundamental resonant mode).

BLOCK DIAGRAM



PIN CONFIGURATION



OUTPUT RANGE

MULTIPLIER	FREQUENCY RANGE	OUTPUT BUFFER
X4	48 - 96MHz	CMOS

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PIN DESCRIPTIONS

Name	Number	Type	Description
CLK	1	O	Output clock pin.
VDD	2	P	+3.3V VDD power supply pin.
OE	3	I	Output enable input pin. Disables (tri-state) output when low. Internal pull-up enables output by default if pin is not connected to low.
XIN	4	I	Crystal input pin.
XOUT	5	I	Crystal output pin.
N/C	6	-	Not connected.
GND	7, 8	P	Ground pin.

ELECTRICAL SPECIFICATIONS
1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{CC}	-0.5	7	V
Input Voltage Range	V_I	-0.5	$V_{CC}+0.5$	V
Output Voltage Range	V_O	-0.5	$V_{CC}+0.5$	V
Soldering Temperature			260	°C
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature		0	70	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. AC Specification

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Frequency		12		24	MHz
Output Frequency		48		96	MHz
Output Rise Time	0.8V to 2.0V with no load			1.5	ns
Output Fall Time	2.0V to 0.8V with no load			1.5	ns
Duty Cycle	At VDD/2	45	50	55	%

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3. Jitter and Phase Noise specification

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	With capacitive decoupling between VDD and GND. VIN = 3.3V		TBM		ps
Accumulated jitter RMS	With capacitive decoupling between VDD and GND. Over 10,000 cycles. VIN = 3.3V		TBM		ps
Phase Noise relative to carrier	100Hz offset, VIN = 3.3V		-101		dBc/Hz
Phase Noise relative to carrier	1kHz offset, VIN = 3.3V		-127		dBc/Hz
Phase Noise relative to carrier	10kHz offset, VIN = 3.3V		-137		dBc/Hz
Phase Noise relative to carrier	100kHz offset, VIN = 3.3V		-137		dBc/Hz

4. DC Specification

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Voltage	VDD		3.135		3.465	V
Input High Voltage	V _{IH}		2			V
Input Low Voltage	V _{IL}				0.8	V
Input High Voltage	V _{IH}	For XIN pin	(VDD/2) + 1	VDD/2		V
Input Low Voltage	V _{IL}	For XIN pin		VDD/2	(VDD/2) - 1	V
Output High Voltage	V _{OH}	I _{OH} = -25mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 25mA			0.4	V
Output High Voltage At CMOS Level	V _{OH}	I _{OH} = -8mA	VDD-0.4			V
Operating Supply Current	I _{DD}	No Load		35		mA
Short-circuit Current	I _S			±120		mA
Input Capacitance	C _{IN}	OE, Select Pins		5		pF

5. Crystal Specifications

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F _{XIN}	12		24	MHz
Crystal Loading Capacitance Rating	C _{L (xtal)}		TBD		pF
Driving power			1		mW
ESR	R _S			25	Ω

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PACKAGE INFORMATION

8 PIN (dimensions in mm)

Symbol	Narrow SOIC		TSSOP	
	Min.	Max.	Min.	Max.
A	1.47	1.73	-	1.20
A1	0.10	0.25	0.05	0.15
B	0.33	0.51	0.19	0.30
C	0.19	0.25	0.09	0.20
D	4.80	4.95	2.90	3.10
E	3.80	4.00	4.30	4.50
H	5.80	6.20	6.20	6.60
L	0.38	1.27	0.45	0.75
e	1.27 BSC		0.65 BSC	

ORDERING INFORMATION

For part ordering, please contact our Sales Department:
 47745 Fremont Blvd., Fremont, CA 94538, USA
 Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
 Device number, Package type and Operating temperature range

PLL602-41 X C

PART NUMBER _____

- _____ TEMPERATURE
 C=COMMERCIAL
 M=MILITARY
 I=INDUSTRIAL
- _____ PACKAGE TYPE
 S=SOIC, O=TSSOP, D=DIE

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