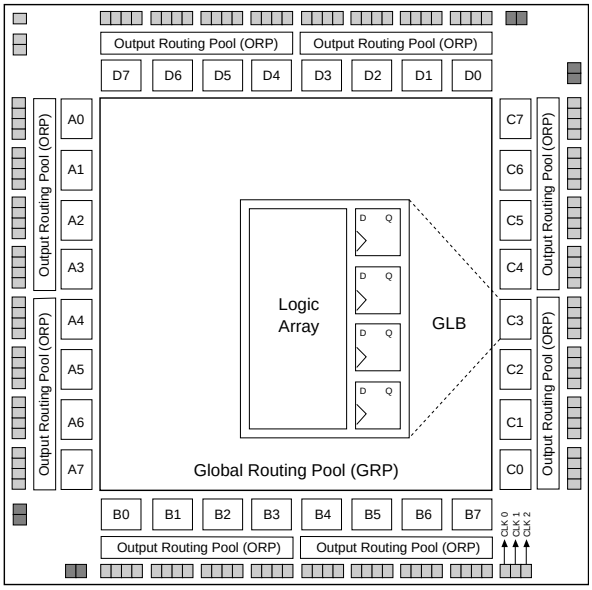
ispLSI® 2128VE

3.3V In-System Programmable SuperFAST™ High Density PLD

Features

- **SuperFAST HIGH DENSITY IN-SYSTEM PROGRAMMABLE LOGIC**
  - **— 6000 PLD Gates**
  - **— 128 and 64 I/O Pin Versions, Eight Dedicated Inputs**
  - **— 128 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
  - **— 100% Functional, JEDEC and Pinout Compatible with ispLSI 2128V Devices**
- **3.3V LOW VOLTAGE 2128 ARCHITECTURE**
  - **— Interfaces with Standard 5V TTL Devices**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— f_{max} = 250MHz Maximum Operating Frequency**
  - **— t_{pd} = 4.0ns Propagation Delay**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **IN-SYSTEM PROGRAMMABLE**
  - **— 3.3V In-System Programmability (ISP™) Using Boundary Scan Test Access Port (TAP)**
  - **— Open-Drain Output Option for Flexible Bus Interface Capability, Allowing Easy Implementation of Wired-OR Bus Arbitration Logic**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Prototyping**
- **100% IEEE 1149.1 BOUNDARY SCAN TESTABLE**
- **THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FPGAS**
  - **— Enhanced Pin Locking Capability**
  - **— Three Dedicated Clock Input Pins**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control**
  - **— Flexible Pin Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispDesignEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - **— Superior Quality of Results**
  - **— Tightly Integrated with Leading CAE Vendor Tools**
  - **— Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™**
  - **— PC and UNIX Platforms**

Functional Block Diagram*



*128 I/O Version Shown

Description

The ispLSI 2128VE is a High Density Programmable Logic Device available in 128 and 64 I/O-pin versions. The device contains 128 Registers, eight Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2128VE features in-system programmability through the Boundary Scan Test Access Port (TAP) and is 100% IEEE 1149.1 Boundary Scan Testable. The ispLSI 2128VE offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 2128VE device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. D7 (see Figure 1). There are a total of 32 GLBs in the ispLSI 2128VE device. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

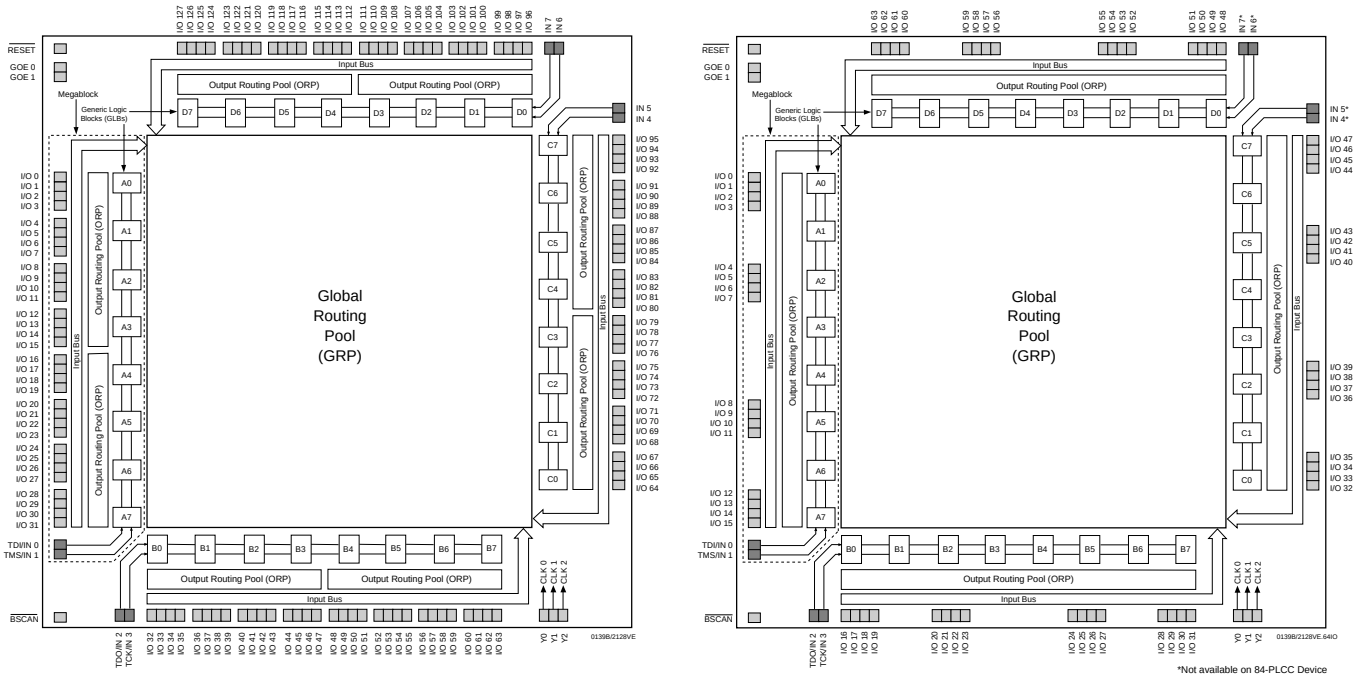
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September 2000

Functional Block Diagram

Figure 1. ispLSI 2128VE Functional Block Diagram (128-I/O and 64-I/O Versions)



The 128-I/O 2128VE contains 128 I/O cells, while the 64-I/O version contains 64 I/O cells. Each I/O cell is directly connected to an I/O pin and can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4mA or sink 8mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise. Device pins can be safely driven to 5V signal levels to support mixed-voltage systems.

Eight GLBs, 32 or 16 I/O cells, two dedicated inputs and two or one ORPs are connected together to make a Megablock (see Figure 1). The outputs of the eight GLBs are connected to a set of 32 or 16 universal I/O cells by the two or one ORPs. Each ispLSI 2128VE device contains four Megablocks.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 2128VE device are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Programmable Open-Drain Outputs

In addition to the standard output configuration, the outputs of the ispLSI 2128VE are individually programmable, either as a standard totem-pole output or an open-drain output. The totem-pole output drives the specified Voh and Vol levels, whereas the open-drain output drives only the specified Vol. The Voh level on the open-drain output depends on the external loading and pull-up. This output configuration is controlled by a programmable fuse. The default configuration when the device is in bulk erased state is totem-pole configuration. The open-drain/totem-pole option is selectable through the ispDesignEXPERT software tools.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +5.4V

Input Voltage Applied ..... -0.5 to +5.6V

Off-State Output Voltage Applied ..... -0.5 to +5.6V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to + 70°C	3.0	3.6	V
		Industrial	T_A = -40°C to + 85°C	3.0	3.6	V
V_{IL}	Input Low Voltage			V_{SS} – 0.5	0.8	V
V_{IH}	Input High Voltage			2.0	5.25	V

Table 2-0005/2128VE

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	V_{CC} = 3.3V, V_{IN} = 0.0V
C_2	I/O Capacitance	6	pf	V_{CC} = 3.3V, $V_{I/O}$ = 0.0V
C_3	Clock and Global Output Enable Capacitance	10	pf	V_{CC} = 3.3V, V_Y = 0.0V

Table 2-0006/2128VE

Erase Reprogram Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Erase/Reprogram Cycles	10,000	–	Cycles

Table 2-0008/2128VE

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 1.5ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

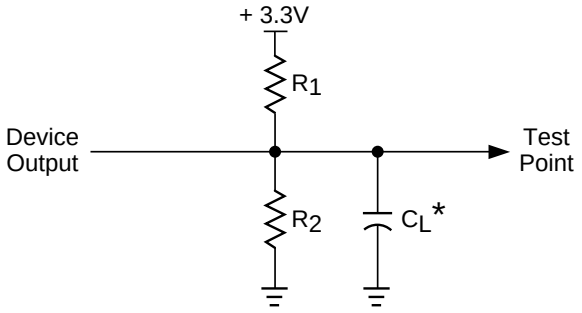
Table 2 - 0003/2128VE

Output Load Conditions (see Figure 2)

TEST CONDITION		R1	R2	CL
A		316Ω	348Ω	35pF
B	Active High	∞	348Ω	35pF
	Active Low	316Ω	348Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	348Ω	5pF
	Active Low to Z at V_{OL} +0.5V	316Ω	348Ω	5pF

Table 2-0004/2128VE

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A/2128VE

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	(V_{CC} - 0.2)V ≤ V_{IN} ≤ V_{CC}	–	–	10	µA
		V_{CC} ≤ V_{IN} ≤ 5.25V	–	–	10	µA
I_{IL-isp}	$\overline{BSCAN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 3.3V, V_{OUT} = 0.5V	–	–	-100	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V f_{CLOCK} = 1 MHz	–	195	–	mA

Table 2-0007/2128VE

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using eight 16-bit counters.
3. Typical values are at V_{CC} = 3.3V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC} .

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[3]	#	DESCRIPTION[1]	-250		-180		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	—	4.0	—	5.0	ns
t_{pd2}	A	2	Data Propagation Delay	—	6.0	—	7.5	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[2]	250	—	180	—	MHz
f_{max} (Ext.)	—	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	158.7	—	125	—	MHz
f_{max} (Tog.)	—	5	Clock Frequency, Max. Toggle	275	—	200	—	MHz
t_{su1}	—	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	2.5	—	3.5	—	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	—	3.0	—	3.5	ns
t_{h1}	—	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	—	0.0	—	ns
t_{su2}	—	9	GLB Reg. Setup Time before Clock	3.3	—	4.5	—	ns
t_{co2}	A	10	GLB Reg. Clock to Output Delay	—	3.7	—	4.5	ns
t_{h2}	—	11	GLB Reg. Hold Time after Clock	0.0	—	0.0	—	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay, ORP Bypass	—	6.0	—	7.0	ns
t_{rw1}	—	13	Ext. Reset Pulse Duration	3.5	—	4.0	—	ns
t_{ptoeen}	B	14	Input to Output Enable	—	6.0	—	10.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	—	6.0	—	10.0	ns
t_{goeen}	B	16	Global OE Output Enable	—	4.0	—	5.0	ns
t_{goedis}	C	17	Global OE Output Disable	—	4.0	—	5.0	ns
t_{wh}	—	18	External Synchronous Clock Pulse Duration, High	1.8	—	2.5	—	ns
t_{wl}	—	19	External Synchronous Clock Pulse Duration, Low	1.8	—	2.5	—	ns

1. Unless noted otherwise, all parameters use a GRP load of four, 20 PTXOR path, ORP and Y0 clock.
2. Standard 16-bit counter using GRP feedback.
3. Reference Switching Test Conditions section.

Table 2-0030A/2128VE
v.1.0

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[3]	#	DESCRIPTION[1]	-135		-100		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	—	7.5	—	10.0	ns
t_{pd2}	A	2	Data Propagation Delay	—	10.0	—	13.0	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[2]	135	—	100	—	MHz
f_{max} (Ext.)	—	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	100	—	77	—	MHz
f_{max} (Tog.)	—	5	Clock Frequency, Max. Toggle	143	—	100	—	MHz
t_{su1}	—	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	5.0	—	6.5	—	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	—	4.0	—	5.0	ns
t_{h1}	—	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	—	0.0	—	ns
t_{su2}	—	9	GLB Reg. Setup Time before Clock	6.0	—	8.0	—	ns
t_{co2}	A	10	GLB Reg. Clock to Output Delay	—	5.0	—	6.0	ns
t_{h2}	—	11	GLB Reg. Hold Time after Clock	0.0	—	0.0	—	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay, ORP Bypass	—	9.0	—	12.5	ns
t_{rw1}	—	13	Ext. Reset Pulse Duration	5.0	—	6.5	—	ns
t_{ptoeen}	B	14	Input to Output Enable	—	12.0	—	15.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	—	12.0	—	15.0	ns
t_{goeen}	B	16	Global OE Output Enable	—	7.0	—	9.0	ns
t_{goedis}	C	17	Global OE Output Disable	—	7.0	—	9.0	ns
t_{wh}	—	18	External Synchronous Clock Pulse Duration, High	3.5	—	5.0	—	ns
t_{wl}	—	19	External Synchronous Clock Pulse Duration, Low	3.5	—	5.0	—	ns

1. Unless noted otherwise, all parameters use a GRP load of four, 20 PTXOR path, ORP and Y0 clock.
2. Standard 16-bit counter using GRP feedback.
3. Reference Switching Test Conditions section.

Table 2-0030B/2128VE
v.1.0

Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-250		-180		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{io}	20	Input Buffer Delay	—	0.5	—	0.5	ns
t_{din}	21	Dedicated Input Delay	—	0.7	—	1.1	ns
GRP							
t_{grp}	22	GRP Delay	—	0.2	—	0.6	ns
GLB							
t_{4ptbpc}	23	4 Product Term Bypass Path Delay (Combinatorial)	—	1.5	—	1.9	ns
t_{4ptbpr}	24	4 Product Term Bypass Path Delay (Registered)	—	2.0	—	2.4	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	—	2.8	—	3.4	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	—	2.8	—	3.4	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	—	2.8	—	3.4	ns
t_{gbp}	28	GLB Register Bypass Delay	—	0.0	—	0.0	ns
t_{gsu}	29	GLB Register Setup Time before Clock	0.8	—	1.2	—	ns
t_{gh}	30	GLB Register Hold Time after Clock	1.7	—	2.3	—	ns
t_{gco}	31	GLB Register Clock to Output Delay	—	0.2	—	0.3	ns
t_{gro}	32	GLB Register Reset to Output Delay	—	0.3	—	0.6	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	—	3.7	—	4.3	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	—	2.9	—	5.9	ns
t_{ptck}	35	GLB Product Term Clock Delay	0.8	3.6	1.0	4.0	ns
ORP							
t_{orp}	36	ORP Delay	—	1.1	—	1.4	ns
t_{orpbp}	37	ORP Bypass Delay	—	0.4	—	0.4	ns
Outputs							
t_{ob}	38	Output Buffer Delay	—	1.4	—	1.6	ns
t_{sl}	39	Output Slew Limited Delay Adder	—	2.0	—	2.0	ns
t_{oen}	40	I/O Cell OE to Output Enabled	—	2.4	—	3.0	ns
t_{odis}	41	I/O Cell OE to Output Disabled	—	2.4	—	3.0	ns
t_{goe}	42	Global Output Enable	—	1.6	—	2.0	ns
Clocks							
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	1.0	1.0	1.2	1.2	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	1.2	1.2	1.4	1.4	ns
Global Reset							
t_{gr}	45	Global Reset to GLB	—	3.9	—	4.4	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Table 2-0036A/2128VE
v.1.0

Internal Timing Parameters[1]

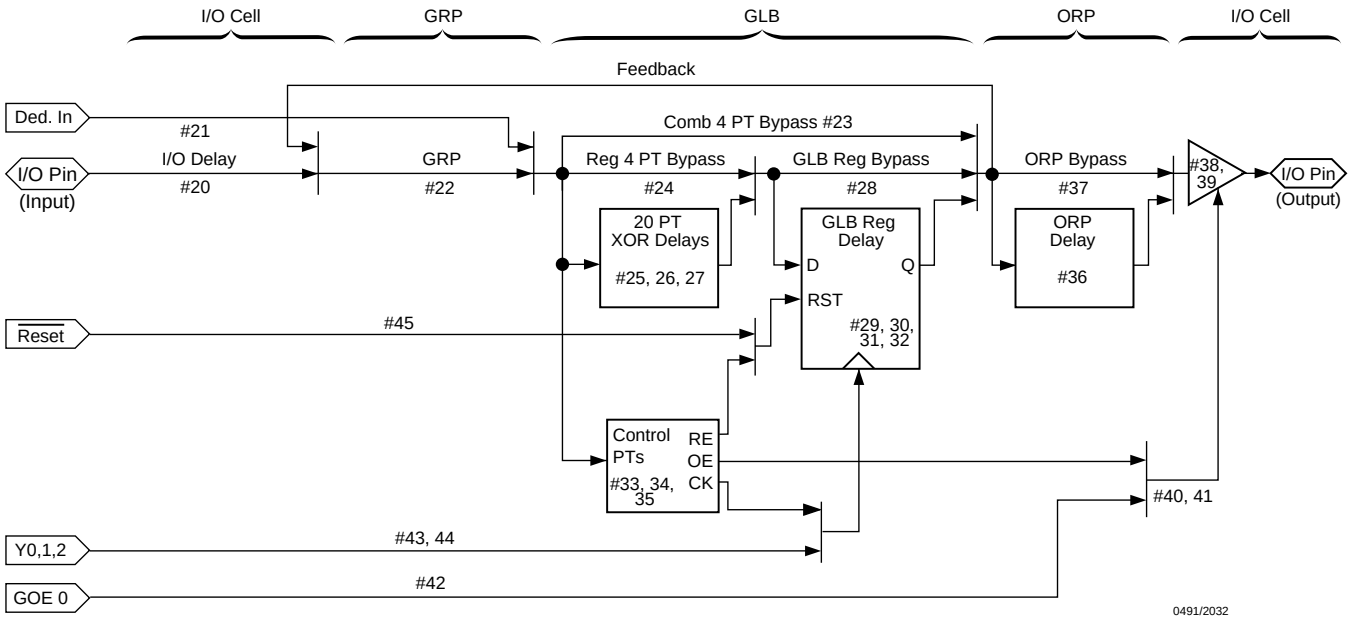
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-135		-100		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{io}	20	Input Buffer Delay	—	0.5	—	0.7	ns
t_{din}	21	Dedicated Input Delay	—	1.7	—	2.5	ns
GRP							
t_{grp}	22	GRP Delay	—	1.2	—	1.8	ns
GLB							
t_{4ptbpc}	23	4 Product Term Bypass Path Delay (Combinatorial)	—	3.7	—	5.2	ns
t_{4ptbpr}	24	4 Product Term Bypass Path Delay (Registered)	—	3.7	—	4.7	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	—	4.7	—	6.2	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	—	4.7	—	6.2	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	—	4.7	—	6.2	ns
t_{gbp}	28	GLB Register Bypass Delay	—	0.5	—	1.0	ns
t_{gsu}	29	GLB Register Setup Time before Clock	1.2	—	1.7	—	ns
t_{gh}	30	GLB Register Hold Time after Clock	3.8	—	4.8	—	ns
t_{gco}	31	GLB Register Clock to Output Delay	—	0.3	—	0.3	ns
t_{gro}	32	GLB Register Reset to Output Delay	—	1.1	—	3.1	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	—	6.1	—	7.1	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	—	6.9	—	9.1	ns
t_{ptck}	35	GLB Product Term Clock Delay	1.6	4.6	2.6	5.6	ns
ORP							
t_{orp}	36	ORP Delay	—	1.5	—	1.7	ns
t_{orpbp}	37	ORP Bypass Delay	—	0.5	—	0.7	ns
Outputs							
t_{ob}	38	Output Buffer Delay	—	1.6	—	1.6	ns
t_{sl}	39	Output Slew Limited Delay Adder	—	2.0	—	2.0	ns
t_{oen}	40	I/O Cell OE to Output Enabled	—	3.4	—	3.4	ns
t_{odis}	41	I/O Cell OE to Output Disabled	—	3.4	—	3.4	ns
t_{goe}	42	Global Output Enable	—	3.6	—	5.6	ns
Clocks							
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	1.6	1.6	2.4	2.4	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	1.8	1.8	2.6	2.6	ns
Global Reset							
t_{gr}	45	Global Reset to GLB	—	5.8	—	7.1	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Table 2-0036B/2128VE
v.1.0

ispLSI 2128VE Timing Model



Derivations of tsu, th and tco from the Product Term Clock

tsu = Logic + Reg su - Clock (min)
= (**t**io + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**io + **t**grp + **t**ptck(min))
= (#20 + #22 + #26) + (#29) - (#20 + #22 + #35)
2.8ns = (0.5 + 0.2 + 2.8) + (0.8) - (0.5 + 0.2 + 0.8)

th = Clock (max) + Reg h - Logic
= (**t**io + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**io + **t**grp + **t**20ptxor)
= (#20 + #22 + #35) + (#30) - (#20 + #22 + #26)
2.5ns = (0.5 + 0.2 + 3.6) + (1.7) - (0.5 + 0.2 + 2.8)

tco = Clock (max) + Reg co + Output
= (**t**io + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#20 + #22 + #35) + (#31) + (#36 + #38)
7.0ns = (0.5 + 0.2 + 3.6) + (0.2) + (1.1 + 1.4)

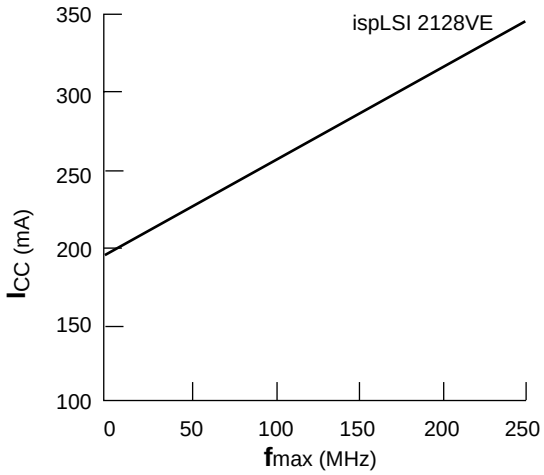
Note: Calculations are based upon timing specifications for the ispLSI 2128VE-250L.

Table 2-0042/2128VE
v.1.0

Power Consumption

Power consumption in the ispLSI 2128VE device depends on two primary factors: the speed at which the device is operating and the number of Product Terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of eight 16-bit counters
Typical current at 3.3V, 25¡ C

I_{CC} can be estimated for the ispLSI 2128VE using the following equation:

I_{CC} = 8 + (# of PTs * 0.669) + (# of nets * max freq * 0.0026)

Where:
- # of PTs = Number of Product Terms used in design
- # of nets = Number of Signals used in device
- Max freq = Highest Clock Frequency to the device (in MHz)

The I_{CC} estimate is based on typical conditions (V_{CC} = 3.3V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127/2128VE

Signal Descriptions

Signal Name	Description
$\overline{\text{RESET}}$	Active Low (0) Reset pin resets all the registers in the device.
GOE 0, GOE1	Global Output Enable input pins.
Y0, Y1, Y2	Dedicated Clock Input – These clock inputs are connected to one of the clock inputs of all the GLBs in the device.
$\overline{\text{BSCAN}}$	Input – Dedicated in-system programming Boundary Scan enable input pin. This pin is brought low to enable the programming mode. The TMS, TDI, TDO and TCK controls become active.
TDI/IN 0	Input – This pin performs two functions. When $\overline{\text{BSCAN}}$ is logic low, it functions as a serial data input pin to load programming data into the device. When $\overline{\text{BSCAN}}$ is high, it functions as a dedicated input pin.
TCK/IN 3	Input – This pin performs two functions. When $\overline{\text{BSCAN}}$ is logic low, it functions as a clock pin for the Boundary Scan state machine. When $\overline{\text{BSCAN}}$ is high, it functions as a dedicated input pin.
TMS/IN 1	Input – This pin performs two functions. When $\overline{\text{BSCAN}}$ is logic low, it functions as a mode control pin for the Boundary Scan state machine. When $\overline{\text{BSCAN}}$ is high, it functions as a dedicated input pin.
TDO/IN 2	Output/Input – This pin performs two functions. When $\overline{\text{BSCAN}}$ is logic low, it functions as an output pin to read serial shift register data. When $\overline{\text{BSCAN}}$ is high, it functions as a dedicated input pin.
IN 4 - IN 7	Dedicated Input Pins to the device.
GND	Ground (GND)
VCC	Vcc
NC[1]	No Connect
I/O	Input/Output Pins – These are the general purpose I/O pins used by the logic array.

1. NC pins are not to be connected to any active signals, VCC or GND.

Signal Locations

Signal	208-Ball fpBGA	176-Pin TQFP	160-Pin PQFP	100-Ball caBGA	100-Pin TQFP
$\overline{\text{RESET}}$	H3	21	19	D2	11
GOE 0, GOE 1	J16, H1	110, 23	100, 21	F9, E1	62, 13
Y0, Y1, Y2	H2, H14, J14	20, 113, 108	18, 103, 98	E3, F6, F8	10, 65, 60
$\overline{\text{BSCAN}}$	J1	25	23	E5	15
TDI/IN 0	J3	26	24	F2	16
TCK/IN 3	J15	107	97	G10	59
TMS/IN 1	P8	66	60	J5	37
TDO/IN 2	C9	154	140	B6	87
IN 4 - IN 7	H16, A9, T8, H4	114, 155, 67, 19	104, 141, 61, 17	E9, A6, K5, D1	66, 88, 38, 9
GND	D4, D13, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, N4, N13	24, 46, 68, 87, 109, 134, 153, 175	22, 42, 62, 79, 99, 122, 139, 159	B7, F1, G9, K6	14, 39, 61, 86
VCC	D5, D6, D12, E4, E13, F4, F13, L4, L13, M4, M13, N5, N11, N12	2, 22, 43, 65, 90, 111, 131, 156	2, 20, 39, 59, 82, 101, 119, 142	A5, E2, F10, J4	12, 36, 63, 89
NC[1]	A2, A3, A15, A16, B1, B2, B3, B14, B15, B16, C2, C3, C14, C15, D14, P1, P2, P3, P13, P14, P15, R1, R2, R3, R14, R15, R16, T1, T2, T15, T16	9, 18, 27, 36, 55, 64, 69, 78, 97, 106, 112, 115, 124, 143, 152, 157, 166	102	A8, C3, C4, D6, D8, E7, E10, F4, G3, G5, H7, H8, K3	4, 21, 25, 31, 44, 50, 54, 64, 71, 75, 81, 94, 100

1. NC pins are not to be connected to any active signals, VCC or GND.

I/O Locations

Signal	208 fpBGA	176 TQFP	160 PQFP	100 caBGA	100 TQFP	Signal	208 fpBGA	176 TQFP	160 PQFP	100 caBGA	100 TQFP
I/O 0	J2	28	25	G1	17	I/O 64	H15	116	105	—	—
I/O 1	J4	29	26	F3	18	I/O 65	H13	117	106	—	—
I/O 2	K1	30	27	E4	19	I/O 66	G16	118	107	—	—
I/O 3	K3	31	28	H1	20	I/O 67	G14	119	108	—	—
I/O 4	K2	32	29	G2	22	I/O 68	G15	120	109	—	—
I/O 5	K4	33	30	J1	23	I/O 69	G13	121	110	—	—
I/O 6	L1	34	31	H2	24	I/O 70	F16	122	111	—	—
I/O 7	L2	35	32	K1	26	I/O 71	F14	123	112	—	—
I/O 8	L3	37	33	J2	27	I/O 72	F15	125	113	—	—
I/O 9	M1	38	34	K2	28	I/O 73	E16	126	114	—	—
I/O 10	M2	39	35	H3	29	I/O 74	E14	127	115	—	—
I/O 11	M3	40	36	J3	30	I/O 75	E15	128	116	—	—
I/O 12	N1	41	37	G4	32	I/O 76	D16	129	117	—	—
I/O 13	N2	42	38	H4	33	I/O 77	C16	130	118	—	—
I/O 14	N3	44	40	K4	34	I/O 78	D15	132	120	—	—
I/O 15	P4	45	41	H5	35	I/O 79	A14	133	121	—	—
I/O 16	T3	47	43	F5	40	I/O 80	C13	135	123	—	—
I/O 17	R4	48	44	J6	41	I/O 81	B13	136	124	—	—
I/O 18	T4	49	45	K7	42	I/O 82	A13	137	125	—	—
I/O 19	P5	50	46	H6	43	I/O 83	C12	138	126	—	—
I/O 20	R5	51	47	K8	45	I/O 84	B12	139	127	—	—
I/O 21	N6	52	48	G6	46	I/O 85	D11	140	128	—	—
I/O 22	T5	53	49	J7	47	I/O 86	A12	141	129	—	—
I/O 23	R6	54	50	K9	48	I/O 87	C11	142	130	—	—
I/O 24	P6	56	51	J8	49	I/O 88	B11	144	131	—	—
I/O 25	T6	57	52	K10	51	I/O 89	D10	145	132	—	—
I/O 26	N7	58	53	J9	52	I/O 90	A11	146	133	—	—
I/O 27	R7	59	54	J10	53	I/O 91	B10	147	134	—	—
I/O 28	P7	60	55	H9	55	I/O 92	C10	148	135	—	—
I/O 29	T7	61	56	H10	56	I/O 93	D9	149	136	—	—
I/O 30	N8	62	57	G7	57	I/O 94	A10	150	137	—	—
I/O 31	R8	63	58	G8	58	I/O 95	B9	151	138	—	—
I/O 32	T9	70	63	D10	67	I/O 96	A8	158	143	—	—
I/O 33	P9	71	64	E8	68	I/O 97	C8	159	144	—	—
I/O 34	R9	72	65	F7	69	I/O 98	B8	160	145	—	—
I/O 35	N9	73	66	C10	70	I/O 99	D8	161	146	—	—
I/O 36	T10	74	67	D9	72	I/O 100	A7	162	147	—	—
I/O 37	P10	75	68	B10	73	I/O 101	C7	163	148	—	—
I/O 38	R10	76	69	C9	74	I/O 102	B7	164	149	—	—
I/O 39	N10	77	70	A10	76	I/O 103	D7	165	150	—	—
I/O 40	T11	79	71	B9	77	I/O 104	A6	167	151	—	—
I/O 41	P11	80	72	A9	78	I/O 105	C6	168	152	—	—
I/O 42	R11	81	73	C8	79	I/O 106	B6	169	153	—	—
I/O 43	T12	82	74	B8	80	I/O 107	A5	170	154	—	—
I/O 44	P12	83	75	D7	82	I/O 108	C5	171	155	—	—
I/O 45	R12	84	76	C7	83	I/O 109	B5	172	156	—	—
I/O 46	T13	85	77	A7	84	I/O 110	A4	173	157	—	—
I/O 47	R13	86	78	C6	85	I/O 111	B4	174	158	—	—
I/O 48	T14	88	80	E6	90	I/O 112	C4	176	160	—	—
I/O 49	N14	89	81	B5	91	I/O 113	A1	1	1	—	—
I/O 50	P16	91	83	A4	92	I/O 114	C1	3	3	—	—
I/O 51	N15	92	84	C5	93	I/O 115	D3	4	4	—	—
I/O 52	N16	93	85	A3	95	I/O 116	D2	5	5	—	—
I/O 53	M14	94	86	D5	96	I/O 117	D1	6	6	—	—
I/O 54	M15	95	87	B4	97	I/O 118	E3	7	7	—	—
I/O 55	M16	96	88	A2	98	I/O 119	E2	8	8	—	—
I/O 56	L15	98	89	B3	99	I/O 120	E1	10	9	—	—
I/O 57	L14	99	90	A1	1	I/O 121	F3	11	10	—	—
I/O 58	L16	100	91	B2	2	I/O 122	F2	12	11	—	—
I/O 59	K13	101	92	B1	3	I/O 123	F1	13	12	—	—
I/O 60	K15	102	93	C2	5	I/O 124	G4	14	13	—	—
I/O 61	K14	103	94	C1	6	I/O 125	G2	15	14	—	—
I/O 62	K16	104	95	D4	7	I/O 126	G3	16	15	—	—
I/O 63	J13	105	96	D3	8	I/O 127	G1	17	16	—	—

Signal Configuration

ispLSI 2128VE 208-Ball fpBGA Signal Diagram

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	NC[1]	NC[1]	I/O 79	I/O 82	I/O 86	I/O 90	I/O 94	IN 5	I/O 96	I/O 100	I/O 104	I/O 107	I/O 110	NC[1]	NC[1]	I/O 113	**A**
B	NC[1]	NC[1]	NC[1]	I/O 81	I/O 84	I/O 88	I/O 91	I/O 95	I/O 98	I/O 102	I/O 106	I/O 109	I/O 111	NC[1]	NC[1]	NC[1]	**B**
C	I/O 77	NC[1]	NC[1]	I/O 80	I/O 83	I/O 87	I/O 92	TDO/ IN 2	I/O 97	I/O 101	I/O 105	I/O 108	I/O 112	NC[1]	NC[1]	I/O 114	**C**
D	I/O 76	I/O 78	NC[1]	GND	VCC	I/O 85	I/O 89	I/O 93	I/O 99	I/O 103	VCC	VCC	GND	I/O 115	I/O 116	I/O 117	**D**
E	I/O 73	I/O 75	I/O 74	VCC									VCC	I/O 118	I/O 119	I/O 120	**E**
F	I/O 70	I/O 72	I/O 71	VCC									VCC	I/O 121	I/O 122	I/O 123	**F**
G	I/O 66	I/O 68	I/O 67	I/O 69			GND	GND	GND	GND			I/O 124	I/O 126	I/O 125	I/O 127	**G**
H	IN 4	I/O 64	Y1	I/O 65			GND	GND	GND	GND			IN 7	$\overline{\text{RESET}}$	Y0	GOE 1	**H**
J	GOE 0	TCK/ IN 3	Y2	I/O 63			GND	GND	GND	GND			I/O 1	TDI/ IN 0	I/O 0	$\overline{\text{BSCAN}}$	**J**
K	I/O 62	I/O 60	I/O 61	I/O 59			GND	GND	GND	GND			I/O 5	I/O 3	I/O 4	I/O 2	**K**
L	I/O 58	I/O 56	I/O 57	VCC									VCC	I/O 8	I/O 7	I/O 6	**L**
M	I/O 55	I/O 54	I/O 53	VCC									VCC	I/O 11	I/O 10	I/O 9	**M**
N	I/O 52	I/O 51	I/O 49	GND	VCC	VCC	I/O 39	I/O 35	I/O 30	I/O 26	I/O 21	VCC	GND	I/O 14	I/O 13	I/O 12	**N**
P	I/O 50	NC[1]	NC[1]	NC[1]	I/O 44	I/O 41	I/O 37	I/O 33	TMS/ IN 1	I/O 28	I/O 24	I/O 19	I/O 15	NC[1]	NC[1]	NC[1]	**P**
R	NC[1]	NC[1]	NC[1]	I/O 47	I/O 45	I/O 42	I/O 38	I/O 34	I/O 31	I/O 27	I/O 23	I/O 20	I/O 17	NC[1]	NC[1]	NC[1]	**R**
T	NC[1]	NC[1]	I/O 48	I/O 46	I/O 43	I/O 40	I/O 36	I/O 32	IN 6	I/O 29	I/O 25	I/O 22	I/O 18	I/O 16	NC[1]	NC[1]	**T**
	16	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	

ispLSI 2128VE

Bottom View

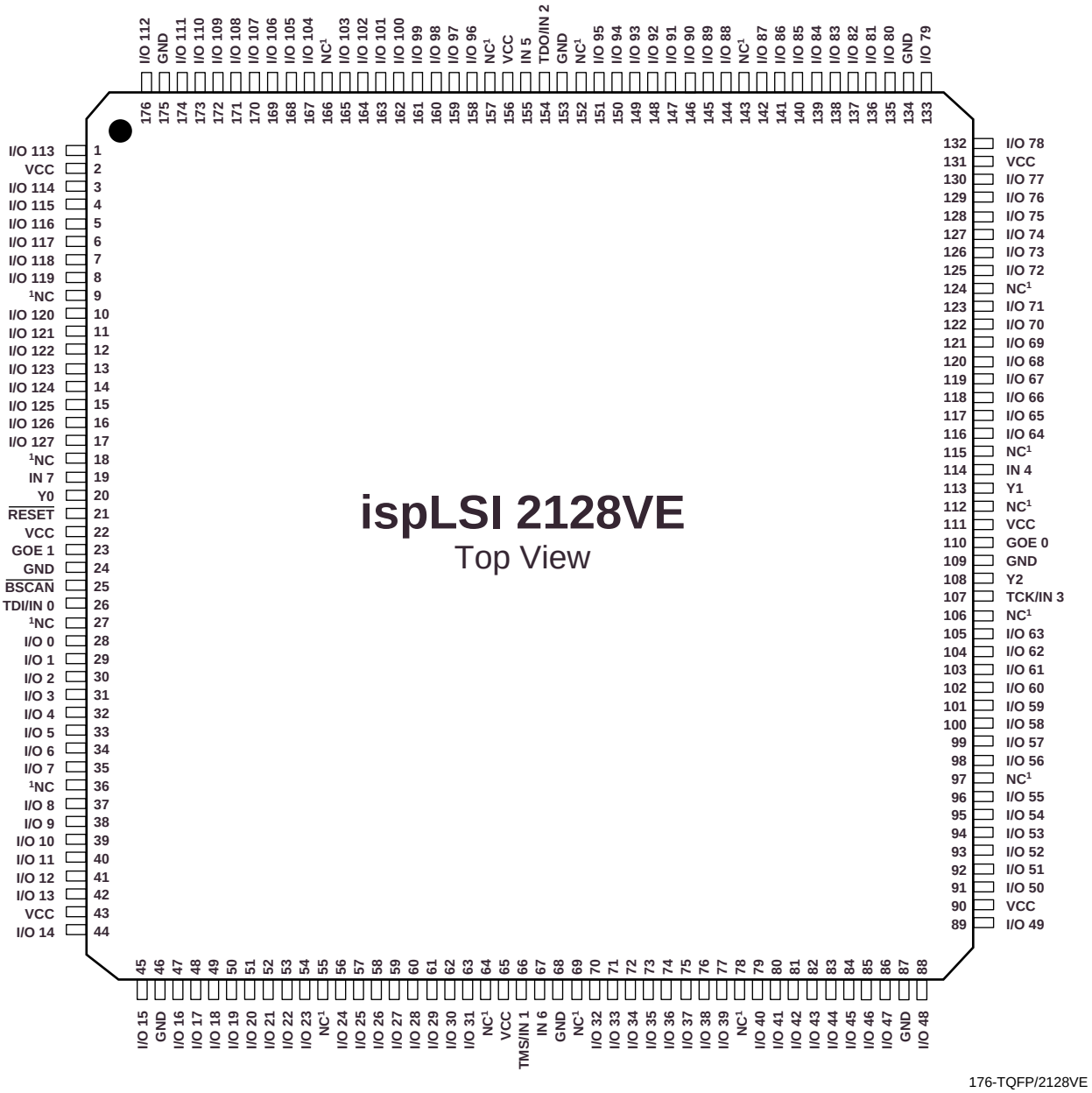
208 BGA/2128VE

1. NCs are not to be connected to any active signals, Vcc or GND.

Note: Ball A1 indicator dot on top side of package.

Pin Configuration

ispLSI 2128VE 176-Pin TQFP Pinout Diagram

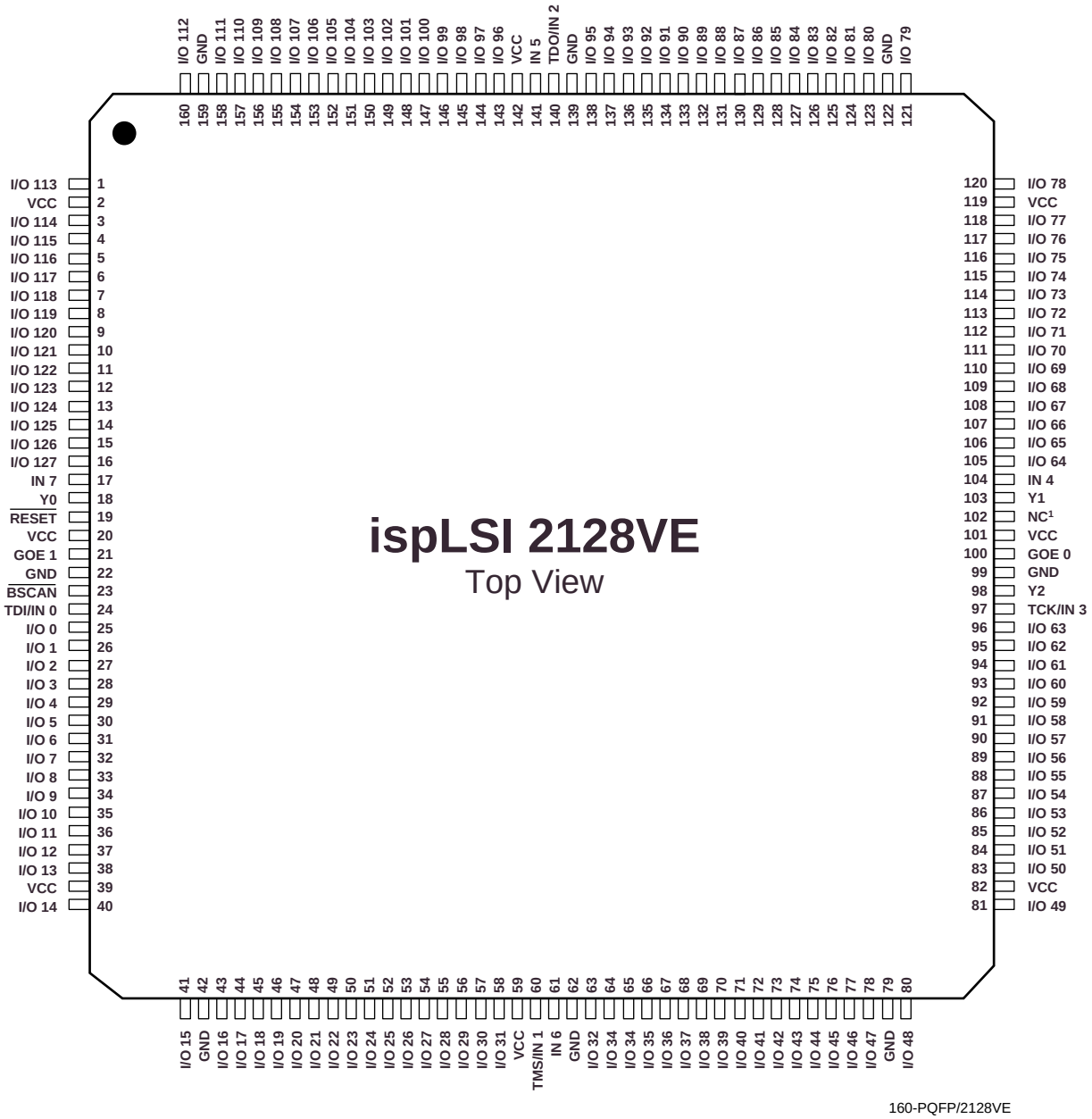


176-TQFP/2128VE

1. NC pins are not to be connected to any active signals, VCC or GND.

Pin Configuration

ispLSI 2128VE 160-Pin PQFP Pinout Diagram

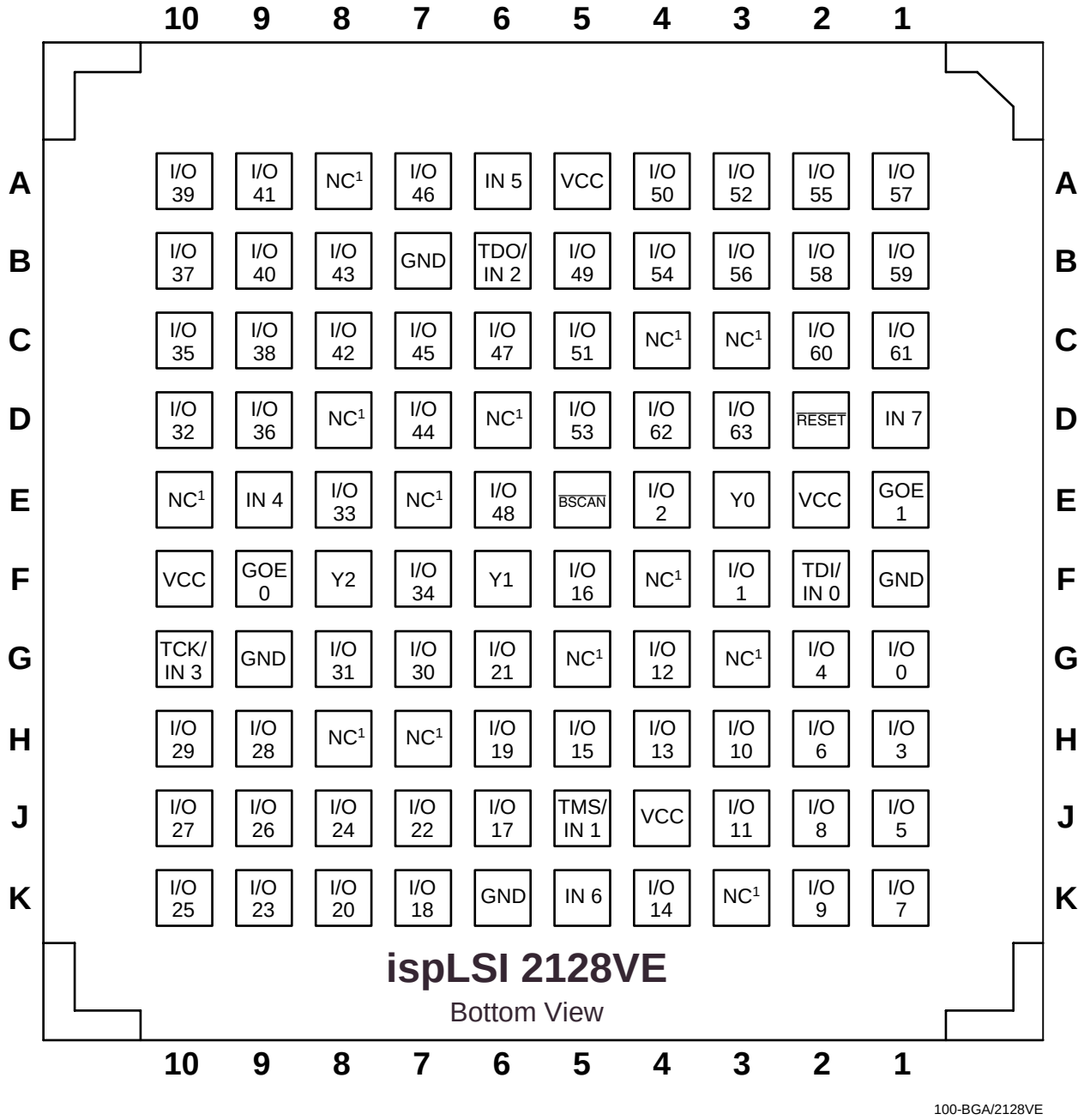


160-PQFP/2128VE

1. NC pins are not to be connected to any active signal, VCC or GND.

Signal Configuration

ispLSI 2128VE 100-Ball caBGA Signal Diagram



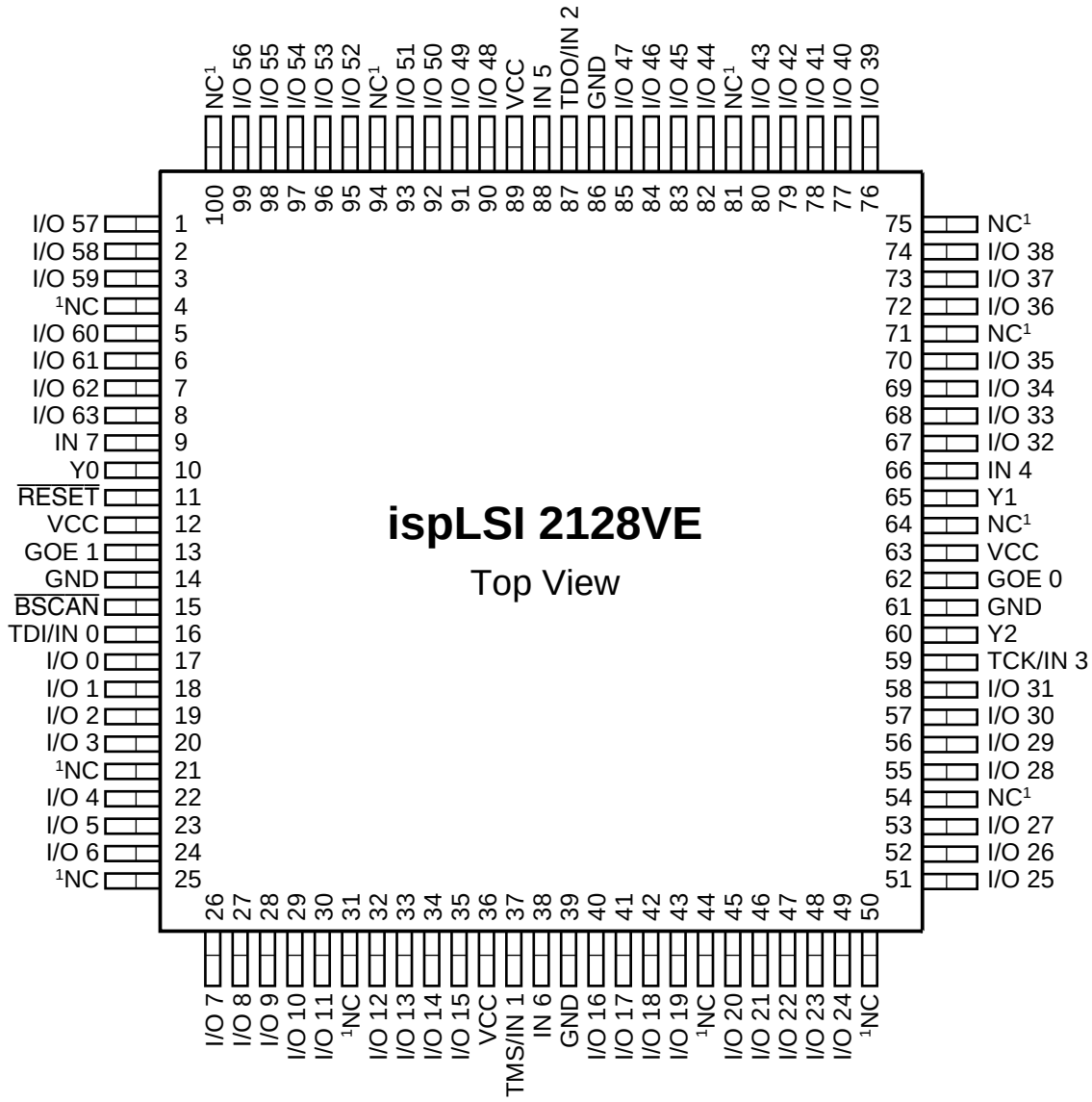
100-BGA/2128VE

[1]NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Pin Configuration

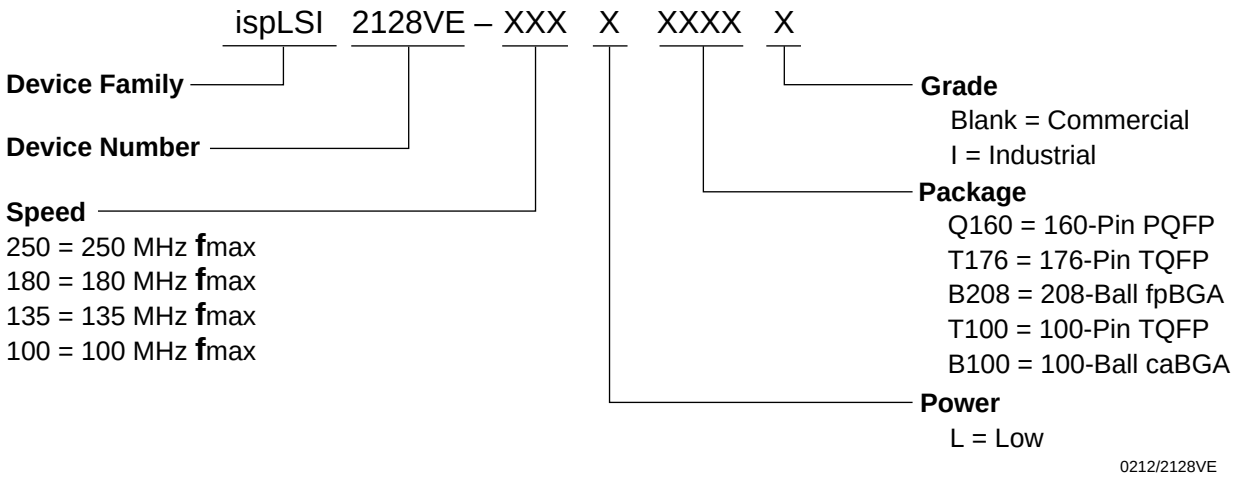
ispLSI 2128VE 100-Pin TQFP Pinout Diagram



100-TQFP/2128VE

1. NC pins are not to be connected to any active signals, VCC or GND.

Part Number Description



0212/2128VE

ispLSI 2128VE Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	I/Os	ORDERING NUMBER	PACKAGE
ispLSI	250	4.0	128	ispLSI 2128VE-250LT176	176-Pin TQFP
	250	4.0	128	ispLSI 2128VE-250LQ160	160-Pin PQFP
	250	4.0	128	ispLSI 2128VE-250LB208	208-Ball fpBGA
	180	5.0	128	ispLSI 2128VE-180LT176	176-Pin TQFP
	180	5.0	128	ispLSI 2128VE-180LQ160	160-Pin PQFP
	180	5.0	128	ispLSI 2128VE-180LB208	208-Ball fpBGA
	180	5.0	64	ispLSI 2128VE-180LT100	100-Pin TQFP
	180	5.0	64	ispLSI 2128VE-180LB100	100-Ball caBGA
	135	7.5	128	ispLSI 2128VE-135LT176	176-Pin TQFP
	135	7.5	128	ispLSI 2128VE-135LQ160	160-Pin PQFP
	135	7.5	128	ispLSI 2128VE-135LB208	208-Ball fpBGA
	135	7.5	64	ispLSI 2128VE-135LT100	100-Pin TQFP
	135	7.5	64	ispLSI 2128VE-135LB100	100-Ball caBGA
	100	10	128	ispLSI 2128VE-100LT176	176-Pin TQFP
	100	10	128	ispLSI 2128VE-100LQ160	160-Pin PQFP
	100	10	128	ispLSI 2128VE-100LB208	208-Ball fpBGA
	100	10	64	ispLSI 2128VE-100LT100	100-Pin TQFP
	100	10	64	ispLSI 2128VE-100LB100	100-Ball caBGA

Table 2-0041A/2128VE

INDUSTRIAL

FAMILY	fmax (MHz)	tpd (ns)	I/Os	ORDERING NUMBER	PACKAGE
ispLSI	135	7.5	64	ispLSI 2128VE-135LT100I	100-Pin TQFP
	135	7.5	128	ispLSI 2128VE-135LT176I	176-Pin TQFP

Table 2-0041B/2128VE