Dual RF/IF PLL Frequency Synthesizers

ADF4210/ADF4211/ADF4212/ADF4213

FEATURES

ADF4210: 550 MHz/1.2 GHz
ADF4211: 550 MHz/2.0 GHz
ADF4212: 1.0 GHz/2.7 GHz
ADF4213: 1.0 GHz/3 GHz
2.7 V to 5.5 V Power Supply
Separate Charge Pump Supply (V_P) Allows Extended Tuning Voltage in 3 V Systems
Programmable Dual Modulus Prescaler
RF and IF: 8/9, 16/17, 32/33, 64/65
Programmable Charge Pump Currents
3-Wire Serial Interface
Analog and Digital Lock Detect
Fastlock Mode
Power-Down Mode

APPLICATIONS

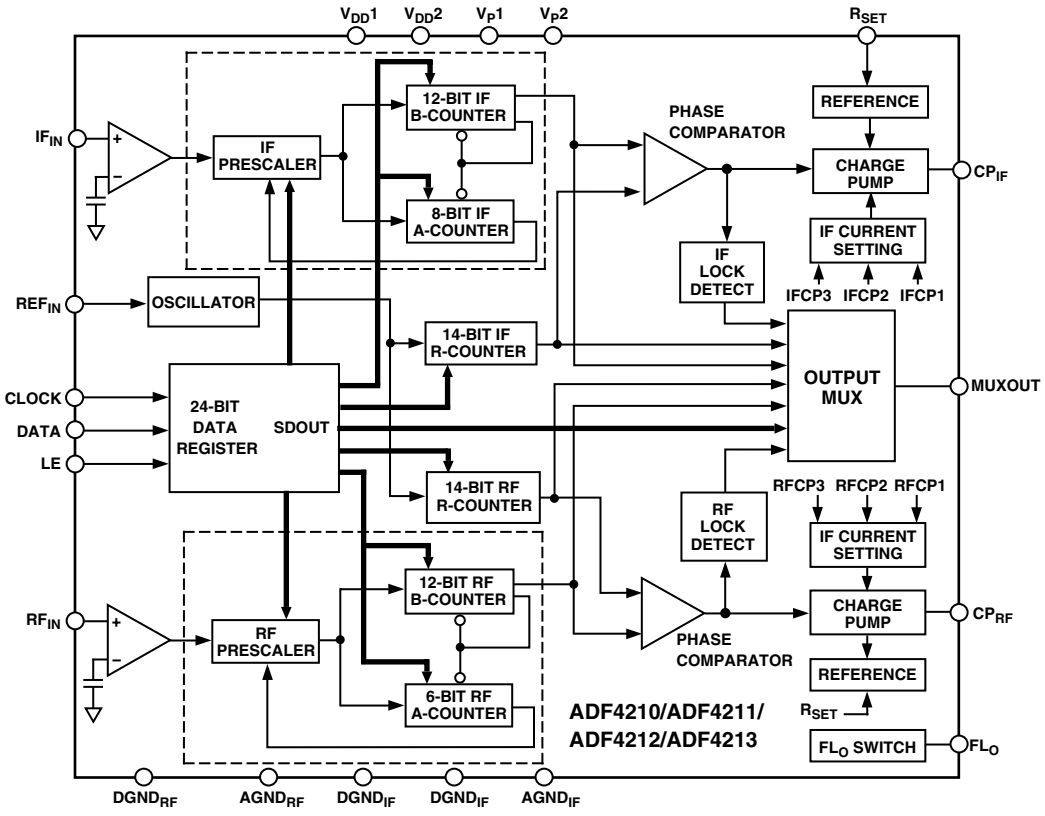
Base Stations for Wireless Radio (GSM, PCS, DCS, CDMA, WCDMA)
Wireless Handsets (GSM, PCS, DCS, CDMA, WCDMA)
Wireless LANS
Communications Test Equipment
CATV Equipment

GENERAL DESCRIPTION

The ADF4210/ADF4211/ADF4212/ADF4213 is a dual frequency synthesizer that can be used to implement local oscillators (LO) in the upconversion and downconversion sections of wireless receivers and transmitters. They can provide the LO for both the RF and IF sections. They consist of a low-noise digital PFD (Phase Frequency Detector), a precision charge pump, a programmable reference divider, programmable A and B Counters and a dual-modulus prescaler (P/P + 1). The A (6-bit) and B (12-bit) counters, in conjunction with the dual modulus prescaler (P/P + 1), implement an N divider (N = BP + A). In addition, the 14-bit reference counter (R Counter), allows selectable REFIN frequencies at the PFD input. A complete PLL (Phase-Locked Loop) can be implemented if the synthesizer is used with an external loop filter and VCO (Voltage Controlled Oscillators).

Control of all the on-chip registers is via a simple 3-wire interface. The devices operate with a power supply ranging from 2.7 V to 5 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM



REV. A

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ADF4210/ADF4211/ADF4212/ADF4213–SPECIFICATIONS[1]

($V_{DD}1 = V_{DD}2 = 3$ V ± 10%, 5 V ± 10%; $V_{DD}1$, $V_{DD}2 \le V_P1$, $V_P2 \le 6.0$ V; $AGND_{RF} = DGND_{RF} = AGND_{IF} = DGND_{IF} = 0$ V; $R_{SET} = 2.7$ kΩ dBm to 50 Ω; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.)

Parameter	B Version	B Chips[2]	Unit	Test Conditions/Comments
RF/IF CHARACTERISTICS (3 V)				
RF Input Frequency (RF_{IN})				See Figure 3 for Input Circuit.
ADF4210	0.1/1.2	0.1/1.2	GHz min/max	Use a square wave for frequencies lower than F_{MIN}.
ADF4211	0.1/2.0	0.1/2.0	GHz min/max	
ADF4212	0.15/2.7	0.15/2.7	GHz min/max	
ADF4213	0.2/3.0	0.2/3.0	GHz min/max	
RF Input Sensitivity	–10/0	–10/0	dBm min/max	
IF Input Frequency (IF_{IN})				
ADF4210	60/550	60/550	MHz min/max	
ADF4211	60/550	60/550	MHz min/max	
ADF4212	0.06/1.0	0.06/1.0	GHz min/max	
ADF4213	0.06/1.0	0.06/1.0	GHz min/max	
IF Input Sensitivity	–10/0	–10/0	dBm min/max	
Maximum Allowable Prescaler Output Frequency[3]	165	165	MHz max	
RF/IF CHARACTERISTICS (5 V)				
RF Input Frequency (RF_{IN})				See Figure 3 for Input Circuit.
ADF4210	0.18/1.2	0.18/1.2	GHz min/max	Use a square wave for frequencies lower than F_{MIN}.
ADF4211	0.18/2.0	0.18/2.0	GHz min/max	
ADF4212	0.2/2.3	0.2/2.3	GHz min/max	
ADF4213	0.2/2.5	0.2/2.5	GHz min/max	
RF Input Sensitivity	–5/0	–5/0	dBm min/max	
IF Input Frequency (IF_{IN})				
ADF4210	100/550	100/550	MHz min/max	
ADF4211	100/550	100/550	MHz min/max	
ADF4212	0.1/1.0	0.1/1.0	GHz min/max	
ADF4213	0.1/1.0	0.1/1.0	GHz min/max	
IF Input Sensitivity	–5/0	–5/0	dBm min/max	
Maximum Allowable Prescaler Output Frequency[3]	200	200	MHz max	
REFIN CHARACTERISTICS				See Figure 2 for Input Circuit.
REFIN Input Frequency	0/115	0/115	MHz min/max	For F < 5 MHz, use dc-coupled square wave (0 to V_{DD}).
REFIN Input Sensitivity[4]	–5/0	–5/0	dBm min/max	AC-Coupled. When dc-coupled, 0 to V_{DD} max (CMOS-Compatible)
REFIN Input Capacitance	10	10	pF max	
REFIN Input Current	±100	±100	µA max	
PHASE DETECTOR				
Phase Detector Frequency[5]	55	55	MHz max	
CHARGE PUMP				
I_{CP} Sink/Source				Programmable: See Table V
High Value	5	5	mA typ	With $R_{SET} = 2.7$ kΩ
Low Value	625	625	µA typ	
Absolute Accuracy	3	3	% typ	With $R_{SET} = 2.7$ kΩ
R_{SET} Range	1.5/5.6	1.5/5.6	kΩ, min/max	
I_{CP} Three-State Leakage Current	1	1	nA typ	
Sink and Source Current Matching	2	2	% typ	$0.5 \text{ V} \le V_{CP} \le V_P - 0.5$ V
I_{CP} vs. V_{CP}	2	2	% typ	$0.5 \text{ V} \le V_{CP} \le V_P - 0.5$ V
I_{CP} vs. Temperature	2	2	% typ	$V_{CP} = V_P/2$
LOGIC INPUTS				
V_{INH}, Input High Voltage	$0.8 \times DV_{DD}$	$0.8 \times DV_{DD}$	V min	
V_{INL}, Input Low Voltage	$0.2 \times DV_{DD}$	$0.2 \times DV_{DD}$	V max	
I_{INH}/I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	$DV_{DD} - 0.4$	$DV_{DD} - 0.4$	V min	$I_{OH} = 500$ µA
V_{OL}, Output Low Voltage	0.4	0.4	V max	$I_{OL} = 500$ µA

Parameter	B Version	B Chips[2]	Unit	Test Conditions/Comments
POWER SUPPLIES				
$V_{DD}1$	2.7/5.5	2.7/5.5	V min/V max	
$V_{DD}2$	$V_{DD}1$	$V_{DD}1$		
V_P	$V_{DD}1$/6.0	$V_{DD}1$/6.0	V min/V max	$V_{DD}1$, $V_{DD}2 \leq V_{DD}1$, $V_{DD}2 \leq 6.0$ V
I_{DD} (RF + IF)[6]				
ADF4210	11.5	11.5	mA max	9.0 mA typical
ADF4211	15.0	15.0	mA max	11.0 mA typical
ADF4212	17.5	17.5	mA max	13.0 mA typical
ADF4213	20	20	mA max	15 mA typical
I_{DD} (RF Only)				
ADF4210	6.75	6.75	mA max	5.0 mA typical
ADF4211	10	10	mA max	7.0 mA typical
ADF4212	12.5	12.5	mA max	9.0 mA typical
ADF4213	15	15	mA max	11 mA typical
I_{DD} (IF Only)				
ADF4210	5.5	5.5	mA max	4.5 mA typical
ADF4211	5.5	5.5	mA max	4.5 mA typical
ADF4212	5.5	5.5	mA max	4.5 mA typical
ADF4213	5.5	5.5	mA max	4.5 mA typical
I_P (I_P1 + I_P2)	1.0	1.0	mA max	T_A = 25°C, 0.55 mA typical
Low-Power Sleep Mode	1	1	µA typ	
NOISE CHARACTERISTICS				
ADF4213 Phase Noise Floor[7]	–171	–171	dBc/Hz typ	@ 25 kHz PFD Frequency
	–164	–164	dBc/Hz typ	@ 200 kHz PFD Frequency
Phase Noise Performance[8]				@ VCO Output
ADF4210/ADF4211, IF: 540 MHz Output[9]	–91	–91	dBc/Hz typ	@ 1 kHz Offset and 200 kHz PFD Frequency
ADF4212/ADF4213, IF: 900 MHz Output[10]	–89	–89	dBc/Hz typ	See Note 11
ADF4210/ADF4211, RF: 900 MHz Output[10]	–89	–89	dBc/Hz typ	See Note 11
ADF4212/ADF4213, RF: 900 MHz Output[10]	–91	–91	dBc/Hz typ	See Note 11
ADF4211/ADF4212, RF: 1750 MHz Output[12]	–85	–85	dBc/Hz typ	See Note 11
ADF4211/ADF4212, RF: 1750 MHz Output[13]	–67	–67	dBc/Hz typ	@ 200 Hz Offset and 10 kHz PFD Frequency
ADF4212/ADF4213, RF: 2400 MHz Output[14]	–88	–88	dBc/Hz typ	@ 1 kHz Offset and 1 MHz PFD Frequency
Spurious Signals				
ADF4210/ADF4211, IF: 540 MHz Output[9]	–88/–90	–88/–90	dB typ	@ 200 kHz/400 kHz and 200 kHz PFD Frequency
ADF4212/ADF4213, IF: 900 MHz Output[10]	–90/–94	–90/–94	dB typ	See Note 11
ADF4210/ADF4211, RF: 900 MHz Output[10]	–90/–94	–90/–94	dB typ	See Note 11
ADF4212/ADF4213, RF: 900 MHz Output[10]	–90/–94	–90/–94	dB typ	See Note 11
ADF4211/ADF4212, RF: 1750 MHz Output[12]	–80/–82	–80/–82	dB typ	See Note 11
ADF4211/ADF4212, RF: 1750 MHz Output[13]	–65/–70	–65/–70	dB typ	@ 10 kHz/20 kHz and 10 kHz PFD Frequency
ADF4212/ADF4213, RF: 2400 MHz Output[14]	–80/–82	–80/–82	dB typ	@ 200 kHz/400 kHz and 200 kHz PFD Frequency

NOTES

[1]Operating temperature range is as follows: B Version: –40°C to +85°C.

[2]The B Chip specifications are given as typical values.

[3]This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the IF/RF input is divided down to a frequency that is less than this value.

[4]$V_{DD}1 = V_{DD}2$ = 3 V; For $V_{DD}1 = V_{DD}2$ = 5 V, use CMOS-compatible levels, T_A = 25°C.

[5]Guaranteed by design. Sample tested to ensure compliance.

[6]V_{DD} = 3 V; P = 16; RF_{IN} = 900 MHz; IF_{IN} = 540 MHz, T_A = 25°C.

[7]The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 logN (where N is the N divider value). See TPC 16.

[8]The phase noise is measured with the EVAL-ADF4210/ADF4212/ADF4213EB Evaluation Board and the HP8562E Spectrum Analyzer. The spectrum analyzer provides the REFIN for the synthesizer (f_{REFOUT} = 10 MHz @ 0 dBm).

[9]f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{IF} = 540 MHz; N = 2700; Loop B/W = 20 kHz.

[10]f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{RF} = 900 MHz; N = 4500; Loop B/W = 20 kHz.

[11]Same conditions as listed in Note 10.

[12]f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; Offset frequency = 1 kHz; f_{RF} = 1750 MHz; N = 8750; Loop B/W = 20 kHz.

[13]f_{REFIN} = 10 MHz; f_{PFD} = 10 kHz; Offset frequency = 200 Hz; f_{RF} = 1750 MHz; N = 175000; Loop B/W = 1 kHz.

[14]f_{REFIN} = 10 MHz; f_{PFD} = 1 MHz; Offset frequency = 1 kHz; f_{RF} = 1960 MHz; N = 9800; Loop B/W = 20 kHz.

Specifications subject to change without notice.

TIMING CHARACTERISTICS

($V_{DD}1 = V_{DD}2 = 3\ V \pm 10\%, 5\ V \pm 10\%$; $V_{DD}1, V_{DD}2 \le V_P1, V_P2 \le 6\ V \pm 10\%$; $AGND_{RF} = DGND_{RF} = AGND_{IF} = DGND_{IF} = 0\ V$; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.)

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	10	ns min	DATA to CLOCK Set-Up Time
t_2	10	ns min	DATA to CLOCK Hold Time
t_3	25	ns min	CLOCK High Duration
t_4	25	ns min	CLOCK Low Duration
t_5	10	ns min	CLOCK to LE Set-Up Time
t_6	20	ns min	LE Pulsewidth

NOTES
Guaranteed by design but not production tested.
Specifications subject to change without notice.

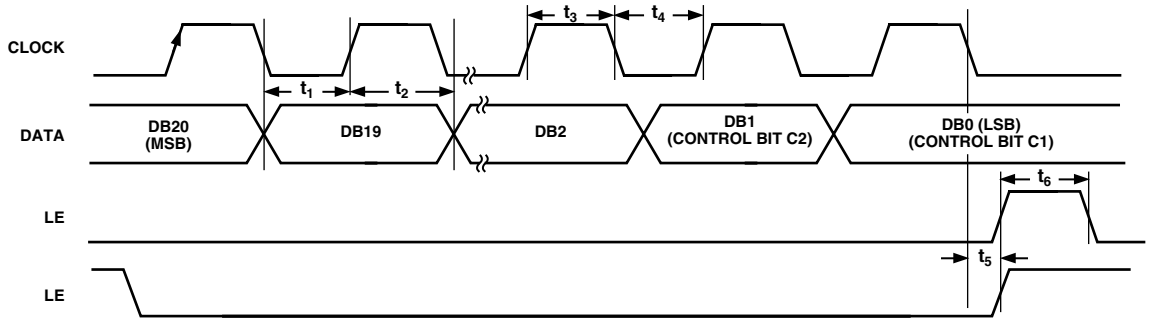


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = 25°C unless otherwise noted)

$V_{DD}1$ to GND[3] . . . . . –0.3 V to +7 V
$V_{DD}1$ to $V_{DD}2$ . . . . . –0.3 V to +0.3 V
V_P1, V_P2 to GND . . . . . –0.3 V to +7 V
V_P1, V_P2 to $V_{DD}1$ . . . . . –0.3 V to +5.5 V
Digital I/O Voltage to GND . . . . . –0.3 V to DV_{DD} + 0.3 V
Analog I/O Voltage to GND . . . . . –0.3 V to V_P + 0.3 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$,
$IF_{IN}A$, $IF_{IN}B$ to GND . . . . . –0.3 V to VDD + 0.3 V
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . 150°C
TSSOP θ_{JA} Thermal Impedance . . . . . 150.4°C/W
CSP θ_{JA} (Paddle Soldered) . . . . . 122°C/W
CSP θ_{JA} (Paddle Not Soldered) . . . . . 216°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]This device is a high-performance RF integrated circuit with an ESD rating of < 2 kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.
[3]GND = AGND = DGND = 0 V.

TRANSISTOR COUNT

11749 (CMOS) and 522 (Bipolar).

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADF4210/ADF4211/ADF4212/ADF4213 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
ADF4210BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-20
ADF4210BCP	–40°C to +85°C	Chip Scale Package	CP-20
ADF4211BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-20
ADF4211BCP	–40°C to +85°C	Chip Scale Package	CP-20
ADF4212BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-20
ADF4212BCP	–40°C to +85°C	Chip Scale Package	CP-20
ADF4213BRU	–40°C to +85°C	Thin Shrink Small Outline Package (TSSOP)	RU-20
ADF4213BCP	–40°C to +85°C	Chip Scale Package	CP-20

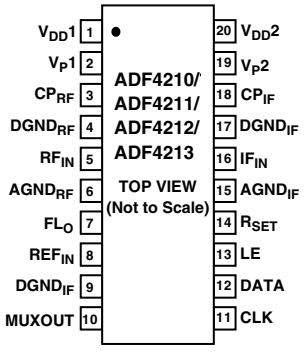
*Contact the factory for chip availability.

PIN FUNCTION DESCRIPTIONS

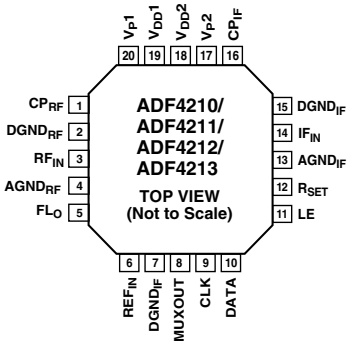
Pin Number TSSOP	Mnemonic	Function
1	$V_{DD}1$	Power Supply for the RF Section. Decoupling capacitors to the ground plane should be placed as close as possible to this pin. $V_{DD}1$ should have a value of between 2.7 V and 5.5 V. $V_{DD}1$ must have the same potential as $V_{DD}2$.
2	V_P1	Power Supply for the RF Charge Pump. This should be greater than or equal to $V_{DD}1$. In systems where $V_{DD}1$ is 3 V, it can be set to 6 V and used to drive a VCO with a tuning range up to 6 V.
3	CP_{RF}	Output from the RF Charge Pump. This is normally connected to a loop filter which drives the input to an external VCO.
4	$DGND_{RF}$	Ground Pin for the RF Digital Circuitry.
5	RF_{IN}	Input to the RF Prescaler. This low level input signal is ac-coupled from the RF VCO.
6	$AGND_{RF}$	Ground Pin for the RF Analog Circuitry.
7	FL_O	RF/IF Fastlock Mode.
8	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and an equivalent input resistance of 100 kΩ. This input can be driven from a TTL or CMOS crystal oscillator.
9	$DGND_{IF}$	Digital Ground for the IF Digital, Interface and Control Circuitry.
10	MUXOUT	This multiplexer output allows either the IF/RF Lock Detect, the scaled RF, scaled IF or the scaled Reference Frequency to be accessed externally.
11	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
13	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
14	R_{SET}	Connecting a resistor between this pin and ground sets the maximum RF and IF charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.66 V. The relationship between I_{CP} and R_{SET} is $$I_{CP\,MAX} = \frac{13.5}{R_{SET}}$$ So, with R_{SET} = 2.7 kΩ, $I_{CP\,MAX}$ = 5 mA for both the RF and IF Charge Pumps.
15	$AGND_{IF}$	Ground Pin for the IF Analog Circuitry.
16	IF_{IN}	Input to the RF Prescaler. This low-level input signal is ac-coupled from the IF VCO.
17	$DGND_{IF}$	Ground Pin for the IF Digital, Interface, and Control Circuitry.
18	CP_{IF}	Output from the IF Charge Pump. This is normally connected to a loop filter which drives the input to an external VCO.
19	V_P2	Power Supply for the IF Charge Pump. This should be greater than or equal to $V_{DD}2$. In systems where $V_{DD}2$ is 3 V, it can be set to 6 V and used to drive a VCO with a tuning range up to 6 V.
20	$V_{DD}2$	Power Supply for the IF, Digital and Interface Section. Decoupling capacitors to the ground plane should be placed as close as possible to this pin. $V_{DD}2$ should have a value of between 2.7 V and 5.5 V. $V_{DD}2$ must have the same potential as $V_{DD}1$.

PIN CONFIGURATIONS

TSSOP

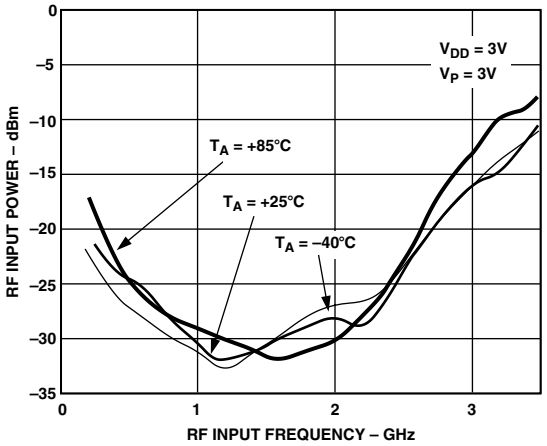


CP-20

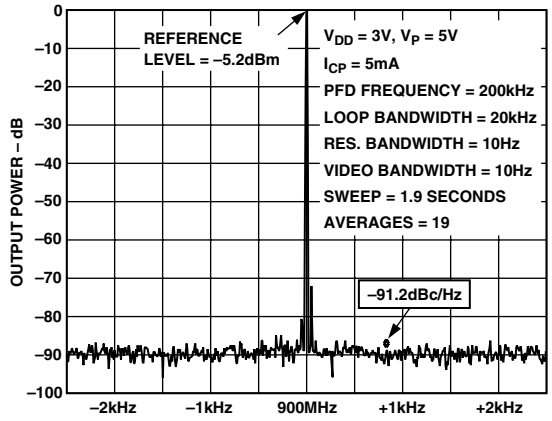


FREQUENCY	S_{11} REAL	S_{11} IMAG	FREQUENCY	S_{11} REAL	S_{11} IMAG
50000000.0	0.955683	–0.052267	2150000000.0	0.138086	–0.699896
150000000.0	0.956993	–0.112191	2250000000.0	0.102483	–0.704160
250000000.0	0.935463	–0.185212	2350000000.0	0.054916	–0.696325
350000000.0	0.919706	–0.252576	2450000000.0	0.018475	–0.669617
450000000.0	0.871631	–0.323799	2550000000.0	–0.019935	–0.668056
550000000.0	0.838141	–0.350455	2650000000.0	–0.054445	–0.666995
650000000.0	0.799005	–0.408344	2750000000.0	–0.083716	–0.634725
750000000.0	0.749065	–0.455840	2850000000.0	–0.129543	–0.615246
850000000.0	0.706770	–0.471011	2950000000.0	–0.154974	–0.610398
950000000.0	0.671007	–0.535268			
1050000000.0	0.630673	–0.557699			
1150000000.0	0.584013	–0.604256			
1250000000.0	0.537311	–0.622297			
1350000000.0	0.505090	–0.642019			
1450000000.0	0.459446	–0.686409			
1550000000.0	0.381234	–0.693908			
1650000000.0	0.363150	–0.679602			
1750000000.0	0.330545	–0.721812			
1850000000.0	0.264232	–0.697386			
1950000000.0	0.242065	–0.711716			
2050000000.0	0.181238	–0.723232			

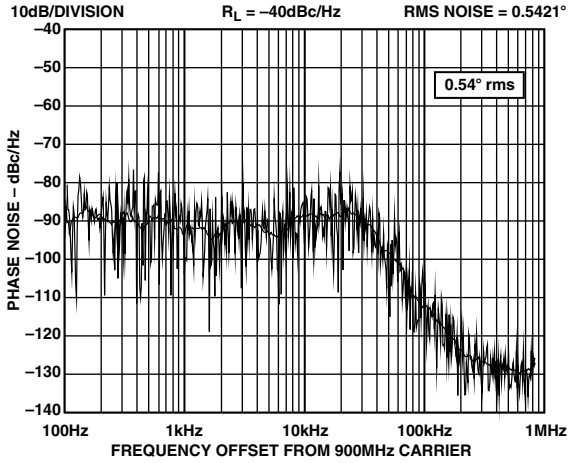
TPC 1. S-Parameter Data for the ADF4213 RF Input (Up to 3.0 GHz)



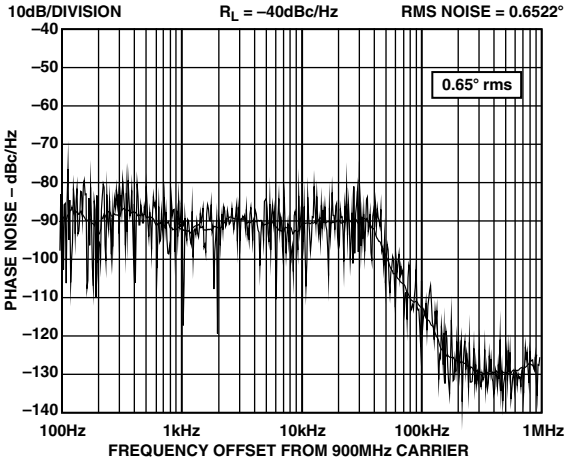
TPC 4. Input Sensitivity (ADF4213)



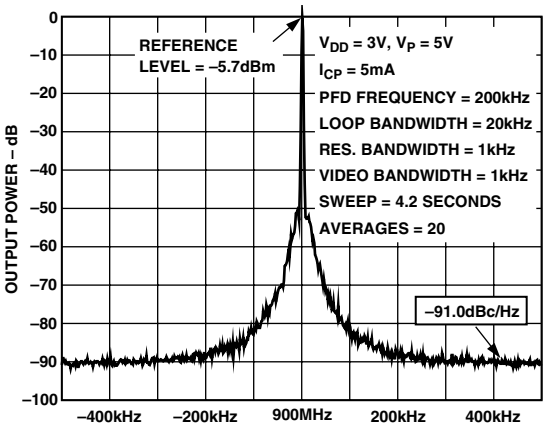
TPC 2. ADF4213 Phase Noise (900 MHz, 200 kHz, 20 kHz)



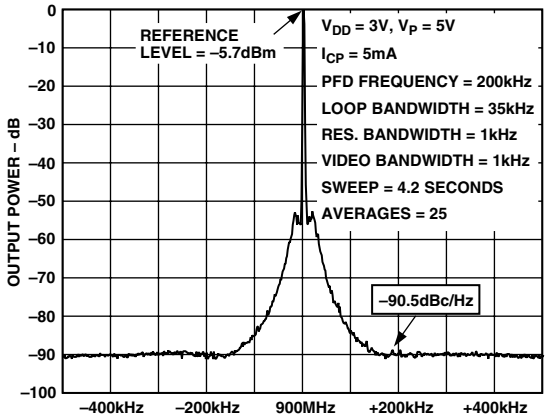
TPC 5. ADF4213 Integrated Phase Noise (900 MHz, 200 kHz, 20 kHz, Typical Lock Time: 400 μs)



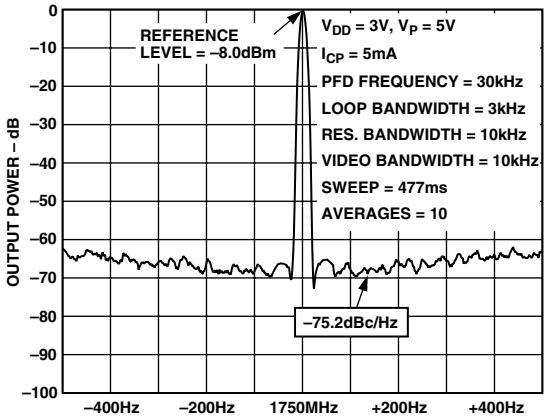
TPC 3. ADF4213 Integrated Phase Noise (900 MHz, 200 kHz, 35 kHz, Typical Lock Time: 200 μs)



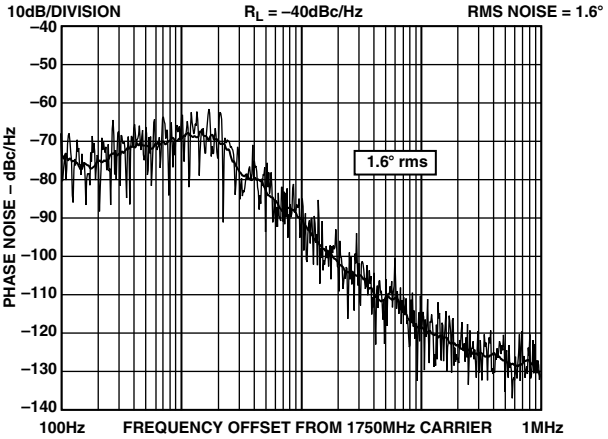
TPC 6. ADF4213 Reference Spurs (900 MHz, 200 kHz, 20 kHz)



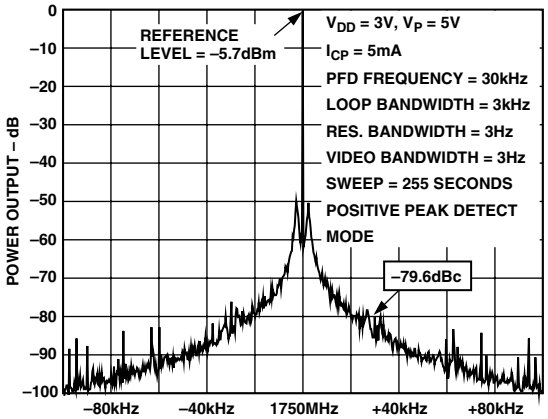
TPC 7. ADF4213 Reference Spurs (900 MHz, 200 kHz, 35 kHz)



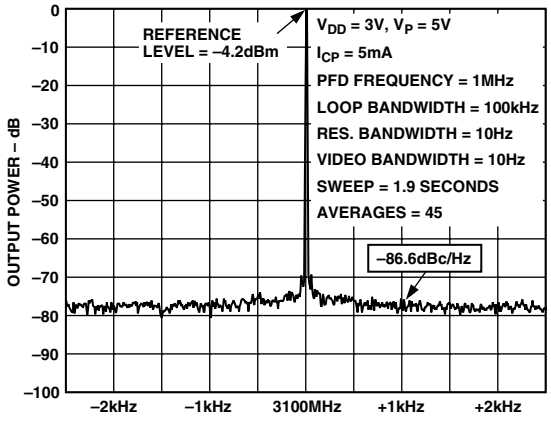
TPC 10. ADF4213 Phase Noise (1750 MHz, 30 kHz, 3 kHz)



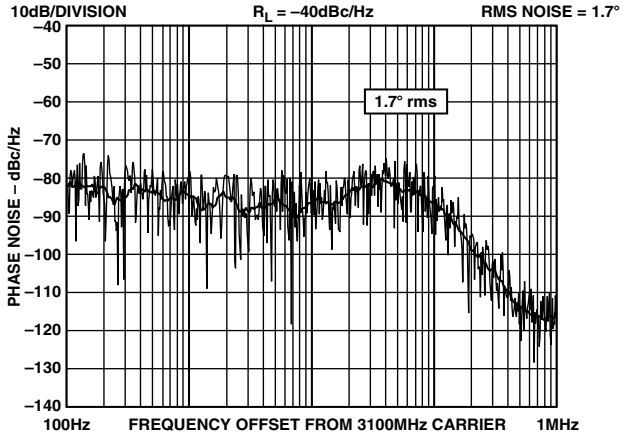
TPC 8. ADF4213 Integrated Phase Noise (1750 MHz, 30 kHz, 3 kHz)



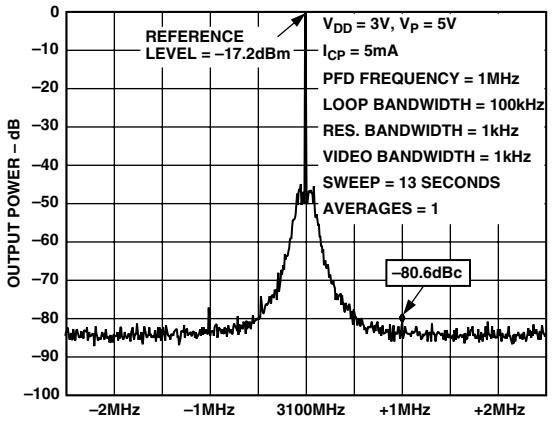
TPC 11. ADF4213 Reference Spurs (1750 MHz, 30 kHz, 3 kHz)



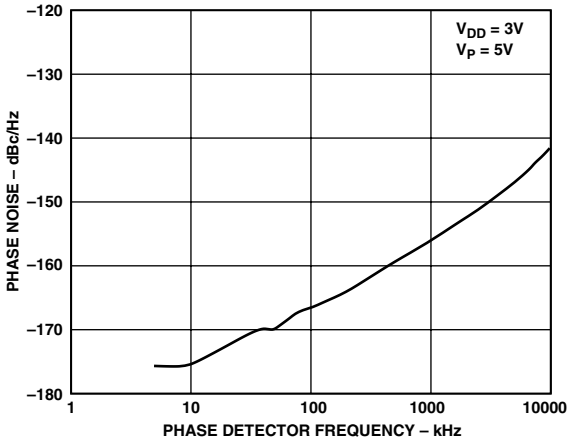
TPC 9. ADF4213 Phase Noise (2800 MHz, 1 MHz, 100 kHz)



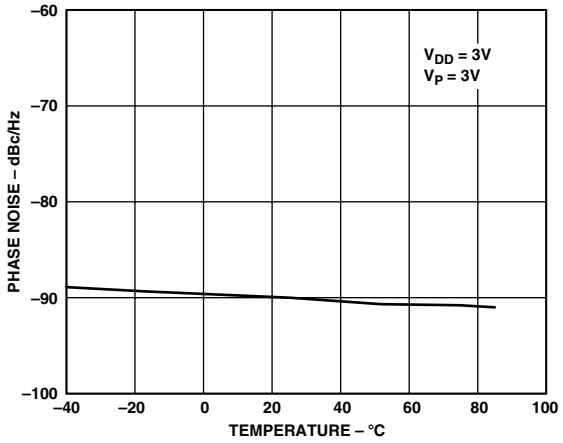
TPC 12. ADF4213 Integrated Phase Noise (2800 MHz, 1 MHz, 100 kHz)



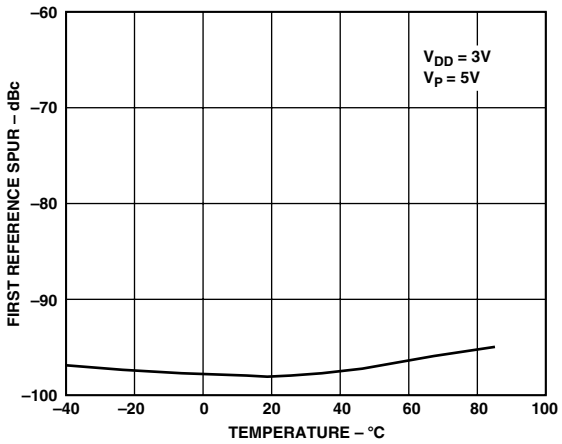
TPC 13. ADF4213 Reference Spurs (2800 MHz, 1 MHz, 100 kHz)



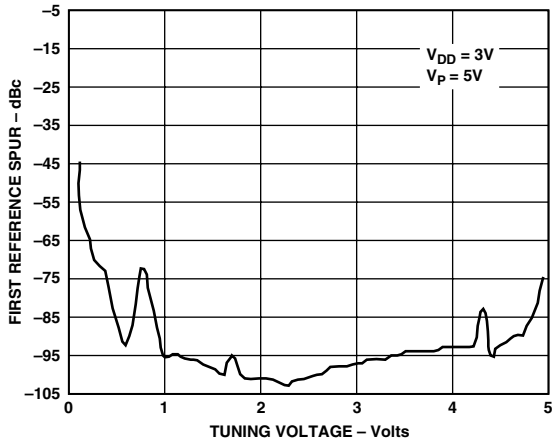
TPC 16. ADF4213 Phase Noise (Referred to CP Output) vs. PFD Frequency



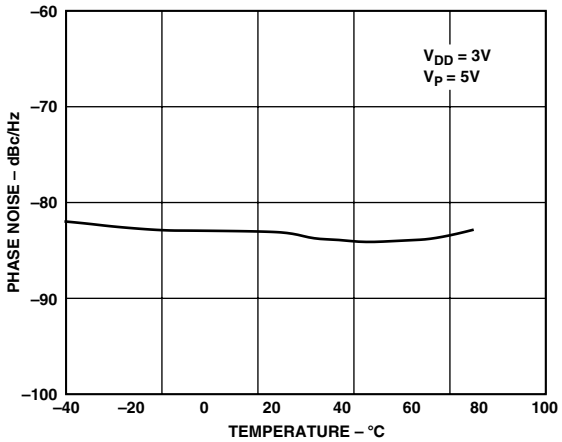
TPC 14. ADF4213 Phase Noise vs. Temperature (900 MHz, 200 kHz, 20 kHz)



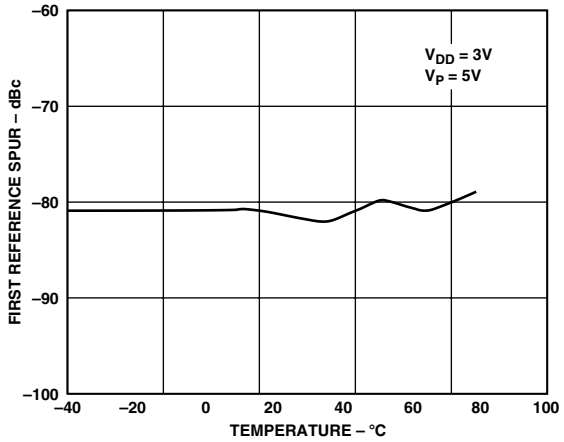
TPC 17. ADF4213 Reference Spurs vs. Temperature (900 MHz, 200 kHz, 20 kHz)



TPC 15. ADF4213 Reference Spurs (200 kHz) vs. V_{TUNE} (900 MHz, 200 kHz, 20 kHz)



TPC 18. ADF4213 Phase Noise vs. Temperature (836 MHz, 30 kHz, 3 kHz)



TPC 19. ADF4213 Reference Spurs vs. Temperature (836 MHz, 30 kHz, 3 kHz)

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown below in Figure 2. SW1 and SW2 are normally-closed switches. SW3 is normally-open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

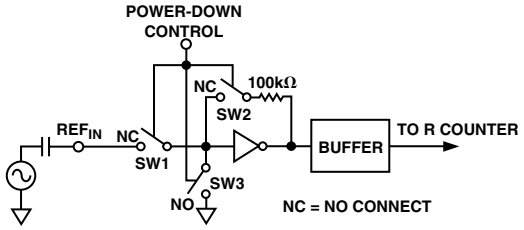


Figure 2. Reference Input Stage

RF/IF INPUT STAGE

The RF/IF input stage is shown in Figure 3. It is followed by a 2-stage limiting amplifier to generate the CML (Current Mode Logic) clock levels needed for the prescaler.

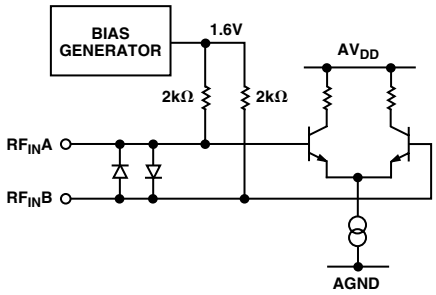


Figure 3. RF/IF Input Stage

PRESCALER (P/P + 1)

The dual modulus prescaler (P/P + 1), along with the A and B counters, enables the large division ratio, N, to be realized (N = PB + A). The dual-modulus prescaler, operating at CML levels, takes the clock from the RF/IF input stage and divides it down to a manageable frequency for the CMOS A and B counters in the RF and If sections. The prescaler in both sections is programmable. It can be set in software to 8/9, 16/17, 32/33, or 64/65. See Tables IV and VI. It is based on a synchronous 4/5 core.

RF/IF A AND B COUNTERS

The A and B CMOS counters combine with the dual modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 200 MHz or less, when V_{DD} = 5 V. Typically, they will work with 250 MHz output from the prescaler. Thus, with an RF input frequency of 2.5 GHz, a prescaler value of 16/17 is valid, but a value of 8/9 is not valid.

Pulse Swallow Function

The A and B counters, in conjunction with the dual modulus prescaler make it possible to generate output frequencies which are spaced only by the Reference Frequency divided by R. The equation for the VCO frequency is as follows:

$$f_{VCO} = [(P \times B) + A] \times f_{REFIN}/R$$

f_{VCO} = Output Frequency of external voltage controlled oscillator (VCO).

P = Preset modulus of dual modulus prescaler (8/9, 16/17, etc.).

B = Preset Divide Ratio of binary 13-bit counter (3 to 8191).

A = Preset Divide Ratio of binary 6-bit A counter (0 to 63).

f_{REFIN} = External reference frequency oscillator.

R = Preset divide ratio of binary 15-bit programmable reference counter (1 to 32767).

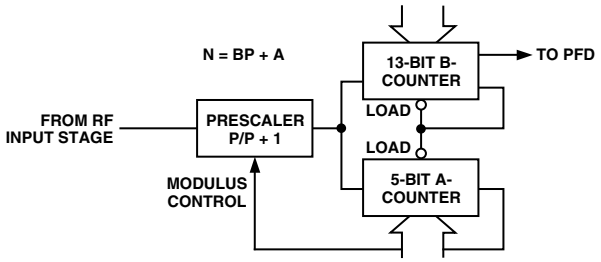


Figure 4. RF/IF A and B Counters

RF/IF COUNTER

The 15-bit RF/IF R counter allows the input reference frequency to be divided down to product the input clock to the phase frequency detector (PFD). Division ratios from 1 to 32767 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 5 is a simplified schematic. The PFD includes a fixed-delay element that sets the width of the antibacklash pulse. This is typically 3 ns. This pulse ensures that there is no deadzone in the PFD transfer function and gives a consistent reference spur level.

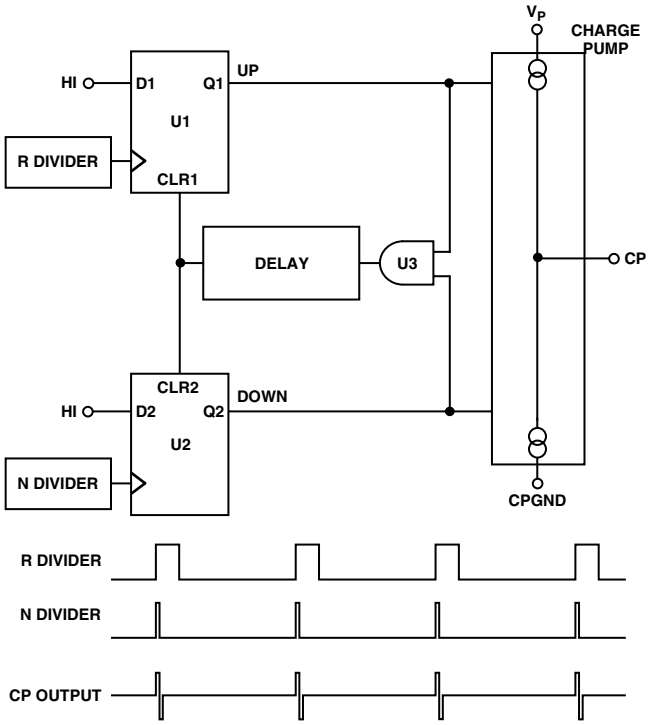


Figure 5. RF/IF PFD Simplified Schematic and Timing (In Lock)

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF421x family allows the user to access various internal points on the chip. The state of MUXOUT is controlled by P3, P4, P11, and P12. See Tables III and V. Figure 6 shows the MUXOUT section in block diagram form.

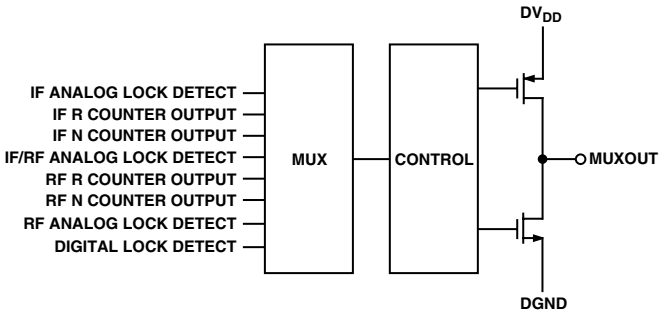


Figure 6. MUXOUT Circuit

Lock Detect

MUXOUT can be programmed for two types of lock detect: Digital Lock Detect and Analog Lock Detect. Digital Lock Detect is active high. It is set high when the phase error on three consecutive Phase Detector cycles is less than 15 ns. It will stay set high until a phase error of greater than 25 ns is detected on any subsequent PD cycle. The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected, it is high with narrow low-going pulses.

RF/IF INPUT SHIFT REGISTER

The ADF421x family digital section includes a 24-bit input shift register, a 14-bit IF R counter and a 18-bit IF N counter, comprising a 6-bit IF A counter and a 12-bit IF B counter. Also present is a 14-bit RF R counter and an 18-bit RF N counter, comprising a 6-bit RF A counter and a 12-bit RF B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs DB1, DB0 as shown in the timing diagram of Figure 1. The truth table for these bits is shown in Table VI. Table I shows a summary of how the latches are programmed.

Table I. C2, C1 Truth Table

Control Bits C2	Control Bits C1	Data Latch
0	0	IF R Counter
0	1	IF AB Counter (A and B)
1	0	RF R Counter
1	1	RF AB Counter (A and B)

Table II. ADF421x Family Latch Summary

IF R COUNTER LATCH

IF CP CURRENT SETTING			IF F_O	LOCK DETECT PRECISION	THREE-STATE CP	IF PD POLARITY	15-BIT REFERENCE COUNTER															CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
IF CP2	IF CP1	IF CP0	P4	P3	P2	P1	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

IF N COUNTER LATCH

IF CP GAIN	IF POWER-DOWN	IF PRESCALER		12-BIT B COUNTER												6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P8	P7	P6	P5	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

RF R COUNTER LATCH

RF CP CURRENT SETTING			RF F_O	RF LOCK DETECT	THREE-STATE CP	RF PD POLARITY	15-BIT REFERENCE COUNTER															CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RF CP2	RF CP1	RF CP0	P12	P11	P10	P9	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (1)	C1 (0)

RF N COUNTER LATCH

RF CP GAIN	RF POWER-DOWN	RF PRESCALER		12-BIT B COUNTER												6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P17	P16	P15	P14	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (1)	C1 (1)

Table III. IF R Counter Latch Map

IF R COUNTER LATCH

IF CP CURRENT SETTING			IF F_O	LOCK DETECT PRECISION	THREE-STATE CP	IF PD POLARITY	15-BIT REFERENCE COUNTER														CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
IF CP2	IF CP1	IF CP0	P4	P3	P2	P1	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

R15	R14	R13	.....	R3	R2	R1	DIVIDE RATIO
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	32764
1	1	1	.....	1	0	1	32765
1	1	1	.....	1	1	0	32766
1	1	1	.....	1	1	1	32767

P1	IF PD POLARITY
0	NEGATIVE
1	POSITIVE

P2	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

P12 FROM RF R LATCH	P11 FROM RF R LATCH	P4	P3	MUXOUT
0	0	0	0	LOGIC LOW STATE
0	0	0	1	IF ANALOG LOCK DETECT
0	0	1	0	IF REFERENCE DIVIDER OUTPUT
0	0	1	1	IF N DIVIDER OUTPUT
0	1	0	0	RF ANALOG LOCK DETECT
0	1	0	1	RF/IF ANALOG LOCK DETECT
0	1	1	0	IF DIGITAL LOCK DETECT
0	1	1	1	LOGIC HIGH STATE
1	0	0	0	RF REFERENCE DIVIDER OUTPUT
1	0	0	1	RF N DIVIDER OUTPUT
1	0	1	0	THREE-STATE OUTPUT
1	0	1	1	IF COUNTER RESET
1	1	0	0	RF DIGITAL LOCK DETECT
1	1	0	1	RF/IF DIGITAL LOCK DETECT
1	1	1	0	RF COUNTER RESET
1	1	1	1	IF AND RF COUNTER RESET

			I_{CP} (mA)		
IF CP2	IF CP1	IF CP0	1.5kΩ	2.7kΩ	5.6kΩ
0	0	0	1.088	0.625	0.294
0	0	1	2.176	1.25	0.588
0	1	0	3.264	1.875	0.882
0	1	1	4.352	2.5	1.176
1	0	0	5.44	3.125	1.47
1	0	1	6.528	3.75	1.764
1	1	0	7.616	4.375	2.058
1	1	1	8.704	5.0	2.352

Table IV. IF N Counter Latch Map

IF N COUNTER LATCH

IF CP GAIN	IF POWER-DOWN	IF PRESCALER		12-BIT B COUNTER												6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P8	P7	P6	P5	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

P6	P5	IF PRESCALER
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

P7	IF POWER-DOWN
0	DISABLE
1	ENABLE

A6	A5	.....	A2	A1	A COUNTER DIVIDE RATIO
0	0	.....	0	1	1
0	0	.....	1	0	2
0	0	.....	1	1	3
0	0	.....	0	0	4
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	60
1	1	.....	0	1	61
1	1	.....	1	0	62
1	1	.....	1	1	63

B12	B11	B10		B3	B2	B1	B COUNTER DIVIDE RATIO
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	4092
1	1	1	.....	1	0	1	4093
1	1	1	.....	1	1	0	4094
1	1	1	.....	1	1	1	4095

P8	IF CP GAIN
0	DISABLE
1	ENABLE

N = BP + A, P IS PRESCALER VALUE SET IN THE FUNCTION LATCH. B MUST BE GREATER THAN OR EQUAL TO A. FOR CONTIGUOUS VALUES OF N × F_{REF}, N_{MIN} is (P^2 – P).

Table V. RF R Latch Map

RF R COUNTER LATCH

RF CP CURRENT SETTING			RF F_O	RF LOCK DETECT	THREE-STATE CP	RF PD POLARITY	15-BIT REFERENCE COUNTER														CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RF CP2	RF CP1	RF CP0	P12	P11	P10	P9	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (1)	C1 (0)

R15	R14	R13	.....	R3	R2	R1	DIVIDE RATIO
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	32764
1	1	1	.....	1	0	1	32765
1	1	1	.....	1	1	0	32766
1	1	1	.....	1	1	1	32767

P9	RF PD POLARITY
0	NEGATIVE
1	POSITIVE

P10	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

P12	P11	FROM IF R LATCH P4	FROM IF R LATCH P3	MUXOUT
0	0	0	0	LOGIC LOW STATE
0	0	0	1	IF ANALOG LOCK DETECT
0	0	1	0	IF REFERENCE DIVIDER OUTPUT
0	0	1	1	IF N DIVIDER OUTPUT
0	1	0	0	RF ANALOG LOCK DETECT
0	1	0	1	RF/IF ANALOG LOCK DETECT
0	1	1	0	IF DIGITAL LOCK DETECT
0	1	1	1	LOGIC HIGH STATE
1	0	0	0	RF REFERENCE DIVIDER OUTPUT
1	0	0	1	RF N DIVIDER OUTPUT
1	0	1	0	THREE-STATE OUTPUT
1	0	1	1	IF COUNTER RESET
1	1	0	0	RF DIGITAL LOCK DETECT
1	1	0	1	RF/IF DIGITAL LOCK DETECT
1	1	1	0	RF COUNTER RESET
1	1	1	1	IF AND RF COUNTER RESET

RF CP2	RF CP1	RF CP0	I_{CP} (mA) 1.5kΩ	I_{CP} (mA) 2.7kΩ	I_{CP} (mA) 5.6kΩ
0	0	0	1.125	0.625	0.301
0	0	1	2.25	1.25	0.602
0	1	0	3.375	1.875	0.904
0	1	1	4.5	2.5	1.205
1	0	0	5.625	3.125	1.506
1	0	1	6.75	3.75	1.808
1	1	0	7.7875	4.375	2.109
1	1	1	9.0	5.0	2.411

Table VI. RF N Counter Latch Map

RF N COUNTER LATCH

RF CP GAIN	RF POWER-DOWN	RF PRESCALER		12-BIT B COUNTER												6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P17	P16	P15	P14	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (1)	C1 (1)

P15	P14	PRESCALER
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

P16	RF POWER-DOWN
0	DISABLE
1	ENABLE

A6	A5	.....	A2	A1	A COUNTER DIVIDE RATIO
0	0	.....	0	1	1
0	0	.....	1	0	2
0	0	.....	1	1	3
0	0	.....	0	0	4
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	60
1	1	.....	0	1	61
1	1	.....	1	0	62
1	1	.....	1	1	63

B12	B11	B10	.....	B3	B2	B1	B COUNTER DIVIDE RATIO
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	4092
1	1	1	.....	1	0	1	4093
1	1	1	.....	1	1	0	4094
1	1	1	.....	1	1	1	4095

P17	RF CP GAIN
0	DISABLE
1	ENABLE

N = BP + A, P IS PRESCALER VALUE SET IN THE FUNCTION LATCH. B MUST BE GREATER THAN OR EQUAL TO A. FOR CONTIGUOUS VALUES OF N × F_{REF}, N_{MIN} is (P^2 – P).

PROGRAM MODES

Table III and Table V show how to set up the Program Modes in the ADF421x family. The following should be noted:

1. IF and RF Analog Lock Detect indicate when the PLL is in lock. When the loop is locked and either IF or RF Analog Lock Detect is selected, the MUXOUT pin will show a logic high with narrow low-going pulses. When the IF/RF Analog Lock Detect is chosen, the locked condition is indicated only when both IF and RF loops are locked.
2. The IF Counter Reset mode resets the R and AB counters in the IF section and also puts the IF charge pump into three-state. The RF Counter Reset mode resets the R and AB counters in the RF section and also puts the RF charge pump into three-state. The IF and RF Counter Reset mode does both of the above. Upon removal of the reset bits, the AB counter resumes counting in close alignment with the R counter (maximum error is one prescaler output cycle).
3. The Fastlock mode uses MUXOUT to switch a second loop filter damping resistor to ground during Fastlock operation. Activation of Fastlock occurs whenever RF CP Gain in the RF Reference counter is set to one.

IF Power-Down

It is possible to program the ADF421x family for either synchronous or asynchronous power-down on either the IF or RF side.

Synchronous IF Power-Down

Programming a "1" to P7 of the ADF421x family will initiate a power-down. If P2 of the ADF421x family has been set to "0" (normal operation), a synchronous power-down is conducted. The device will automatically put the charge pump into three-state and then complete the power-down.

Asynchronous IF Power-Down

If P2 of the ADF421x family has been set to "1" (three-state the IF charge pump), and P7 is subsequently set to "1," an asynchronous power-down is conducted. The device will go into power-down on the rising edge of LE, which latches the "1" to the IF power-down bit (P7).

Synchronous RF Power-Down

Programming a "1" to P16 of the ADF421x family will initiate a power-down. If P10 of the ADF421x family has been set to "0" (normal operation), a synchronous power-down is conducted. The device will automatically put the charge pump into three-state and then complete the power-down.

Asynchronous RF Power-Down

If P10 of the ADF421x family has been set to "1" (three-state the RF charge pump), and P16 is subsequently set to "1," an asynchronous power-down is conducted. The device will go into power down on the rising edge of LE, which latches the "1" to the RF power-down bit (P16).

Activation of either synchronous or asynchronous power-down forces the IF/RF loop's R and AB dividers to their load state conditions and the IF/RF input section is debiased to a high-impedance state.

The REF_{IN} oscillator circuit is only disabled if both the IF and RF power-downs are set.

The input register and latches remain active and are capable of loading and latching data during all the power-down modes.

The IF/RF section of the devices will return to normal powered up operation immediately upon LE latching a "0" to the appropriate power-down bit.

IF SECTION

PROGRAMMABLE IF REFERENCE (R) COUNTER

If control bits C2, C1 are 0, 0, the data is transferred from the input shift register to the 14-bit IFR counter. Table III shows the input shift register data format for the IFR counter and the divide ratios possible.

IF Phase Detector Polarity

P1 sets the IF Phase Detector Polarity. When the IF VCO characteristics are positive this should be set to "1." When they are negative it should be set to "0." See Table III.

IF Charge Pump Three-State

P2 puts the IF charge pump into three-state mode when programmed to a "1." It should be set to "0" for normal operation. See Table III.

IF PROGRAM MODES

Table III and Table V show how to set up the Program Modes in the ADF421x family.

IF Charge Pump Currents

IFCP2, IFCP1, IFCP0 program current setting for the IF charge pump. See Table III.

PROGRAMMABLE IF AB COUNTER

If control bits C2, C1 are 0, 1, the data in the input register is used to program the IF AB counter. The N counter consists of a 6-bit swallow counter (A counter) and 12-bit programmable counter (B counter). Table IV shows the input register data format for programming the IF AB counter and the possible divide ratios.

IF Prescaler Value

P5 and P6 in the IF A, B Counter Latch sets the IF prescaler value. See Table IV.

IF Power-Down

Table III and Table V show the power-down bits in the ADF421x family.

IF Fastlock

The IF CP Gain bit (P8) of the IF N register in the ADF421x family is the Fastlock Enable Bit. Only when this is "1" is IF Fastlock enabled. When Fastlock is enabled, the IF CP current is set to its maximum value. Since the IF CP Gain bit is contained in the IF N Counter, only one write is needed to both program a new output frequency and also initiate Fastlock. To come out of Fastlock, the IF CP Gain bit on the IF N register must be set to "0." See Table IV.

RF SECTION

PROGRAMMABLE RF REFERENCE (R) COUNTER

If control bits C2, C1 are 1, 0, the data is transferred from the input shift register to the 14-bit RFR counter. Table V shows the input shift register data format for the RFR counter and the possible divide ratios.

RF Phase Detector Polarity

P9 sets the IF Phase Detector Polarity. When the RF VCO characteristics are positive this should be set to "1." When they are negative it should be set to "0." See Table V.

RF Charge Pump Three-State

P10 puts the RF charge pump into three-state mode when programmed to a "1." It should be set to "0" for normal operation. See Table V.

RF PROGRAM MODES
Table III and Table V show how to set up the Program Modes in the ADF421x family.

RF Charge Pump Currents
RFCP2, RFCP1, RFCP0 program current setting for the RF charge pump. See Table V.

PROGRAMMABLE RF N COUNTER
If control bits C2, C1 are 1, 1, the data in the input register is used to program the RF N (A + B) counter. The N counter consists of a 6-bit swallow counter (A Counter) and 12-bit programmable counter (B Counter). Table IV shows the input register data format for programming the RF N counter and the possible divide ratios.

RF Prescaler Value
P14 and P15 in the RF A, B Counter Latch sets the RF prescaler value. See Table VI.

RF Power-Down
Table III and Table V show the power-down bits in the ADF421x family.

RF Fastlock
The RF CP Gain bit (P17) of the RF N register in the ADF421x family is the Fastlock Enable Bit. Only when this is "1" is IF Fastlock enabled. When Fastlock is enabled, the RF CP current is set to its maximum value. Also an extra loop filter damping resistor to ground is switched in using the FL_O pin, thus compensating for the change in loop characteristics while in Fastlock. Since the RF CP Gain bit is contained in the RF N Counter, only one write is needed to both program a new output frequency and also initiate Fastlock. To come out of Fastlock, the RF CP Gain bit on the RF N register must be set to "0." See Table VI.

APPLICATIONS SECTION
Local Oscillator for GSM Handset Receiver
Figure 7 shows the ADF4210/ADF4211/ADF4212/ADF4213 being used with a VCO to produce the LO for a GSM base station transmitter.

The reference input signal is applied to the circuit at $FREF_{IN}$ and, in this case, is terminated in 50 Ω. A typical GSM system would have a 13 MHz TCXO driving the reference input without any 50 Ω termination. In order to have a channel spacing of 200 kHz (the GSM standard), the reference input must be divided by 65, using the on-chip reference.

WIDEBAND PLL
Many of the wireless applications for synthesizers and VCOs in PLLs are narrowband in nature. These applications include various wireless standards such as GSM, DSC1800, CDMA, or WCDMA. In each of these cases, the total tuning range for the local oscillator is less than 100 MHz. However, there are also wideband applications where the local oscillator could have up to an octave tuning range. For example, cable TV tuners have a total range of about 400 MHz. Figure 8 shows an application where the ADF4213 is used to control and program the Micronetics M3500–1324. The loop filter was designed for an RF output of 2100 MHz, a loop bandwidth of 40 kHz, a PFD frequency of 1 MHz, I_{CP} of 10 mA (2.5 mA synthesizer I_{CP} multiplied by the gain factor of 4), VCO K_D of 80 MHz/V (sensitivity of the M3500–1324 at an output of 2100 MHz) and a phase margin of 45°C.

In narrowband applications, there is generally a small variation (less than 10%) in output frequency and also a small variation (typically < 10%) in VCO sensitivity over the range. However,

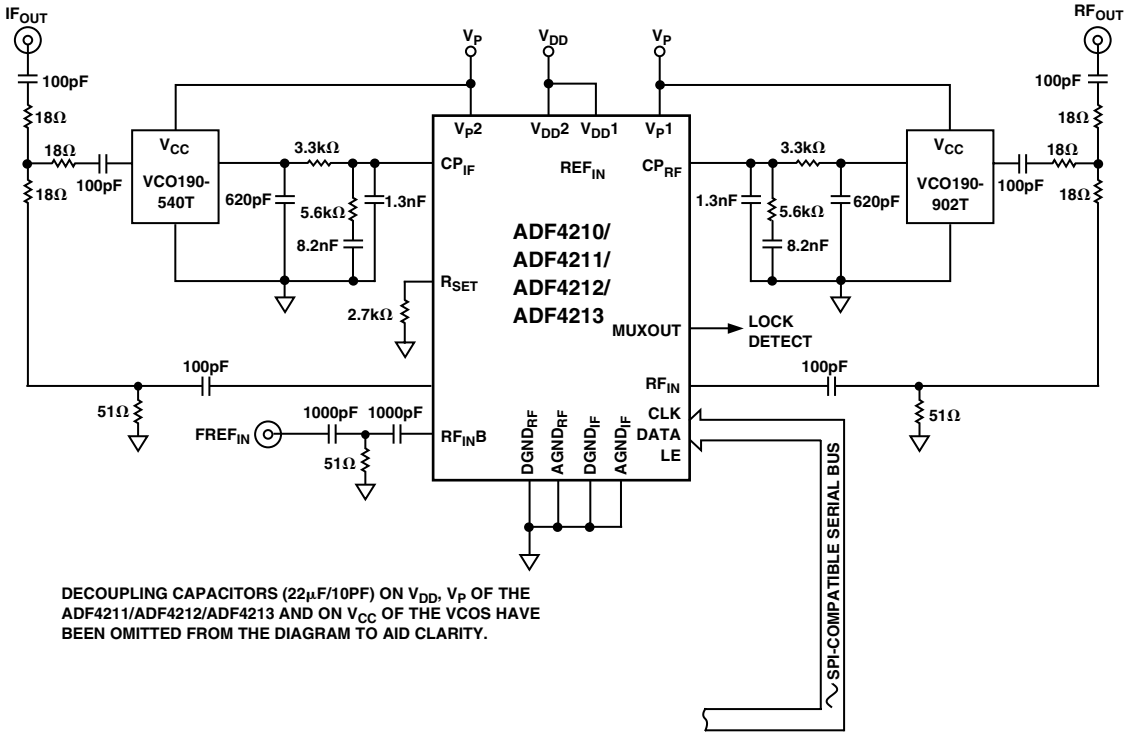


Figure 7. GSM Handset Receiver Local Oscillator Using the ADF4210/ADF4211/ADF4212/ADF4213

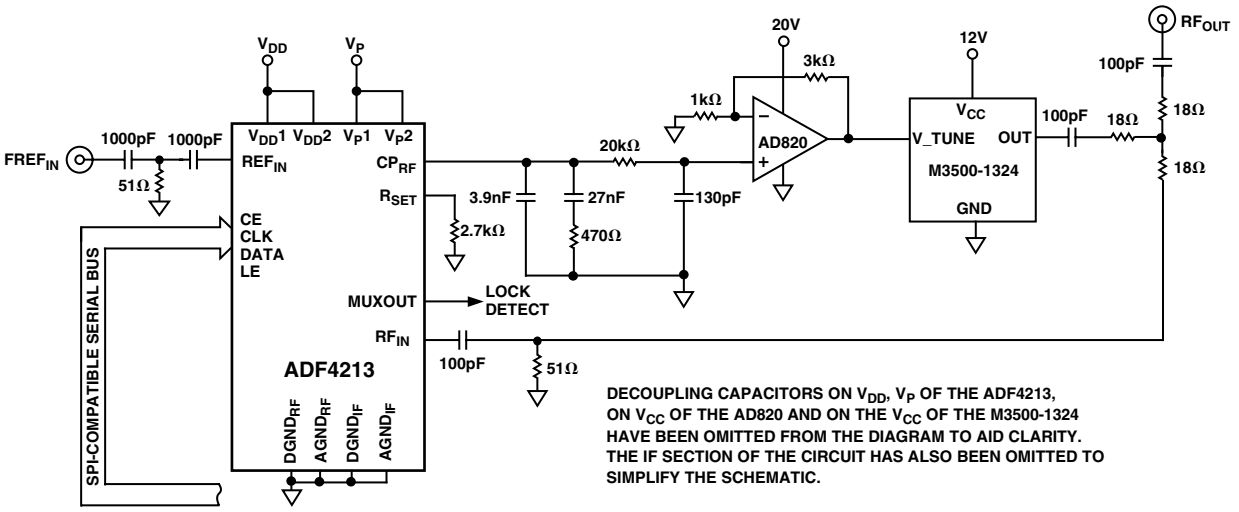


Figure 8. Wideband PLL Circuit

in wide-band applications both of these parameters have a much greater variation. In Figure 8, for example, we have –25% and +30% variation in the RF output from the nominal 1.8 GHz. The sensitivity of the VCO can vary from 130 MHz/V at 1900 MHz to 30 MHz/V at 2400 MHz. Variations in these parameters will change the loop bandwidth. This in turn can affect stability and lock time. By changing the programmable I_{CP}, it is possible to obtain compensation for these varying loop conditions and ensure that the loop is always operating close to optimal conditions.

INTERFACING

The ADF4210/ADF4211/ADF4212/ADF4213 family has a simple SPI-compatible serial interface for writing to the device. SCLK, SDATA, and LE control the data transfer. When LE (Latch Enable) goes high, the 22 bits that have been clocked into the input register on each rising edge of SCLK will be transferred to the appropriate latch. See Figure 1 for the Timing Diagram and Table I for the Latch Truth Table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 909 kHz, or one update every 1.1 ms. This is certainly more than adequate for systems that will have typical lock times in hundreds of microseconds.

ADuC812 to ADF421x Family Interface

Figure 9 shows the interface between the ADF421x family and the ADuC812 microconverter. Since the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The microconverter is set up for SPI Master Mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF421x family needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the microconverter to the device. When the third byte has been written, the LE input should be brought high to complete the transfer.

On first applying power to the ADF421x family, it needs four writes (one each to the R counter latch and the AB counter latch for both RF1 and RF2 sides) for the output to become active.

When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed will be about 180 kHz.

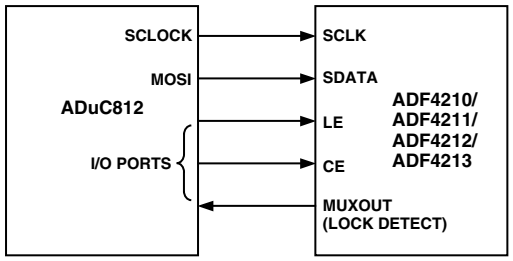


Figure 9. ADuC812 to ADF421x Family Interface

ADSP-21xx to ADF421x Family Interface

Figure 10 shows the interface between the ADF421x family and the ADSP-21xx Digital Signal Processor. As previously discussed, the ADF421x family needs a 24-bit serial word for each latch write. The easiest way to accomplish this, using the ADSP-21xx family, is to use the Autobuffered Transmit Mode of operation with Alternate Framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for eight bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the Autobuffered mode, and write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

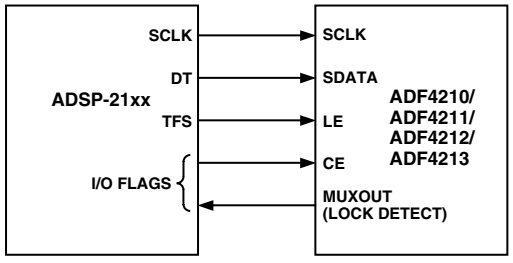


Figure 10. ADSP-21xx to ADF421x Family Interface

PCB Guidelines for Chip Scale Package

The lands on the chip scale package (CP-20), are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This will ensure that the solder joint size is maximized.

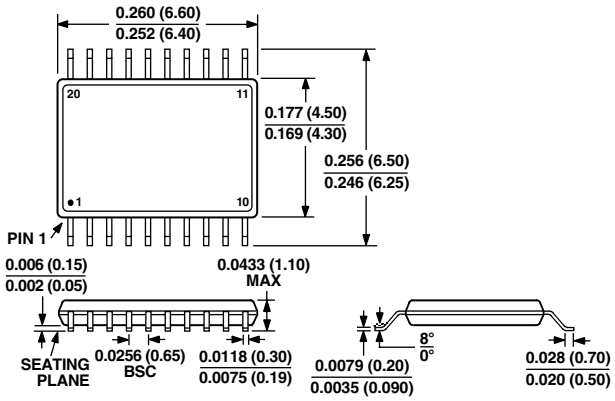
The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be clearance of at least 0.25 mm between the thermal pad and inner edges of the pad pattern. This will ensure that shorting is avoided.

Thermal vias may be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm grid pitch. The via diameter should be between 0.3 mm and 0.33 mm and the via barrel should be plated with 1 oz. copper to plug the via. The user should connect the printed circuit board pad to AGND.

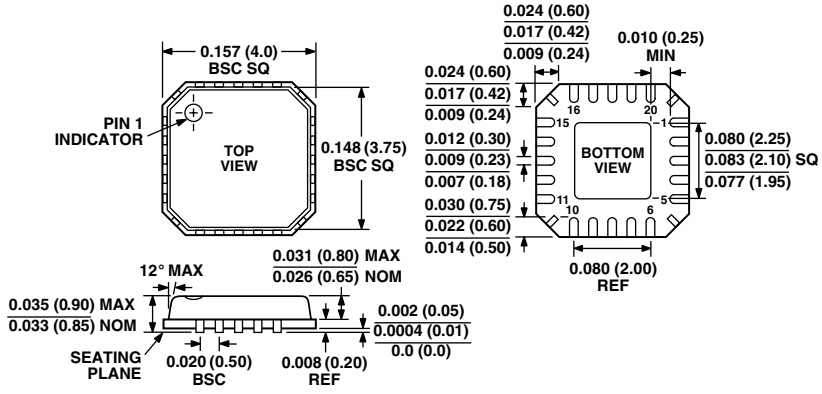
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Thin Shrink Small Outline Package (TSSOP)
(RU-20)



Chip Scale Package
(CP-20)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS

ADF4210/ADF4211/ADF4212/ADF4213–Revision History

Location	Page
Data Sheet changed from REV. 0 to REV. A.	
Changes to Test Conditions/Comments section of Specifications	2
Edit to RF_{IN} and IF_{IN} Function text	5
PCB Guidelines for Chip Scale Package section added	19
CP-20 Package replaced by CP-20[2]	19

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