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NTE2732A
Integrated Circuit
32K (4K x 8) NMOS UV Erasable PROM

Description:

The NTE2732A is a 32,768–bits ultraviolet erasable and electrically programmable read–only memory (EPROM) organized as 4,096 words by 8 bits and manufactured using N–Channel Si–Gate MOS processing. With its single +5V power supply and with an access time of 200ns, the NTE2732A is ideal for use with high performance +5V microprocessors such as the NTE3880.

The NTE2732A has an important feature which is the separate output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems.

The NTE2732A also features an standby mode which reduces the power dissipation without increasing access time. The active current is 125mA while the maximum standby mode is achieved by applying a TTL–high signal to the $\overline{CE}$ input.

Features:

- Fast Access Time: 200ns Max
- 0° to +70°C Standard Temperature Range
- Single +5V Power Supply
- Low Standby Current (35mA Max)
- Inputs and Outputs TTL Compatible During Read and Program
- Completely Static

Absolute Maximum Ratings: (Note 1)

All Input or Output Voltages with respect to GND, V_I . . . . . +6 to –0.6V
Supply Voltage with respect to GND during Program, V_{pp} . . . . . +22 to –0.6V
Ambient Temperature under Bias, T_A . . . . . –10° to +80°C
Storage Temperature Range, T_{stg} . . . . . –65° to +125°C

Note 1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Modes:

PINS / MODE	$\overline{CE}$ (18)	$\overline{OE}/V_{pp}$ (20)	V_{CC} (24)	OUTPUTS (9 – 11, 13–17)
READ	V_{IL}	V_{IL}	+5	D_{OUT}
STANDBY	V_{IH}	Don’t Care	+5	HIGH Z
PROGRAM	V_{IL}	V_{PP}	+5	D_{IN}
PROGRAM VERIFTY	V_{IL}	V_{IL}	+5	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{PP}	+5	HIGH Z

Read Operation (DC and AC Conditions):

Operating Temperature Range, T_{opr} . . . . . 0° to +70°C
V_{CC} Power Supply (Note 2, Note 3) . . . . . 5V ± 5%
V_{pp} Voltage (Note 3) . . . . . $V_{pp} = V_{CC}$

Note 2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Note 3. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.

DC and Operating Characteristics:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Load Current	I_{LI}	V_{IN} = 5.5V	–	–	10	µA
Output Leakage Current	I_{LO}	V_{OUT} = 5.5V	–	–	10	µA
V_{CC} Current Standby	I_{CC1}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}, Note 3	–	–	35	mA
V_{CC} Current Standby	I_{CC2}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, Note 3	–	70	125	mA
Input Low Voltage	V_{IL}		–0.1	–	+0.8	V
Input High Voltage	V_{IH}		2.0		V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL}= 2.1mA	–	–	0.45	V
Output High Voltage	V_{OH}	I_{OH} = –400µA	2.4	–	–	V

Note 3. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.

Note 4. Typical values are for T_A = +25°C and nominal supply voltages.

AC Characteristics:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	–	200	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	–	200	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	–	–	100	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL}, Note 5	0	–	60	ns
Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ whichever occurred first	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	–	ns

Note 4. Typical values are for T_A = +25°C and nominal supply voltages.

Note 5. This parameter is only sampled and is not 100% tested.

Capacitance: (T_A = +25°C, f = 1MHz, Note 5 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance except $\overline{OE}/V_{pp}$	C_{IN1}	V_{IN} = 0	–	4	6	pF
$\overline{OE}/V_{pp}$ Input Capacitance	C_{IN2}	V_{IN} = 0	–	–	20	pF
Output capacitance	C_{OUT}	V_{OUT} = 0	–	8	12	pF

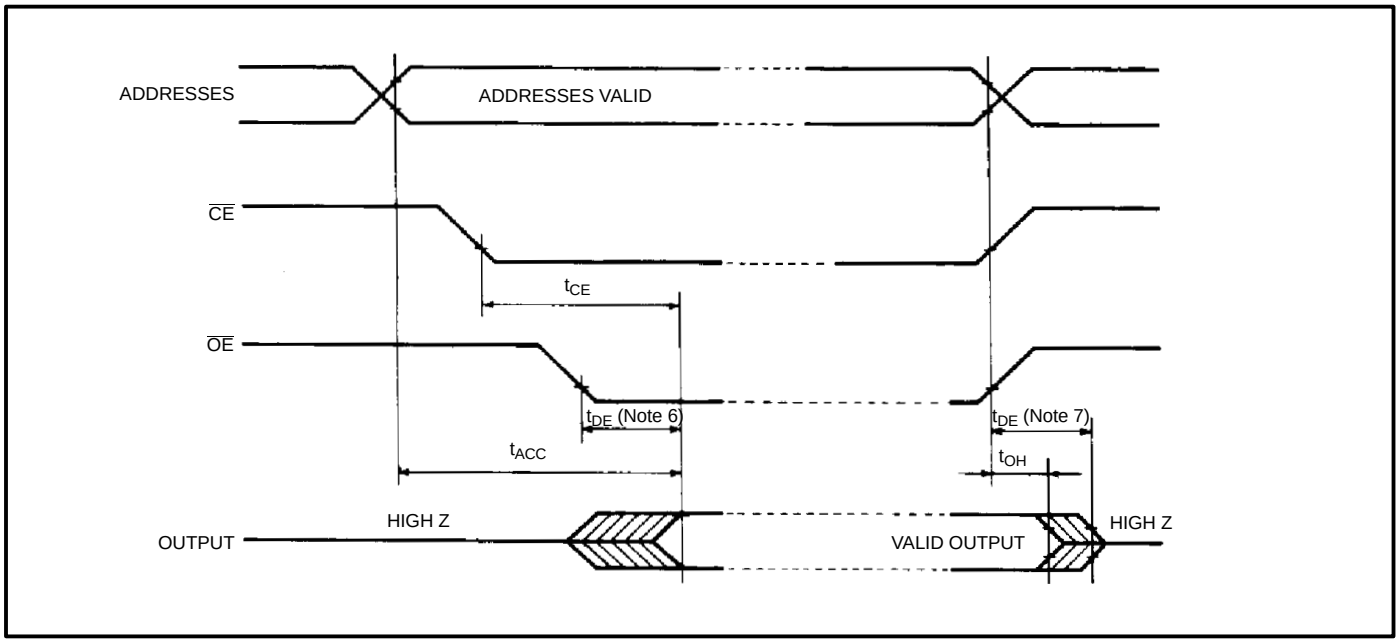
Note 4. Typical values are for T_A = +25°C and nominal supply voltages.

Note 5. This parameter is only sampled and is not 100% tested.

Read Operation (AC Test Conditions):

Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs 0.8 and 2V/0.8 and 2V

AC Waveforms:



Note 6. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{ACC}.
Note 7. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

Read Mode:
The NTE2732A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that addresses are stable, address access time (t_{ACC}) is equal to delay from $\overline{CE}$ to output ($t_{\overline{CE}}$). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}–t_{OE}$.

Standby Mode:
The NTE2732A has a standby mode which reduces the active power current by 70%, from 125mA to 35mA. The NTE2732A is placed in the standby mode by applying a TTL high signal to $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR–Tieing:
Because NTE2732A's are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a) the lowest possible memory power dissipation

b) complete assurance that output bus contention will not occur

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

Programming Operation: (T_A = +25°C ± 5°C, V_{CC} = 5V ±5%, V_{PP} = 21V ± 0.5V, Note 8, Note 9)

DC and AC Operating Characteristics:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Current (All Inputs)	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}	–	–	10	µA
Input Low Level	V_{IL}		–0.1	–	0.8	V
Input High Level	V_{IH}		2.0	–	V_{CC}+1	V
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = –400µA	2.4	–	–	V
V_{CC} Supply Current (Active)	I_{CC2}		–	70	125	mA
V_{PP} Supply Current	I_{PP}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$	–	–	30	mA

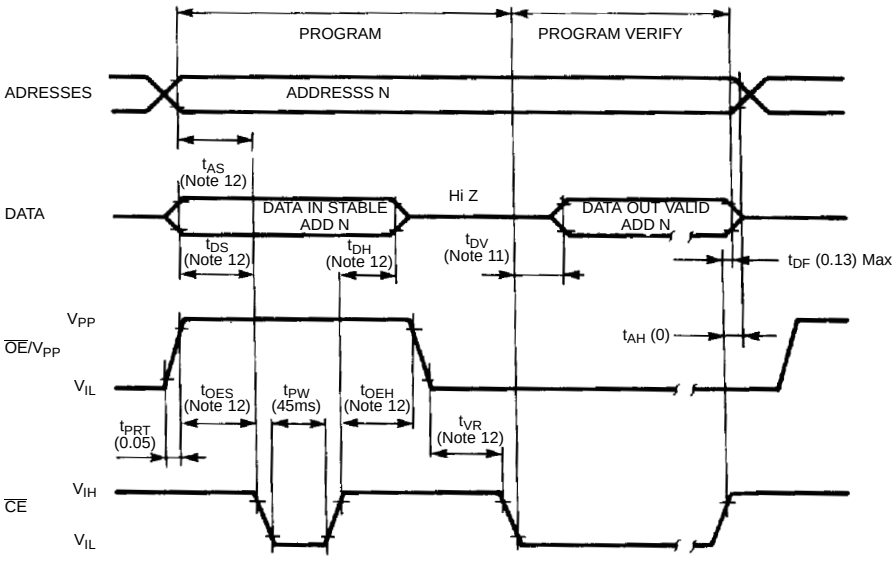
Note 8. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}. The NTE2732A must not be inserted into or removed from a board with V_{PP} at 21 ± 0.5V or damage may occur to the device.

Note 9. The maximum allowable voltage which may be applied to the V_{PP} pin during programming is +22V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 22V maximum specification.

AC Characteristics:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Address Set Up Time	t_{AS}		2	–	–	µs
$\overline{OE}$ Set Up Time	t_{OES}		2	–	–	µs
Data Set Up Time	t_{DS}		2	–	–	µs
Address Hold Time	t_{AH}		0	–	–	µs
Data Hold Time	t_{DH}		2	–	–	µs
Chip Enable to Output Float Delay	t_{DF}		0	–	130	ns
Data Valid from $\overline{CE}$	t_{DV}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$	–	–	1	µs
$\overline{CE}$ Pulse Width During Programming	t_{PW}		45	50	55	ms
$\overline{OE}$ Pulse Rise Time During Programming	t_{PRT}		50	–	–	ns
V_{PP} Recovery Time	t_{VR}		2	–	–	µs

Programming Waveforms:



Note 11. All times shown in ( ) are minimum and in µs unless otherwise specified.

Note 12. The input timing reference level is 1V for V_{IL} and 2V for V_{IH}.

Note 13. t_{OE} and T_{DF} are characteristics of the device but must be accommodate by the programmer.

Programming (CAUTION: Exeeding 22V on pin (V_{pp}) will damage the NTE2732A);

When delivered, and after each erasure, all bits of the NTE2732A are in the “1” state. Data is introduced by selectively programming “0”s into the desired bit locations. Although only “0”s will be programmed, both “1”s and “0”s can be presented in the data word. The only way to change a “0” to a “1” is by ultraviolet light erasure.

The NTE2732A is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 21V. It is required that a 0.1μF capacitor be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50msec, active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time–either individualy, sequentially, or at random. The program pulse has a maximum width of 55msec. The NTE2732A must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple NTE2732A is in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NTE2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NTE2732As.

Program Inhibit:

Programming of multiple NTE2732As in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}/V_{pp}$) of the parallel NTE2732As may be common. A TTL level program pulse applied to a NTE2732As $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 21V will program that NTE2732A. A high level $\overline{CE}$ input inhibits the other NTE2732As from being programmed.

Program Verify:

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}.

Erasure Operation:

The erasure characteristics of the NTE2732A are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstroms (A). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical NTE2732A in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to the direct sunlight. If the NTE2732A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the NTE2732A window to prevent unintentional erasure.

The recommended erasure procedure for the NTE2732A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (A). The integrated dose (i.e. UV intensity x exposure time) for erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm2 power rating. The NTE2732A should be placed within 2.5cm of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Pin Connection Diagram

