**Freescale Semiconductor**
Advance Information

Document Number: MAG3110
Rev 2.0, 02/2011

RoHS

# 3-Axis, Digital Magnetometer

**MAG3110**

**MAG3110: 3-AXIS DIGITAL MAGNETOMETER**

Freescale's MAG3110 is a small, low-power, digital 3-axis magnetometer.

The device can be used in conjunction with a 3-axis accelerometer to produce orientation independent accurate compass heading information. It features a standard $I^2C$ serial interface output and smart embedded functions.

The MAG3110 is capable of measuring magnetic fields with an Output Data Rate (ODR) up to 80 Hz; these output data rates correspond to sample intervals from 12 ms to several seconds.

The MAG3110 is available in a plastic DFN package and it is guaranteed to operate over the extended temperature range of -40°C to +85°C.

**Top and Bottom View**


**10 PIN DFN**
**2 mm x 2 mm x 0.85 mm**
**CASE 2154**

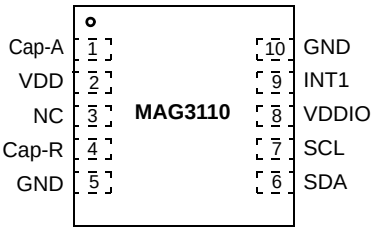
### Features

- 1.95V to 3.6V Supply Voltage (VDD)
- 1.65V to VDD IO Voltage (VDDIO)
- Ultra Small 2 mm x 2 mm x 0.85 mm, 0.4 mm Pitch, 10 Pin Package
- Full Scale Range ±1000 μT
- Sensitivity of 0.10 μT
- Noise down to 0.05 μT rms
- Output Data Rates (ODR) up to 80 Hz
- $I^2C$ digital output interface (operates up to 400 kHz Fast Mode)
- 7-bit $I^2C$ address = 0x0E
- Sampled Low Power Mode
- RoHS compliant

### Applications

- Electronic Compass
- Dead-reckoning assistance for GPS backup
- Location-based Services

**Top View**




**Pin Connections**

| ORDERING INFORMATION | | | |
|---|---|---|---|
| **Part Number** | **Temperature Range** | **Package Description** | **Shipping** |
| MAG3110FCR2 | -40°C to +85°C | DFN-10 | Tape and Reel |

This document contains information on a new product.
Specifications and information herein are subject to change without notice.



freescale Xtrinsic

### Application Notes for Reference

The following is a list of Freescale Application Notes written for the MAG3110:

- **AN4246**, *Calibrating for Soft Iron and Hard Iron Distortions*
- **AN4247***, PCB Layout Guidelines and Recommendations*
- **AN4248***, Using the MAG3110 Magnetometer for an eCompass Application*
- **AN4249**, *Using the MAG3110 Magnetometer to Implement a 3-D Pointer*

# 1 Block Diagram and Pin Description

## 1.1 Block Diagram

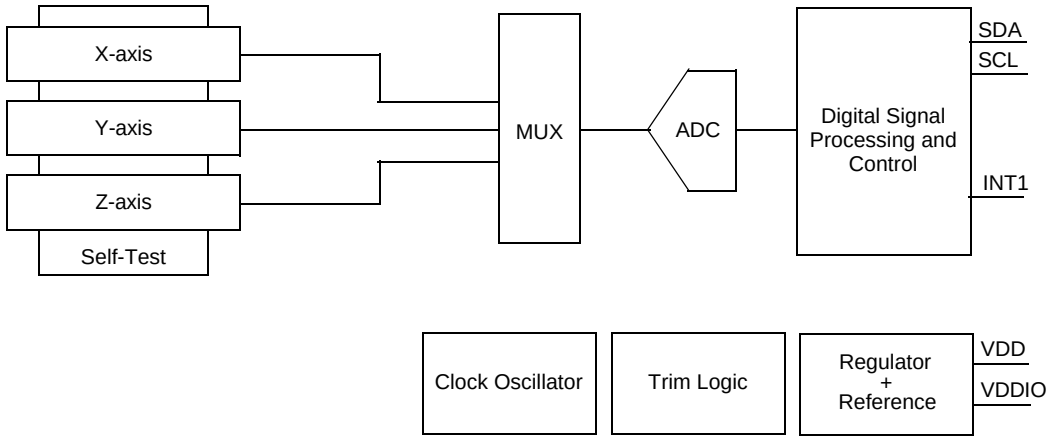



**Figure 1. Block Diagram**

## 1.2 Pin Description

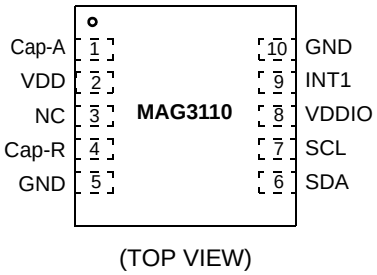



**Figure 2. Pin Connections**

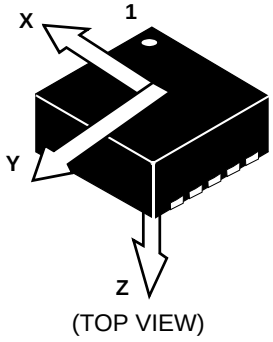



**Figure 3. Measurement Coordinate System**

**Table 1. Pin Description**

| Pin | Name | Function |
|---|---|---|
| 1 | Cap-A | Bypass Cap for Internal Regulator |
| 2 | VDD | Power Supply, 1.95V – 3.6V |
| 3 | NC | No Connect – do not connect |
| 4 | Cap-R | Cap for Reset Pulse |
| 5 | GND | GND |
| 6 | SDA | $I^2C$ Serial Data (Write = 0x1C; Read = 0x1D) |
| 7 | SCL | $I^2C$ Serial Clock |
| 8 | VDDIO | Power for I/O Buffers, 1.65V - VDD |
| 9 | INT1 | Interrupt - Active High Output |
| 10 | GND | GND |

## 1.3 Application Circuit

The device power is supplied through VDD line. Power supply decoupling capacitors (100 nF ceramic) should be placed as near as possible to pins 1 and 2 of the device. VDDIO supplies power for the I/O pins SCL, SDA, and INT1.

The control signals SCL and SDA, are not tolerant of voltages more than VDDIO + 0.3 volts. If VDDIO is removed, the control signals SCL and SDA will clamp any logic signals with their internal ESD protection diodes.

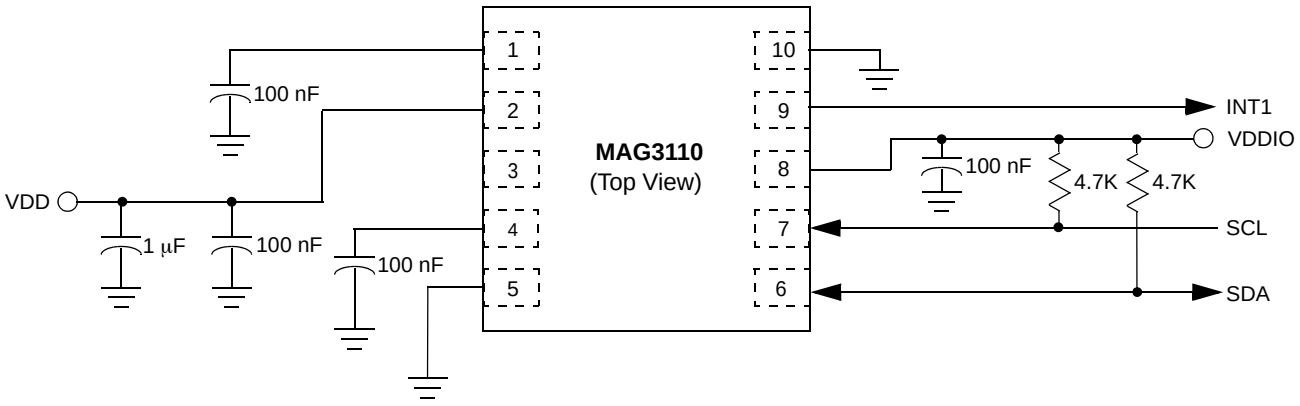



**Figure 4. Electrical Connection**

# 2 Operating and Electrical Specifications

## 2.1 Operating Characteristics

**Table 2. Operating Characteristics @ VDD = 1.8 V, T = 25°C unless otherwise noted.**

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Full Scale Range | | FS | | ±1000 | | µT |
| Output Data Range (RAW = 1) | | | -15,000 | | 15,000 | bits |
| Output Data Range (RAW = 0) | | | -30,000 | | 30,000 | bits |
| Sensitivity | | So | | 0.10 | | µT/bits |
| Sensitivity Change vs. Temperature | | Tc | | ±0.1 | | %/°C |
| Zero Flux Offset Accuracy | | | | ±500 | | µT |
| Zero Flux Change with Temperature | | Tco | | ±0.01 | | µT/°C |
| Hysteresis | | | | | 1 | % |
| Non Linearity<br>Best Fit Straight Line | | NL | -1 | ±0.3 | 1 | %FS |
| Temp Sensor Repeatability | | | | 1 | | °C |
| Magnetometer Output Noise | OS = 00[1] | Noise | | 0.14 | | µT rms |
| | OS = 01 | | | 0.1 | | |
| | OS = 10 | | | 0.07 | | |
| | OS = 11 | | | 0.05 | | |
| Self-test Output Change[2]<br>X-axis<br>Y-axis<br>Z-axis | | Vst | 20<br>20<br>20 | | | LSB<br>LSB<br>LSB |
| Operating Temperature Range | | $T_{op}$ | -40 | | +85 | °C |

1. OS = Over Sampling Ratio.
2. Self-test is one direction only.

## 2.2 Absolute Maximum Ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 3. Maximum Ratings**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | VDD | -0.3 to +3.6 | V |
| Input Voltage on any Control Pin (SCL, SDA) | Vin | -0.3 to VDD + 0.3 | V |
| Maximum Applied Magnetic Field | — | 100,000 | µT |
| Operating Temperature Range | $T_{op}$ | -40 to +85 | °C |
| Storage Temperature Range | $T_{STG}$ | -40 to +125 | °C |

**Table 4. ESD and Latch-up Protection Characteristics**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Human Body Model | HBM | ±2000 | V |
| Machine Model | MM | ±200 | V |
| Charge Device Model | CDM | ±500 | V |
| Latch-up Current at T = 85°C | — | ±100 | mA |


This device is sensitive to mechanical shock. Improper handling can cause permanent damage of the part or cause the part to otherwise fail.


This is an ESD sensitive, improper handling can cause permanent damage to the part.

## 2.3 Electrical Characteristics

**Table 5. Electrical Characteristics @ VDD = 2.0V, VDDIO = 1.8V, T = 25°C unless otherwise noted**

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | | VDD | 1.95 | 2.4 | 3.6 | V |
| Interface Supply Voltage | | VDDIO | 1.62 | | VDD | V |
| Supply Current in ACTIVE Mode | ODR[1] 10 Hz, OS[1] = 11 | $I_{dd}$ | | 900 | | µA |
| | ODR 10 Hz, OS = 10 | | | 480 | | |
| | ODR 10 Hz, OS = 01 | | | 280 | | |
| | ODR 10 Hz, OS = 00 | | | 140 | | |
| | ODR 5 Hz, OS = 00 | | | 70 | | |
| | ODR 1.25 Hz, OS = 00 | | | 24 | | |
| Supply Current Drain in STANDBY Mode | Measurement mode off | $I_{dd}$Stby | | 2 | | µA |
| Digital High Level Input Voltage SCL, SDA | | VIH | 0.75*VDDIO | | | V |
| Digital Low Level Input Voltage SCL, SDA | | VIL | | | 0.3* VDDIO | V |
| High Level Output Voltage INT1 | $I_O$ = 500 µA | VOH | 0.9*VDDIO | | | V |
| Low Level Output Voltage INT1 | $I_O$ = 500 µA | VOL | | | 0.1* VDDIO | V |
| Low Level Output Voltage SDA | $I_O$ = 500 µA | VOLS | | | 0.1* VDDIO | V |
| Output Data Rate (ODR) | | ODR | 0.8*ODR | ODR | 1.2 *ODR | Hz |
| Signal Bandwidth | | BW | | ODR/2 | | Hz |
| Boot Time from Power applied to Boot Complete | | BT | | | 10 | ms |
| Turn-on Time[2] | OS = 1 | $T_{on}$ | | 25 | | ms |
| Operating Temperature Range | | $T_{op}$ | -40 | | +85 | °C |

1. ODR = Output Data Rate; OS = Over Sampling Ratio.
2. Time to obtain valid data from STANDBY mode to ACTIVE Mode.

## 2.4 I²C Interface Characteristics

**Table 6. I²C Slave Timing Values(1)**

| Parameter | Symbol | I²C Fast Mode | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| SCL Clock Frequency<br>Pull-up = 1 kΩ, $C_b$ = 20 pF<br>Pull-up = 1 kΩ, $C_b$ = 400 pF | $f_{SCL}$ | <br>0<br>0 | <br>400<br>TBD | <br>kHz<br>kHz |
| Bus Free Time between STOP and START Condition | $t_{BUF}$ | 1.3 | | µs |
| Repeated START Hold Time | $t_{HD;STA}$ | 0.6 | | µs |
| Repeated START Set-up Time | $t_{SU;STA}$ | 0.6 | | µs |
| STOP Condition Set-up Time | $t_{SU;STO}$ | 0.6 | | µs |
| SDA Data Hold Time(2) | $t_{HD;DAT}$ | 50(3) | (4) | µs |
| SDA Valid Time (5) | $t_{VD;DAT}$ | | 0.9(4) | µs |
| SDA Valid Acknowledge Time (6) | $t_{VD;ACK}$ | | 0.9(4) | µs |
| SDA Set-up Time | $t_{SU;DAT}$ | 100(7) | | ns |
| SCL Clock Low Time | $t_{LOW}$ | 1.3 | | µs |
| SCL Clock High Time | $t_{HIGH}$ | 0.6 | | µs |
| SDA and SCL Rise Time | $t_r$ | 20 + 0.1$C_b$(8) | 1000 | ns |
| SDA and SCL Fall Time (3) (8) (9) (10) | $t_f$ | 20 + 0.1$C_b$(8) | 300 | ns |
| Pulse width of spikes on SDA and SCL that must be suppressed by input filter | $t_{SP}$ | | 50 | ns |

1. All values referred to VIH (min) and VIL (max) levels.
2. $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
3. A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the VIH (min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
4. The maximum $t_{HD;DAT}$ could be must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This device does not stretch the LOW period ($t_{LOW}$) of the SCL signal.
5. $t_{VD;DAT}$ = time for Data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
6. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
7. A Fast mode I²C device can be used in a Standard mode I²C system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_r$(max) + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I²C specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time
8. $C_b$ = total capacitance of one bus line in pF.
9. The maximum $t_f$ for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage $t_f$ is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified $t_f$.
10. In Fast mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

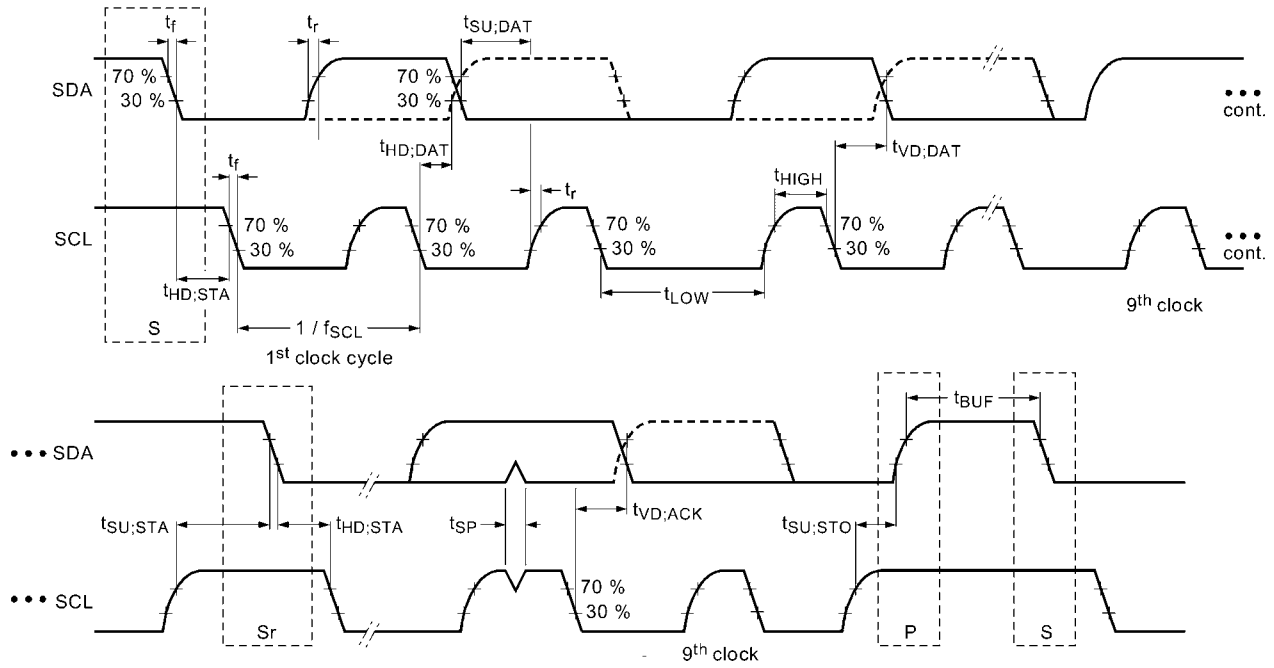



**Figure 5. I²C Slave Timing Diagram**

## 2.5 General I²C Information

The SCL and SDA signals are driven by open-drain buffers and a pull-up resistor is required to make the signals rise to the high state. The value of the pull-up resistors depends on the system I²C clock rate and the capacitance load on the I²C bus.

Higher resistance value pull-up resistors consume less power, but have a slower the rise time (due to the RC time constant between the bus capacitance and the pull-up resistor) and will limit the I²C clock frequency.

Lower resistance value pull-up resistors consume more power, but enable higher I²C clock operating frequencies.

High bus capacitance is due to long bus lines or a high number of I²C devices connected to the bus. A lower value resistance pull-up resistor is required in higher bus capacitance systems.

For standard 100 kHz clock I²C, pull-up resistors typically are between 5k and 10 kΩ. For a heavily loaded bus, the pull-up resistor value may need to be reduced. For higher speed 400 kHz or 800 kHz clock I²C, bus capacitance will need to be kept low, in addition to selecting a lower value resistance pull-up resistor. Pull-up resistors for high speed buses typically are about 1 KΩ.

In a well designed system with a microprocessor and one I²C device on the bus, with good board layout and routing, the I²C bus capacitance can be kept under 20 pF. With a 1K pull-up resistor, the I²C clock rates can be well in excess of a few megahertz.

# 3 Modes of Operation

**Table 7. Modes of Operation Description**

| Mode | I²C Bus State | Function Description |
|---|---|---|
| STANDBY | I²C communication is possible. | Only POR and digital blocks are enabled. Analog subsystem is disabled. |
| ACTIVE | I²C communication is possible. | All blocks are enabled (POR, Digital, Analog). |

# 4 Functionality

MAG3110 is a small low-power, digital output, 3-axis linear magnetometer packaged in a 10 pin DFN. The device contains a magnetic transducer for sensing and an ASIC for control and digital $I^2C$ communications.

## 4.1 $I^2C$ Serial Interface

Communication with the MAG3110 takes place over an $I^2C$ bus. The MAG3110 also has an interrupt signal indicating that new magnetic data readings are available. Interrupt driven sampling allows operation without the overhead of software polling.

## 4.2 Factory Calibration

MAG3110 is factory calibrated for sensitivity, offset and temperature coefficient. All factory calibration coefficients are applied automatically by the MAG3110 ASIC before the magnetic field readings are written to registers 0x01 to 0x06 (see section 5). There is no need for the user to apply the calibration correction in the software and the calibration coefficients are not therefore accessible to the user.

The offset registers in the addresses 0x09 to 0x0E are not a factory calibration offset but allow the user to define a hard iron offset which can be automatically subtracted from the magnetic field readings (see section 4.3.3).

## 4.3 Digital Interface

**Table 8. Serial Interface Pin Description**

| Pin Name | Pin Description |
|---|---|
| VDDIO | IO voltage |
| SCL | $I^2C$ Serial Clock |
| SDA | $I^2C$ Serial Data |
| INT | Data ready interrupt pin |

There are two signals associated with the $I^2C$ bus: the Serial Clock Line (SCL) and the Serial Data line (SDA). External pull-up resistors (connected to VDDIO) are needed for SDA and SCL. When the bus is free, both lines are high. The $I^2C$ interface is compliant with Fast mode (400 kHz), and Normal mode (100 kHz) $I^2C$ standards.

### 4.3.1 General $I^2C$ Operation

$I^2C$ is an asynchronous, open collector driven, addressed and packetized serial bus interface. It is capable of supporting multiple masters and multiple slave devices on the same bus. $I^2C$ uses two bi-directional lines, the serial clock line or SCL and the serial data line or SDA. Pull-up resistors are required on both lines.

An $I^2C$ transaction starts with a start condition (START) and ends with a stop condition (STOP). A START condition is defined as a HIGH to LOW transition on the data line while the clock line is held HIGH. A STOP condition is defined as a LOW to HIGH transition on the data line while the clock line is held HIGH. At all other times, the data line can only change state when the clock line is low. If the data line changes state when the clock is high, the $I^2C$ transaction is aborted and the new start or stop condition is recognized.

After START has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after START condition is the slave address in the first 7 bits, and the eighth bit is the Read/Write (R/W) bit (read = 1, write = 0). The R/W bit determines whether the $I^2C$ master intends on receiving data from the slave – Read mode or intends to transmit data to the slave – Write mode. When an address is sent, each device on the $I^2C$ bus compares the first 7 bits after a start condition with its own internal address. If the address matches, the device considers itself addressed by the Master and continues to respond. If the address does not match, the device ignores further bus activity until the next start condition happens.

The ninth bit (clock pulse), following each $I^2C$ byte is for the acknowledge (ACK) bit. The master releases the SDA line during the ACK period. Because of the pull-up resistor, the data line will tend to float high. To signal ACK back to the master, the slave must then pull the data line low during this clock period.

The number of bytes per transfer can be unlimited. If a receiving device can't accept another complete byte of data until it has performed some other function, it can hold the clock line, SCL, low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. This delay action is called clock stretching. The MAG3110 device does clock stretching.

A data transfer is always terminated by a STOP.

The MAG3110 $I^2C$ 7-bit device address is 0x0E. In $I^2C$ practice, the device address is shifted left by one bit field and a read/write bit is set in the lowest bit position. The $I^2C$ 8-bit write address is 0x1C and the read address is 0x1D.

The $I^2C$ 8-bit write address is 0x3A and the read address is 0x3B. Please consult the factory for alternate addresses.

See Figure 6 for details on how to perform read/write operations with MAG3110.

**Single/Burst Write Operation**

| | | | | | | |
|---|---|---|---|---|---|---|
| IIC Start | IIC Slave ADDR (R/W bit = 0) | MAG3110 Register Address to Start Write | Data0* | Data1 | — | IIC STOP |

* Data Bytes Outgoing

**Single/Burst Read Operation**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| IIC Start | IIC Slave ADDR (R/W bit = 0) | MAG3110 Register Address to Start Read | IIC Repeated Start | IIC Slave ADDR (R/W bit = 1) | Data0* | Data1 | — | IIC STOP |

* Data Bytes Incoming

**Figure 6. MAG3110 $I^2C$ Generic Read/Write Operations**

### 4.3.2 Fast Read Mode

When the Fast Read (FR) bit is set (CTRL_REG1, 0x10, bit 2), the MSB 8-bit data is read through the $I^2C$ bus. Auto-increment is set to skip over the LSB data. When FR bit is cleared, the complete 16-bit data is read accessing all 6 bytes sequentially (OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, OUT_Z_LSB).

### 4.3.3 User Offset Corrections

The 2's complement user offset correction register values are used to compensate for correcting the X, Y, and Z-axis after device board mount. These values may be used to compensate for hard iron interference.

Depending on the setting of the RAW bit (CTRL_REG2, 0x11, bit 5) the magnetic field sample data is corrected with the user offset values (RAW = 0), or can be read out uncorrected for user offset values (RAW = 1). The factory calibration correction is always applied irrespective of the setting of the RAW bit.

The factory calibration for gain, offset and temperature compensation is always automatically applied irrespective of the setting of the RAW bit which only controls the subtraction of the user defined hard iron offset.

### 4.3.4 INT1

The DR_STATUS register (see section 5.1.1) contains the ZYXDR bit which denotes the presence of new measurement data on one or more axes. Software polling can be used to detect the transition of the ZYXDR bit from 0 to 1 but, since the ZYXDR bit is also logically connected to the INT1 pin, a more efficient approach is to use INT1 to trigger a software interrupt when new measurement data is available as follows:

1. Put MAG3110 in ACTIVE mode (CTRL_REG1 = 0bXXXXXX01).
2. Idle until INT1 goes HIGH and activates an interrupt service routine in the user software.
3. Read magnetometer data as required from registers 0x01 to 0x06. INT1 is cleared when register 0x01 OUT_X_MSB is read and this register must therefore always be read in the interrupt service routine.
4. Return to idle in step 2.

### 4.3.5 Triggered Measurements

Set the TM bit in CTRL_REG1 when you want the part to acquire only 1 sample on each axis. See table below for details.

| AC | TM | Description |
|---|---|---|
| 0 | 0 | ASIC is in low power standby mode. |
| 0 | 1 | The ASIC shall exit standby mode, perform one measurement cycle based on the programmed ODR and OSR setting, update the $I^2C$ data registers and re-enter standby mode. |
| 1 | 0 | The ASIC shall perform continuous measurements based on the current OSR and ODR settings. |
| 1 | 1 | The ASIC shall continue current measurement at fastest applicable ODR for programmed OSR. The ASIC shall return to programmed ODR after completing the triggered measurement. |

# 5 Register Description

**Table 9. Register Address Map**

| Name | Type | Register Address | Auto-Increment Address (Fast Read)(1) | Default Value | Comment |
|---|---|---|---|---|---|
| DR_STATUS(2) | R | 0x00 | 0x01 | 0000 0000 | Data ready status per axis |
| OUT_X_MSB(2) | R | 0x01 | 0x02 (0x03) | data | Bits [15:8] of X measurement |
| OUT_X_LSB(2) | R | 0x02 | 0x03 | data | Bits [7:0] of X measurement |
| OUT_Y_MSB(2) | R | 0x03 | 0x04 (0x05) | data | Bits [15:8] of Y measurement |
| OUT_Y_LSB(2) | R | 0x04 | 0x05 | data | Bits [7:0] of Y measurement |
| OUT_Z_MSB(2) | R | 0x05 | 0x06 (0x07) | data | Bits [15:8] of Z measurement |
| OUT_Z_LSB(2) | R | 0x06 | 0x07 | data | Bits [7:0] of Z measurement |
| WHO_AM_I(2) | R | 0x07 | 0x08 | 0xC4 | Device ID Number |
| SYSMOD(2) | R | 0x08 | 0x09 | data | Current System Mode |
| OFF_X_MSB | R/W | 0X09 | 0x0A | 0000 0000 | Bits [14:7] of user X offset |
| OFF_X_LSB | R/W | 0X0A | 0X0B | 0000 0000 | Bits [6:0] of user X offset |
| OFF_Y_MSB | R/W | 0X0B | 0X0C | 0000 0000 | Bits [14:7] of user Y offset |
| OFF_Y_LSB | R/W | 0X0C | 0X0D | 0000 0000 | Bits [6:0] of user Y offset |
| OFF_Z_MSB | R/W | 0X0D | 0X0E | 0000 0000 | Bits [14:7] of user Z offset |
| OFF_Z_LSB | R/W | 0X0E | 0X0F | 0000 0000 | Bits [6:0] of user Z offset |
| DIE_TEMP(2) | R | 0X0F | 0X10 | data | Temperature, signed 8 bits in °C |
| CTRL_REG1(3) | R/W | 0X10 | 0X11 | 0000 0000 | Operation modes |
| CTRL_REG2(3) | R/W | 0X11 | 0x12 | 0000 0000 | Operation modes |

1. Fast Read mode for quickly reading the Most Significant Bytes (MSB) of the sampled data.
2. Register contents are preserved when transitioning from “ACTIVE” to “STANDBY” mode.
3. Modification of this register’s contents can only occur when device is “STANDBY” mode, except the TM and AC bit fields in CTRL_REG1 register.

## 5.1 Sensor Status

### 5.1.1 DR_STATUS (0x00)

**Data Ready Status**

This read-only status register provides the acquisition status information on a per-sample basis, and reflects real-time updates to the OUT_X, OUT_Y, and OUT_Z registers.

**Table 10. DR_STATUS Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| ZYXOW | ZOW | YOW | XOW | ZYXDR | ZDR | YDR | XDR |

**Table 11. DR_STATUS Description**

| | |
|---|---|
| ZYXOW | X, Y, Z-axis Data Overwrite. Default value: 0.<br>0: No data overwrite has occurred.<br>1: Previous X or Y or Z data was overwritten by new X or Y or Z data before it was completely read. |
| ZOW | Z-axis Data Overwrite. Default value: 0.<br>0: No data overwrite has occurred.<br>1: Previous Z-axis data was overwritten by new Z-axis data before it was read. |
| YOW | Y-axis Data Overwrite. Default value: 0.<br>0: No data overwrite has occurred.<br>1: Previous Y-axis data was overwritten by new Y-axis data before it was read. |
| XOW | X-axis Data Overwrite. Default value: 0<br>0: No data overwrite has occurred.<br>1: Previous X-axis data was overwritten by new X-axis data before it was read. |
| ZYXDR | X or Y or Z-axis new Data Ready. Default value: 0.<br>0: No new set of data ready.<br>1: New set of data is ready. |
| ZDR | Z-axis new Data Available. Default value: 0.<br>0: No new Z-axis data is ready.<br>1: New Z-axis data is ready. |
| YDR | Z-axis new Data Available. Default value: 0.<br>0: No new Y-axis data is ready.<br>1: New Y-axis data is ready. |
| XDR | Z-axis new Data Available. Default value: 0.<br>0: No new X-axis data is ready.<br>1: New X-axis data is ready. |

**ZYXOW** is set to 1 whenever new data is acquired before completing the retrieval of the previous set. This event occurs when the content of at least one data register (i.e. OUT_X, OUT_Y, OUT_Z) has been overwritten. ZYXOW is cleared when the high-bytes of the data (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) of all active channels are read.

**ZOW** is set to 1 whenever new Z-axis acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. ZOW is cleared any time OUT_Z_MSB register is read.

**YOW** is set to 1 whenever new Y-axis acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. YOW is cleared any time OUT_Y_MSB register is read.

**XOW** is set to 1 whenever new X-axis acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. XOW is cleared any time OUT_X_MSB register is read.

**ZYXDR** signals that new acquisition for any of the enabled channels is available. ZYXDR is cleared when the high-bytes of the data (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) of all the enabled channels are read.

**ZDR** is set to 1 whenever new Z-axis data acquisition is completed. ZDR is cleared any time OUT_Z_MSB register is read.

**YDR** is set to 1 whenever new Y-axis data acquisition is completed. YDR is cleared any time OUT_Y_MSB register is read.

**XDR** is set to 1 whenever new X-axis data acquisition is completed. XDR is cleared any time OUT_X_MSB register is read.

### 5.1.2 OUT_X_MSB (0x01), OUT_X_LSB (0x02), OUT_Y_MSB (0x03), OUT_Y_LSB (0x04), OUT_Z_MSB (0x05), OUT_Z_LSB (0x06)

X-axis, Y-axis, and Z-axis 16-bit output sample data of the magnetic field strength expressed as signed 2's complement numbers.

When RAW mode is enabled (RAW = 1), the output range is between -15,000 to 15,000 bit counts (the combination of the 1000 μT full scale range and the zero flux offset ranging up to 500 μT).

When RAW mode is not enabled (RAW = 0), the output range is between -30,000 to 30,000 bit counts when the user offset ranging between -15,000 to 15,000 bit counts is included

The DR_STATUS register, OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, and OUT_Z_LSB are stored in the auto-incrementing address range of 0x00 to 0x06. Data acquisition is a sequential read of 6 bytes.

If the Fast Read (FR) bit is set in CTRL_REG1 (0x10), auto-increment will skip over LSB of the X, Y, Z sample registers. This will shorten the data acquisition from 6 bytes to 3 bytes. If the LSB registers are directly addressed, the LSB information can still be read regardless of FR bit setting.

The preferred method for reading data registers is the burst read method where the user application acquires data sequentially starting from register 0x01. If register 0x01 is not read, the rest of the data registers (0x02 - 0x06) will not be updated with the most recent acquisition. It is still possible to address individual data registers, however register 0x01 must be read prior to ensure reading latest acquisition.

**Table 12. OUT_X_MSB Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| XD15 | XD14 | XD13 | XD12 | XD11 | XD10 | XD9 | XD8 |

**Table 13. OUT_X_LSB Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| XD7 | XD6 | XD5 | XD4 | XD3 | XD2 | XD1 | XD0 |

**Table 14. OUT_Y_MSB Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| YD15 | YD14 | YD13 | YD12 | YD11 | YD10 | YD9 | YD8 |

**Table 15. OUT_Y_LSB Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| YD7 | YD6 | YD5 | YD4 | YD3 | YD2 | YD1 | YD0 |

**Table 16. OUT_Z_MSB Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| ZD15 | ZD14 | ZD13 | ZD12 | ZD11 | ZD10 | ZD9 | ZD8 |

**Table 17. OUT_Z_LSB Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| ZD6 | ZD6 | ZD5 | ZD4 | ZD3 | ZD2 | ZD1 | ZD0 |

## 5.2 Device ID

### 5.2.1 WHO_AM_I (0x07)

Device identification register. This read-only register contains the device identifier which is set to 0xC4. This value is factory programmed. Consult factory for custom alternate values.

**Table 18. WHO_AM_I Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

### 5.2.2 SYSMOD (0x08)

The read-only system mode register indicates the current device operating mode.

**Table 19. SYSMOD Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | SYSMOD1 | SYSMOD0 |

**Table 20. SYSMOD Description**

| | |
|---|---|
| SYSMOD | System Mode. Default value: 00.<br>00: STANDBY mode.<br>01: ACTIVE mode, RAW data.<br>10: ACTIVE mode, non-RAW user-corrected data. |

## 5.3 User Offset Correction

### 5.3.1 OFF_X_MSB (0x09), OFF_X_LSB (0x0A), OFF_Y_MSB (0x0B), OFF_Y_LSB (0x0C), OFF_Z_MSB (0x0D), OFF_Z_LSB (0x0E)

X-axis, Y-axis, and Z-axis user defined offsets in 2's complement format which are used when RAW = 0 (see section 5.5.2) to correct for the MAG3110 zero flux offset and for hard iron offsets on the PCB caused by external components. The maximum sensible range for the user offsets is in the range -15,000 to 15,000 bit counts comprising the sum of the correction for the zero flux offset (range -500 μT to 500 μT or -5000 to 5000 bit counts) and the PCB hard iron offset (range -1000 μT to 1000 μT or -10,000 to 10,000 bit counts).

The user offsets are automatically subtracted by the MAG3110 logic when RAW = 0 before the magnetic field readings are written to the data measurement registers 0x01 to 0x06. The maximum range of the X, Y and Z data measurement registers when RAW = 0 is therefore -30,000 to 30,000 bit counts and is computed without clipping. The user offsets are not subtracted when RAW = 1. The least significant bit of the user defined X, Y and Z offsets is forced to be zero irrespective of the value written by the user.

If the MAG3110 zero flux offset and PCB hard iron offset corrections are performed by an external microprocessor (the most likely scenario) then the user offset registers can be ignored and the RAW bit should be set to 1.

The user offset registers should not be confused with the factory calibration corrections which are not user accessible and which are always applied to the measured magnetic data.

**Table 21. OFF_X_MSB Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| XD14 | XD13 | XD12 | XD11 | XD10 | XD9 | XD8 | XD7 |

**Table 22. OFF_X_LSB Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| XD6 | XD5 | XD4 | XD3 | XD2 | XD1 | XD0 | 0 |

**Table 23. OFF_Y_MSB Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| YD14 | YD13 | YD12 | YD11 | YD10 | YD9 | YD8 | YD7 |

**Table 24. OFF_Y_LSB Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| YD6 | YD5 | YD4 | YD3 | YD2 | YD1 | YD0 | 0 |

**Table 25. OFF_Z_MSB Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| ZD14 | ZD13 | ZD12 | ZD11 | ZD10 | ZD9 | ZD8 | ZD7 |

**Table 26. OFF_Z_LSB Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| ZD6 | ZD5 | ZD4 | ZD3 | ZD2 | ZD1 | ZD0 | 0 |

## 5.4 Temperature

### 5.4.1 DIE_TEMP (0x0F)

Temperature °C expressed as an 8-bit 2's complement number. The data allows for temperatures from -128°C to 127°C but in actual function the range is from -40°C to 125°C.

**Table 27. TEMP Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |

## 5.5 Control Registers

**Note:** Except for STANDBY mode selection, the device must be in STANDBY mode to change any of the fields within CTRL_REG1 (0x10).

### 5.5.1 CTRL_REG1 (0x10)

**Table 28. CTRL_REG1 Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| DR2 | DR1 | DR0 | OS1 | OS0 | FR | TM | AC |

**Table 29. CTRL_REG1 Description**

| | |
|---|---|
| DR[2:0] | Data rate selection. Default value: 000.<br>See Table 30 for more information. |
| OS [1:0] | This register configures the over sampling ratio or measurement integration time.<br>Default value: 00.<br>See Table 30 for more information. |
| FR | Fast Read selection. Default value: 0.<br>0: The full 16-bit values are read.<br>1: Fast Read, 8-bit values read from the MSB registers. |
| TM | Trigger immediate measurement. Default value: 0<br>0: Normal operation based on AC condition.<br>1: Trigger measurement.<br>If part is in ACTIVE mode, any measurement in progress will complete before triggered measurement.<br>In STANDBY mode triggered measurement will occur immediately and part will return to STANDBY mode as soon as the measurement is complete. |
| AC | Operating mode selection. Default value: 0.<br>0: STANDBY mode.<br>1: ACTIVE mode.<br>ACTIVE mode will make periodic measurements based on values programmed in the Data Rate (DR) and Over Sampling Ratio bits (OS). |

**Table 30. Over Sampling Ratio and Data Rate Description**

| DR2 | DR1 | DR0 | OS1 | OS0 | Output Rate (Hz) | Over Sample Ratio | Current Est μA | Noise Est μT rms |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 80.00 | 1 | 900.0 | 0.14 |
| 0 | 0 | 0 | 0 | 1 | 40.00 | 2 | 900.0 | 0.1 |
| 0 | 0 | 0 | 1 | 0 | 20.00 | 4 | 900.0 | 0.07 |
| 0 | 0 | 0 | 1 | 1 | 10.00 | 8 | 900.0 | 0.05 |
| 0 | 0 | 1 | 0 | 0 | 40.00 | 1 | 480.0 | 0.14 |
| 0 | 0 | 1 | 0 | 1 | 20.00 | 2 | 480.0 | 0.1 |
| 0 | 0 | 1 | 1 | 0 | 10.00 | 4 | 480.0 | 0.07 |
| 0 | 0 | 1 | 1 | 1 | 5.00 | 8 | 480.0 | 0.05 |
| 0 | 1 | 0 | 0 | 0 | 20.00 | 1 | 275.0 | 0.14 |
| 0 | 1 | 0 | 0 | 1 | 10.00 | 2 | 275.0 | 0.1 |
| 0 | 1 | 0 | 1 | 0 | 5.00 | 4 | 275.0 | 0.07 |
| 0 | 1 | 0 | 1 | 1 | 2.50 | 8 | 275.0 | 0.05 |
| 0 | 1 | 1 | 0 | 0 | 10.00 | 1 | 137.5 | 0.14 |
| 0 | 1 | 1 | 0 | 1 | 5.00 | 2 | 137.5 | 0.1 |
| 0 | 1 | 1 | 1 | 0 | 2.50 | 4 | 137.5 | 0.07 |
| 0 | 1 | 1 | 1 | 1 | 1.25 | 8 | 137.5 | 0.05 |
| 1 | 0 | 0 | 0 | 0 | 5.00 | 1 | 68.8 | 0.14 |
| 1 | 0 | 0 | 0 | 1 | 2.50 | 2 | 68.8 | 0.1 |
| 1 | 0 | 0 | 1 | 0 | 1.25 | 4 | 68.8 | 0.07 |
| 1 | 0 | 0 | 1 | 1 | 0.63 | 8 | 68.8 | 0.05 |
| 1 | 0 | 1 | 0 | 0 | 2.50 | 1 | 34.4 | 0.14 |
| 1 | 0 | 1 | 0 | 1 | 1.25 | 2 | 34.4 | 0.1 |
| 1 | 0 | 1 | 1 | 0 | 0.63 | 4 | 34.4 | 0.07 |
| 1 | 0 | 1 | 1 | 1 | 0.31 | 8 | 34.4 | 0.05 |
| 1 | 1 | 0 | 0 | 0 | 1.25 | 1 | 17.2 | 0.14 |
| 1 | 1 | 0 | 0 | 1 | 0.63 | 2 | 17.2 | 0.1 |

**Table 30. Over Sampling Ratio and Data Rate Description**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 0.31 | 4 | 17.2 | 0.07 |
| 1 | 1 | 0 | 1 | 1 | 0.16 | 8 | 17.2 | 0.05 |
| 1 | 1 | 1 | 0 | 0 | 0.63 | 1 | 8.6 | 0.14 |
| 1 | 1 | 1 | 0 | 1 | 0.31 | 2 | 8.6 | 0.1 |
| 1 | 1 | 1 | 1 | 0 | 0.16 | 4 | 8.6 | 0.07 |
| 1 | 1 | 1 | 1 | 1 | 0.08 | 8 | 8.6 | 0.05 |

### 5.5.2 CTRL_REG2 (0x11)

**Table 31. CTRL_REG2 Register**

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| AUTO_MRST_EN | — | RAW | Mag_RST | — | ST_Z | ST_Y | ST_X |

**Table 32. CTRL_REG2 Description**

| | |
|---|---|
| AUTO_MRST_EN | Automatic Magnetic Sensor Reset. Default value: 0.<br>0: Automatic magnetic sensor resets off.<br>1: Automatic magnetic sensor resets on.<br>Similar to Mag_RST, however, the resets occur before each data acquisition. |
| RAW | Data output correction. Default value: 0.<br>0: Normal mode: data values are corrected by the user offset register values.<br>1: Raw mode: data values are not corrected by the user offset register values.<br>The factory calibration is always applied to the measured data stored in registers 0x01 to 0x06 irrespective of the setting of the RAW bit. |
| Mag_RST | Magnetic Sensor Reset. Default value: 0.<br>0: Reset cycle not active.<br>1: Reset cycle initiate or Reset cycle busy/active.<br>When asserted, initiates a magnetic sensor reset cycle that will restore correct operation after exposure to an excessive magnetic field which exceeds the Full Scale Range (see Table 2) but is less than the Maximum Applied Magnetic Field (see Table 3).<br>When the cycle is finished, value returns to 0. |
| ST_Z | Self-test Z-axis Default value: 0.<br>0: No Self-test.<br>1: Self-test, active Z-axis.<br>When this bit is asserted, a magnetic field is generated on the MAG3110 Z-axis to test the operation of this axis. The size of the resulting change is defined as Self-test Output Change in Table 2. The ST_Z bit should be de-asserted at the end of the self-test. |
| ST_Y | Self-test Y-axis. Default value: 0.<br>0: No Self-test.<br>1: Self-test, active Y-axis.<br>When this bit is asserted, a magnetic field is generated on the MAG3110 Y-axis to test the operation of this axis. The size of the resulting change is defined as Self-test Output Change in Table 2. The ST_Y bit should be de-asserted at the end of the self-test. |
| ST_X | Self-test X-axis. Default value: 0.<br>0: No Self-test.<br>1: Self-test, active X-axis.<br>When this bit is asserted, a magnetic field is generated on the MAG3110 X-axis to test the operation of this axis. The size of the resulting change is defined as Self-test Output Change in Table 2. The ST_X bit should be de-asserted at the end of the self-test. |

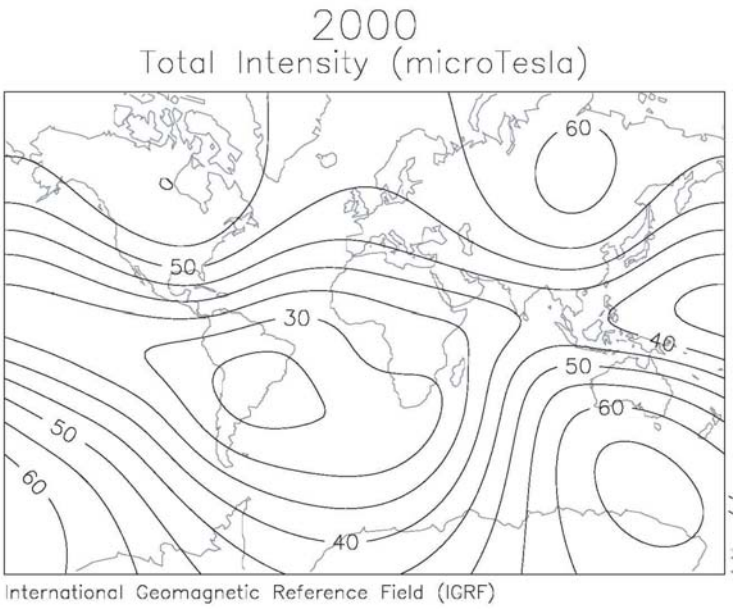
# 6 Geomagnetic Field Maps

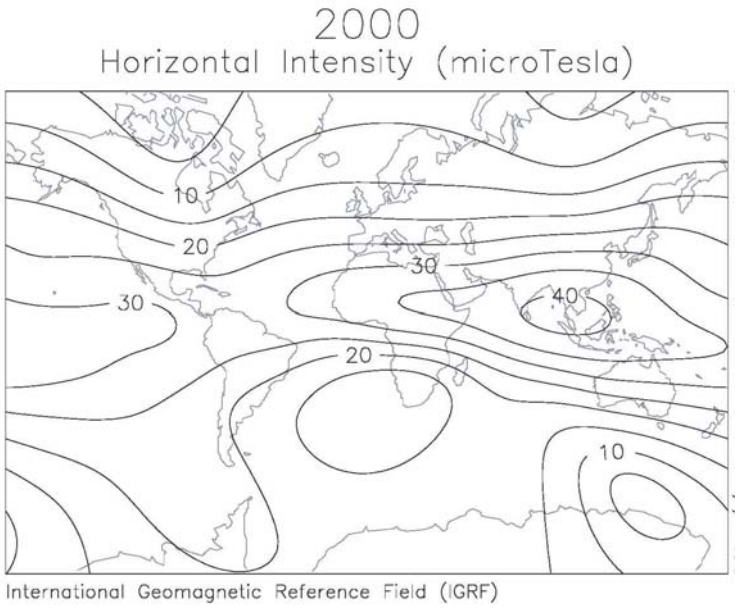
The magnitude of the geomagnetic field varies from 25 μT in South America to about 60 μT over Northern China. The horizontal component of the field varies from zero at the magnetic poles to 40 μT.

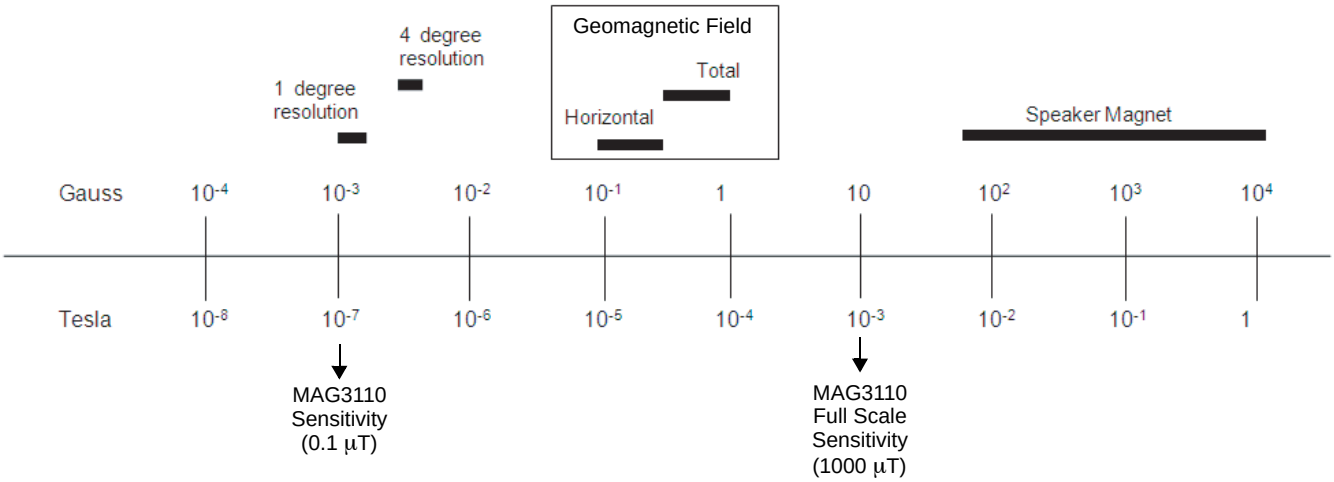
These web sites have further information:

http://wdc.kugi.kyoto-u.ac.jp/igrf/

http://geomag.usgs.gov



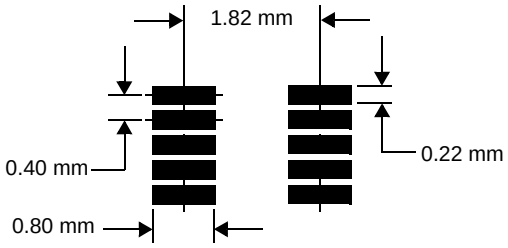






The placement of MAG3110 on the application PCB should be done based on the guidelines given in AN4247, “PCB Layout Guidelines and Recommendations” to minimize magnetic interference to the MAG3110 from other components and ensure that the MAG3110 output does not saturate in fields above 1000 μT.

# 7 Suggested PCB Footprint

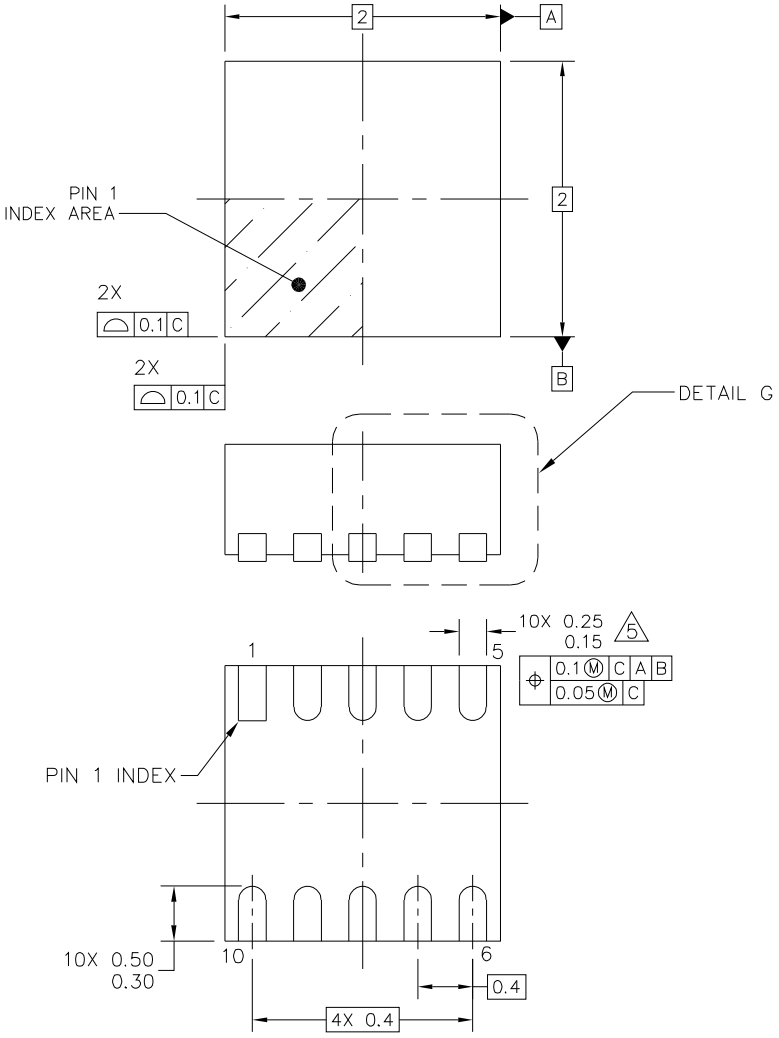
Please see Freescale application note AN1902 for additional information on guidelines for QFN and DFN printed circuit board design and assembly.




Footprint Compiles with IPC-7351A
Footprint Tolerance: 0.02 mm
Solder Paste Stencil: 4 mil thickness, type 3 paste is recommended.

**Figure 7. PCB Footprint Dimensions**

## PACKAGE DIMENSIONS

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| | STANDARD: NON-JEDEC | |

**CASE 2154-01**
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**10 PIN DFN**

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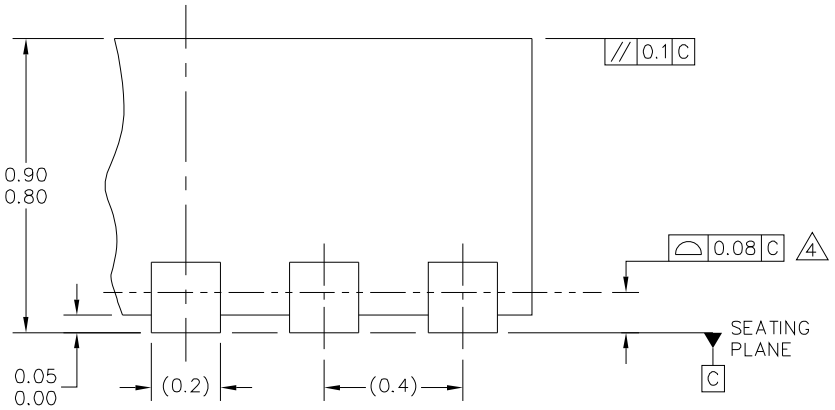


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## PACKAGE DIMENSIONS

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3. THIS IS NON JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO THE TERMINALS AND ALL OTHER BOTTOM SURFACE METALLIZATION.
5. THIS DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURE BETWEEN 0.15 AND 0.25 FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THIS DIMENSION SHALL NOT BE MEASURED IN THE RADIUS AREA.



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02/2011