SSL4120

Resonant power supply controller IC with PFC for LED lighting

Rev. 2 — 1 November 2012 Product data sheet

1. General description

The SSL4120 integrates a Power Factor Corrector (PFC) controller and a controller for a Half-Bridge resonant Converter (HBC) in a multi-chip IC. It provides the drive function for the discrete MOSFET in an up-converter and for the two discrete power MOSFETs in a resonant half-bridge configuration.

Efficient PFC operation is achieved by implementing functions for Quasi-Resonant (QR) operation at high-power levels and QR with valley skipping at lower power levels. OverCurrent Protection (OCP), OverVoltage Protection (OVP) and demagnetization sensing ensure safe operation under all conditions

The HBC module is a high-voltage controller for a zero-voltage switching LLC resonant converter. It contains a high-voltage level shift circuit and several protection circuits including OCP, open-loop protection, capacitive mode protection and a general purpose latched protection input.

The high-voltage chip is fabricated using a proprietary high-voltage Bipolar-CMOS-DMOS power logic process enabling efficient direct start-up from the rectified universal mains voltage. The low-voltage Silicon-On-Insulator (SOI) chip is used for accurate, high-speed protection functions and control.

The SSL4120 controlled PFC circuit and resonant converter topology is very flexible. It can be used for a broad range of applications over a wide mains voltage range. Combining PFC and HBC controllers in a single IC makes the SSL4120 ideal for controlling compact power supplies in lighting applications, such as LED drivers.

Using the SSL4120, highly efficient and reliable power supplies providing over 100 W can be designed easily which use the minimum of external components.

Remark: Unless otherwise stated, all values are typical.

2. Features and benefits

2.1 General features

- Integrated PFC and HBC controllers
- Universal mains supply operation from 85 V to 305 V (AC)
- High level of integration resulting in a low external component count and a cost effective design
- Enable input to enable only the PFC or both the PFC and HBC controllers
- On-chip high-voltage start-up source
- Stand-alone operation or IC supplied from external DC source

2.2 PFC controller features

- Boundary mode operation with on-time control
- Valley/zero-voltage switching for minimum switching losses
- Frequency limiting to reduce switching losses
- Accurate boost voltage regulation
- Burst mode switching with soft-start and soft-stop

2.3 HBC controller features

- Integrated high-voltage level shifter
- Adjustable minimum and maximum frequency
- Maximum 500 kHz half-bridge switching frequency
- Adaptive non-overlap time
- Burst mode switching

2.4 Protection features

- Safe restart mode for system fault conditions
- General latched protection input for output overvoltage protection or external temperature protection
- Protection timer for time-out and restart
- Overtemperature protection
- Soft (re)start for both controllers
- Undervoltage protection for mains (brownout), boost, IC supply and output voltage
- Overcurrent regulation and protection for both controllers
- Accurate overvoltage protection for the boost voltage
- Capacitive mode protection for the HBC controller

3. Applications

The IC is used in all LED lighting applications that require very efficient, low Total Harmonic Distortion (THD), high Power Factor (PF) and a universal mains input voltage.

The SSL4120 provides a cost-effective power supply solution between 25 W and 400 W.

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4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SSL4120T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

5. Block diagram

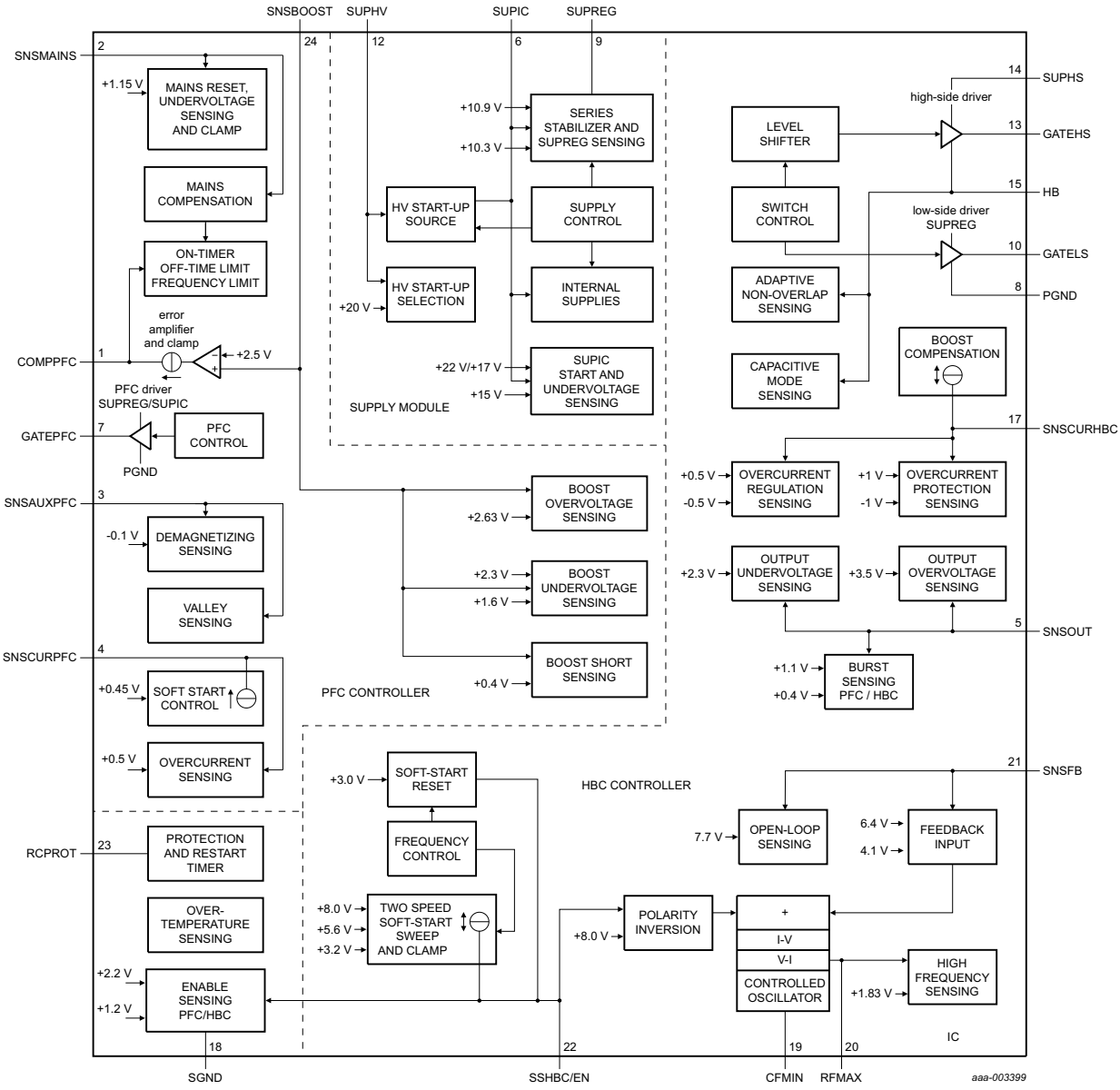


Fig 1. SSL4120 block diagram

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6. Pinning information

6.1 Pinning

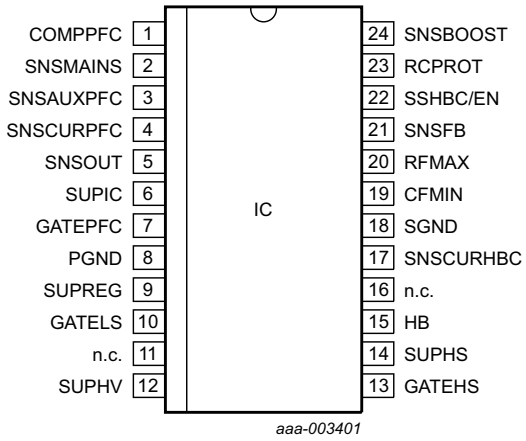


Fig 2. SSL4120T pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
COMPPFC	1	PFC controller frequency compensation. Externally connected to filter
SNSMAINS	2	mains voltage sense input. Externally connected to resistive divided mains voltage
SNSAUXPFC	3	PFC demagnetization timing sense input. Externally connected to the PFC auxiliary winding
SNSCURPFC	4	PFC controller sense input for momentary current and soft-start. Externally connected to current sense resistor and soft-start filter
SNSOUT	5	• HBC output voltage sense input • HBC controller or PFC and HBC controllers sense input for burst mode Externally connected to the HBC transformer auxiliary winding
SUPIC	6	SUPIC input low-voltage supply and output of internal HV start-up source. Externally connected to HBC transformer auxiliary winding or to the external DC supply
GATEPFC	7	PFC MOSFET gate driver output
PGND	8	power ground. HBC low-side and PFC driver reference (ground)
SUPREG	9	regulated SUPREG IC supply; internal regulator output; input drivers. Externally connected to SUPREG buffer capacitor
GATELS	10	HBC low-side MOSFET gate driver output
n.c.	11	not connected; high-voltage spacer.

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Table 2. Pin description *...continued*

Symbol	Pin	Description
SUPHV	12	internal HV start-up source high-voltage supply input. Externally connected to the boost voltage
GATEHS	13	HBC high-side MOSFET gate driver output
SUPHS	14	high-side driver supply input. Externally connected to the bootstrap capacitor
HB	15	reference for high-side driver and input for half-bridge slope detection. Externally connected to half-bridge node HB between HBC MOSFETs (see Figure 19)
n.c.	16	not connected; high-voltage spacer
SNSCURHBC	17	momentary HBC current sense input. Externally connected to the resonant current sense resistor
SGND	18	signal ground and IC reference (ground).
CFMIN	19	HBC minimum frequency setting. Externally connected to the capacitor
RFMAX	20	HBC maximum frequency setting. Externally connected to the resistor
SNSFB	21	output voltage regulation feedback sense input. Externally connected to opto-coupler
SSHBC/EN	22	• HBC soft-start timing input • IC enable input. Enables PFC only or both PFC and HBC controllers. Externally connected to soft-start capacitor and enable pull-down signal
RCPROT	23	protection timer setting for time-out and restart. Externally connected to resistor and capacitor
SNSBOOST	24	sense input for boost voltage regulation. Externally connected to resistive divided V_{boost}

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7. Functional description

7.1 Overview of IC modules

The functionality of the SSL4120 is grouped as follows:

- Supply module:

  Supply management for the IC. Includes the restart and (latched) shut-down states
- Protection and restart timer:

  An externally adjustable timer used for delayed protection and restart timing
- Enable input:

  Control input for enabling and disabling the controllers. When disabled has very low current consumption
- PFC controller:

  Controls and protects the power factor converter. Generates a 400 V (DC) boost voltage V_{boost} from the rectified AC mains input with a high PF
- HBC controller:

  Controls and protects the resonant converter. generates a regulated, mains isolated output voltage from the 400 V (DC) boost voltage V_{boost}

Figure 1 shows the block diagram of the SSL4120. A typical application is shown in Figure 19.

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7.2 Power supply

The SSL4120 contains several supply-related pins SUPIC, SUPREG, SUPHS and SUPHV. These pins are described in Section 7.2.1 to Section 7.2.4

7.2.1 Low-voltage supply input (SUPIC pin)

The SUPIC pin is the main low-voltage supply input to the IC. All internal circuits are supplied from this pin directly or indirectly using the SUPREG pin. The high-voltage circuit however, is not supplied from the SUPIC pin. The SUPIC pin is connected externally to a buffer capacitor C_{SUPIC}. This buffer capacitor can be charged in several ways:

- from the internal high voltage start-up source
- from the HBC transformer auxiliary winding
- from the switching half-bridge node capacitive supply
- from an external DC supply, for example, a standby supply

The IC starts operating when voltage on the SUPIC pin reaches the start level, provided the voltage on the SUPREG pin has also reached the start level. The start level depends on the condition of the SUPHV pin:

- High voltage present on the SUPHV pin ($V_{SUPHV} > V_{det(SUPHV)}$).

  In a stand-alone application this is the case because C_{SUPIC} is initially charged from the HV start-up source. The start level is $V_{start(hvd)(SUPIC)}$ = 22 V. The wide difference between the start and stop ($V_{uvp(SUPIC)}$) levels allows sufficient energy to be drawn from the SUPIC buffer capacitor until the output voltage stabilizes.
- Not connected or voltage not present on the SUPHV pin ($V_{SUPHV} < V_{det(SUPHV)}$).

  When the SSL4120 is supplied from an external DC source, this is the case. The start level is $V_{start(nohvd)(SUPIC)}$ = 17 V. The IC is supplied from the DC supply during start-up. To minimize power dissipation, the DC supply to the SUPIC pin must be higher than but close to $V_{uvp(SUPIC)}$ = 15 V.

The IC stops operating when $V_{SUPIC} < V_{uvp(SUPIC)}$. This voltage is the SUPIC pin UnderVoltage Protection (UVP) voltage (UVP-SUPIC; see Section 7.9). The PFC controller stops switching immediately but the HBC controller continues operating until the low-side MOSFET is active.

The current consumption depends on the state of the IC. The SSL4120 operating states are described in Section 7.3.

- Disabled IC state

  When the IC is disabled using the SSHBC/EN pin, the current consumption is very low ($I_{dism(SUPIC)}$).
- SUPIC charge, SUPREG charge, Thermal hold, Restart and Protection shut-down states

  Only a small section of the IC is active while C_{SUPIC} and C_{SUPREG} are charging during a restart sequence before start-up or during shut-down after a protection function has been activated. The PFC and HBC controllers are disabled. Current consumption is limited to $I_{protm(SUPIC)}$.

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- Boost charge state

  The PFC controller is switching; the HBC controller is off. The current from the high-voltage start-up source is large enough to supply the SUPIC pin (current consumption < $I_{ch(nom)(SUPIC)}$).

- Operational supply state

  Both the PFC and HBC controllers are switching. Current consumption is $I_{oper(SUPIC)}$. When the HBC controller is enabled, the switching frequency is initially high and the HBC MOSFET drivers current consumption is dominant. The stored energy in C_{SUPIC} supplies the initial SUPIC current before the SUPIC supply source takes over.

The SUPIC pin has a low short-circuit detection voltage ($V_{scp(SUPIC)}$ = 0.65 V). The current dissipated in the HV start-up source is limited while $V_{SUPIC} < V_{scp(SUPIC)}$ (see Section 7.2.4).

7.2.2 Regulated supply (SUPREG pin)

The voltage range on the SUPIC pin exceeds that of the external MOSFETs gate voltages. The SSL4120 contains an integrated series stabilizer for this reason. The series stabilizer creates an accurate regulated voltage ($V_{reg(SUPREG)}$ = 10.9 V) at the buffer capacitor C_{SUPREG}. This stabilized voltage is used to:

- supply the internal PFC driver

Remark: The internal SUPIC pin supply provides most of the external MOSFET charge current.

- supply the internal low-side HBC driver
- supply the internal high-side driver using external components
- as a reference voltage for optional external circuits

The SUPREG series stabilizer is enabled after C_{SUPIC} has been fully charged. Enabling the stabilizer after charging C_{SUPIC} ensures any optional external circuitry connected to SUPREG does not dissipate any of the start-up current.

To ensure that the external MOSFETs receive sufficient gate drive current, the voltage on the SUPREG pin must reach $V_{start(SUPREG)}$. In addition, the voltage on the SUPIC pin must reach the start level. The IC starts operating when both voltages reach their start levels.

SUPREG is provided with undervoltage protection (UVP-SUPREG; see Section 7.9). When $V_{SUPREG} < V_{uvp(SUPREG)}$ = 10.3 V, two events are triggered:

- The IC stops operating to prevent unreliable switching because the gate driver voltage is too low. The PFC controller stops switching immediately but the HBC controller continues until the low-side stroke is active.
- The maximum current from the internal SUPREG series stabilizer is reduced to $I_{ch(red)(SUPREG)}$ = 5.4 mA. This feature reduces the dissipation in the series stabilizer when an overload occurs at the SUPREG pin while the SUPIC pin is supplied from an external DC supply.

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7.2.3 High-side driver floating supply (SUPHS pin)

The high-side driver is supplied by an external bootstrap buffer capacitor, C_{SUPHS}. The bootstrap capacitor is connected between the high-side reference the HB pin and the high-side driver supply input the SUPHS pin. C_{SUPHS} is charged from the SUPREG pin using an external diode D_{SUPHS}.

Careful selection of the appropriate diode minimizes the voltage drop between SUPREG and SUPHS, especially when large MOSFETs and high switching frequencies are used.

7.2.4 High-voltage supply input (SUPHV pin)

In a stand-alone power supply application, the SUPHV pin is connected to V_{boost}. C_{SUPIC} and C_{SUPREG} are charged using the HV start-up source (which delivers a constant current from SUPHV to SUPIC) using this pin.

Short-circuit protection on the SUPIC pin (SCP-SUPIC; see Section 7.9) limits dissipation in the HV start-up source when SUPIC is shorted to ground. SCP-SUPIC limits the current on SUPHV to $I_{red(SUPHV)}$ when the voltage on SUPIC is less than $V_{scp(SUPIC)}$.

Under normal operating conditions, the SUPIC pin voltage exceeds $V_{scp(SUPIC)}$ very quickly after start-up and the HV start-up source switches to $I_{nom(SUPHV)}$.

During start-up and restart, the HV start-up source charges C_{SUPIC} and regulates the voltage on SUPIC using hysteretic control. The start level has a small amount of hysteresis $V_{start(hys)(SUPIC)}$. The HV start-up source switches-off when V_{SUPIC} exceeds the start level $V_{start(hvd)(SUPIC)}$. Current consumption through the SUPHV pin is low ($I_{tko(SUPHV)}$).

Once start-up is complete and the HBC controller is operating, SUPIC is supplied from the HBC transformer auxiliary winding. In operational state, the HV start-up source is disabled.

7.3 Flow diagram

The operation of the SSL4120 can be divided into a number of states (see Figure 3). The abbreviations used in Figure 3 are explained in Table 8.

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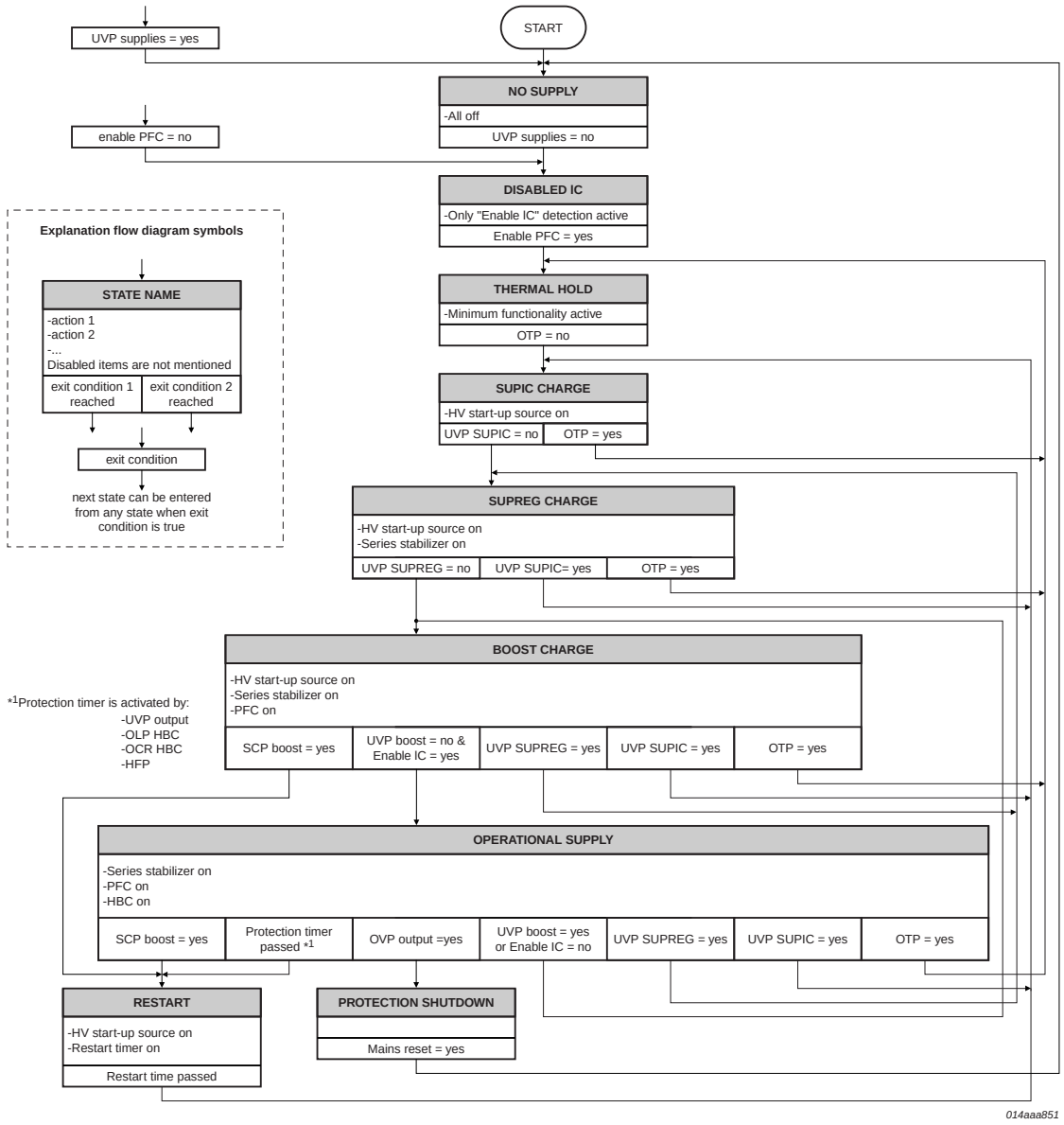


Fig 3. SSL4120 flow diagram

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Table 3. Operating states

State	Description
No supply	Supply voltages on the SUPIC and SUPHV pins are too low to provide any functionality. Undervoltage protection (UVP supplies; see Section 7.9) is active when $V_{SUPHV} < V_{rst(SUPHV)}$ and $V_{SUPIC} < V_{rst(SUPIC)}$. The IC is reset.
Disabled IC	The IC is disabled because the SSHBC/EN pin is LOW.
Thermal hold	Activated when OTP is active. The IC is not operating. The PFC and HBC controllers are disabled and C_{SUPIC} and C_{SUPREG} are not charged.
SUPIC charge	The HV start-up source charges the IC supply capacitor (C_{SUPIC}). C_{SUPREG} is not charged.
SUPREG charge	The series regulator charges the stabilized supply capacitor (C_{SUPREG}).
Boost charge	The operational PFC builds up V_{boost}.
Operational supply	The output voltage is generated. Both the PFC and HBC controllers are fully operational.
Restart	Activated when a protection function is triggered. The restart timer is activated. During this time, both the PFC/HBC controllers are disabled and C_{SUPREG} is not charged. C_{SUPIC} is charged.
Protection shut-down	Activated when a protection function is triggered. The IC is not operational. The PFC and HBC controllers are disabled and C_{SUPIC}/C_{SUPREG} are not charged.

7.4 Enable input (SSHBC/EN pin)

The power supply application is disabled by pulling the SSHBC/EN pin LOW.

Figure 4 shows the internal functionality. When a voltage is present on the SUPHV pin or on the SUPIC pin, a current $I_{pu(EN)}$ = 42 µA flows from the SSHBC/EN pin. If the pin is not pulled down, the current increases the voltage up to $V_{pu(EN)}$ = 3 V. Since the voltage is above both $V_{en(PFC)(EN)}$ = 1.2 V and $V_{en(IC)(EN)}$ = 2.2 V, the IC is enabled.

The IC is disabled when the SSHBC/EN pin voltage is pulled down under $V_{en(PFC)(EN)}$ and $V_{en(IC)(EN)}$ via an optocoupler driven from the HBC transformer secondary side (see Figure 4). The PFC controller stops switching immediately but the HBC controller continues switching until the low-side stroke is active. It is also possible to control the voltage on the SSHBC/EN pin from another circuit on the secondary side via a diode. The external pull-down current must be larger than the internal soft-start charge current $I_{ss(hf)(SSHBC)}$.

If the voltage on SSHBC/EN is pulled under $V_{en(IC)(EN)}$, but not under $V_{en(PFC)(EN)}$, only the HBC is disabled. This feature is useful when another power converter is connected to the PFC V_{boost}.

The low-side power switch of the HBC is on when the HBC is disabled using the SSHBC/EN pin.

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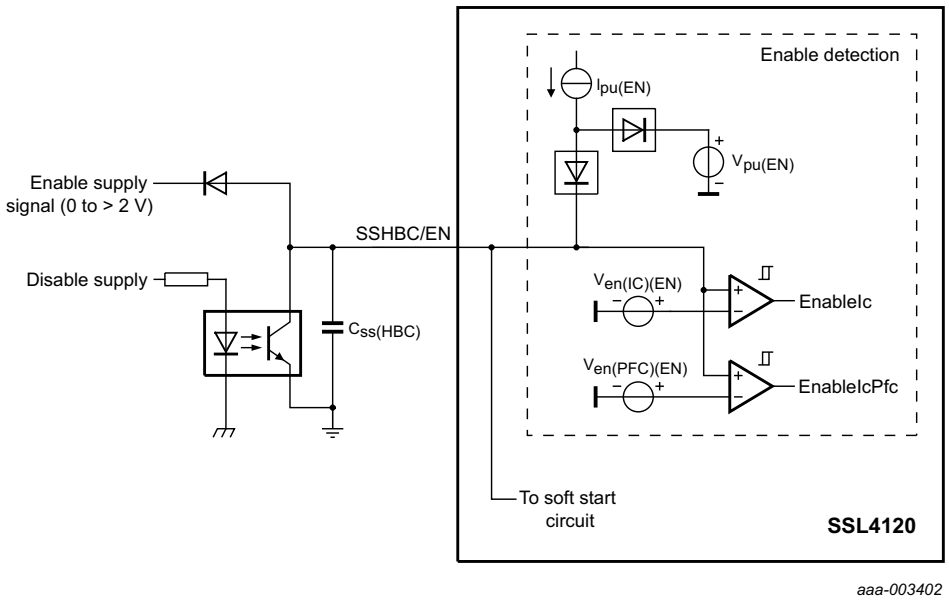


Fig 4. Circuit configuration around the SSHBC/EN pin

7.5 IC protection

7.5.1 IC restart and shut-down

In addition to the protection functions influencing the PFC and HBC controller operation, several protection functions are provided to disable both controllers. See the protection overview in Section 7.9 for details on which protection functions trigger a restart or protection shut-down.

- Restart

  When the SSL4120 enters the Restart state, the PFC and HBC controllers are switched off. After a period defined by the restart timer, the IC automatically restarts following the normal start-up cycle.

- Protection shut-down

  When the SSL4120 enters the Protection shut-down state, the PFC and HBC controllers are switched off. The Protection shut-down state is latched, the IC does not automatically start up again. It can be restarted by resetting the Protection shut-down state in one of the following ways:

  – lower V_{SUPIC} and V_{SUPHV} below their respective reset levels, $V_{rst(SUPIC)}$ and $V_{rst(SUPHV)}$
  – using a fast shut-down reset (see Section 7.5.3).
  – using the enable pin (see Section 7.4)

- Thermal hold

  In the Thermal hold state, the PFC and HBC controllers are switched off. The Thermal hold state remains active until the IC junction temperature drops to approximately 10 °C below T_{otp} (see Section 7.5.6).

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7.5.2 Protection and restart timer

The SSL4120 contains a programmable timer which can be used for timing several protection functions. The timer can be used in two ways: as a protection timer and as a restart timer. The timing of the timers is set independently using the external resistor R_{prot} and capacitor C_{prot} connected to the RCPROT pin.

7.5.2.1 Protection timer

Certain error conditions are allowed to persist for a time period before protective action must be taken. The protection timer defines the protection period (how long the error can persist before the protection function is triggered). The protection functions that use the protection timer are found in the protection overview in Section 7.9.

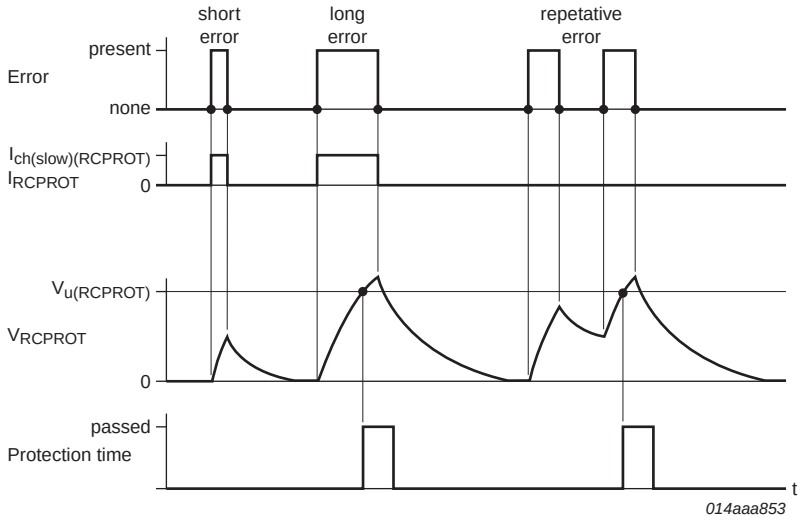


Fig 5. Operation of the protection timer

Figure 5 shows the operation of the protection timer. When an error condition occurs, a fixed current $I_{ch(slow)(RCPROT)}$ = 100 µA flows from the RCPROT pin and charges C_{prot}. R_{prot} causes the voltage to increase exponentially. The protection time elapses when the RCPROT voltage reaches the upper switching level. When the protection time has elapsed, the appropriate protective action is taken and C_{prot} is discharged.

If the error condition is removed before the voltage on the RCPROT pin reaches $V_{u(RCPROT)}$, C_{prot} is discharged using R_{prot} and no action is taken.

The RCPROT voltage can be forced > $V_{u(RCPROT)}$ by an external circuit to trigger a restart.

7.5.2.2 Restart timer

The IC must be disabled for a time period on certain error conditions. Particularly when the error condition can cause components to overheat. In such cases, the IC is disabled to allow the power supply to cool down. It automatically restarts. The restart timer determines the restart time. The restart timer is active in the Restart state. The protection functions which trigger a restart are found in the protection functions overview in Section 7.9.

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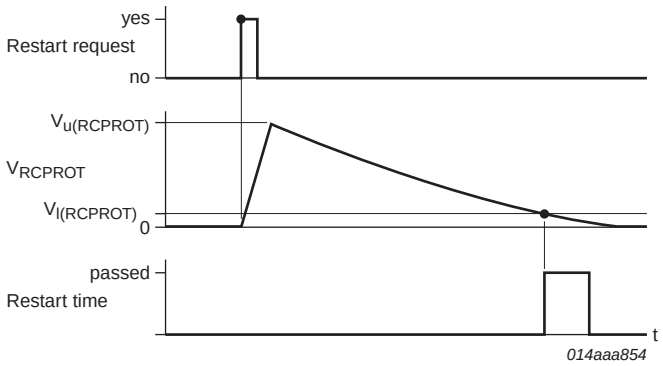


Fig 6. Operation of the restart timer

Figure 6 shows the operation of the restart timer. Normally C_{prot} is discharged to 0 V. When a restart is requested, C_{prot} is quickly charged to the upper switching level $V_{u(RCPROT)}$. Then the RCPROT pin becomes high ohmic and C_{prot} discharges through R_{prot}. The restart time has elapsed when V_{RCPROT} reaches the lower switching level $V_{l(RCPROT)}$ = 0.5 V. The IC restarts and C_{prot} is discharged.

7.5.3 Fast shut-down reset (SNSMAINS pin)

The latched Protection shut-down state is reset when V_{SUPIC} and V_{SUPHV} drop below their respective reset levels, $V_{rst(SUPIC)}$ and $V_{rst(SUPHV)}$. Typically, the PFC boost capacitor C_{boost}, must discharge before V_{SUPIC} and V_{SUPHV} drop below their reset levels. Discharging C_{boost} can take a long time.

Fast shut-down reset causes a faster reset. When the mains supply is interrupted, the voltage on the SNSMAINS pin falls. When $V_{SNSMAINS}$ falls below $V_{rst(SNSMAINS)}$ and then increases again by a hysteresis value, the IC leaves the Protection shut-down state. The boost capacitor C_{boost} does not require discharging to trigger a new start-up.

The Protection shutdown state is also exited by pulling down the enable input (the SSHBC/EN pin).

7.5.4 Output overvoltage protection (SNSOUT pin)

The SSL4120 outputs are provided with overvoltage protection (OVP output; see Section 7.9). The output voltage is measured using the resonant transformer auxiliary winding. The voltage is sensed on the SNSOUT pin using an external rectifier and resistive divider. An overvoltage is detected when the SNSOUT voltage exceeds $V_{ovp(SNSOUT)}$. When an overvoltage is detected, the SSL4120 enters the Protection shut-down state.

Additional external protection circuits, such as an external OTP circuit, can be connected to this pin. Connect them to the SNSOUT pin using a diode to ensure that an error condition triggers an OVP event.

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7.5.5 Output undervoltage protection (SNSOUT pin)

If an error condition causes an output voltage drop when the SSL4120 is supplied from the HBC transformer auxiliary winding, a SUPIC UVP event is automatically triggered.

If an error condition causes a decrease in the output voltage when the IC is supplied from a separate DC source (for example, a standby supply), the IC does not automatically stop switching. To counter this, the IC outputs are provided with undervoltage protection (UVP output; see Section 7.9).

If $V_{SNSOUT} < V_{uvp(SNSOUT)} = 2.3$ V, a UVP output event restarts the IC.

During start-up, the output voltage is less than $V_{uvp(SNSOUT)}$ for a time. This voltage drop is not considered as an error condition if it does not last longer than expected. The protection timer is started when $V_{SNSOUT} < V_{uvp(SNSOUT)}$ for this reason. The Restart state is activated if the UVP output event is still active when the protection time has expired.

7.5.6 OverTemperature Protection (OTP)

Accurate internal overtemperature protection is provided in the SSL4120. When the junction temperature exceeds the overtemperature protection activation temperature, $T_{otp} = 150$ °C), the IC enters the Thermal hold state. The SSL4120 exits the Thermal hold state when the temperature falls again to approximately $T_{otp} - 10$ °C.

7.6 Burst mode operation (SNSOUT pin)

The HBC and PFC controllers can be operated in burst mode. In burst mode, the controllers are on for a period, then off for a period. Burst mode operation increases efficiency under low-load conditions.

A low-load condition can be detected using a simple external circuit that uses the information from the feedback loop or from the average primary current. The detection circuit can pull down the SNSOUT pin to pause the SSL4120 operation for a burst-off time. Only the HBC controller or both controllers can be paused during the burst-off time:

- Burst-off level for HBC, $V_{burst(HBC)} = 1$ V

  When $V_{SNSOUT} < V_{burst(HBC)}$, the HBC controller is suspended. Both the high-side and the low-side power switches are off. The PFC continues to operate normally. When $V_{SNSOUT} > V_{burst(HBC)}$ again, the HBC controller resumes normal operation, without executing a soft-start sequence.
- Burst-off level for PFC, $V_{burst(PFC)} = 0.4$ V

  When $V_{SNSOUT} < V_{burst(PFC)}$, operation of the PFC controller is also suspended (the HBC is already paused). When $V_{SNSOUT} > V_{burst(PFC)}$ again, the PFC controller resumes normal operation using a PFC soft-start (see Section 7.7.6).

To ensure that burst mode is not activated before the output voltage becomes valid, current from the SNSOUT pin (100 μA) holds V_{SNSOUT} at $V_{pu(SNSOUT)}$. This level is above both burst levels. The resistance between the SNSOUT pin and ground must be > 20 kΩ.

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7.7 PFC controller

The PFC controller converts the rectified universal mains voltage into an accurately regulated V_{boost} of 400 V (DC) or 450 V (DC). It operates in Quasi-Resonant (QR) or Discontinuous Conduction Mode (DCM) and is controlled using an on-time control system. The resulting mains harmonic current emissions of a typical application can meet the Class-C MHR requirements for lighting applications.

The PFC controller uses valley switching to minimize losses. A primary stroke is only started once the previous secondary stroke ends and the voltage across the PFC MOSFET reaches a minimum value.

7.7.1 PFC gate driver (GATEPFC pin)

The circuit driving the gate of the power MOSFET has a high current sourcing capability $I_{source(GATEPFC)}$ of 500 mA. It also has a high current sink capability $I_{sink(GATEPFC)}$ of 1.2 A. The source and sink capabilities enable fast power MOSFET switch-on and switch-off to ensure efficient operation. The driver is supplied from the regulated SUPREG supply.

7.7.2 PFC on-time control

The PFC operates under on-time control. The following determine the PFC MOSFET on-time:

- the error amplifier and the loop compensation using the COMPPFC pin voltage
  - At $V_{ton(COMPPFC)zero}$ = 3.5 V, the on-time is reduced to zero.
  - At $V_{ton(COMPPFC)max}$ = 1.25 V, the on-time is at a maximum
- Mains compensation using the SNSMAINS pin voltage

The on-time must be modulated with the mains voltage to reach the Class-C MHR requirements. In the application, this is achieved when a modulation current is injected into the COMPPFC network using a capacitor which connects to the mains voltage, see Figure 19.

7.7.2.1 PFC error amplifier (COMPPFC and SNSBOOST pins)

V_{boost} is divided using a high-ohmic resistive divider. It is supplied to the SNSBOOST pin. The transconductance error amplifier, which compares the SNSBOOST voltage with an accurate trimmed reference voltage $V_{reg(SNSBOOST)}$, is connected to this pin. The external loop compensation network on the COMPPFC pin filters the output current. In a typical application, a resistor and two capacitors set the regulation loop bandwidth.

The COMPPFC voltage is clamped at a maximum of $V_{clamp(COMPPFC)}$. This clamp avoids a long recovery time if V_{boost} rises above the regulation level for a period.

7.7.2.2 PFC mains compensation (SNSMAINS pin)

The mathematical equation for the transfer function of a power factor corrector contains the square of the mains input voltage. In a typical application, this results in a low bandwidth for low mains input voltages. At high mains input voltages, the MHR requirements are hard to meet.

The SSL4120 contains a correction circuit to compensate for this effect. The average mains voltage is measured using the SNSMAINS pin and this information is supplied to an internal compensation circuit.

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Figure 7 illustrates the relationship between $V_{SNSMAINS}$, $V_{COMPPFC}$ and the on-time. The compensation makes it is possible to keep the regulation loop bandwidth constant over the full mains input range. This feature provides a fast transient response on load steps, while still meeting the Class-C MHR requirements.

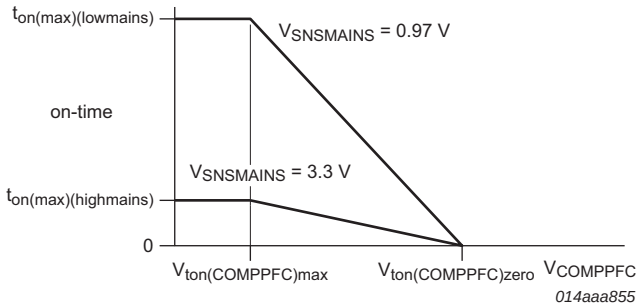


Fig 7. Relationship between on-time, SNSMAINS voltage and COMPPFC voltage

7.7.3 PFC demagnetization sensing (SNSAUXPFC pin)

The voltage on the SNSAUXPFC pin is used to detect transformer demagnetization. During the secondary stroke, the transformer is magnetized and current flows in the boost output. During this time, $V_{SNSAUXPFC} < V_{demag(SNSAUXPFC)} = -100$ mV and the PFC MOSFET remains switched off.

When the transformer becomes demagnetized, the current stops flowing to the boost output $V_{SNSAUXPFC} > V_{demag(SNSAUXPFC)}$ and valley detection is started. The MOSFET remains switched off.

To ensure that switching continues under all circumstances, the MOSFET is forced to switch on if the magnetizing of the transformer ($V_{SNSAUXPFC} < V_{demag(SNSAUXPFC)}$) is not detected within $t_{to(mag)} = 50$ μs after the GATEPFC pin goes LOW.

Connect a 5 kΩ series resistor to this pin to protect the internal circuitry, against lightning for example. Place the resistor close to the IC on the PCB to prevent incorrect switching due to external disturbances.

7.7.4 PFC valley sensing (SNSAUXPFC pin)

If the voltage at the MOSFET drain is at its minimum (valley switching), the PFC MOSFET is switched on for the next stroke. This action reduces switching losses and EMI (see Figure 8).

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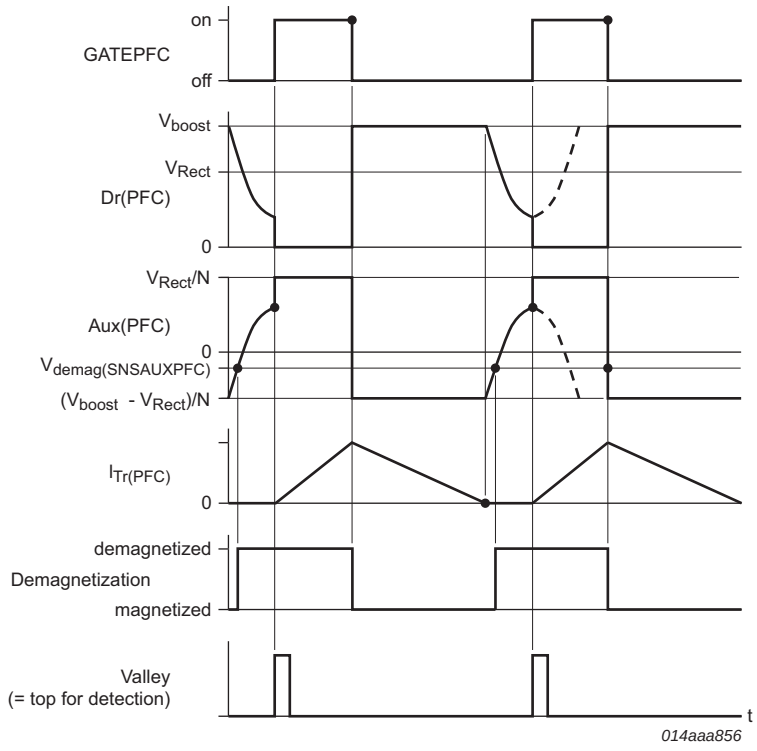


Fig 8. Demagnetization and valley detection

The valley sensing block connected to the SNSAUXPFC pin detects the valleys. This block measures the PFC transformer auxiliary winding voltage which is a reduced and inverted copy of the MOSFET drain voltage. When a valley of the drain voltage (= top at SNSAUXPFC voltage) is detected, the MOSFET is switched on.

If a top is not detected on the SNSAUXPFC pin (a valley at the drain) within $t_{to(vrec)}$ = 4 µs after demagnetization is detected, the MOSFET is forced to switch on.

7.7.5 PFC frequency and off-time limiting

The switching frequency is limited to $f_{max(PFC)}$ for transformer optimization and to minimize switching losses. If the frequency for quasi-resonant operation > $f_{max(PFC)}$, the system switches to DCM. The PFC MOSFET is switched on when the drain-source voltage is at a minimum (valley switching).

The minimum off-time is limited at $t_{off(PFC)min}$ to ensure correct control of the PFC MOSFET under all circumstances.

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7.7.6 PFC soft-start and soft-stop (SNSCURPFC pin)

The PFC controller features a soft-start function. The function slowly increases the primary peak current during start-up. The soft-stop function slowly decreases the transformer peak current before operations are stopped. These functions prevent transformer rattle during start-up and burst mode operation.

Connecting a resistor $R_{ss(PFC)}$ and capacitor $C_{ss(PFC)}$ between the SNSCURPFC pin and the current sense resistor $R_{cur(PFC)}$ achieves this. During start-up, an internal current source $I_{ch(ss)(PFC)}$ charges the capacitor to $V_{SNSCURPFC} = I_{ch(ss)(PFC)} \times R_{ss(PFC)}$.

The voltage is limited to the maximum PFC soft-start clamp voltage, $V_{clamp(ss)PFC}$. The additional voltage across the charged capacitor reduces the peak current. After start-up, the internal current source is switched-off, capacitor $C_{ss(PFC)}$ discharges across $R_{ss(PFC)}$ and the peak current increases.

The start level and the time constant of the rising primary current can be adjusted externally by changing the values of $R_{ss(PFC)}$ and $C_{ss(PFC)}$.

$$I_{Cur(PFC)(pk)} = \frac{V_{ocr(PFC)} - (I_{ch(ss)(PFC)} \times R_{ss(PFC)})}{R_{cur(PFC)}}$$

$$\tau = R_{ss(PFC)} \times C_{ss(PFC)}$$

Switching on the internal current source $I_{ch(ss)(PFC)}$ starts a soft-stop. $I_{ch(ss)(PFC)}$ charges $C_{ss(PFC)}$. The increasing capacitor voltage decreases the peak current. The charge current flows when the voltage on the SNSCURPFC pin is less than the maximum PFC soft-start voltage = 0.5 V. If $V_{SNSCURPFC}$ exceeds the maximum PFC soft-start voltage, the soft-start current source starts limiting the charge current. To determine accurately if the capacitor is charged, the voltage is only measured during the PFC power switch off-time. The PFC is stopped when $V_{SNSCURPFC} > V_{stop(ss)(PFC)}$.

7.7.7 PFC overcurrent regulation, OCR-PFC (SNSCURPFC pin)

The maximum peak current is limited cycle-by-cycle by sensing the voltage across an external sense resistor ($R_{cur(PFC)}$) connected to the source of the external MOSFET. The voltage is measured via the SNSCURPFC pin and is limited to $V_{ocr(PFC)}$.

A voltage peak appears on $V_{SNSCURPFC}$ when the PFC MOSFET is switched on due to the discharging of the drain capacitance. The leading-edge blanking time $t_{leb(PFC)}$ ensures that the overcurrent sensing block does not react to this transitory peak.

7.7.8 PFC mains undervoltage protection/brownout protection, UVP mains (SNSMAINS pin)

The voltage on the SNSMAINS pin is continuously sensed to prevent the PFC trying to operate at very low mains input voltages. PFC switching stops when $V_{SNSMAINS} < V_{uvp(SNSMAINS)}$. Mains undervoltage protection is also called brownout protection.

$V_{SNSMAINS}$ is clamped to a minimum value of $V_{pu(SNSMAINS)}$ for fast restart as soon as the mains input voltage recovers after a mains dropout. The PFC starts or restarts once $V_{SNSMAINS}$ exceeds the $V_{start(SNSMAINS)}$ start level.

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7.7.9 PFC boost overvoltage protection, OVP boost (SNSBOOST pin)

An overvoltage protection circuit has been built in to prevent boost overvoltage during load steps and mains transients. Switching of the power factor correction circuit is inhibited when the voltage on the SNSBOOST pin > $V_{ovp(SNSBOOST)}$.

PFC switching resumes when $V_{SNSBOOST} < V_{ovp(SNSBOOST)}$ again.

Overvoltage protection is also triggered when an open circuit occurs at the resistor connected between the SNSBOOST pin and ground.

7.7.10 PFC short circuit/open-loop protection, SCP/OLP-PFC (SNSBOOST pin)

The PFC circuit does not start switching until the voltage on the SNSBOOST pin > $V_{scp(SNSBOOST)}$. This acts as short-circuit protection for the V_{boost} (SCP boost).

The SNSBOOST pin draws a small input current $I_{prot(SNSBOOST)}$. If this pin gets disconnected, the residual current pulls down $V_{SNSBOOST}$ which triggers the short-circuit protection (SCP boost). This combination creates an open-loop protection (OLP-PFC).

7.8 HBC controller

The HBC controller converts the V_{boost} 400 V from the PFC into one or more regulated DC output voltages and drives two external MOSFETs in a half-bridge configuration connected to a transformer. The transformer forms the resonant circuit in combination with the resonant capacitor and the load at the output. The transformer has a leakage inductance and a magnetizing inductance. The regulation is realized using frequency control.

7.8.1 HBC high-side and low-side driver (GATEHS and GATELS pins)

Both drivers have an identical driving capability. The output of each driver is connected to the equivalent gate of an external high-voltage power MOSFET.

The low-side driver is referenced to the PGND pin and is supplied from the SUPREG pin.

The high-side driver is floating. The reference for the high-side driver is the HB pin, connected to the midpoint of the external half-bridge. The high-side driver is supplied from the SUPHS pin which is connected to the external bootstrap capacitor C_{SUPHS}. When the low-side MOSFET is on, the bootstrap capacitor is charged from the SUPREG pin using the external diode D_{SUPHS}.

7.8.2 HBC boost undervoltage protection, UVP boost (SNSBOOST pin)

The SNSBOOST pin voltage is sensed continuously to prevent the HBC controller trying to operate at very low boost input voltages. When $V_{SNSBOOST} < V_{uvp(SNSBOOST)}$ HBC switching stops the next time the GATELS pin goes HIGH. HBC switching resumes when $V_{SNSBOOST} > V_{start(SNSBOOST)}$.

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7.8.3 HBC switch control

HBC switch control determines when the MOSFETs switch on and off. It uses the output from several other blocks.

- A divider is used to alternate switching of the high and low-side MOSFETs for each oscillator cycle. The oscillator frequency is twice the half-bridge frequency.
- The controlled oscillator determines the switch-off point.
- Adaptive non-overlap time sensing determines the switch-on point. This function is the adaptive non-overlap time.
- Several protection circuits and the state of the SSHBC/EN input pin specify if the resonant converter is allowed to start switching.

Figure 9 provides an overview of typical switching behavior.

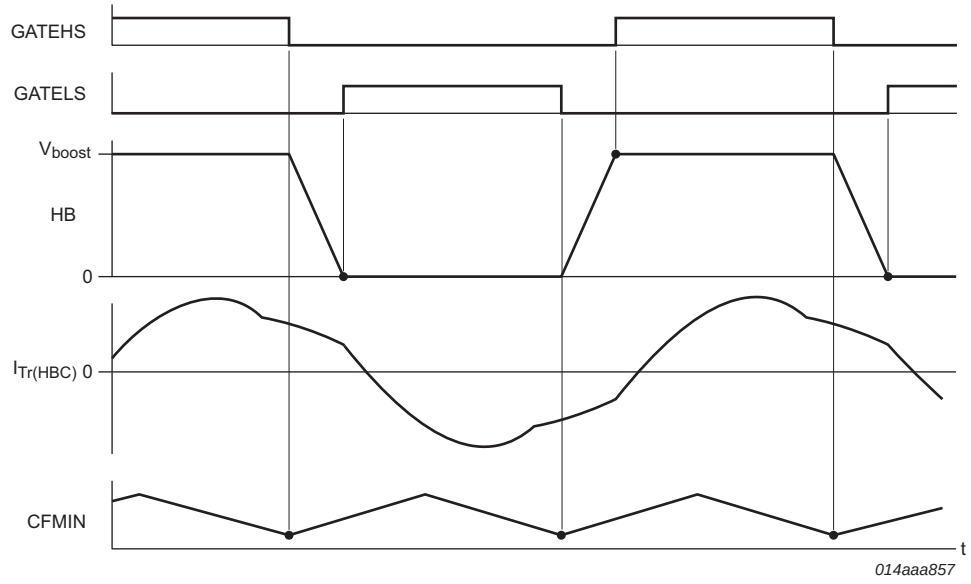


Fig 9. Switching behavior of the HBC

7.8.4 HBC Adaptive Non-Overlap (ANO) time function (HB pin)

7.8.4.1 Inductive mode (normal operation)

The high efficiency characteristic of a resonant converter is the result of Zero-Voltage Switching (ZVS) of the power MOSFETs. ZVS is also called soft switching. To allow soft switching, a small non-overlap time is required between the high-side on-times and low-side MOSFETs. During this non-overlap time, the primary resonant current charges or discharges the half-bridge capacitance between ground and V_{boost}.

After the charge or discharge cycles, the MOSFET body diode starts conducting and because the voltage across the MOSFET is zero, when the MOSFET is switched on there are no switching losses. This operating mode is called inductive mode. In inductive mode, the switching frequency is above the resonance frequency and the resonant tank has an inductive impedance.

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The HB transition time depends on the resonant current amplitude when switching starts. There is a complex relationship between this amplitude, the frequency, V_{boost} and the output voltage. Ideally, the IC switches on the MOSFET when the HB transition is complete. If it waits any longer, V_{HB} can swing back, especially at high output loads. The advanced adaptive non-overlap time function controls the timing. The adaptive non-overlap time function makes it unnecessary to choose a fixed dead time (which is always a compromise). This saves on external components.

Adaptive non-overlap time sensing measures the HB slope after one MOSFET has been switched off. Normally, the HB slope starts immediately (the voltage starts rising or falling). Once the transition at the HB node is complete, the slope ends (the voltage stops rising/falling). This slope end is detected by the ANO time sensor and the other MOSFET is switched on. In this way, the non-overlap time is automatically optimized even when the HB transition cannot be completed which minimizes switching losses.

Figure 10 illustrates the adaptive non-overlap time function operation of the inductive mode.

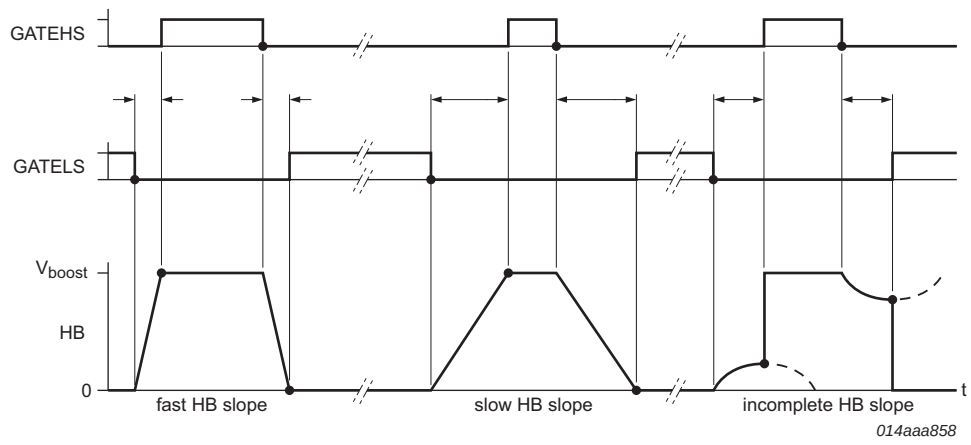


Fig 10. Adaptive non-overlap time function (normal inductive operation)

The non-overlap time depends on the HB slope but it has upper and lower limits.

An integrated minimum non-overlap time, $t_{no(min)}$ prevents cross conduction occurring under any circumstances.

The maximum non-overlap time is limited to the oscillator charge time. If the HB slope is longer than the oscillator charge time (¼ of HB switching period), the MOSFET is forced to switch on. In this case, the MOSFET is not soft switching. This limitation ensures the MOSFET on-time is at least ¼ of the HB switching period at very high switching frequencies.

7.8.4.2 Capacitive mode

Section 7.8.4.1 is true for normal operation with a switching frequency higher than the resonance frequency. When an error condition occurs (for example; output short, load pulse too high) the switching frequency is lower than the resonance frequency. The resonant tank then has a capacitive impedance. In capacitive mode, the HB slope does not start after the MOSFET switches off. Switching on the other MOSFET is not recommended in this situation. The absence of soft switching increases dissipation in the

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MOSFETs. In capacitive mode, the body diode in the switched off MOSFET can start conducting. Switching on the other MOSFET at this instant can result in the immediate destruction of the MOSFETs.

The advanced adaptive non-overlap time of the SSL4120 always waits until the slope at the half-bridge node starts. It guarantees safe switching of the MOSFETs in all circumstances. Figure 11 shows the adaptive non-overlap time function operation in capacitive mode.

In capacitive mode, half the resonance period can elapse before the resonant current changes back to the correct polarity and starts charging the half-bridge node. The oscillator is slowed down until the half-bridge slope starts to allow this relatively long waiting time. See Section 7.8.5 for more details on the oscillator.

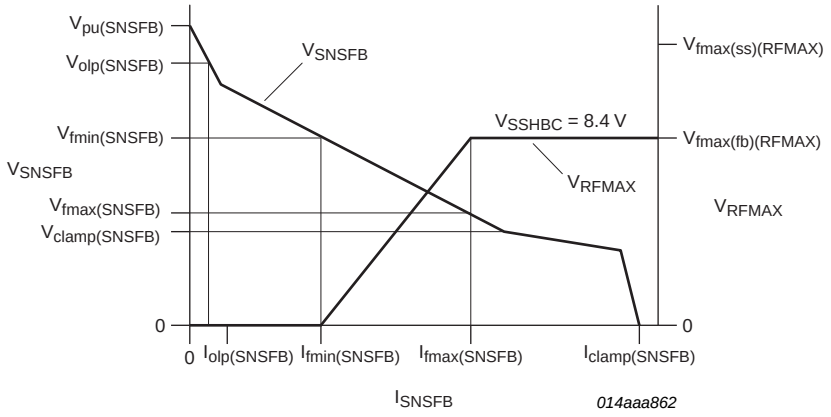


Fig 11. Adaptive non-overlap time function (capacitive operation)

The MOSFET is forced to switch on when the half-bridge slope fails to start and the oscillator voltage reaches $V_{u(CFMIN)}$.

The switching frequency is increased to eliminate the problems associated with capacitive mode operation (see Section 7.8.11).

7.8.5 HBC slope controlled oscillator (CFMIN and RFMAX pins)

The slope-controlled oscillator determines the half-bridge switching frequency. The oscillator generates a triangular waveform between $V_{u(CFMIN)}$ and $V_{l(CFMIN)}$ at the external capacitor C_{fmin}.

Figure 12 shows how the frequency is determined.

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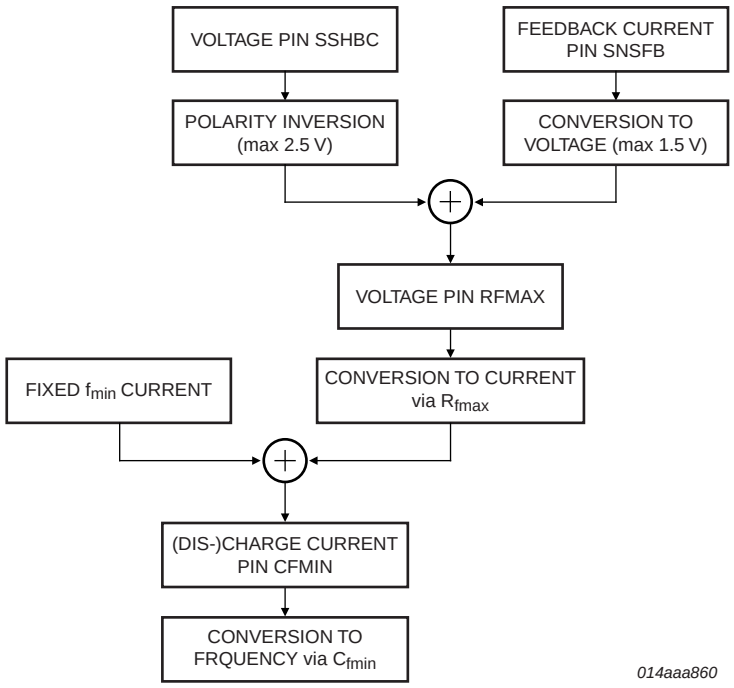


Fig 12. Determination of frequency

Two external components determine the frequency range:

- Capacitor C_{fmin} connected between the CFMIN pin and ground sets the minimum frequency in combination with an internally trimmed current source $I_{osc(min)}$.
- Resistor R_{fmax} connected between the RFMAX pin and ground sets the frequency range and thus the maximum frequency.

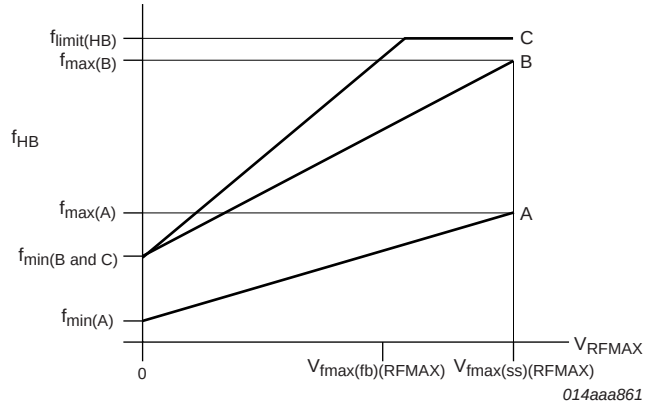
The oscillator frequency depends on the charge and discharge currents of C_{fmin}. The charge and discharge current contains a fixed component, $I_{osc(min)}$, which determines the minimum frequency. In addition, a variable component that is 4.9 times greater than the current in the RFMAX pin. The value of R_{fmax} and the RFMAX voltage pin determine I_{RFMAX}:

- The voltage on the RFMAX pin is $V_{fmin(RFMAX)}$ = 0 V at the minimum frequency.
- The voltage on the RFMAX pin is $V_{fmax(fb)(RFMAX)}$ = 1.5 V at the maximum feedback frequency.
- The voltage on the RFMAX pin is $V_{fmax(ss)(RFMAX)}$ = 2.5 V at the maximum soft-start frequency.

The maximum frequency of the oscillator is internally limited. The HB frequency is limited to $f_{limit(HB)}$ (minimum. 500 kHz). Figure 13 shows the relationship between V_{RFMAX}, R_{fmax}, C_{fmin} and f_{HB}.

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A: C_{fmin} = high, R_{fmax} = high.

B: C_{fmin} = low, R_{fmax} = low.

C: C_{fmin} = low, R_{fmax} = too low.

Fig 13. Function of R_{fmax} and C_{fmin}

The half-bridge slope controls the oscillator. The oscillator charge current is initially set to a low value $I_{osc(red)}$ = 30 μA. When the start of the half-bridge slope is detected, the charge current is increased to its normal value. This feature is used in combination with the adaptive non-overlap time function as described in Section 7.8.4.2 and Figure 11.

The length of time the oscillator current is low is negligible under normal operating conditions because the half-bridge slope normally starts directly after the MOSFET is switched off.

7.8.6 HBC feedback input (SNSFB pin)

In a typical power supply application, the output voltage is compared and amplified on the secondary side. The error amplifier output is transferred to the primary side using an optocoupler. This optocoupler can be connected directly to the SNSFB pin.

The SNSFB pin supplies the optocoupler from an internal voltage source $V_{pu(SNSFB)}$ = 8.4 V with the $R_{O(SNSFB)}$ series resistance. The series resistance allows spike filtering using an external capacitor. To ensure sufficient optocoupler bias current, the feedback input has a threshold current $I_{fmin(SNSFB)}$ = 0.66 mA at which the frequency is at a minimum.

The maximum frequency is reached at $I_{fmax(SNSFB)}$ = 2.2 mA. The maximum frequency that can be reached using the SNSFB pin is lower (60 %) than the maximum frequency that can be reached using the SSHBC/EN pin. Figure 14 shows the relationship between I_{SNSFB}, V_{SNSFB} and V_{RFMAX}.

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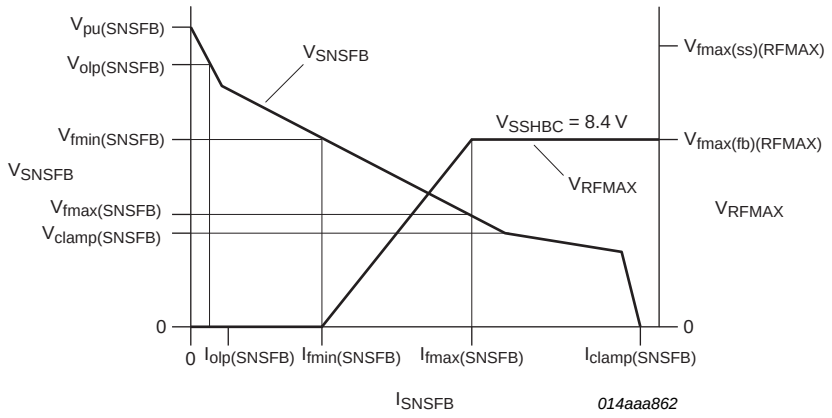


Fig 14. Transfer function of feedback input

Below the minimum frequency level, V_{SNSFB} is clamped at $V_{clamp(SNSFB)}$ = 3.2 V. This clamp enables a fast recovery of the output voltage regulation loop after an overshoot of the output voltage. The maximum current the clamp can deliver is $I_{clamp(SNSFB)}$ = 7.3 mA.

7.8.7 HBC open-loop protection, OLP-HBC (SNSFB pin)

Under normal operating conditions, the optocoupler current is between $I_{fmin(SNSFB)}$ and $I_{fmax(SNSFB)}$ and pulls down the voltage at the SNSFB pin. Due to an error in the feedback loop, the current could be less than $I_{fmin(SNSFB)}$ with the HBC controller delivering maximum output power.

The HBC controller features open-loop protection (OLP-HBC) which monitors the SNSFB pin voltage. When $V_{SNSFB} > V_{olp(SNSFB)}$, the protection timer is started. The Restart state is activated if the OLP condition is still present after the protection time has elapsed.

7.8.8 HBC soft start (SSHBC/EN pin)

The relationship between switching frequency and output current is not constant. It depends strongly on the output voltage V_O and V_{boost}. This relationship can be complex. The SSL4120 contains a soft-start function to ensure that the resonant converter starts or restarts with safe currents. This soft-start function forces a start at such a high frequency that the currents are acceptable under all conditions. The soft-start then slowly decreases the frequency. Normally, output voltage regulation takes over frequency control before soft-start reaches its minimum frequency. Limiting the output current during start-up also limits the rate at which the output voltage rises and prevents an overshoot.

Soft-start utilizes the SSHBC/EN pin voltage. The external capacitor $C_{ss(HBC)}$ sets the timing of the soft-start. The SSHBC/EN pin is also used as an enable input. Soft-start voltage levels are above the enable voltage thresholds.

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7.8.8.1 Soft-start voltage levels

The relationship between the soft-start voltage at the SSHBC/EN pin and the RFMAX pin voltage is shown in Figure 15. The relationship is directly related to the frequency.

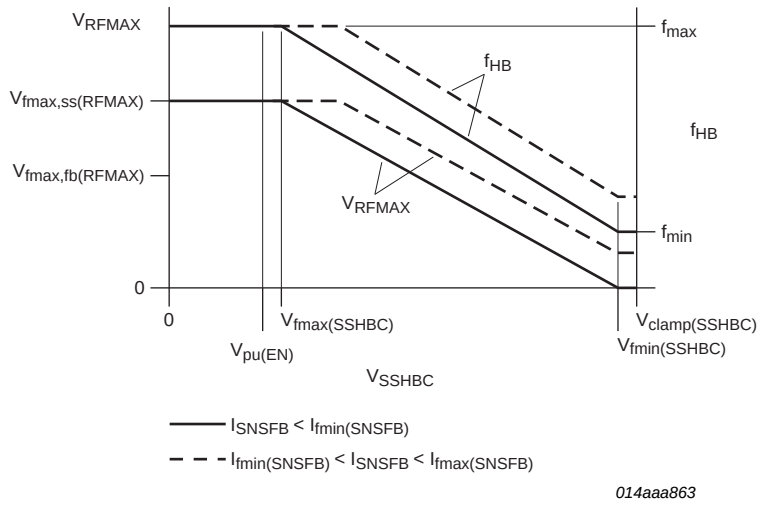


Fig 15. Relation between SSHBC/EN voltage and frequency

V_{RFMAX} and $V_{SSHBC/EN}$ are of opposite polarity. $V_{SSHBC/EN} < V_{fmax(SSHBC)}$ = 3.2 V at initial start-up which corresponds to the maximum frequency. During start-up, $C_{ss(HBC)}$ is charged, $V_{SSHBC/EN}$ increases and the frequency decreases. The contribution of the soft-start function is zero when $V_{SSHBC/EN} = V_{fmin(SSHBC)}$ = 7.9 V.

$V_{SSHBC/EN}$ is clamped at a maximum of $V_{clamp(SSHBC)}$ = 8.4 V (frequency is at a minimum) and at a minimum (≈ 3 V). Under $V_{fmax(SSHBC)}$ (maximum frequency), the discharge current is reduced to a maximum frequency soft-start current of 5 μA The voltage is clamped at a minimum of $V_{pu(EN)}$ = 3 V. Both clamp levels are just outside the operating area of $V_{fmax(SSHBC)}$ to $V_{fmin(SSHBC)}$. The margins avoid frequency disturbance during normal output voltage regulation but ensure that overcurrent regulation can respond quickly.

7.8.8.2 Soft-start charge and discharge

At initial start-up, the soft-start capacitor $C_{ss(HBC)}$ is charged to obtain a decreasing frequency sweep from the maximum to the operating frequency. As well as being used to soft-start the resonant converter, the soft-start functionality is also used for regulation (such as overcurrent regulation). $C_{ss(HBC)}$ can therefore be charged or discharged. A continuous alternation between charging and discharging occurs during overcurrent regulation. In this way $V_{SSHBC/EN}$ can be regulated, overruling the signal from the feedback input.

The charge and discharge current can have a high value, $I_{ss(hf)(SSHBC)}$ = 160 μA. This current results in fast charging and discharging. In addition, it can have a low value $I_{ss(lf)(SSHBC)}$ = 40 μA, resulting in a slow charge and discharge. This two-speed soft-start sweep allows a combination of a short start-up time for the resonant converter and stable regulation loops (such as overcurrent regulation).

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The fast charge and discharge is used for the upper frequency range where $V_{SSHBC/EN} < V_{ss(hf-lf)(SSHBC)} = 5.6$ V. In the upper frequency range, the currents in the converter do not react strongly to frequency variations.

The slow charge and discharge speed is used for the lower frequency range where $V_{SSHBC/EN} > V_{ss(hf-lf)(SSHBC)} = 5.6$ V. In the lower frequency range, the currents in the converter react strongly to frequency variations.

Section 7.8.10.2 describes how the two-speed soft-start function is used for overcurrent regulation.

The soft-start capacitor is not charged or discharged during non-operation time in burst mode. The soft-start voltage does not change during this time.

7.8.8.3 Soft-start reset

Some protection functions, such as overcurrent protection, require fast correction of the operating frequency set point, but do not require switching to stop. See the protection overview in Section 7.9 for details on which protection functions use this step to the maximum frequency. The SSL4120 has a special fast soft-start reset feature for the HBC controller that forces $V_{fmax(ss)(RFMAX)}$ on the RFMAX pin. Soft-start reset is also used when the HBC controller is enabled using the SSHBC/EN pin or after a restart to ensure a safe-start at maximum frequency. Soft-start reset is not used when the operation was stopped in burst mode.

When a protection function is activated, the oscillator control input is disconnected from the soft-start capacitor $C_{ss(HBC)}$ which is connected between the SSHBC/EN pin and ground. The switching frequency is immediately set to a maximum. Setting the switching frequency to a maximum restores safe switching operation in most cases. At the same time, the capacitor is discharged to the maximum frequency level $V_{fmax(SSHBC)}$. Once $V_{SSHBC/EN}$ has reached this level, the oscillator control input is connected to the pin again and the normal soft-start sweep follows. Figure 16 shows the soft-start reset and the two-speed frequency sweep downwards.

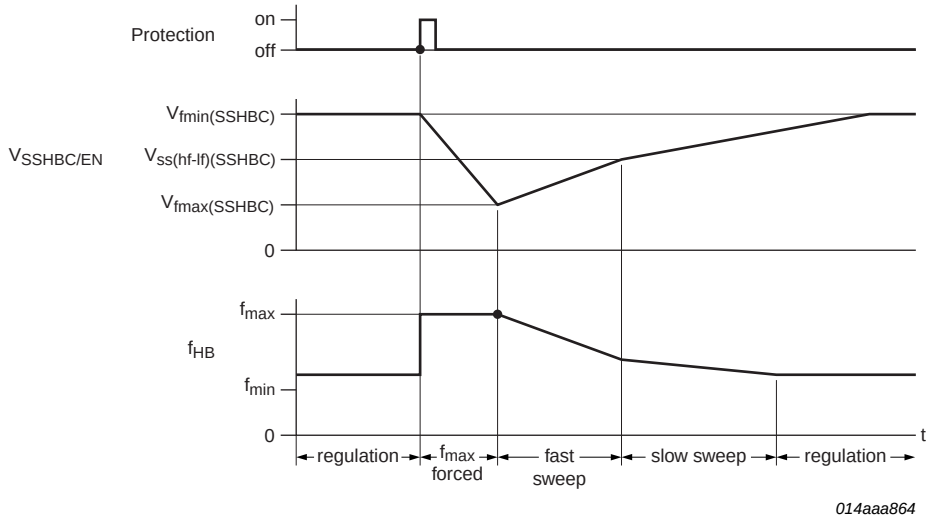


Fig 16. Soft-start reset and two-speed soft-start

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7.8.9 HBC high-frequency protection, HFP-HBC (RFMAX pin)

Normally the converter does not operate continuously at maximum frequency because it sweeps down to much lower values. Certain error conditions, such as a disconnected transformer, could cause the converter to operate continuously at maximum frequency. If zero-voltage switching conditions are no longer present, the MOSFETs can overheat. The SSL4120 features High-Frequency Protection (HFP) for the HBC controller to protect it from being damaged in such circumstances.

HFP senses the RFMAX pin voltage. This voltage indicates the current frequency. When the frequency is higher than 75 % of the soft-start frequency range, the protection timer is started. The 75 % level corresponds to an RFMAX voltage of $V_{hfp(RFMAX)}$ = 1.83 V.

7.8.10 HBC overcurrent regulation and protection, OCR and OCP (SNSCURHBC pin)

The HBC controller is protected against overcurrent in two ways:

- Overcurrent regulation (OCR-HBC) which increases the frequency slowly. The protection timer is also started.
- Overcurrent protection (OCP-HBC) which steps to maximum frequency.

A V_{boost} compensation function is used to reduce the variation in the output current protection level.

7.8.10.1 Boost voltage compensation

The primary current, also known as the resonant current, is sensed using the SNSCURHBC pin. It senses the momentary voltage across an external current sense resistor $R_{cur(HBC)}$. The use of the momentary current signal allows fast overcurrent protection and simplifies the stabilizing of overcurrent regulation. The OCR and OCP comparators compare $V_{SNSCURHBC}$ with the maximum positive and negative values.

The primary current is higher when V_{boost} is low for the same output power. Boost compensation is included to reduce the dependency of the protected output current level on V_{boost}. The boost compensation sources and sinks a current from the SNSCURHBC pin. This current creates a voltage drop across the series resistor R_{curcmp}.

The amplitude of the current is linearly dependent on V_{boost}. At $V_{boost(nom)}$, the current is zero and the voltage $V_{Cur(HBC)}$ across the current sense resistor is also present on the SNSCURHBC pin.

At the UVP boost start level $V_{uvp(SNSBOOST)}$, the current is at a maximum. The current sink or source direction depends on the active gate signal. The voltage drop created across R_{curcmp} reduces the amplitude at the pin. This reduction in amplitude results in a higher effective current protection level. The R_{curcmp} value sets the amount of compensation. Figure 17 shows how the boost compensation works for an artificial current signal. The sinking compensation current only flows when $V_{SNSCURHBC}$ is positive because of the circuit implementation.

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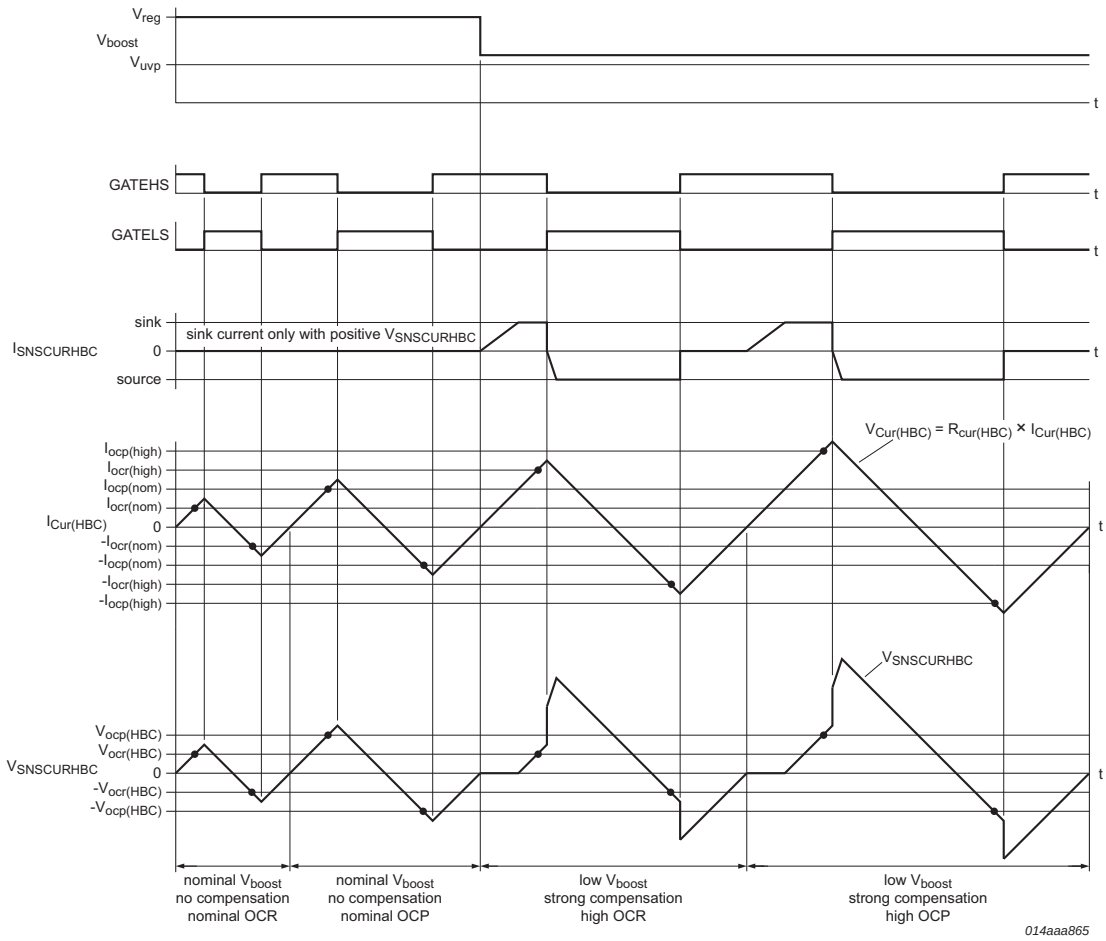


Fig 17. Boost voltage compensation

7.8.10.2 Overcurrent regulation, OCR-HBC

The lowest comparator levels at the SNSCURHBC pin ($V_{ocr(HBC)}$ = −0.5 V and +0.5 V), relate to the overcurrent regulation voltage. There are comparators for both the positive and negative polarities. The positive comparator is active during the high-side on-time and the following high-side to low-side non-overlap time. The negative comparator is active during the remaining time. If either level is exceeded, the frequency is slowly increased. Discharging the soft-start capacitor achieves this decrease.

Each time the OCR level is exceeded, the event is latched until the next stroke and the soft-start discharge current is enabled. When both the positive and negative OCR levels are exceeded, the soft-start discharge current flows continuously.

Overcurrent regulation is very effective at limiting the output current during start-up. A smaller soft-start capacitor is used to achieve a faster start-up. Using a smaller capacitor can result in an output current that is too high at times. However, the OCR function slows down the frequency sweep when required to keep the output current within the specified limits. Figure 18 shows the operation of the OCR during output voltage start-up.

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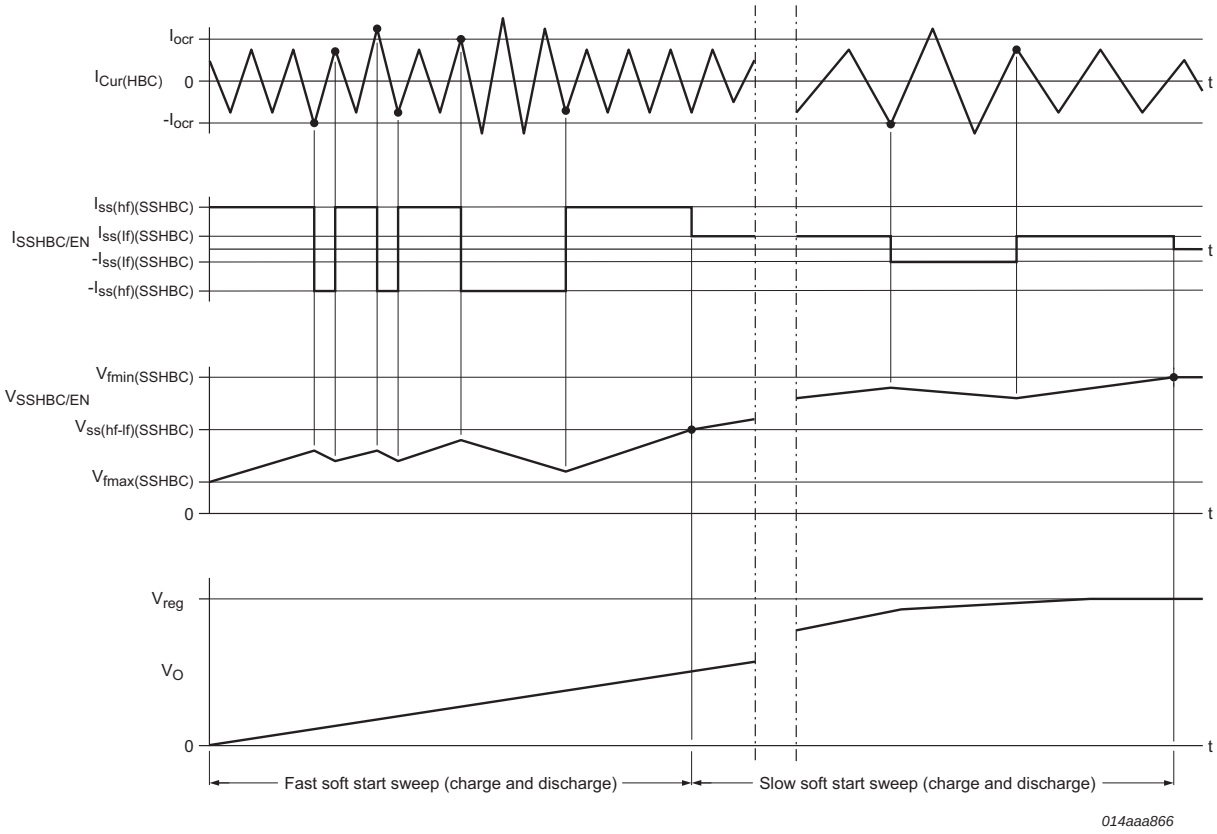


Fig 18. Overcurrent regulation during start-up

The protection timer is also started. The Restart state is activated when the OCR-HBC condition is still present after the protection time has elapsed.

7.8.10.3 Overcurrent protection, OCP-HBC

Under normal operating conditions, OCR is able to ensure the current remains below the specified maximum values. However, in the event of certain error conditions, it is not fast enough to limit the current. OCP is implemented to protect against those error conditions. The OCP level ($V_{ocp(HBC)}$ = –1 V and +1 V), is higher than the OCR level $V_{ocr(HBC)}$.

When the OCP level is reached, the frequency immediately jumps to the maximum value using the soft-start reset, then a normal sweep down.

7.8.11 HBC capacitive mode regulation, CMR (HB pin)

The MOSFETs in the half-bridge drive the resonant circuit. Depending on the output load, the output voltage and the switching frequency this resonant circuit can have an inductive or a capacitive impedance. Inductive impedance is preferred because it facilitates efficient zero-voltage switching.

Harmful switching in capacitive mode is avoided using the adaptive non-overlap time function (see Section 7.8.4.2). An extra action is performed which results in Capacitive Mode Regulation (CMR). CMR causes the half-bridge circuit to return to Inductive mode from Capacitive mode.

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Capacitive mode is detected when the HB slope does not start within $t_{to(cmr)}$ after the MOSFETs have switched off. Detection of Capacitive mode increases the switching frequency. This increase is caused by discharging the soft-start capacitor with a relatively high current $I_{cmr(hf)(SSHBC)}$ immediately after $t_{to(cmr)}$ expires until the half-bridge slope starts. The frequency increase regulates the HBC to the border between capacitive and inductive mode.

7.9 Protection functions overview

Table 4. Overview protections

Protected part	Symbol	Protection	Affected	Action	Description
IC	UVP-SUPIC	Undervoltage protection SUPIC	IC	disable	Section 7.2.1
IC	UVP-SUPREG	Undervoltage protection SUPREG	IC	disable	Section 7.2.2
IC	UVP-supplies	Undervoltage protection supplies	IC	disable and reset	Section 7.3
IC	SCP-SUPIC	Short circuit protection SUPIC	IC	low HV start-up current	Section 7.2.4
IC	OVP output	Overvoltage protection output	IC	shutdown	Section 7.5.4
IC	UVP output	Undervoltage protection output	IC	restart after protection time	Section 7.5.5
IC	OTP	Overtemperature protection	IC	disable	Section 7.5.6
PFC	OCR-PFC	Overcurrent regulation PFC	PFC	switch off cycle-by-cycle	Section 7.7.7
PFC	UVP mains	Undervoltage protection mains	PFC	suspend switching	Section 7.7.8
PFC	OVP boost	Overvoltage protection boost	PFC	suspend switching	Section 7.7.9
PFC	SCP boost	Short circuit protection boost	IC	restart	Section 7.7.10
PFC	OLP-PFC	Open-loop protection PFC	IC	restart	Section 7.7.10
HBC	UVP boost	Undervoltage protection boost	HBC	disable	Section 7.8.2
HBC	OLP-HBC	Open-loop protection HBC	IC	restart after protection time	Section 7.8.7
HBC	HFP-HBC	High-frequency protection HBC	IC	restart after protection time	Section 7.8.9
HBC	OCR-HBC	Overcurrent regulation HBC	HBC IC	increase frequency restart after protection time	Section 7.8.10.2
HBC	OCP-HBC	Overcurrent protection HBC	HBC	step to maximum frequency	Section 7.8.10.3
HBC	CMR	Capacitive mode regulation	HBC	increase frequency	Section 7.8.11
HBC	ANO	Adaptive non-overlap	HBC	prevent hazardous switching	Section 7.8.4

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to pin SGND; Currents are positive when flowing into the IC; The voltage ratings are valid provided other ratings are not violated; Current ratings are valid provided the maximum power rating is not violated.

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{SUPHV}	voltage on pin SUPHV	continuous	−0.4	+630	V
V_{SUPHS}	voltage on pin SUPHS	DC	−0.4	+570	V
		t < 0.5 s	−0.4	+630	V
		referenced to the HB pin	−0.4	+14	V
V_{SUPIC}	voltage on pin SUPIC		−0.4	+38	V
$V_{SNSAUXPFC}$	voltage on pin SNSAUXPFC		−25	+25	V
V_{SUPREG}	voltage on pin SUPREG		−0.4	+12	V
V_{SNSOUT}	voltage on pin SNSOUT		−0.4	+12	V
V_{RCPROT}	voltage on pin RCPROT		−0.4	+12	V
V_{SNSFB}	voltage on pin SNSFB		−0.4	+12	V
$V_{SSHBC/EN}$	voltage on pin SSHBC/EN		−0.4	+12	V
V_{GATEHS}	voltage on pin GATEHS	t < 10 µs for I > 10 mA	−0.4	V_{SUPHS} + 0.4	V
V_{GATELS}	voltage on pin GATELS	t < 10 µs for I > 10 mA	−0.4	V_{SUPREG} + 0.4	V
$V_{GATEPFC}$	voltage on pin GATEPFC	t < 10 µs for I > 10 mA	−0.4	V_{SUPREG} + 0.4	V
$V_{SNSCURHBC}$	voltage on pin SNSCURHBC		−5	+5	V
$V_{SNSBOOST}$	voltage on pin SNSBOOST		−0.4	+5	V
$V_{SNSMAINS}$	voltage on pin SNSMAINS		−0.4	+5	V
$V_{SNSCURPFC}$	voltage on pin SNSCURPFC	current limited	−0.4	+5	V
$V_{COMPPFC}$	voltage on pin COMPPFC		−0.4	+5	V
V_{CFMIN}	voltage on pin CFMIN		−0.4	+5	V
V_{PGND}	voltage on pin PGND		−1	+1	V
Currents					
$I_{GATEPFC}$	current into pin GATEPFC	duty cycle < 10 %	−0.8	+2	A
$I_{SNSCURPFC}$	current into pin SNSCURPFC		−1	+10	mA
General					
P_{tot}	total power dissipation	T_{amb} < 75 °C	-	0.8	W
T_{stg}	storage temperature		−55	+150	°C
T_j	junction temperature		−40	+150	°C

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Table 5. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to pin SGND; Currents are positive when flowing into the IC; The voltage ratings are valid provided other ratings are not violated; Current ratings are valid provided the maximum power rating is not violated.

Symbol	Parameter	Conditions		Min	Max	Unit
ESD						
V_{ESD}	Electrostatic discharge voltage	Human body model				
		pin 12 (SUPHV)	[1]	-	1.5	kV
		pin 13,14,15 (HS driver)	[1]	-	1	kV
		other pins	[1]	-	2	kV
		Machine model				
		all pins	[2]	-	200	V
		Charged device model				
		all pins		-	500	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω resistor.

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; JEDEC single layer test board	90	K/W

10. Characteristics

Table 7. Characteristics

T_{amb} = 25 °C; V_{SUPIC} = 20 V; V_{SUPHV} > 40 V; all voltages are measured with respect to SGND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High-voltage start-up source (SUPHV pin)						
$I_{dism(SUPHV)}$	disable mode current on pin SUPHV	disabled IC state	-	150	-	μA
$I_{red(SUPHV)}$	reduced current on pin SUPHV	$V_{SUPIC} < V_{scp(SUPIC)}$	-	1.1	-	mA
$I_{nom(SUPHV)}$	nominal current on pin SUPHV	$V_{SUPIC} < V_{start(hvd)(SUPIC)}$	-	5.1	-	mA
$I_{tko(SUPHV)}$	takeover current on pin SUPHV	$V_{SUPIC} > V_{start(hvd)(SUPIC)}$	-	7	-	μA
$V_{det(SUPHV)}$	detection voltage on pin SUPHV		-	-	25	V
$V_{rst(SUPHV)}$	reset voltage on pin SUPHV	$V_{SUPIC} < V_{rst(SUPIC)}$	-	7	-	V
Low-voltage IC supply (SUPIC pin)						
$V_{start(hvd)(SUPIC)}$	start voltage with high voltage detected	$V_{SUPHV} > V_{det(SUPHV)}$	21	22	23	V
$V_{start(nohvd)(SUPIC)}$	start voltage with no high voltage detected	$V_{SUPHV} < V_{det(SUPHV)}$ or open	16.1	17	17.9	V
$V_{start(hys)(SUPIC)}$	hysteresis of start voltage on pin SUPIC		-	0.3	-	V
$V_{uvp(SUPIC)}$	undervoltage protection voltage on pin SUPIC		14.2	15	15.8	V

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Table 7. Characteristics *...continued*

T_{amb} = 25 °C; V_{SUPIC} = 20 V; V_{SUPHV} > 40 V; all voltages are measured with respect to SGND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{rst(SUPIC)}$	reset voltage on pin SUPIC	$V_{SUPHV} < V_{rst(SUPHV)}$		-	7	-	V
$V_{scp(SUPIC)}$	short-circuit protection voltage on pin SUPIC			0.55	0.65	0.75	V
$I_{ch(red)(SUPIC)}$	reduced charge current on pin SUPIC	$V_{SUPIC} < V_{scp(SUPIC)}$		-	−0.95	-	mA
$I_{ch(nom)(SUPIC)}$	nominal charge current on pin SUPIC			-	−4.8	-	mA
$I_{dism(SUPIC)}$	current on pin SUPIC in disabled mode	disabled IC state		-	0.25	-	mA
$I_{protm(SUPIC)}$	current on pin SUPIC in protection mode	SUPIC charge, SUPREG charge; Restart or Shut-down state		-	0.4	-	mA
$I_{oper(SUPIC)}$	current on pin SUPIC in operating mode	Operational supply state; Driver pins open.		-	3	-	mA
Regulated supply (SUPREG pin)							
$V_{reg(SUPREG)}$	regulation voltage on pin SUPREG	I_{SUPREG} = −40 mA	[1]	10.6	10.9	11.2	V
$V_{start(SUPREG)}$	start voltage on pin SUPREG		[1]	-	10.7	-	V
$V_{uvp(SUPREG)}$	undervoltage protection voltage on pin SUPREG		[1]	-	10.3	-	V
$I_{ch(SUPREG)max}$	maximum charge current on pin SUPREG	$V_{SUPREG} > V_{uvp(SUPREG)}$		−40	−100	-	mA
$I_{ch(red)(SUPREG)}$	reduced charge current on pin SUPREG	$V_{SUPREG} < V_{uvp(SUPREG)}$; T = 25 °C.		-	−5.5	-	mA
		T = 140 °C		−2.5	-	-	mA
Enable input (SSHBC/EN pin)							
$V_{en(PFC)(EN)}$	PFC enable voltage on pin EN	PFC only	[2]	0.8	1.2	1.4	V
$V_{en(IC)(EN)}$	IC enable voltage on pin EN	PFC + HBC	[2]	1.8	2.2	2.4	V
$I_{pu(EN)}$	pull-up current on pin EN	$V_{SSHBC/EN}$ = 2.5 V		-	−42	-	µA
$V_{pu(EN)}$	pull-up voltage on pin EN			-	3	-	V
Fast shut-down reset (SNSMAINS pin)							
$V_{rst(SNSMAINS)}$	reset level on pin SNSMAINS		[2]	-	0.8	-	V
Protection and restart timer (RCPROT pin)							
$V_{u(RCPROT)}$	upper voltage on pin RCPROT			3.8	4	4.2	V
$V_{l(RCPROT)}$	lower voltage on pin RCPROT			0.4	0.5	0.6	V
$I_{ch(fast)(RCPROT)}$	fast-charge current on pin RCPROT			-	−2.2	-	mA
$I_{ch(slow)(RCPROT)}$	slow-charge current on pin RCPROT			−120	−100	−80	µA

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Table 7. Characteristics *...continued*

T_{amb} = 25 °C; V_{SUPIC} = 20 V; V_{SUPHV} > 40 V; all voltages are measured with respect to SGND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Output voltage protection sensing, UVP/OVP output (SNSOUT pin)							
$V_{ovp(SNSOUT)}$	overvoltage protection voltage on pin SNSOUT		[2]	3.4	3.5	3.6	V
$V_{uvp(SNSOUT)}$	under-voltage protection voltage on pin SNSOUT		[2]	2.2	2.35	2.5	V
Overtemperature protection							
T_{otp}	overtemperature protection trip temperature		[2]	130	150	160	°C
Burst mode activation (SNSOUT pin)							
$V_{burst(HBC)}$	HBC burst mode voltage		[2]	0.9	1.1	1.2	V
$V_{burst(PFC)}$	PFC burst mode voltage		[2]	0.3	0.4	0.5	V
$I_{pu(SNSOUT)}$	pull-up current on pin SNSOUT			-	−100	−80	µA
$V_{pu(SNSOUT)}$	pull-up voltage on pin SNSOUT	R_{SNSOUT} = 25 kΩ to SGND		-	1.5	-	V
PFC driver (GATEPFC pin)							
$I_{source(GATEPFC)}$	source current on pin GATEPFC	$V_{GATEPFC}$ = 2 V		-	−0.5		A
$I_{sink(GATEPFC)}$	sink current on pin GATEPFC	$V_{GATEPFC}$ = 2 V		-	0.7	-	A
		$V_{GATEPFC}$ = 10 V		-	1.2	-	A
PFC on-timer (COMPPFC pin)							
$V_{ton(COMPPFC)zero}$	zero on-time voltage on pin COMPPFC			-	3.5	-	V
$V_{ton(COMPPFC)max}$	maximum on-time voltage on pin COMPPFC			-	1.25	-	V
$f_{max(PFC)}$	PFC maximum frequency			300	380	460	kHz
$t_{off(PFC)min}$	minimum PFC off-time			-	1.1	-	µs
PFC error amplifier (SNSBOOST and COMPPFC pins)							
$V_{reg(SNSBOOST)}$	regulation voltage on pin SNSBOOST pin	$I_{COMPPFC}$ = 0 A		2.475	2.5	2.525	V
g_m	transconductance	$V_{SNSBOOST}$ to $I_{COMPPFC}$		-	80	-	µA/V
$I_{sink(COMPPFC)}$	sink current on pin COMPPFC	$V_{SNSBOOST}$ = 2 V		-	39	-	µA
$I_{source(COMPPFC)}$	source current on pin COMPPFC	$V_{SNSBOOST}$ = 3.3 V		-	−39	-	µA
$V_{clamp(COMPPFC)}$	clamp voltage on pin COMPPFC		[3]	-	3.9	-	V
PFC mains compensation (SNSMAINS pin)							
$t_{on(max)}$	maximum on-time	high mains; $V_{SNSMAINS}$ = 3.3 V		3.5	4.7	5.9	µs
		low mains; $V_{SNSMAINS}$ = 0.97 V		29	44	59	µs
$V_{mvc(SNSMAINS)max}$	maximum mains voltage compensation voltage on pin SNSMAINS			4	-	-	V

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Table 7. Characteristics *...continued*

T_{amb} = 25 °C; V_{SUPIC} = 20 V; V_{SUPHV} > 40 V; all voltages are measured with respect to SGND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PFC demagnetization sensing (SNSAUXPFC pin)							
$V_{demag(SNSAUXPFC)}$	demagnetization voltage on pin SNSAUXPFC			–150	–100	–50	mV
$t_{to(mag)}$	magnetization time-out time			40	50	60	µs
$I_{prot(SNSAUXPFC)}$	protection current on pin SNSAUXPFC	$V_{SNSAUXPFC}$ = 50 mV		–75	–33	-	nA
PFC valley sensing (SNSAUXPFC pin)							
$(dV/dt)_{vrec(min)}$	minimum valley recognition rate of voltage change			-	-	1.7	V/µs
$t_{slope(vrec)min}$	minimum valley recognition slope time	$V_{SNSAUXPFC}$ = 1 V_{pp}	[4]	-	-	300	ns
		demagnetization to $\Delta V/\Delta t$ = 0	[5]	-	-	50	ns
$t_{d(val-dem)max}$	maximum valley-to-demag delay time			-	200	-	ns
$t_{to(vrec)}$	valley recognition time-out time			3	4	6	µs
PFC soft start (SNSCURPFC pin)							
$I_{ch(ss)(PFC)}$	PFC soft-start charge current			-	–60	-	µA
$V_{clamp(ss)(PFC)}$	PFC soft-start clamp voltage		[1]	0.46	0.5	0.54	V
$V_{stop(ss)(PFC)}$	PFC soft-start stop voltage		[1]	-	0.45	-	V
$R_{ss(PFC)}$	PFC soft-start resistor			12	-	-	kΩ
PFC overcurrent sensing (SNSCURPFC pin)							
$V_{ocr(PFC)}$	PFC overcurrent regulation voltage	dV/dt = 50 mV/µs		0.49	0.52	0.55	V
		dV/dt = 200 mV/µs		0.51	0.54	0.57	V
$t_{leb(PFC)}$	leading edge blanking time			250	310	370	ns
$I_{prot(SNSCURPFC)}$	protection current on pin SNSCURPFC			–50	–33	-	nA
PFC mains voltage sensing and clamp (SNSMAINS pin)							
$V_{start(SNSMAINS)}$	start voltage on pin SNSMAINS		[1]	1.11	1.15	1.19	V
$V_{uvp(SNSMAINS)}$	undervoltage protection voltage on pin SNSMAINS		[1]	0.84	0.89	0.94	V
$V_{pu(SNSMAINS)}$	pull-up voltage on pin SNSMAINS	UVP mains active	[1]	-	1.05	-	V
$I_{pu(SNSMAINS)}$	maximum clamp current	UVP mains active		-	–42	–35	µA
$I_{prot(SNSMAINS)}$	Protection current on pin SNSMAINS	$V_{SNSMAINS}$ > $V_{uvp(SNSMAINS)}$		-	33	100	nA
PFC boost voltage protection sensing, SCP/UVP/OVP boost (SNSBOOST pin)							
$V_{scp(SNSBOOST)}$	short-circuit protection voltage on pin SNSBOOST			0.35	0.4	0.45	V
$V_{start(SNSBOOST)}$	start voltage on pin SNSBOOST			-	2.3	2.4	V
$V_{uvp(SNSBOOST)}$	undervoltage protection voltage on pin SNSBOOST			1.5	1.6	-	V
$V_{ovp(SNSBOOST)}$	overvoltage protection voltage on pin SNSBOOST			2.59	2.63	2.67	V

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Table 7. Characteristics *...continued*

T_{amb} = 25 °C; V_{SUPIC} = 20 V; V_{SUPHV} > 40 V; all voltages are measured with respect to SGND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{prot(SNSBOOST)}$	protection current on pin SNSBOOST	$V_{SNSBOOST}$ = 2.5 V		-	45	100	nA
HBC high-side and low-side driver (GATEHS and GATELS pins)							
$I_{source(GATEHS)}$	source current on pin GATEHS	$V_{GATEHS} - V_{HB}$ = 4 V		-	−310	-	mA
$I_{source(GATELS)}$	source current on pin GATELS	$V_{GATELS} - V_{PGND}$ = 4 V		-	−310	-	mA
$I_{sink(GATEHS)}$	sink current on pin GATEHS	$V_{GATEHS} - V_{HB}$ = 2 V;		-	560	-	mA
		$V_{GATEHS} - V_{HB}$ = 11 V		-	1.9	-	A
$I_{sink(GATELS)}$	sink current on pin GATELS	$V_{GATELS} - V_{PGND}$ = 2 V		-	560	-	mA
		$V_{GATELS} - V_{PGND}$ = 11 V		-	1.9	-	A
$V_{rst(SUPHS)}$	reset voltage on pin SUPHS			-	4.5	-	V
$I_{q(SUPHS)}$	quiescent current on pin SUPHS	$V_{SUPHS} - V_{HB}$ = 11 V		-	37	-	µA
HBC adaptive non-overlap time (HB pin)							
$(dV/dt)_{ano(min)}$	minimum adaptive non-overlap time rate of voltage change			-	-	120	V/µs
$t_{no(min)}$	minimum non-overlap time			-	-	160	ns
HBC current controlled oscillator (CFMIN and RFMAX pin)							
$f_{min(HB)}$	minimum frequency on pin HB	C_{fmin} = 390 pF; $V_{SSHBC/EN} > V_{fmin(SSHBC)}$ $V_{SNSFB} > V_{fmin(SNSFB)}$		40	44	48	kHz
$I_{osc(min)}$	minimum oscillator current	V_{RFMAX} = 0 V; charge and discharge		-	150	-	µA
$I_{osc(max)}$	maximum oscillator current	R_{fmax} = 15 kΩ; V_{RFMAX}=2.5 V; $V_{SSHBC/EN} < V_{fmax(SSHBC)}$		-	970	-	µA
$I_{osc(red)}$	reduced oscillator current	slowed-down oscillator		-	−30	-	µA
I_{CFMIN}/I_{RFMAX}	current on pin CFMIN to current on pin RFMAX ratio			-	4.9	-	
$f_{limit(HB)}$	limit frequency on pin HB	C_{fmin} = 20 pF		500	670	-	kHz
$V_{u(CFMIN)}$	upper voltage on pin CFMIN			2.85	3	3.15	V
$V_{l(CFMIN)}$	lower voltage on pin CFMIN			0.9	1	1.1	V
$V_{fmin(RFMAX)}$	minimum frequency voltage on pin RFMAX			-	0	-	V
$V_{fmax(ss)(RFMAX)}$	maximum soft start frequency voltage on pin RFMAX	$V_{SSHBC/EN} < V_{fmax(SSHBC)}$		2.4	2.5	2.6	V
$V_{fmax(fb)(RFMAX)}$	maximum feedback frequency voltage on pin RFMAX	$V_{SNSFB} < V_{fmax(SNSFB)}$		1.45	1.55	1.65	V
HBC feedback input (SNSFB pin)							
$V_{pu(SNSFB)}$	pull-up voltage on pin SNSFB			-	8.4	-	V
$R_{O(SNSFB)}$	output resistance on pin SNSFB			-	1.5	-	kΩ
$V_{olp(SNSFB)}$	open-loop protection voltage on pin SNSFB		[2]	7	7.7	7.9	V
$I_{olp(SNSFB)}$	open-loop protection current on pin SNSFB		[2]	−0.35	−0.26	−0.1	mA

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Table 7. Characteristics *...continued*

T_{amb} = 25 °C; V_{SUPIC} = 20 V; V_{SUPHV} > 40 V; all voltages are measured with respect to SGND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{fmin(SNSFB)}$	minimum frequency voltage on pin SNSFB			6.1	6.4	6.9	V
$I_{fmin(SNSFB)}$	minimum frequency current on pin SNSFB	$V_{SSHBC/EN} > V_{fmin(SSHBC)}$		–0.86	–0.66	–0.46	mA
$V_{fmax(SNSFB)}$	maximum frequency voltage on pin SNSFB	$V_{SSHBC/EN} > V_{fmin(SSHBC)}$		3.9	4.1	4.3	V
$I_{fmax(SNSFB)}$	maximum frequency current on pin SNSFB	$V_{SSHBC/EN} > V_{fmin(SSHBC)}$		-	–2.2	-	mA
$V_{clamp(SNSFB)}$	clamp voltage on pin SNSFB	maximum frequency; I_{SNSFB} = –4 mA		-	3.2	-	V
$I_{clamp(SNSFB)}$	clamp current on pin SNSFB	maximum frequency; V_{SNSFB} = 0 V		-	–7.3	-	mA
HBC soft-start (SSHBC/EN pin)							
$V_{fmax(SSHBC)}$	maximum frequency voltage on pin SSHBC			-	3.2	-	V
$V_{fmin(SSHBC)}$	minimum frequency voltage on pin SSHBC	$V_{SNSFB} > V_{fmin(SNSFB)}$		7.5	7.9	8.3	V
$V_{clamp(SSHBC)}$	clamp voltage on pin SSHBC			-	8.4	-	V
$V_{ss(hf-lf)(SSHBC)}$	high-low frequency soft-start voltage on pin SSHBC		[2]	-	5.6	-	V
$I_{ss(hf)(SSHBC)}$	high frequency soft-start current on pin SSHBC	$V_{SSHBC} < V_{ss(lf-hf)(SSHBC)}$					
		charge current		-	–160	-	µA
		discharge current		-	160	-	µA
$I_{ss(lf)(SSHBC)}$	low frequency soft-start current on pin SSHBC	$V_{SSHBC} > V_{ss(lf-hf)(SSHBC)}$					
		charge current		-	–40	-	µA
		discharge current		-	40	-	µA
$I_{cmr(hf)(SSHBC)}$	high frequency CMR current on pin SSHBC	$V_{SSHBC} < V_{ss(lf-hf)(SSHBC)}$ discharge only		-	1800	-	µA
$I_{cmr(lf)(SSHBC)}$	low frequency CMR current on pin SSHBC	$V_{SSHBC} > V_{ss(lf-hf)(SSHBC)}$ discharge only		-	440	-	µA
HBC high frequency sensing, HFP - HBC (RFMAX pin)							
$V_{hfp(RFMAX)}$	High-frequency protection voltage on pin RFMAX		[2]	1.7	1.83	2	V
HBC overcurrent sensing, OCR/OCP - HBC (SNSCURHBC pin)							
$V_{ocr(HBC)}$	HBC overcurrent regulation voltage						
		positive level; HS on + HS-LS non-overlap time		0.45	0.5	0.55	V
		negative level; LS on + LS-HS non-overlap time		–0.55	–0.5	–0.45	V

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Table 7. Characteristics *...continued*

T_{amb} = 25 °C; V_{SUPIC} = 20 V; V_{SUPHV} > 40 V; all voltages are measured with respect to SGND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ocp(HBC)}$	HBC overcurrent protection voltage					
		positive level; HS on + HS-LS non-overlap time	0.9	1	1.1	V
		negative level; LS on + LS-HS non-overlap time	−1.1	−1	−0.9	V
$I_{bstc(SNSCURHBC)max}$	maximum boost compensation current on pin SNSCURHBC	$V_{SNSBOOST}$ = 1.8 V				
		source current; $V_{SNSCURHBC}$ = −0.5 V	-	−170	-	μA
		sink current; $V_{SNSCURHBC}$ = 0.5 V	-	170	-	μA
HBC Capacitive Mode Protection (CMP) (HB pin)						
$t_{to(cmr)}$	time-out capacitive mode regulation		-	690	-	ns

[1] The marked levels on this pin are correlated. The voltage difference between the levels has much less spread than the absolute value of the levels themselves.

[2] Switching level has some hysteresis. The hysteresis falls within the limits.

[3] For a typical application with a compensation network on the COMPPFC pin, as the example in Figure 19.

[4] Minimum required voltage change time for valley recognition on the SNSAUXPFC pin.

[5] Minimum time required between demagnetization detection and $\Delta V/\Delta t$ = 0 on the SNSAUXPFC pin.

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11. Application information

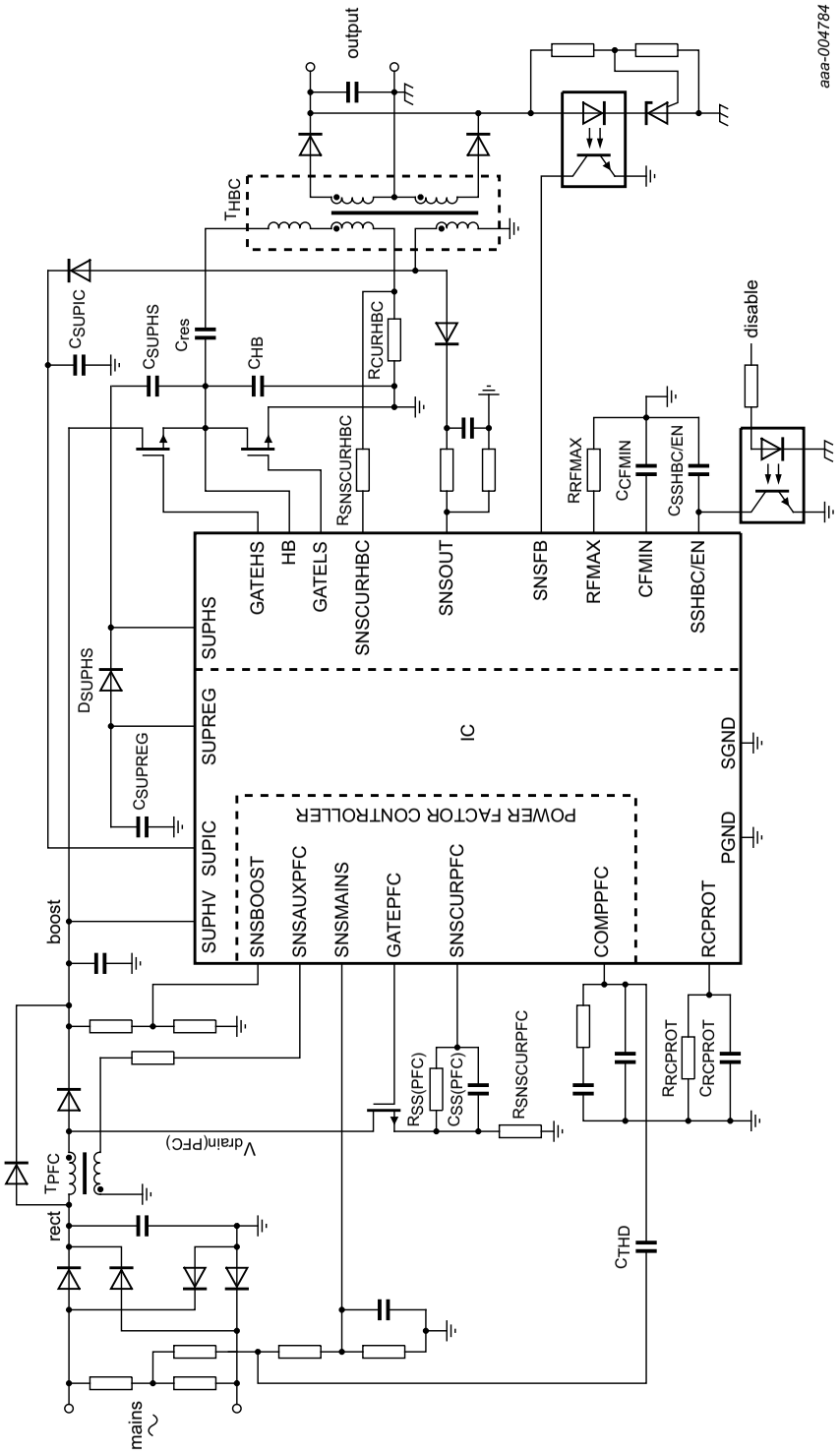


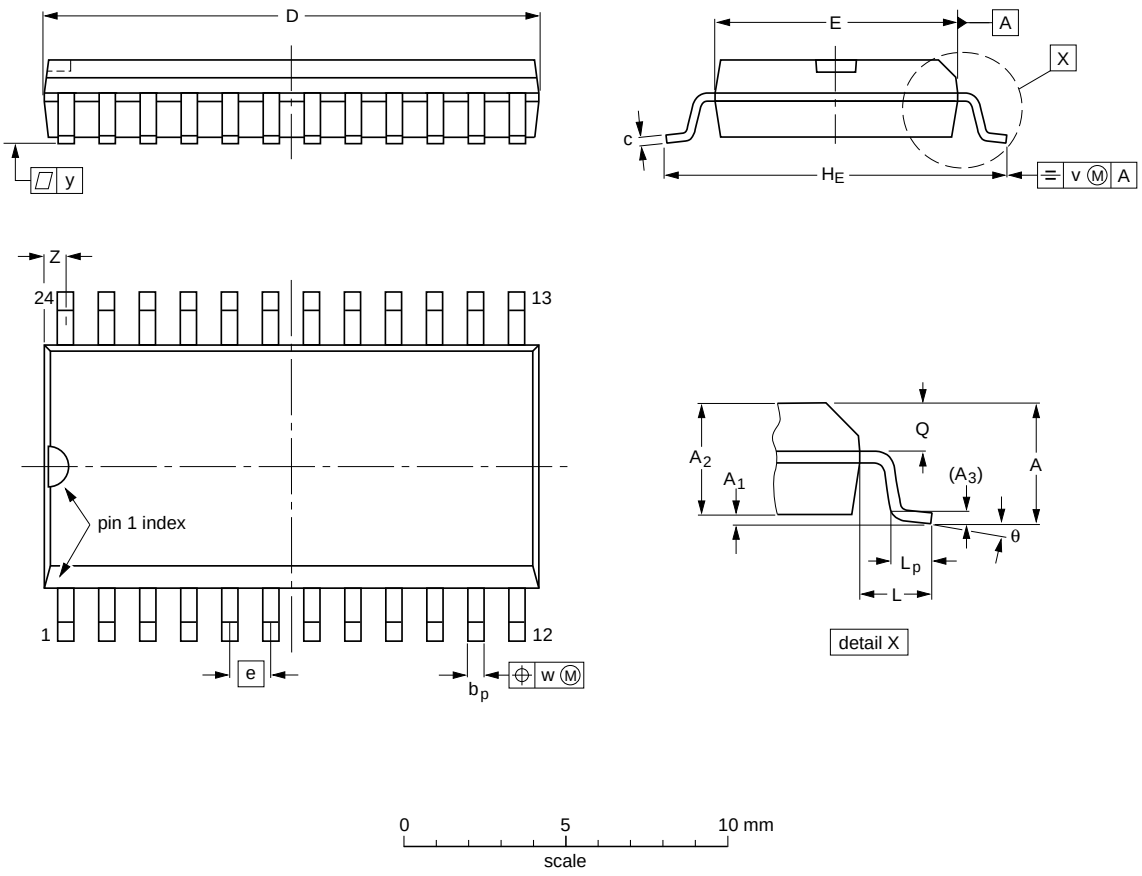
Fig 19. Application diagram of SSL4120

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12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 20. Package outline SOT137 (SO24)

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13. Abbreviations

Table 8. Abbreviations

Acronym	Description
ANO	Adaptive Non-Overlap
CMOS	Complementary Metal-Oxide-Semiconductor'
CMP	Capacitive Mode Protection
CMR	Capacitive Mode Regulation
DMOS	Double-diffused Metal-Oxide-Semiconductor
EMI	ElectroMagnetic Interference
HBC	Half-Bridge Converter or Controller. Resonant converter which generates the regulated output voltage.
HFP	High-Frequency Protection
HV	High-voltage
OCP	OverCurrent Protection
OCR	OverCurrent Regulation
OLP	Open-Loop Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
PFC	Power Factor Converter or Controller. Converter which performs the power factor correction.
UVP	UnderVoltage Protection
SCP	Short-Circuit Protection

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14. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SSL4120 v.2	20121101	Product data sheet	-	SSL4120T v.1
SSL4120T v.1	20120621	Objective data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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