SONY

CXL5506M/P

CMOS-CCD 1H Delay Line for PAL

Description

The CXL5506M/P are CMOS-CCD delay line ICs that provide 1H delay time for PAL signals including the external low-pass filter.

Features

- Single 5V power supply
- Low power consumption 95mW (Typ.)
- Built-in peripheral circuits

Functions

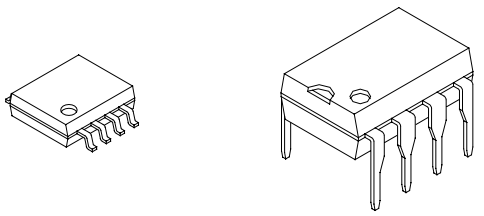
- 1130-bit CCD register
- Clock driver
- Auto-bias circuit
- Input clamp circuit
- Sample-and-hold circuit

Structure

CMOS-CCD

CXL5506M
8 pin SOP (Plastic)

CXL5506P
8 pin DIP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	6	V
• Operating temperature	Topr	–10 to +60	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation			
	P_D		
	CXL5506M	350	mW
	CXL5506P	480	mW

Recommended Operating Condition (Ta = 25°C)

Supply voltage	V_{DD}	5 ± 5%	V

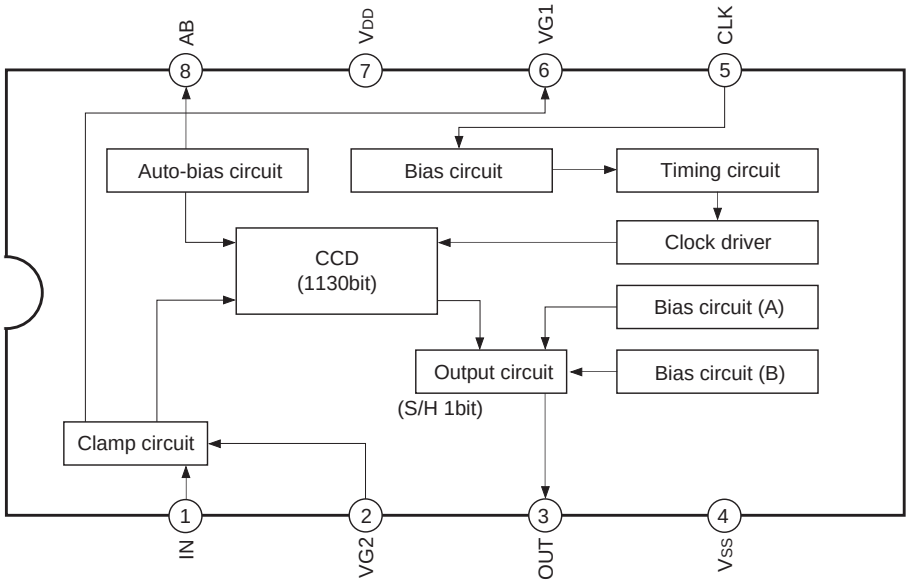
Recommended Clock Conditions (Ta = 25°C)

• Input clock amplitude	V_{CLK}	0.3 to 1.0 (0.5Vp-p typ.)	Vp-p
• Clock frequency	f_{CLK}	17.734475	MHz
• Input clock waveform	Sine wave		

Input Signal Amplitude

V_{SIG} 575mVp-p (Max.) (at internal clamp condition)

Blook Diagram and Pin Configuration (Top View)



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E90632B7X-PS

Pin Description

Pin No.	Symbol	I/O	Description	Impedance
1	IN	I	Signal input	> 10kΩ at no clamp
2 *	VG2	I	Gate bias 2 DC input	
3	OUT	O	Signal output	40 to 500Ω
4	V_{SS}	—	GND	
5	CLK	I	Clock input	> 10kΩ
6	VG1	O	Gate bias 1 DC output	
7	V_{DD}	—	Power supply (5V)	
8	AB	O	Auto-bias DC output	600 to 200kΩ

* Description of Pin 2 (VG2)

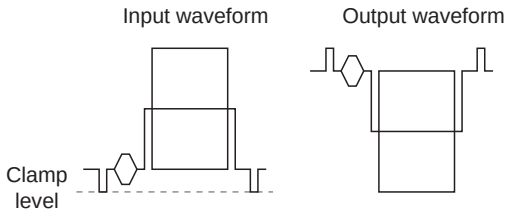
Control of input signal clamp condition

0V ..... Sync tip clamp condition

5V ..... Center bias condition

Center biased to approx. 2.1V by means of the IC internal resistance (approx. 10kΩ).

In this mode, the input signal is limited to APL 50% and the maximum input signal amplitude is 200mVp-p.



Electrical Characteristics

(Ta = 25°C, V_{DD} = 5V, f_{CLK} = 17.734475MHz, V_{CLK} = 500mVp-p, sine wave)
See "Electrical Characteristics Test Circuit"

Item	Symbol	Test condition	SW condition			Min.	Typ.	Max.	Unit	Note
			1	2	3					
Supply current	I_{DD}	—	a	a	—	10	19	28	mA	1
Low frequency gain	GL	200kHz, 500mVp-p, sine wave	a	a	b	–2	0	2	dB	2
Frequency response	fR	200kHz ⟷ 4.43MHz, 150mVp-p, sine wave	b ⇕ c	b	b	–2	–1	0	dB	3
Differential gain	DG	5-staircase wave (See Note 4)	d	a	c	0	3	5	%	4
Differential phase	DP	5-staircase wave (See Note 4)	d	a	c	0	3	5	degree	4
S/H pulse coupling	CP	No signal input	f	b	a	—	—	350	mVp-p	5
S/N ratio	SN	50% white video signal (See Note 6)	e	a	d	52	56	—	dB	6

Notes

(1) This is the IC supply current value during clock and signal input.

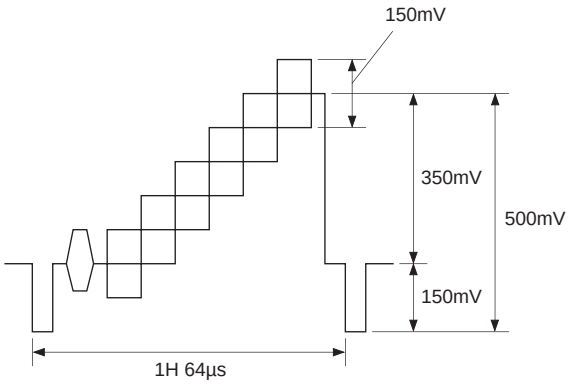
(2) GL is the output gain of OUT pin when a 500mVp-p, 200kHz sine wave is fed to IN pin.

$$GL = 20 \log \frac{\text{OUT pin output voltage [mVp-p]}}{\text{500 [mVp-p]}} \text{ [dB]}$$

(3) Indicates the dissipation at 4.43MHz in relation to 200kHz.
From the output voltage at OUT pin when a 150mVp-p, 200kHz sine wave is fed to IN pin, and from the output voltage at OUT pin when a 150mVp-p, 4.43MHz sine wave is fed to same, calculation is made according to the following formula.

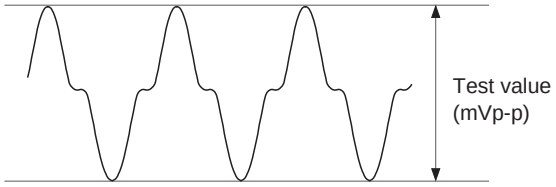
$$fR = 20 \log \frac{\text{OUT pin otuput voltage (4.43MHz) [mVp-p]}}{\text{OUT pin output voltage (200kHz) [mVp-p]}} \text{ [dB]}$$

(4) In figure below, differential gain (DG) and differential phase (DP) are tested with a vector scope when the 5-staircase wave is fed.

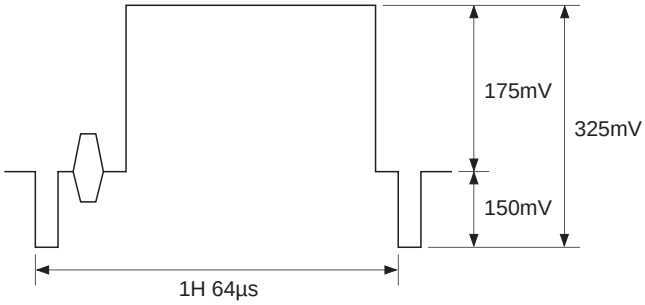


Input waveform

(5) The internal clock component to the output signal during no-signal input and the leakage of that high harmonic component are tested.



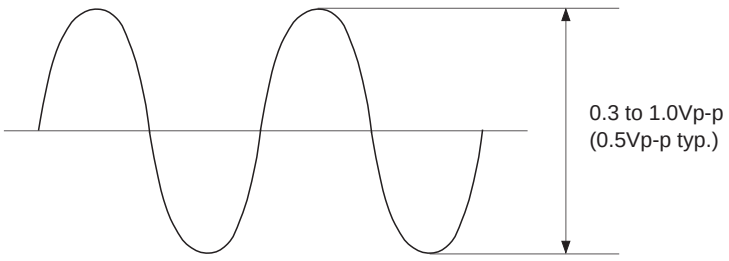
(6) S/N ratio during a 50% white video signal input shown in figure below is tested at a video noise meter, in BPF 100kHz to 5MHz, Sub Carrier Trap mode.



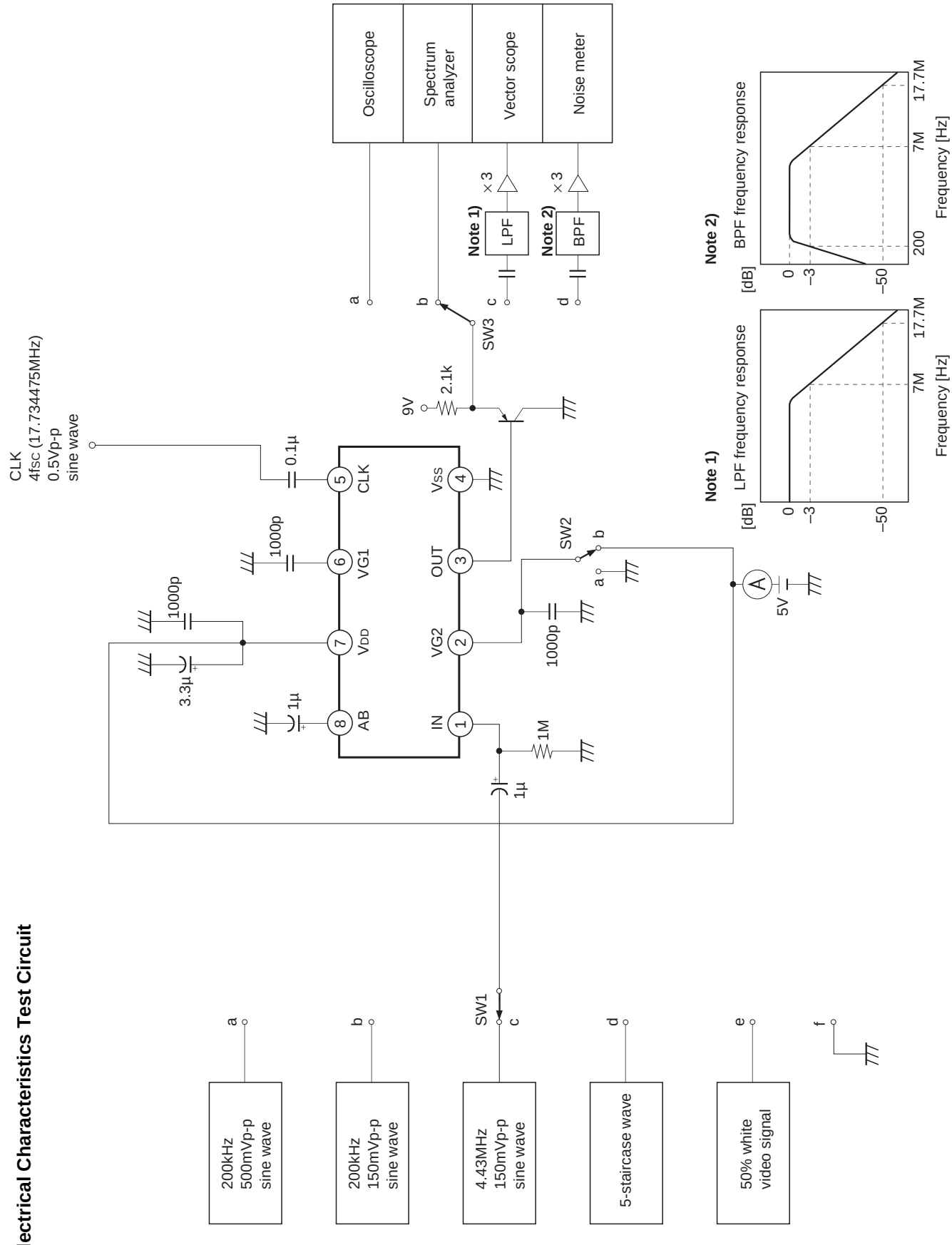
Input waveform

Clock

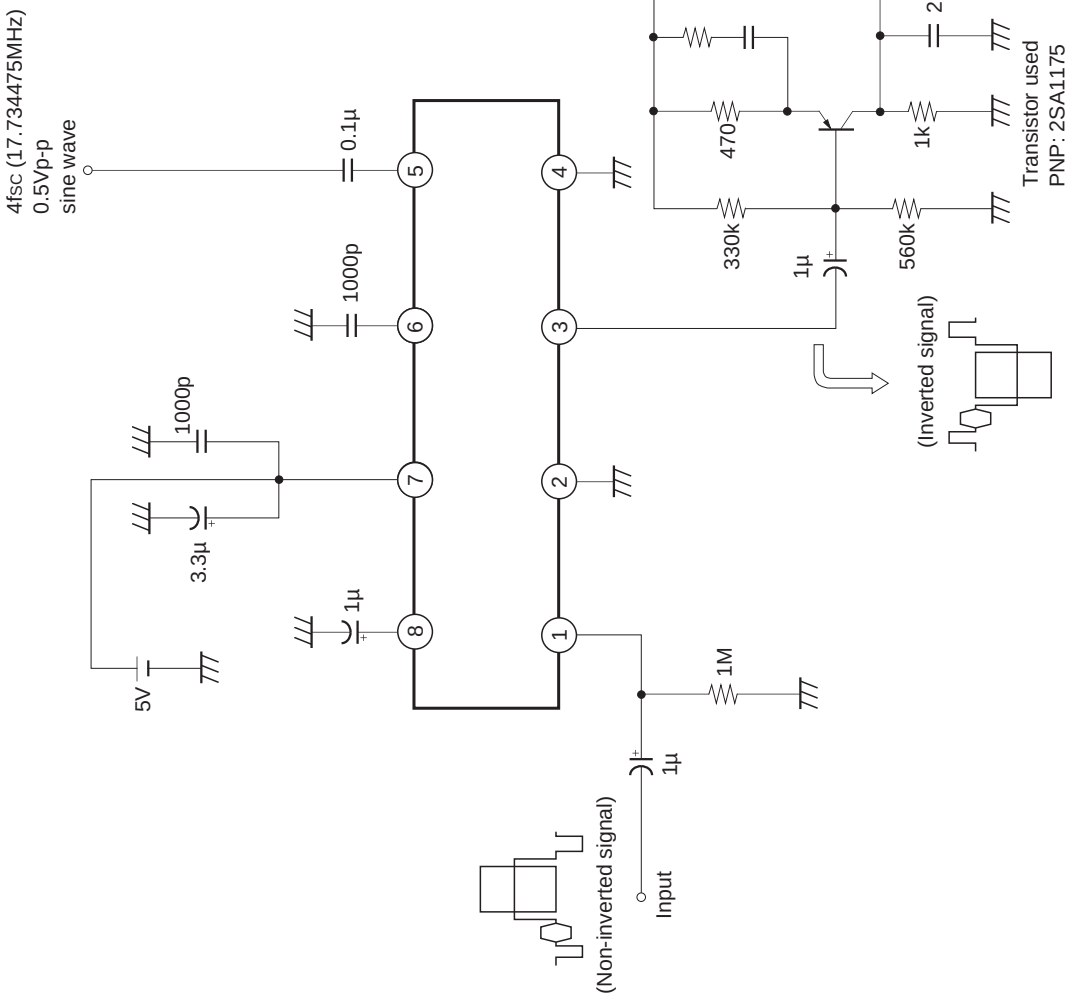
4fsc (17.734475MHz) sine wave



Electrical Characteristics Test Circuit



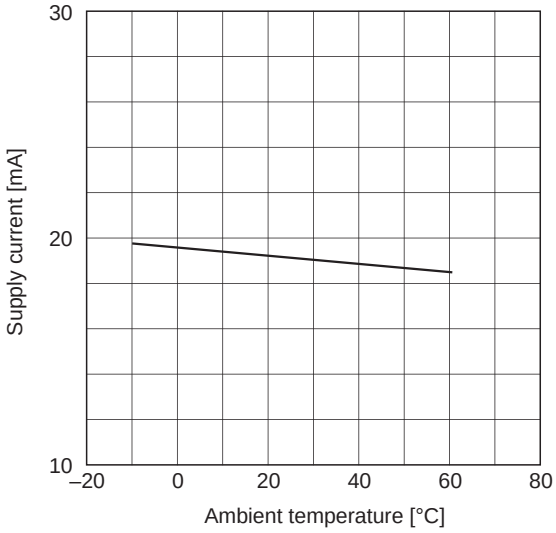
Application Circuit



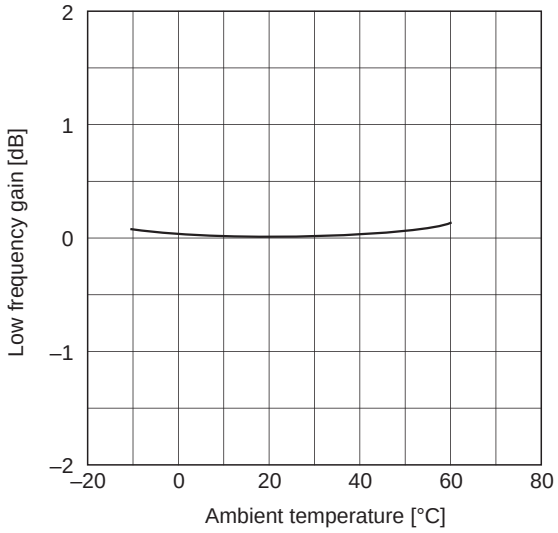
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

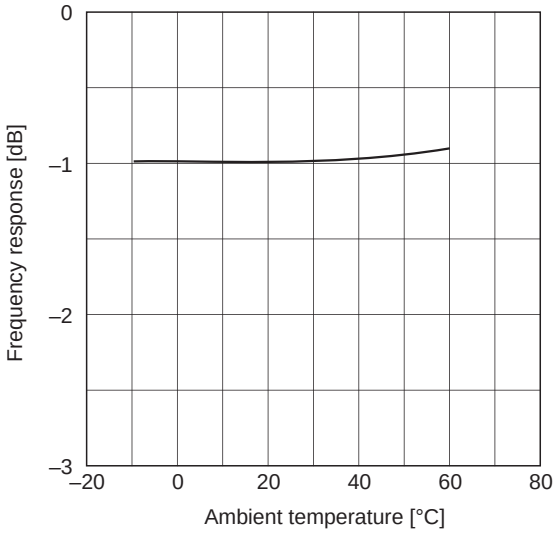
Supply current vs. Ambient temperature



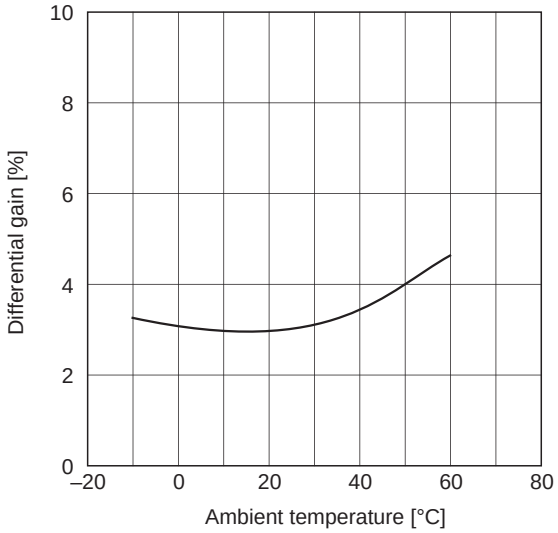
Low frequency gain vs. Ambient temperature



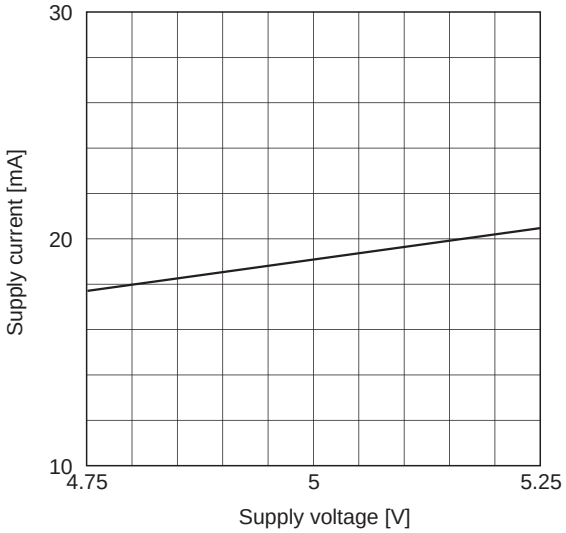
Frequency response vs. Ambient temperature



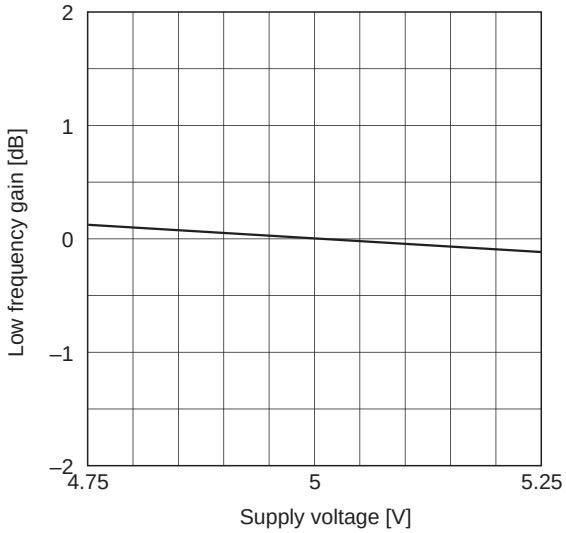
Differential gain vs. Ambient temperature



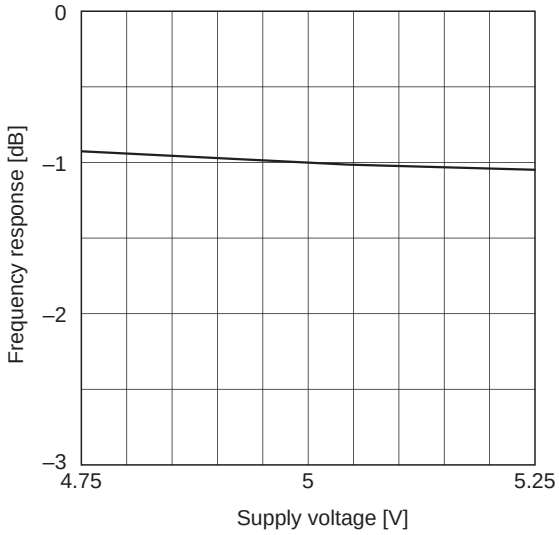
Supply current vs. Supply voltage



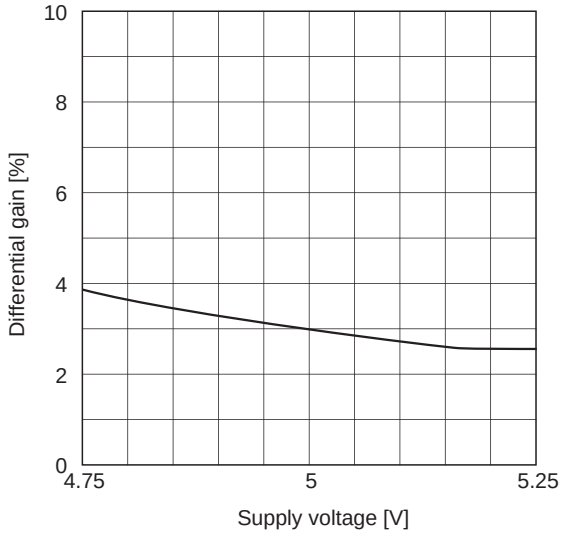
Low frequency gain vs. Supply voltage



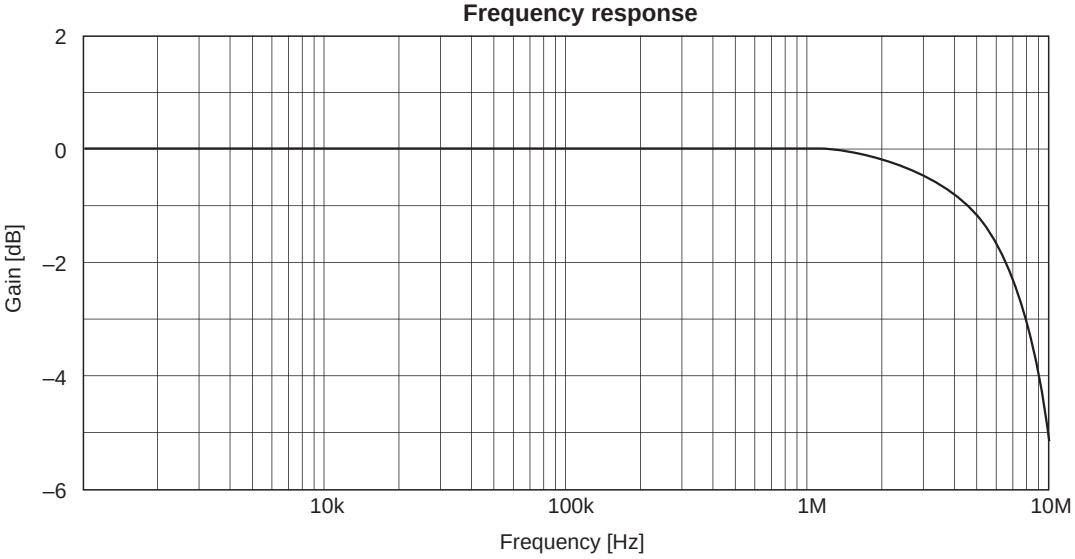
Frequency response vs.Supply voltage



Differential gain vs. Supply voltage



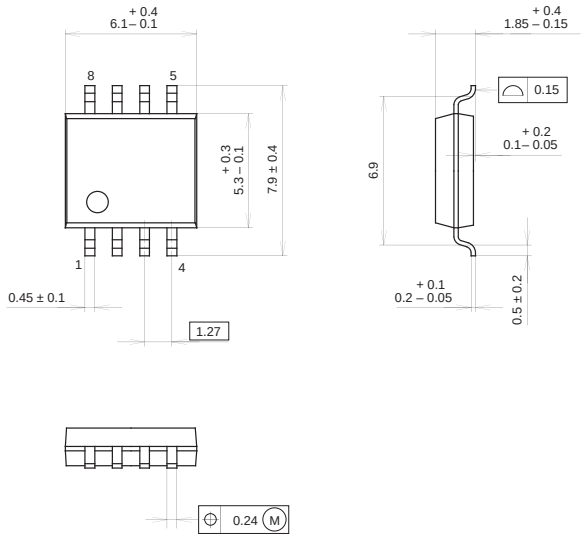
Frequency response



Package Outline Unit: mm

CXL5506M

8PIN SOP (PLASTIC)



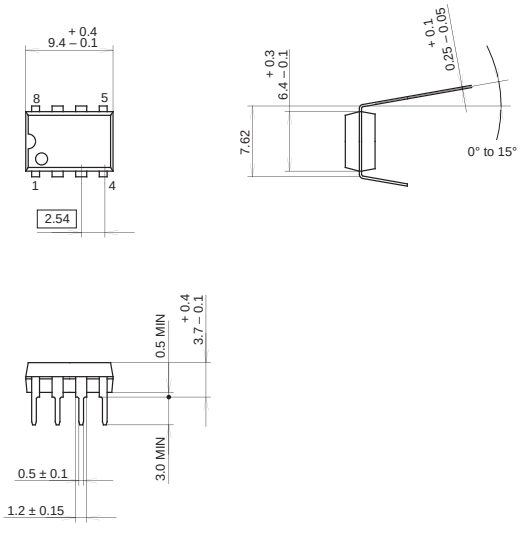
PACKAGE STRUCTURE

SONY CODE	SOP-8P-L01
EIAJ CODE	SOP008-P-0300
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

CXL5506P

8PIN DIP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	DIP-8P-01
EIAJ CODE	DIP008-P-0300
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.5g