ADC08L060 8-Bit, 10 MSPS to 60 MSPS, 0.65 mW/MSPS A/D Converter with Internal Sample-and-Hold

Check for Samples: ADC08L060

FEATURES

- **Single-ended input**
- **Internal sample-and-hold function**
- **Low voltage (single +3V) operation**
- **Small package**
- **Power-down feature**

KEY SPECIFICATIONS

- **Resolution 8 bits**
- **Conversion rate 60 MSPS**
- **DNL ±0.25 LSB (typ)**
- **INL +0.5/−0.2 LSB (typ)**
- **SNR (10.1 MHz) 48 dB (typ)**
- **ENOB (10.1 MHz) 7.6 bits (typ)**
- **THD (10.1 MHz) −57 dB (typ)**
- **Latency 5 Clock Cycles**
- **No missing codes Ensured**
- **Power Consumption**
  - **Operating 0.65 mW/MSPS (typ)**
  - **Power Down Mode 1.0 mW (typ)**

APPLICATIONS

- **Digital Imaging**
- **Set-top boxes**
- **Portable Instrumentation**
- **Communication Systems**
- **X-ray imaging**
- **Viterbi decoders**

DESCRIPTION

The ADC08L060 is a low-power, 8-bit, monolithic analog-to-digital converter with an on-chip track-and-hold circuit. Optimized for low cost, low power, small size and ease of use, this product operates at conversion rates of 10 MSPS to 60 MSPS while consuming just 0.65 mW per MHz of clock frequency, or 39 mW at 60 MSPS. Raising the PD pin puts the ADC08L060 into a Power Down mode where it consumes about 1 mW.

The unique architecture achieves 7.6 Effective Bits. The ADC08L060 is resistant to latch-up and the outputs are short-circuit proof. The top and bottom of the ADC08L060s reference ladder are available for connections, enabling a wide range of input possibilities. The digital outputs are TTL/CMOS compatible with a separate output power supply pin to support interfacing with 1.8V to 3V logic. The output coding is straight binary and the digital inputs (CLK and PD) are TTL/CMOS compatible.

The ADC08L060 is offered in a 24-lead plastic package (TSSOP) and is specified over the industrial temperature range of −40°C to +85°C.

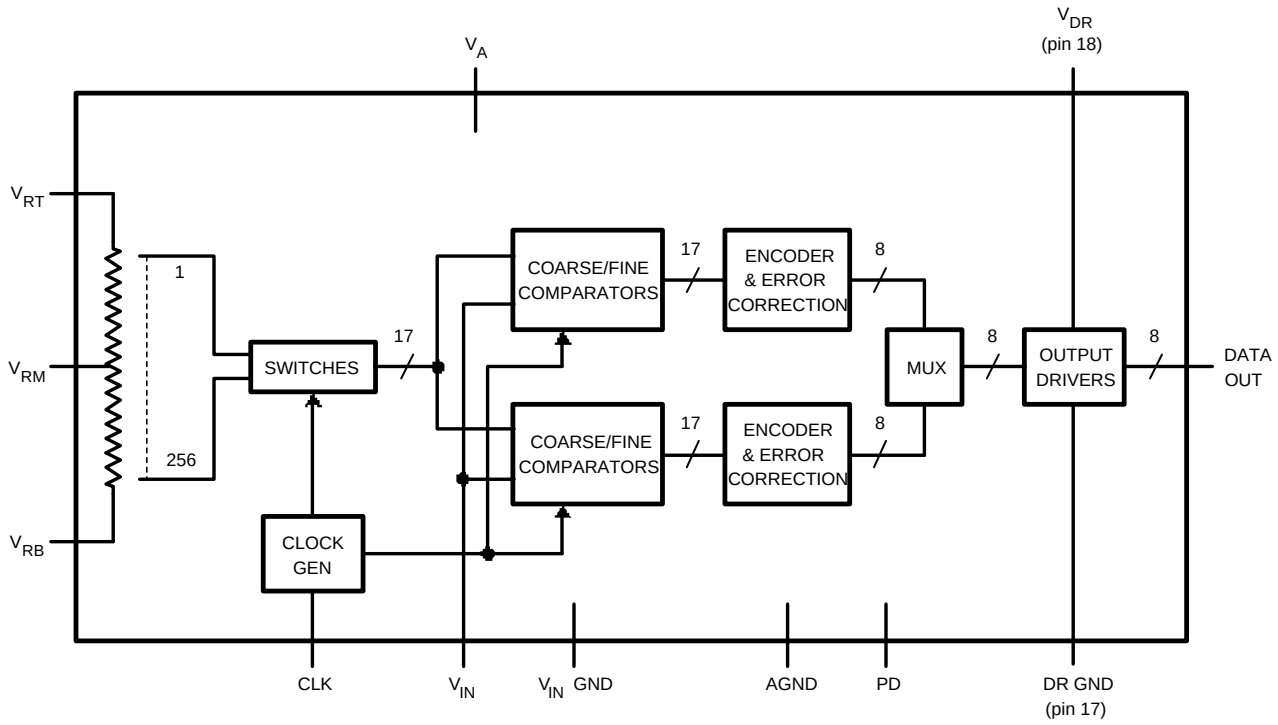
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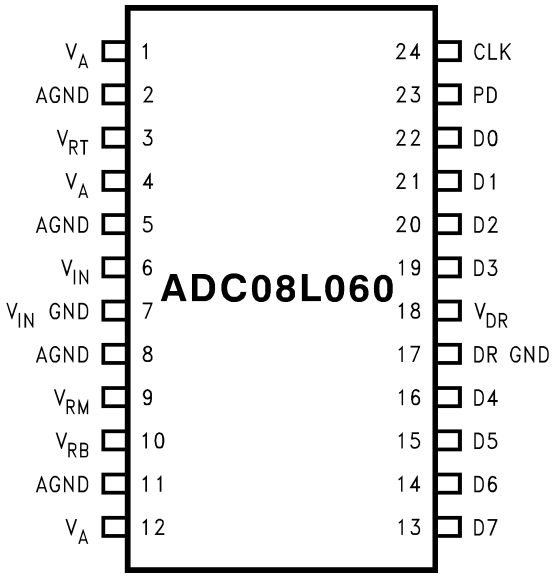
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Block Diagram

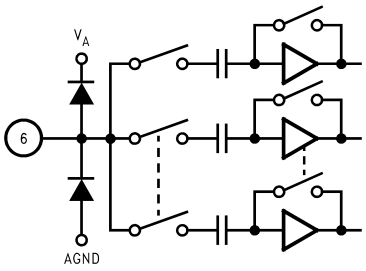
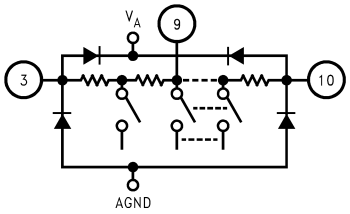
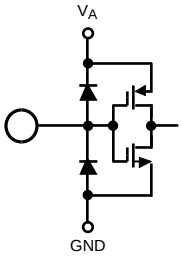
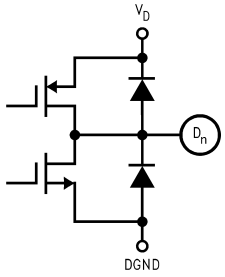


Pin Configuration



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Table 1. Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
6	V_{IN}		Analog signal input. Conversion range is V_{RB} to V_{RT}.
3	V_{RT}		Analog Input that is the high (top) side of the reference ladder of the ADC. Nominal range is 0.5V to V_A. Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.
9	V_{RM}		Mid-point of the reference ladder. This pin should be bypassed to a quiet point in the analog ground plane with a 0.1 µF capacitor.
10	V_{RB}		Analog Input that is the low side (bottom) of the reference ladder of the ADC. Nominal range is 0.0V to (V_{RT} – 0.5V). Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.
23	PD		Power Down input. When this pin is high, the converter is in the Power Down mode and the data output pins hold the last conversion result.
24	CLK		CMOS/TTL compatible digital clock Input. V_{IN} is sampled on the rising edge of CLK input.
13 thru 16 and 19 thru 22	D0–D7		Conversion data digital Output pins. D0 is the LSB, D7 is the MSB. Valid data is output after the rising edge of the CLK input.
7	V_{IN} GND		Reference ground for the single-ended analog input, V_{IN}.
1, 4, 12	V_A		Positive analog supply pin. Connect to a quiet voltage source of +3V. V_A should be bypassed with a 0.1 µF ceramic chip capacitor for each pin, plus one 10 µF capacitor. See Section 3.0 for more information.
18	V_{DR}		Power supply for the output drivers. If connected to V_A, decouple well from V_A.
17	DR GND		The ground return for the output driver supply.
2, 5, 8, 11	AGND		The ground return for the analog supply.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

Supply Voltage (V_A)	3.8V
Driver Supply Voltage (V_{DR})	V_A +0.3V
Voltage on Any Input or Output Pin	−0.3V to V_A
Reference Voltage (V_{RT}, V_{RB})	V_A to AGND
CLK, PD Voltage Range	−0.05V to (V_A + 0.05V)
Input Current at Any Pin (3)	±25 mA
Package Input Current (3)	±50 mA
Power Dissipation at T_A = 25°C	See (4)
ESD Susceptibility (5) Human Body Model Machine Model	 2500V 200V
Soldering Temperature, Infrared, 10 seconds (5)	235°C
Storage Temperature	−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such condition.
(2) All voltages are measured with respect to GND = AGND = DR GND = 0V, unless otherwise specified.
(3) When the input voltage at any pin exceeds the power supplies (that is, less than AGND or DR GND, or greater than V_A or V_{DR}), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.
(4) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A) / \theta_{JA}$. The values for maximum power dissipation will be reached only when this device is operated in a severe fault condition (e.g., when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.
(5) See AN-450, “Surface Mounting Methods and Their Effect on Product Reliability” (SNOA742).

Operating Ratings (1) (2)

Operating Temperature Range	−40°C ≤ T_A ≤ +85°C
Supply Voltage, V_A	+2.4V to +3.6V
Driver Supply Voltage, V_{DR}	+2.4V to V_A
Output Driver Voltage, V_{DR}	1.8V to V_A
Ground Difference |GND − DR GND|	0V to 300 mV
Upper Reference Voltage (V_{RT})	0.5V to (V_A −0.3V)
Lower Reference Voltage (V_{RB})	0V to (V_{RT} −0.5V)
V_{IN} Voltage Range	V_{RB} to V_{RT}

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such condition
(2) All voltages are measured with respect to GND = AGND = DR GND = 0V, unless otherwise specified.

Package Thermal Resistance

Package	θ_{JA}
24-Lead TSSOP	92°C/W

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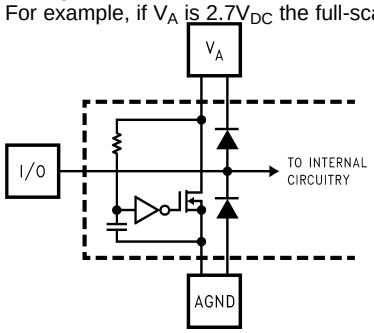
Converter Electrical Characteristics

The following specifications apply for $V_A = V_{DR} = +3.0V_{DC}$, $V_{RT} = +1.9V$, $V_{RB} = 0.3V$, $C_L = 10$ pF, $f_{CLK} = 60$ MHz at 50% duty cycle. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}**: all other limits $T_J = 25°C$ (1)(2) (3)

Symbol	Parameter	Conditions		Typical (4)	Limits (4)	Units (Limits)
DC ACCURACY						
INL	Integral Non-Linearity			+0.5 −0.2	**+1.9** **−1.35**	LSB (max) LSB (min)
DNL	Differential Non-Linearity			±0.25	**±0.90**	LSB (max)
	Missing Codes				**0**	(max)
FSE	Full Scale Error			3.0	**±13**	mV (max)
V_{OFF}	Zero Scale Offset Error			19	**27**	mV (max)
ANALOG INPUT AND REFERENCE CHARACTERISTICS						
V_{IN}	Input Voltage			1.6	**V_{RB}**	V (min)
					V_{RT}	V (max)
C_{IN}	V_{IN} Input Capacitance	V_{IN} = 0.75V +0.5 Vrms	(CLK LOW)	3		pF
			(CLK HIGH)	4		pF
R_{IN}	R_{IN} Input Resistance			>1		MΩ
BW	Full Power Bandwidth			270		MHz
V_{RT}	Top Reference Voltage			1.9	**V_A**	V (max)
					0.5	V (min)
V_{RB}	Bottom Reference Voltage			0.3	**V_{RT} − 0.5**	V (max)
					0	V (min)
V_{RT} - V_{RB}	Reference Delta			1.6	2.3	V (max)
					1.0	V (min)
R_{REF}	Reference Ladder Resistance	V_{RT} to V_{RB}		720	**590**	Ω (min)
					1070	Ω (max)
I_{ref}	Reference Ladder Current	V_{RT} to V_{RB}		2.2	**1.5**	mA (min)
					2.7	mA (max)

(1) The Electrical characteristics tables list ensured specifications under the listed Recommended Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations for room temperature only and are not ensured.

(2) The analog inputs are protected as shown below. Input voltage magnitudes up to V_A + 300 mV or to 300 mV below GND will not damage this device. However, errors in the A/D conversion can occur if the input goes above V_{DR} or below GND by more than 100 mV. For example, if V_A is $2.7V_{DC}$ the full-scale input voltage must be ≤$2.8V_{DC}$ to ensure accurate conversions.



(3) To ensure accuracy, it is required that V_A and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors.

(4) Typical figures are at $T_J = 25°C$, and represent most likely parametric norms at specific conditions at the time of product characterization and are not ensured. Test limits are specifid to TI's AOQL (Average Outgoing Quality Level).

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Converter Electrical Characteristics (continued)

The following specifications apply for $V_A = V_{DR} = +3.0V_{DC}$, $V_{RT} = +1.9V$, $V_{RB} = 0.3V$, $C_L = 10$ pF, $f_{CLK} = 60$ MHz at 50% duty cycle. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}**: all other limits $T_J = 25°C$ (1)(2) (3)

Symbol	Parameter	Conditions	Typical (4)	Limits (4)	Units (Limits)
CLK, PD DIGITAL INPUT CHARACTERISTICS					
V_{IH}	Logical High Input Voltage	$V_{DR} = V_A = 3.6V$		**2.0**	V (min)
V_{IL}	Logical Low Input Voltage	$V_{DR} = V_A = 2.7V$		**0.8**	V (max)
I_{IH}	Logical High Input Current	$V_{IH} = V_{DR} = V_A = 3.6V$	10		nA
I_{IL}	Logical Low Input Current	$V_{IL} = 0V$, $V_{DR} = V_A = 2.7V$	−50		nA
C_{IN}	Logic Input Capacitance		3		pF
DIGITAL OUTPUT CHARACTERISTICS					
V_{OH}	High Level Output Voltage	$V_A = V_{DR} = 2.7V$, $I_{OH} = -400$ µA	2.6	**2.4**	V (min)
V_{OL}	Low Level Output Voltage	$V_A = V_{DR} = 2.7V$, $I_{OL} = 1.0$ mA	0.4	**0.5**	V (max)
DYNAMIC PERFORMANCE					
ENOB	Effective Number of Bits	$f_{IN} = 10.1$ MHz, $V_{IN} = FS - 0.25$ dB	7.6	**6.9**	Bits (min)
		$f_{IN} = 29$ MHz, $V_{IN} = FS - 0.25$ dB	7.4		Bits
SINAD	Signal-to-Noise & Distortion	$f_{IN} = 10.1$ MHz, $V_{IN} = FS - 0.25$ dB	47.4	**43.3**	dB (min)
		$f_{IN} = 29$ MHz, $V_{IN} = FS - 0.25$ dB	46.1		dB
SNR	Signal-to-Noise Ratio	$f_{IN} = 10.1$ MHz, $V_{IN} = FS - 0.25$ dB	48	**44.5**	dB (min)
		$f_{IN} = 29$ MHz, $V_{IN} = FS - 0.25$ dB	47.2		dB
SFDR	Spurious Free Dynamic Range	$f_{IN} = 10.1$ MHz, $V_{IN} = FS - 0.25$ dB	59.1		dBc
		$f_{IN} = 29$ MHz, $V_{IN} = FS - 0.25$ dB	54.5		dBc
THD	Total Harmonic Distortion	$f_{IN} = 10.1$ MHz, $V_{IN} = FS - 0.25$ dB	−56.9		dBc
		$f_{IN} = 29$ MHz, $V_{IN} = FS - 0.25$ dB	−53.3		dBc
HD2	2nd Harmonic Distortion	$f_{IN} = 10.1$ MHz, $V_{IN} = FS - 0.25$ dB	-61.1		dBc
		$f_{IN} = 29$ MHz, $V_{IN} = FS - 0.25$ dB	−54.9		dBc
HD3	3rd Harmonic Distortion	$f_{IN} = 10.1$ MHz, $V_{IN} = FS - 0.25$ dB	−64.2		dBc
		$f_{IN} = 29$ MHz, $V_{IN} = FS - 0.25$ dB	−63.1		dBc
IMD	Intermodulation Distortion	$f_1 = 11$ MHz, $V_{IN} = FS - 6.25$ dB $f_2 = 12$ MHz, $V_{IN} = FS - 6.25$ dB	−55		dBc
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	DC Input	13	**15.9**	mA (max)
		$f_{IN} = 10$ MHz, $V_{IN} = FS - 3$ dB	14		mA
DRI_D	Output Driver Supply Current	DC Input	0.04	**0.2**	mA (max)
		$f_{IN} = 10$ MHz, $V_{IN} = FS - 3$ dB (5)	4.2		mA
$I_A + DRI_D$	Total Operating Current	DC Input	13	**16.1**	mA (max)
		$f_{IN} = 10$ MHz, $V_{IN} = FS - 3$ dB, PD = Low	18.2		mA
		CLK Low, PD = Hi	0.33		mA
PC	Power Consumption	DC Input	39	**48.3**	mW (max)
		$f_{IN} = 10$ MHz, $V_{IN} = FS - 3$ dB, PD = Low	53		mW
		CLK Low, PD = Hi	1		mW
$PSRR_1$	Power Supply Rejection Ratio	FSE change with 2.7V to 3.3V change in V_A	−51		dB
$PSRR_2$	Power Supply Rejection Ratio	SNR reduction with 200 mV at 1MHz on supply	45		dB

(5) I_{DR} is the current consumed by the switching of the output drivers and is primarily determined by the load capacitance on the output pins, the supply voltage, V_{DR}, and the rate at which the outputs are switching (which is signal dependent), $I_{DR} = V_{DR} (C_O \times f_O + C_1 \times f_1 + \ldots + C_{71} \times f_7)$ where V_{DR} is the output driver power supply voltage, C_n is the total capacitance on any given output pin, and f_n is the average frequency at which that pin is toggling.

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Converter Electrical Characteristics (continued)

The following specifications apply for $V_A = V_{DR} = +3.0V_{DC}$, $V_{RT} = +1.9V$, $V_{RB} = 0.3V$, $C_L = 10$ pF, $f_{CLK} = 60$ MHz at 50% duty cycle. **Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}**: all other limits $T_J = 25°C$ (1)(2) (3)

Symbol	Parameter	Conditions	Typical (4)	Limits (4)	Units (Limits)
AC ELECTRICAL CHARACTERISTICS					
f_{C1}	Maximum Conversion Rate		80	**60**	MHz (min)
f_{C2}	Minimum Conversion Rate		10		MHz
t_{CL}	Minimum Clock Low Time		0.62		ns (min)
t_{CH}	Minimum Clock High Time		0.62		ns (min)
DC	Clock Duty Cycle		5 95		%(min) %(max)
t_{OH}	Output Hold Time	CLK to Data Invalid	5.2		ns
t_{OD}	Output Delay	CLK to Data Transition	7.1	**5.0**	ns (min)
				9.4	ns (max)
	Pipeline Delay (Latency)		5		Clock Cycles
t_{AD}	Sampling (Aperture) Delay	CLK Rise to Acquisition of Data	2.6		ns
t_{AJ}	Aperture Jitter		2		ps rms

Specification Definitions

APERTURE (SAMPLING) DELAY is that time required after the rise of the clock input for the sampling switch to open. The Sample/Hold circuit effectively stops capturing the input signal and goes into the "hold" mode t_{AD} after the clock goes high.

APERTURE JITTER is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

CLOCK DUTY CYCLE is the ratio of the time that the clock wave form is at a logic high to the total time of one clock period.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. Measured at 60 MSPS with a ramp input.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD – 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

FULL-SCALE ERROR is a measure of how far the last code transition is from the ideal 1½ LSB below V_{RT} and is defined as:

$$V_{max} + 1.5\ LSB - V_{RT} \quad (1)$$

where V_{max} is the voltage at which the transition to the maximum (full scale) code occurs.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from zero scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value. The end point test method is used. Measured at 60 MSPS with a ramp input.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. it is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is

$$(V_{RT} - V_{RB}) / 2^n \quad (2)$$

where "n" is the ADC resolution, which is 8 in the case of the ADC08L060.

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MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

OUTPUT DELAY is the time delay after the rising edge of the input clock before the data update is present at the output pins.

OUTPUT HOLD TIME is the length of time that the output data is valid after the rise of the input clock.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. New data is available at every clock cycle, but the data lags the conversion by the Pipeline Delay plus the Output Delay.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well the ADC rejects a change in the power supply voltage. For the ADC08L060, PSRR1 is the ratio of the change in Full-Scale Error that results from a change in the d.c. power supply voltage, expressed in dB. PSRR2 is a measure of how well an a.c. signal riding upon the power supply is rejected and is here defined as

$$PSRR2 = 20Log\left(4\sqrt{10^{\frac{-SNR1}{10}} - 10^{\frac{-SNR0}{10}}}\right) \quad (3)$$

where SNR0 is the SNR measured with no noise or signal on the supply lines and SNR1 is the SNR measured with a 1 MHz, 200 mV_{P-P} signal riding upon the supply lines.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$THD = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}} \quad (4)$$

where A_{f1} is the RMS power of the fundamental (output) frequency and A_{f2} through A_{f10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

ZERO SCALE OFFSET ERROR is the error in the input voltage required to cause the first code transition. It is defined as

$$V_{OFF} = V_{ZT} - V_{RB} \quad (5)$$

where V_{ZT} is the first code transition input voltage.

2nd HARMONIC DISTORTION (2nd HARM) is the difference, expressed in dB, between the rms power in the output fundamental frequency and the power in its 2nd harmonic at the output.

3rd HARMONIC DISTORTION (3rd HARM) is the difference, expressed in dB, between the rms power in the output fundamental frequency and the power in its 3rd harmonic at the output.

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Timing Diagram

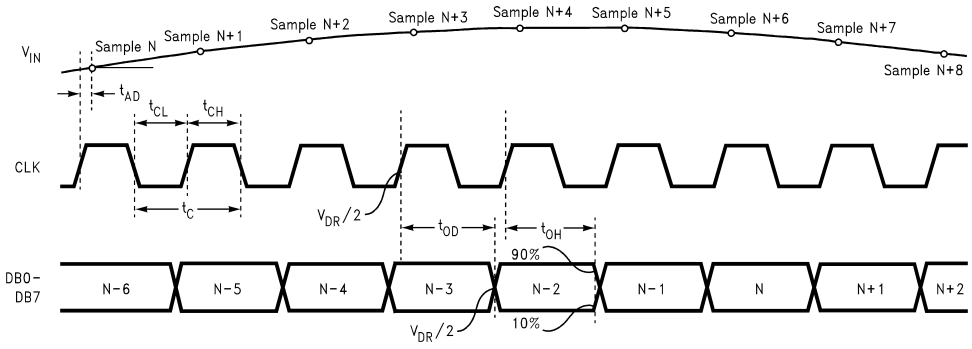


Figure 1. ADC08L060 Timing Diagram

Typical Performance Characteristics

$V_A = V_{DR} = 3V$, $f_{CLK} = 60$ MHz, $f_{IN} = 10$ MHz, unless otherwise stated

INL

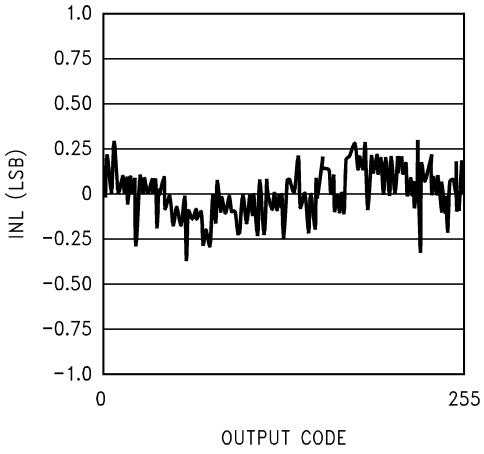


Figure 2.

INL vs Temperature

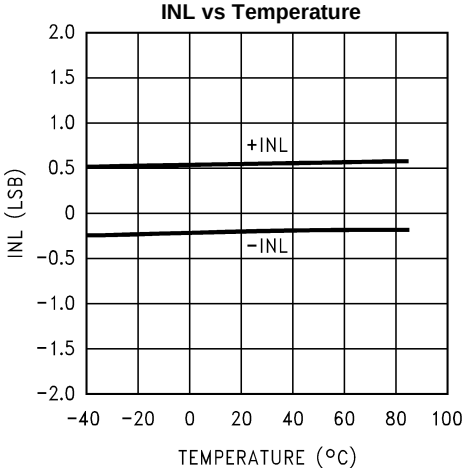


Figure 3.

INL vs Supply Voltage, V_A

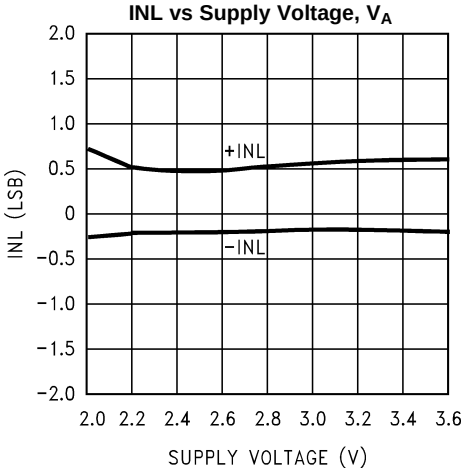


Figure 4.

INL vs Sample Rate

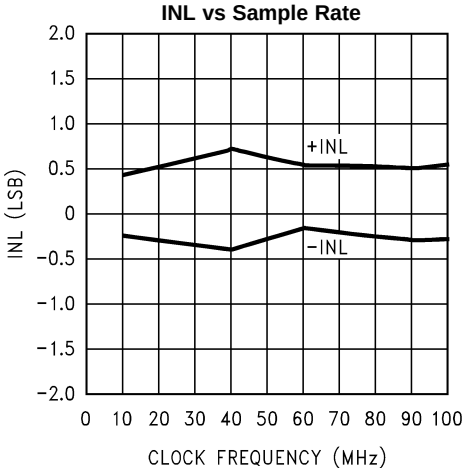


Figure 5.

INL vs Clock Duty Cycle

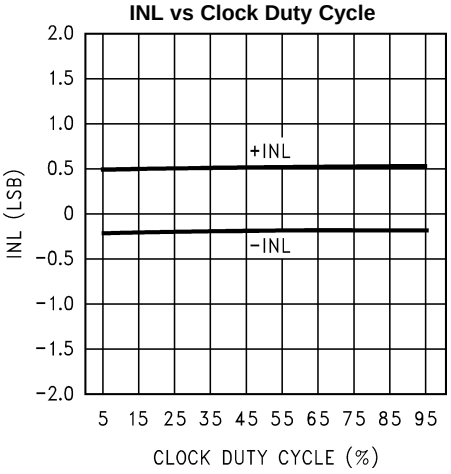


Figure 6.

DNL

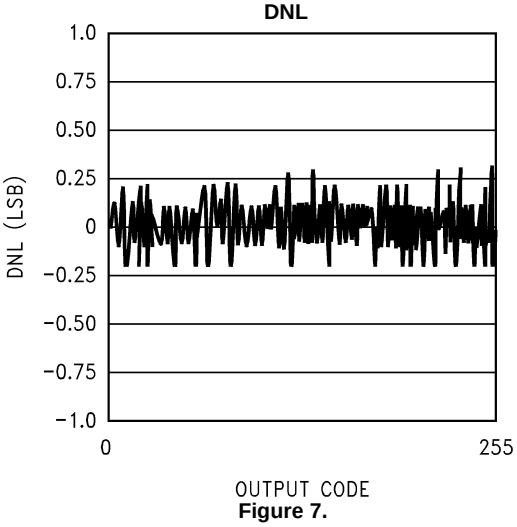


Figure 7.

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Typical Performance Characteristics (continued)

$V_A = V_{DR} = 3V$, $f_{CLK} = 60$ MHz, $f_{IN} = 10$ MHz, unless otherwise stated

DNL vs Temperature

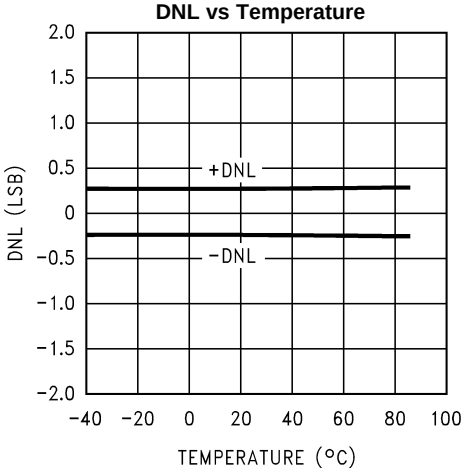


Figure 8.

DNL vs Supply Voltage, V_A

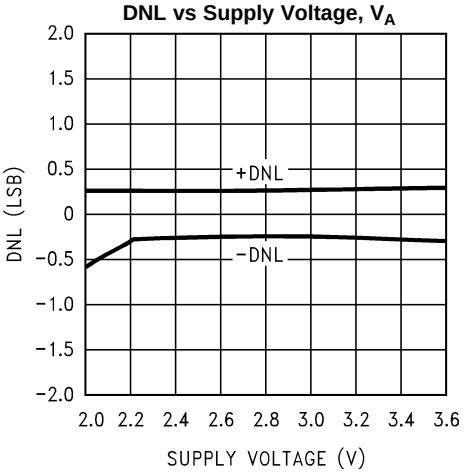


Figure 9.

DNL vs Sample Rate

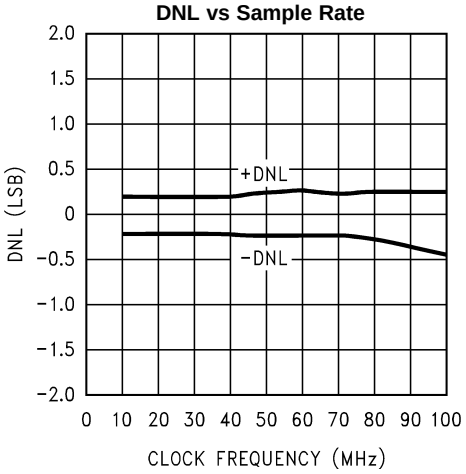


Figure 10.

DNL vs Clock Duty Cycle

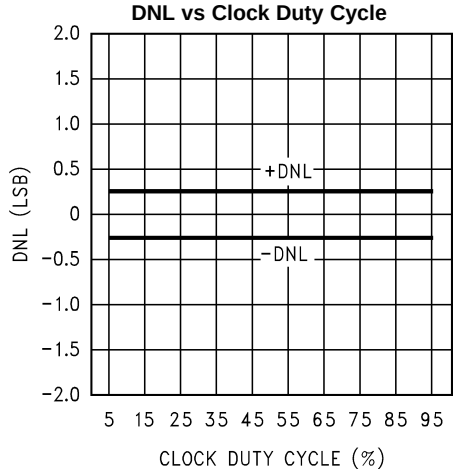


Figure 11.

SNR, SINAD and SFDR vs Temperature

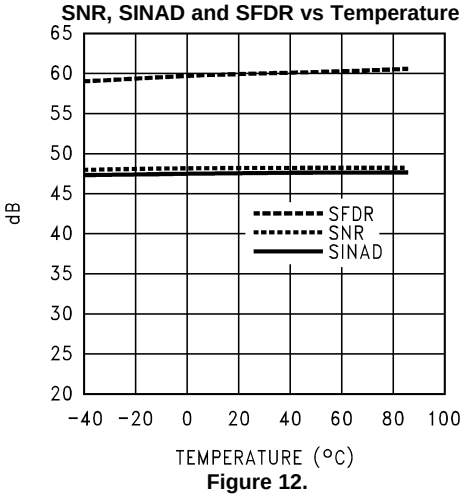


Figure 12.

SNR, SINAD and SFDR vs Supply Voltage, V_A

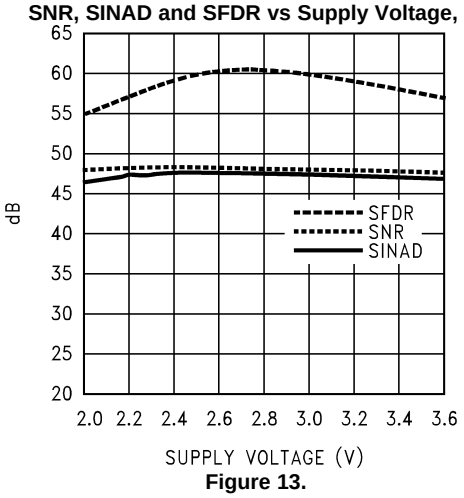


Figure 13.

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Typical Performance Characteristics (continued)

$V_A = V_{DR} = 3V$, $f_{CLK} = 60$ MHz, $f_{IN} = 10$ MHz, unless otherwise stated

SNR, SINAD and SFDR vs Sample Rate

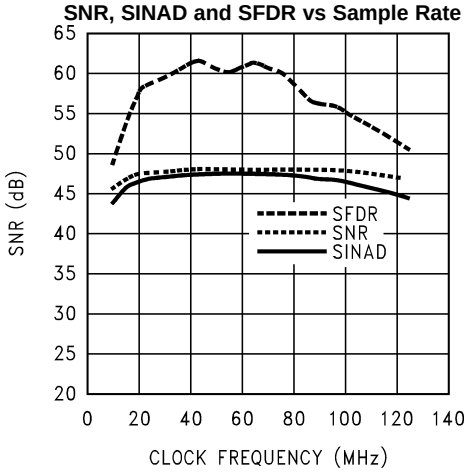


Figure 14.

SNR, SINAD and SFDR vs Input Frequency

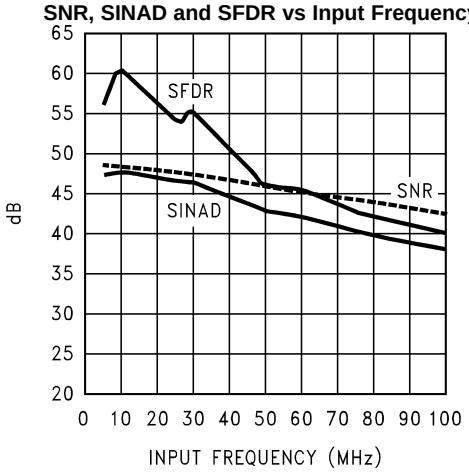


Figure 15.

SNR, SINAD and SFDR vs Clock Duty Cycle

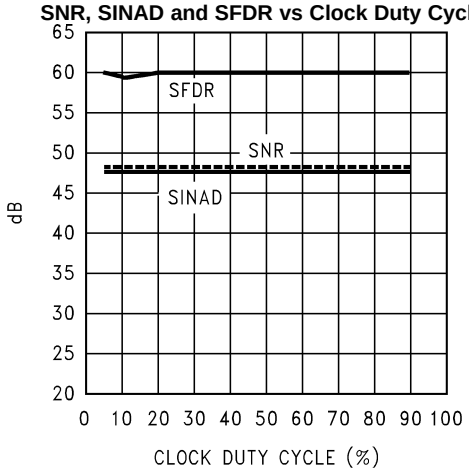


Figure 16.

Distortion vs Temperature

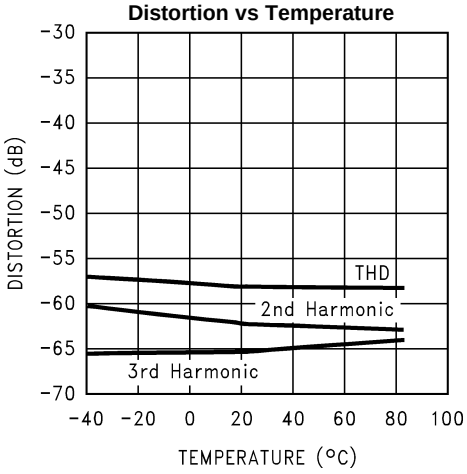


Figure 17.

Distortion vs Supply Voltage, V_A

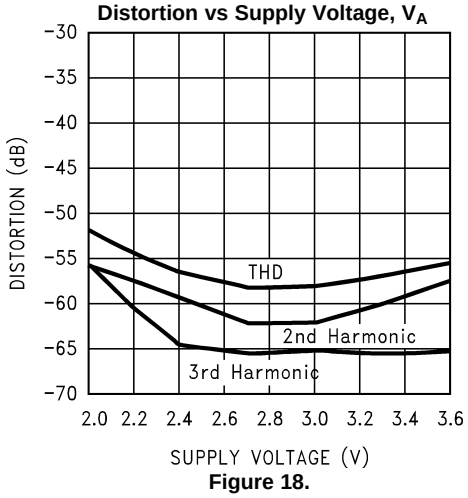


Figure 18.

Distortion vs Sample Rate

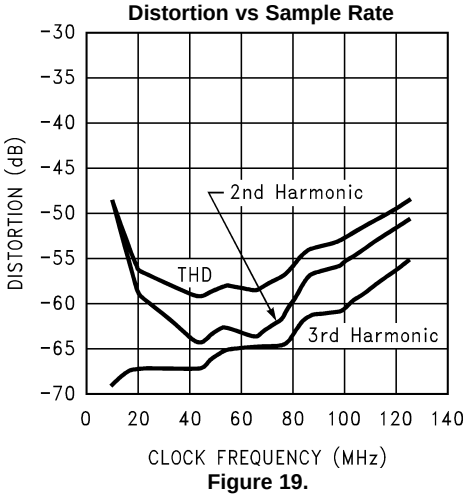


Figure 19.

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Typical Performance Characteristics (continued)

$V_A = V_{DR} = 3V$, $f_{CLK} = 60$ MHz, $f_{IN} = 10$ MHz, unless otherwise stated

Distortion vs Input Frequency

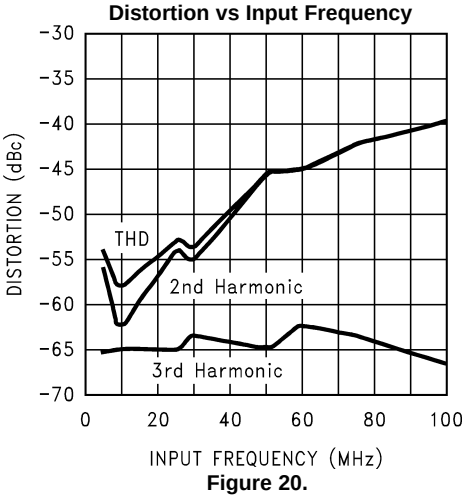


Figure 20.

Distortion vs Clock Duty Cycle

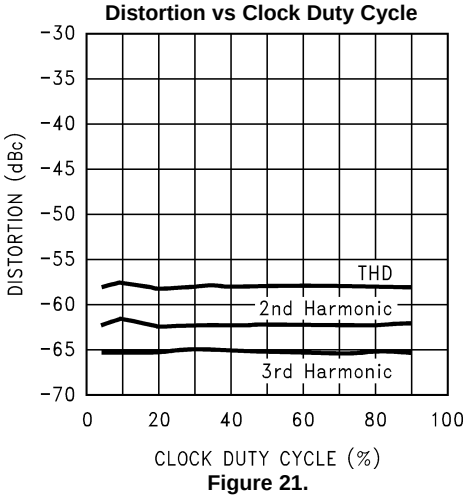


Figure 21.

Power Consumption (Active) vs. Sample Rate (f_{IN} = d.c.)

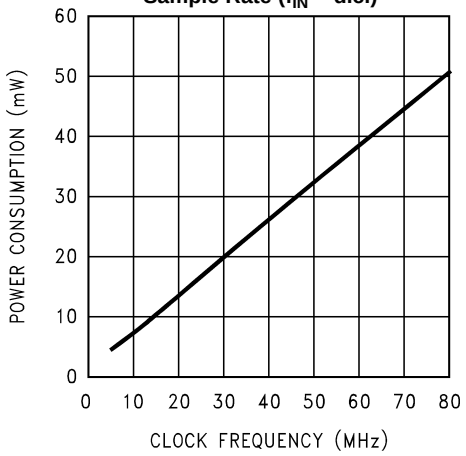


Figure 22.

Power Consumption (Active) vs. Sample Rate (f_{IN} = d.c.)

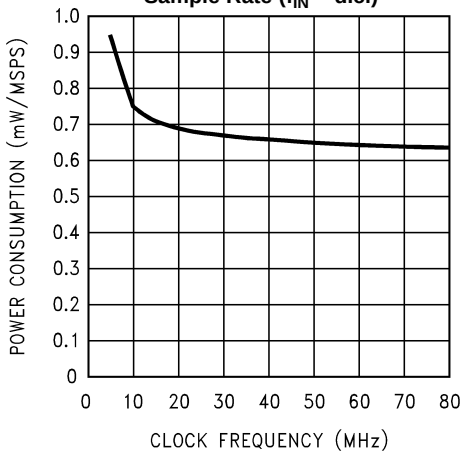


Figure 23.

Power Consumption (Active) vs. Sample Rate (f_{IN} = 1 MHz)

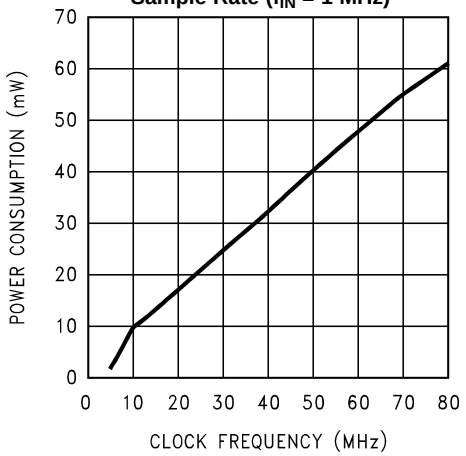


Figure 24.

Power Consumption (Active) vs. Sample Rate (f_{IN} = 1 MHz)

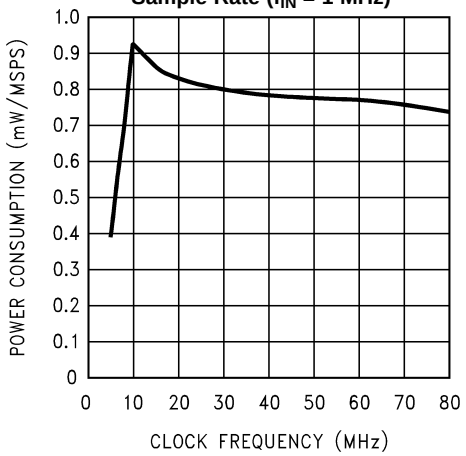


Figure 25.

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Typical Performance Characteristics (continued)

$V_A = V_{DR} = 3V$, $f_{CLK} = 60$ MHz, $f_{IN} = 10$ MHz, unless otherwise stated

Spectral Response @ f_{IN} = 10 MHz

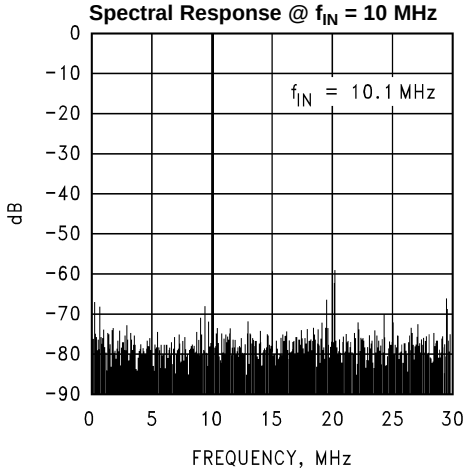


Figure 26.

Spectral Response @ f_{IN} = 29 MHz

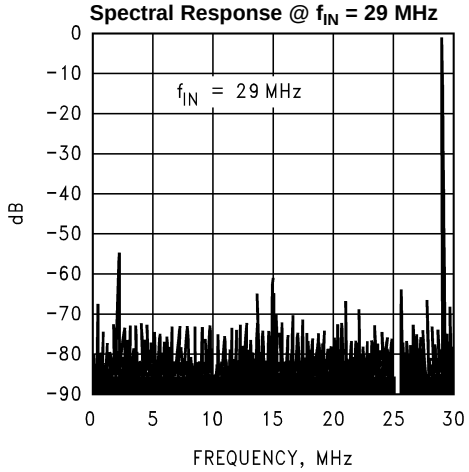


Figure 27.

Spectral Response @ f_{IN} = 75 MHz

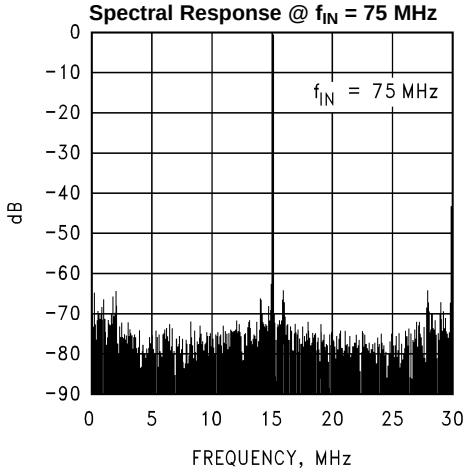


Figure 28.

Spectral Response @ f_{IN} = 98.9 MHz

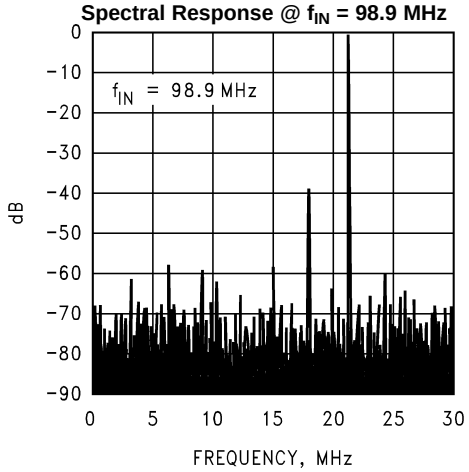


Figure 29.

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FUNCTIONAL DESCRIPTION

The ADC08L060 uses a unique architecture that achieves over 7 effective bits at input frequencies up to and beyond Nyquist.

The analog input signal that is within the voltage range set by V_{RT} and V_{RB} is digitized to eight bits. Input voltages below V_{RB} will cause the output word to consist of all zeroes. Input voltages above V_{RT} will cause the output word to consist of all ones.

Incorporating a switched capacitor bandgap, the ADC08L060 exhibits a power consumption that is proportional to frequency, limiting power consumption to what is needed at the clock rate that is used. This and its excellent performance over a wide range of clock frequencies makes it an ideal choice as a single ADC for many 8-bit needs.

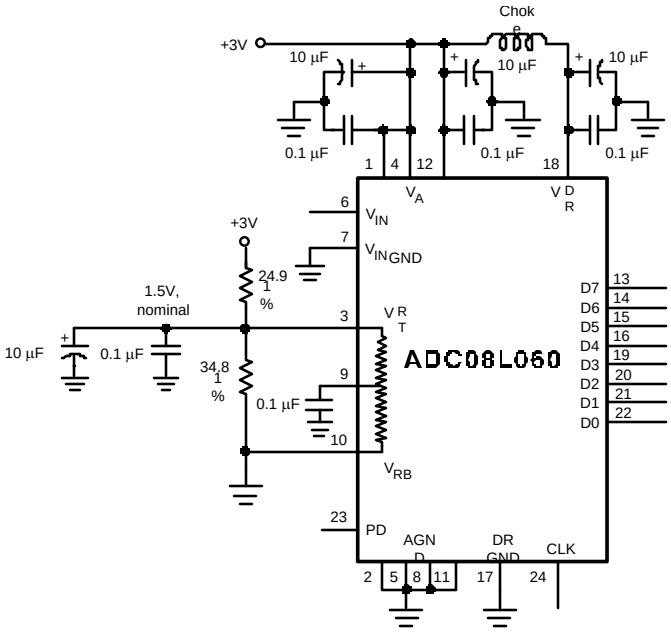
Data is acquired at the rising edge of the clock and the digital equivalent of that data is available at the digital outputs 5 clock cycles plus t_{OD} later. The ADC08L060 will convert as long as an adequate clock signal is present at pin 24. The output coding is straight binary.

The device is in the active state when the Power Down pin (PD) is low. When the PD pin is high, the device is in the power down mode, where the output pins hold the last conversion before the PD pin went high and the device consumes about 1.4 mW. Holding the clock input low will further reduce the power consumption in the power down mode to about 1 mW

APPLICATION INFORMATION

REFERENCE INPUTS

The reference inputs V_{RT} and V_{RB} are the top and bottom of the reference ladder, respectively. Input signals between these two voltages will be digitized to 8 bits. External voltages applied to the reference input pins should be within the range specified in the Operating Ratings table. Any device used to drive the reference pins should be able to source sufficient current into the V_{RT} pin and sink sufficient current from the V_{RB} pin to keep these voltages stable.



A. Because of the ladder and external resistor tolerances, the reference voltage of this circuit can vary too much for some applications.

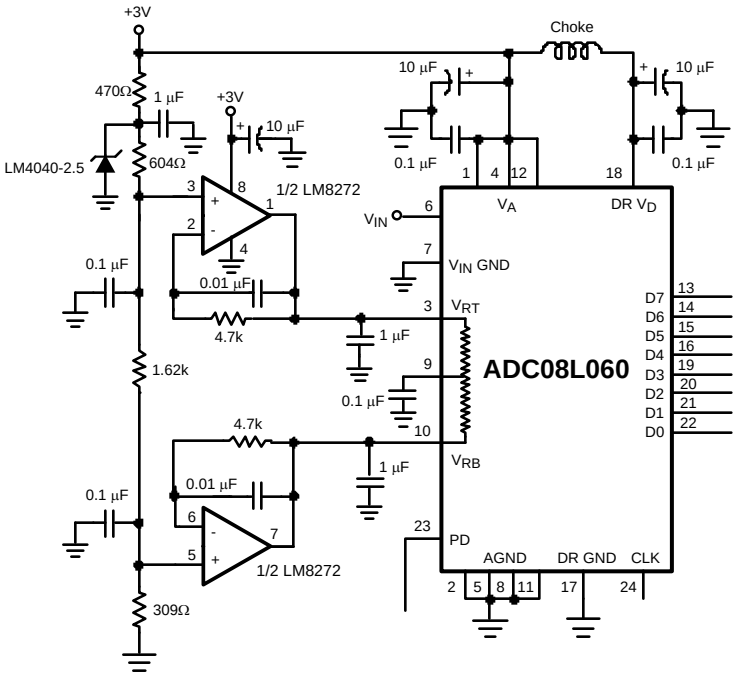
Figure 30. Simple, Low Component Count Reference Biasing

The reference bias circuit of Figure 30 is very simple and the performance is adequate for many applications. However, circuit tolerances will lead to a wide reference voltage range. Better reference stability can be achieved by driving the reference pins with low impedance sources.

The circuit of Figure 31 will allow a more accurate setting of the reference voltages. The upper amplifier must be able to source the reference current as determined by the value of the reference resistor and the value of (V_{RT} - V_{RB}). The lower amplifier must be able to sink this reference current. Both should be stable with a capacitive load. The LM8272 was chosen because of its rail-to-rail input and output capability, its high current output and its ability to drive large capacitance loads. Of course, the divider resistors at the amplifier input could be changed to suit your reference voltage needs, or the divider can be replaced with potentiometers for precise settings. The bottom of the ladder (V_{RB}) may simply be returned to ground if the minimum input signal excursion is 0V. Be sure that the driving source can source sufficient current into the V_{RT} pin and sink enough current from the V_{RB} pin to keep these pins stable.

V_{RT} should always be more positive than V_{RB} by the minimum V_{RT} - V_{RB} difference in the Electrical Characteristics table to minimize noise. Furthermore, the difference between V_{RT} and V_{RB} should not exceed the maximum value specified in the Electrical Characteristics table to avoid signal distortion.

The V_{RM} pin is the center of the reference ladder and should be bypassed to a quiet point in the analog ground plane with a 0.1 µF capacitor. DO NOT allow this pin to float.



A. Driving the reference to force desired values requires driving with a low impedance source.

Figure 31. Setting of Reference Voltages

THE ANALOG INPUT

The analog input of the ADC08L060 is a switch followed by an integrator. The input capacitance changes with the clock level, appearing as 3 pF when the clock is low, and 4 pF when the clock is high. The sampling nature of the analog input causes current spikes that result in voltage spikes at the analog input pin. Any circuit used to drive the analog input must be able to drive that input and to settle within the clock low time. The LMH6702 has been found to be a good amplifier to drive the ADC08L060.

Figure 32 shows an example of an input circuit using the LMH6702. Any input amplifier should incorporate some gain as operational amplifiers exhibit better phase margin and transient response with gains above 2 or 3 than with unity gain. If an overall gain of less than 3 is required, attenuate the input and operate the amplifier at a higher gain, as shown in Figure 32.

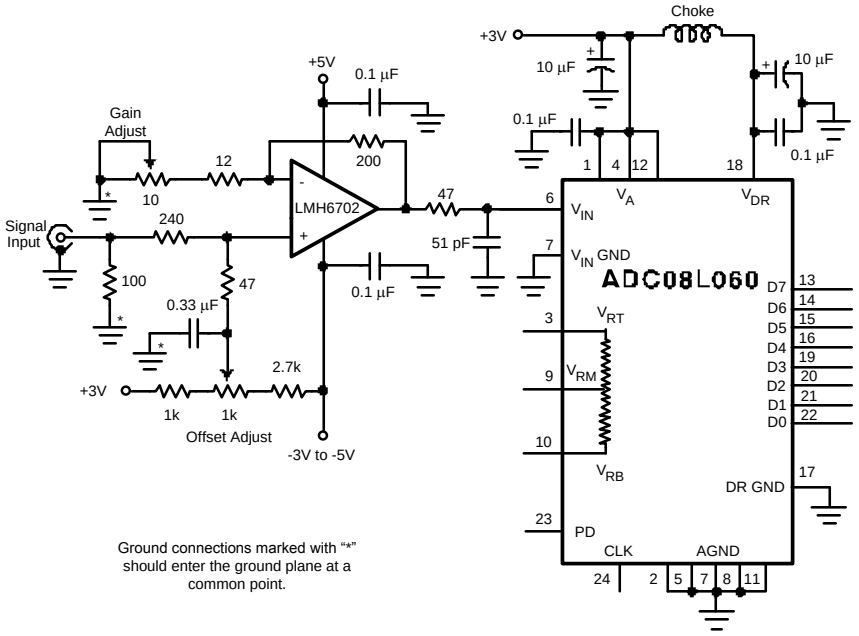
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The RC at the amplifier output filters the clock rate energy that comes out of the analog input due to the input sampling circuit. The optimum time constant for this circuit depends not only upon the amplifier and ADC, but also on the circuit layout and board material. A resistor value should be chosen between 10Ω and 47Ω and the capacitor value chose according to the formula

$$C = \frac{1}{2 \cdot \pi \cdot R \cdot f_{CLK}} \quad (6)$$

This will provide optimum SNR performance. Best THD performance is realized when the capacitor and resistor values are both zero. To optimize SINAD, reduce the capacitor value until SINAD performance is optimized. That is, until SNR = −THD. This value will usually be in the range of 20& to 65% of the value calculated with the above formula. An accurate calculation is not possible because of the board material and layout dependence.

The circuit of Figure 32 has both gain and offset adjustments. If you eliminate these adjustments normal circuit tolerances may result in signal clipping unless care is exercised in the worst case analysis of component tolerances and the input signal excursion is appropriately limited to account for the worst case conditions.



A. The input amplifier should incorporate some gain for best performance (see text).

Figure 32. Input Amplifier

POWER SUPPLY CONSIDERATIONS

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 10 µF tantalum or aluminum electrolytic capacitor should be placed within an inch (2.5 cm) of the A/D power pins, with a 0.1 µF ceramic chip capacitor placed within one centimeter of the converter's power supply pins. Leadless chip capacitors are preferred because they have low lead inductance.

While a single voltage source is recommended for the V_A and V_{DR} supplies of the ADC08L060, these supply pins should be well isolated from each other to prevent any digital noise from being coupled into the analog portions of the ADC. A choke or 27Ω resistor is recommended between these supply lines with adequate bypass capacitors close to the supply pins.

As is the case with all high speed converters, the ADC08L060 should be assumed to have little power supply rejection. None of the supplies for the converter should be the supply that is used for other digital circuitry in any system with a lot of digital power being consumed. The ADC supplies should be the same supply used for other analog circuitry.

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No pin should ever have a voltage on it that is in excess of the supply voltage or below ground by more than 300 mV, not even on a transient basis. This can be a problem upon application of power and power shut-down. Be sure that the supplies to circuits driving any of the input pins, analog or digital, do not come up any faster than does the voltage at the ADC08L060 power pins.

THE DIGITAL INPUT PINS

The ADC08L060 has two digital input pins: The PD pin and the Clock pin.

The PD Pin

The Power Down (PD) pin, when high, puts the ADC08L060 into a low power mode where power consumption is reduced to 1.4 mW with the clock running, or to about 1 mW with the clock held low. Output data is valid and accurate about 1 microsecond after the PD pin is brought low.

The digital output pins retain the last conversion output code when either the clock is stopped or the PD pin is high.

The ADC08L060 Clock

Although the ADC08L060 is tested and its performance is ensured with a 60 MHz clock, it typically will function well with clock frequencies from 10 MHz to 80 MHz.

Clock Duty Cycle

The low and high times of the clock signal can affect the performance of any A/D Converter. Because achieving a precise duty cycle is difficult, the ADC08L060 is designed to maintain performance over a range of duty cycles. While it is specified and performance is ensured with a 50% clock duty cycle and 60 Msps, ADC08L060 performance is typically maintained with clock high and low times of 0.83 ns, corresponding to a clock duty cycle range of 5% to 95% with a 60 MHz clock. Note that minimum low and high times may not be simultaneously asserted.

Clock Line Termination

The **CLOCK** line should be series terminated at the clock source in the characteristic impedance of that line. If the clock line is longer than

$$\frac{t_r}{6 \times t_{prop}} \tag{7}$$

where t_r is the clock rise time and t_{prop} is the propagation rate of the signal along the trace. The **CLOCK** pin should be a.c. terminated with a series RC to ground such that the resistor value is equal to the characteristic impedance of the clock line and the capacitor value is

$$C \geq \frac{4 \times L \times t_{prop}}{Z_o} \tag{8}$$

where “L” is the line length in inches and Z_O is the characteristic impedance of the clock line. Typical t_{PROP} is about 150 ps/inch on FR-4 board material. For FR-4 board material, the value of C becomes

$$C \geq \frac{6 \times 10^{-10} \times L}{Z_o} \tag{9}$$

This termination should be located as close as possible to, but within one centimeter of, the ADC08L060 clock pin.

LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. A combined analog and digital ground plane should be used.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise because of the skin effect. Total surface area is more important than is total ground plane volume. Capacitive coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

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The DR GND connection to the ground plane should not use the same feedthrough used by other ground connections.

High power digital components should not be located on or near a straight line between the ADC or any linear component and the power supply area as the resulting common return current path could cause fluctuation in the analog input “ground” return of the ADC.

Keeping analog and digital return (ground) currents separate from each other will improve system noise performance. Two methods may be used to do this. Use of traces rather than a solid plane to route power to all components will accomplish this because return currents follow the path of the outgoing currents. However, the advantage of the distributed capacitance of a power plane and a ground plane is lost. Analog and digital power should be routed as far from each other as is practical. The analog power trace should also be routed away from digital areas of the board.

The use of power and ground planes in adjacent layers will provide distributed capacitance for a low impedance power distribution system and better system noise performance. The use of separate analog and digital power planes, both in the same PC board layer, and the use of a single, non-split ground plane will keep analog and digital currents separated from each other. Of course, locate all analog circuitry and traces over the analog power plane and the digital circuitry and traces over the digital power plane. To minimize RFI/EMI, give proper attention to any lines crossing the analog/digital power plane boundary.

Noise performance is also enhanced by driving a single gate with each ADC output pin and locating the gate as close as possible to the ADC output. Inserting a 47Ω resistor in series with the ADC digital output pins will also help reduce ADC noise. Be sure to keep the resistors as close to the ADC output pins as possible. Eliminating ground plane copper beneath the ADC output lines can also help ADC noise performance, but could produce unacceptable radiation from the board.

Analog and digital circuitry should be kept well away from each other. Especially troublesome is high power digital components such as processors and large PLDs. Switch mode power supplies, including capacitive DC-DC converters, can cause noise problems with high speed ADCs. Keep such components well away from ADCs and low level analog signal areas. Such components should be located as close to the power supply as possible and should not be in the path of analog signal or power supply currents.

Digital circuits create substantial supply and ground current transients. The noise thus generated could have significant impact upon system noise performance. The best logic family to use in systems with A/D converters is one that employs non-saturating transistor designs, or has low noise characteristics, like the 74LS and the 74AC(T)Q families. The worst noise generators are logic families that draw the largest supply current transients during clock or signal edges, like the 74HC, 74F and 74AC(T) families.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

Clock lines should be isolated from ALL other lines, analog AND digital. Even the generally accepted 90° crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

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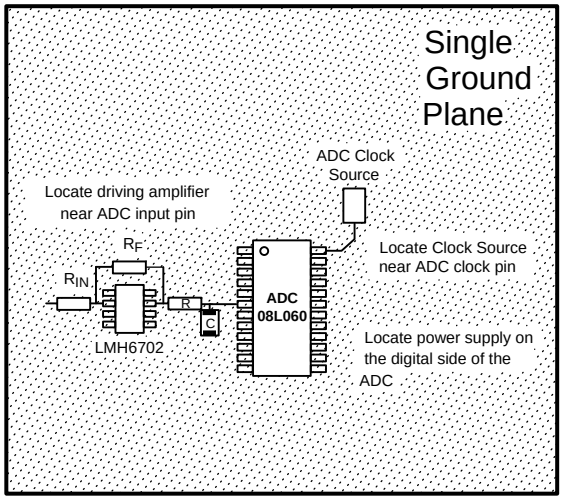


Figure 33. Layout Example

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the ground plane.

Figure 33 gives an example of a suitable layout. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed together away from any digital components.

DYNAMIC PERFORMANCE

The ADC08L060 is a.c. tested and its dynamic performance is ensured. To meet the published specifications, the clock source driving the CLK input should exhibit less than 10 ps (rms) of jitter. For best a.c. performance, isolating the ADC clock from any digital circuitry should be done with adequate buffers, as with a clock tree. See Figure 34.

It is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal. The clock signal can also introduce noise into the analog path.

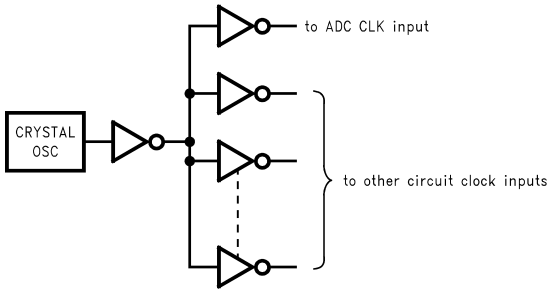


Figure 34. Isolating the ADC Clock from Digital Circuitry

COMMON APPLICATION PITFALLS

Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 300 mV below the ground pins or 300 mV above the supply pins. Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital circuits (e.g., 74F and 74AC devices) to exhibit undershoot that goes more than a volt below ground. A 51Ω resistor in series with the offending digital input will usually eliminate the problem.

Care should be taken not to overdrive the inputs of the ADC08L060. Such practice may lead to conversion inaccuracies and even to device damage.

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Attempting to drive a high capacitance digital data bus. The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current is required from V_{DR} and DR GND. These large charging current spikes can couple into the analog section, degrading dynamic performance. Buffering the digital data outputs (with a 74F541, for example) may be necessary if the data bus capacitance exceeds 5 pF. Dynamic performance can also be improved by adding 100Ω series resistors at each digital output, reducing the energy coupled back into the converter input pins.

Using an inadequate amplifier to drive the analog input. As explained in Section 2.0, the capacitance seen at the input alternates between 3 pF and 4 pF with the clock. This dynamic capacitance is more difficult to drive than is a fixed capacitance, and should be considered when choosing a driving device.

Driving the V_{RT} pin or the V_{RB} pin with devices that can not source or sink the current required by the ladder. As mentioned in Section 1.0, care should be taken to see that any driving devices can source sufficient current into the V_{RT} pin and sink sufficient current from the V_{RB} pin. If these pins are not driven with devices than can handle the required current, these reference pins will not be stable, resulting in a reduction of dynamic performance.

Using a clock source with excessive jitter, using an excessively long clock signal trace, or having other signals coupled to the clock signal trace. This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance. The use of simple gates with RC timing is generally inadequate as a clock source.

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REVISION HISTORY

Changes from Revision F (March 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	21

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC08L060CIMT	NRND	TSSOP	PW	24	61	TBD	Call TI	Call TI	-40 to 85	ADC08L060 CIMT	
ADC08L060CIMT/NOPB	ACTIVE	TSSOP	PW	24	61	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	ADC08L060 CIMT	Samples
ADC08L060CIMTX/NOPB	ACTIVE	TSSOP	PW	24	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	ADC08L060 CIMT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

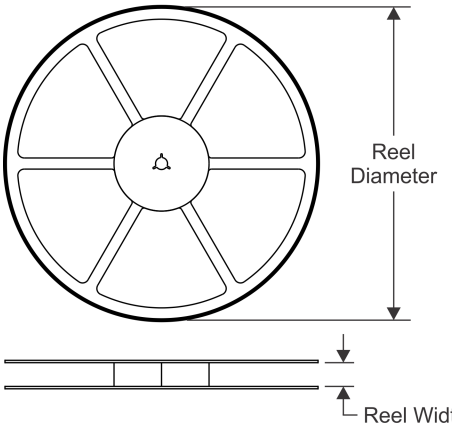
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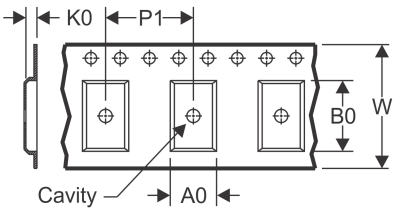
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

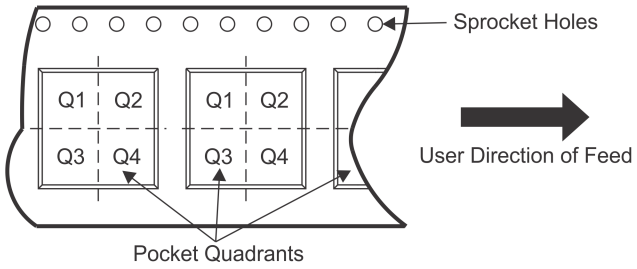


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

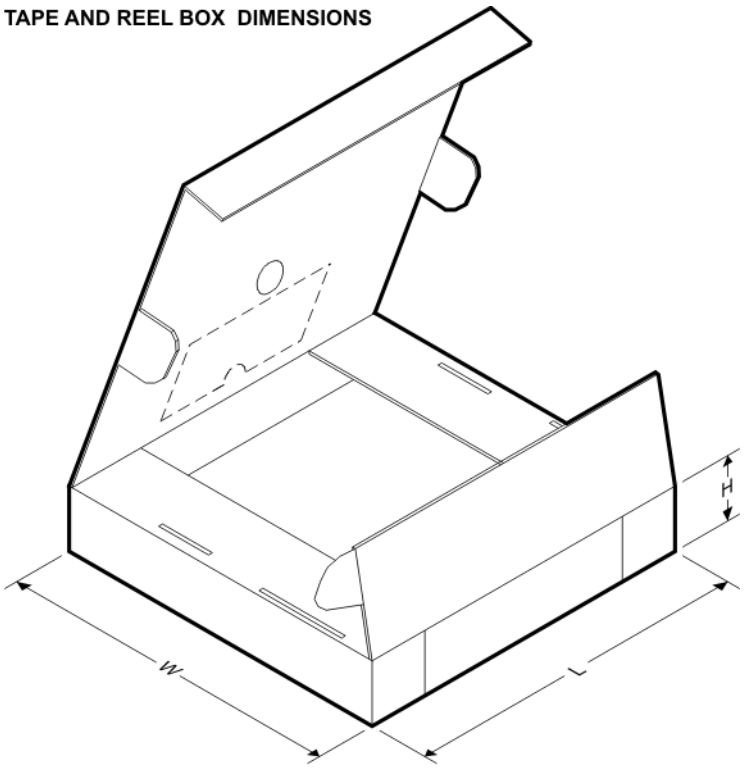
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC08L060CIMTX/NOPB	TSSOP	PW	24	2500	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

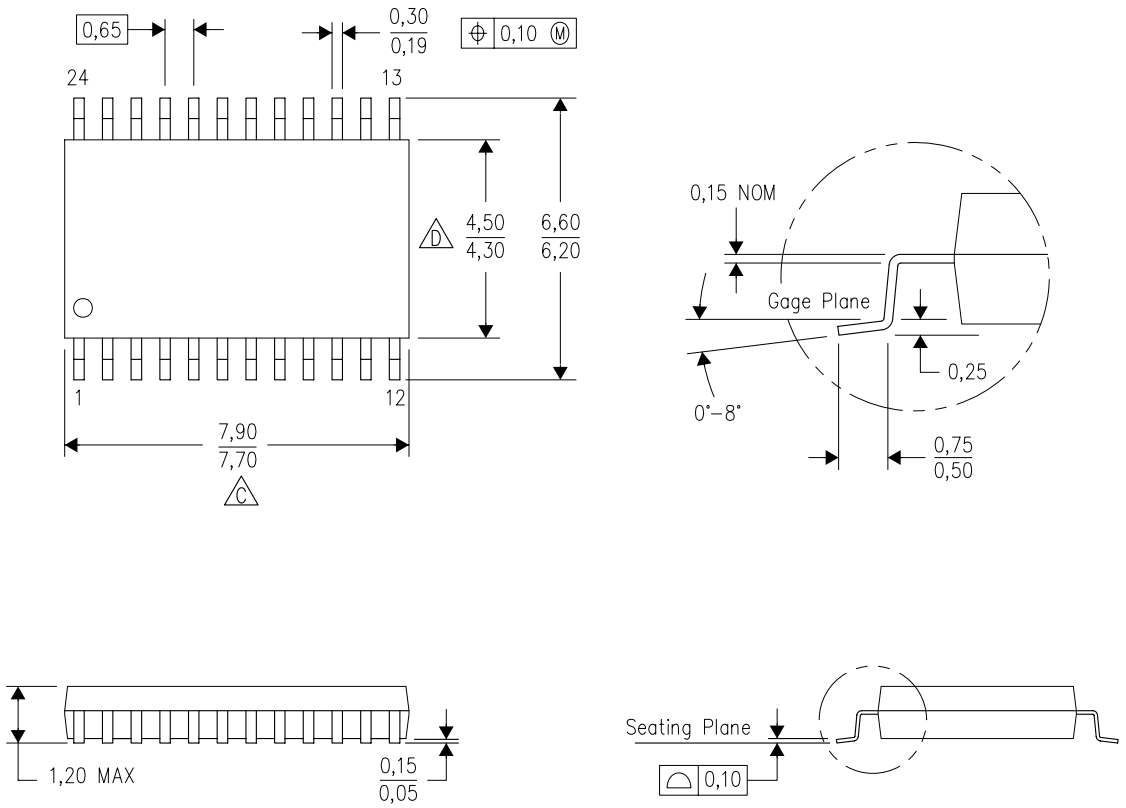
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC08L060CIMTX/NOPB	TSSOP	PW	24	2500	367.0	367.0	35.0

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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