Host-controlled Multi-chemistry Battery Charger with Low Input Power Detect

FEATURES

- NMOS-NMOS Synchronous Buck Converter with 300 kHz Frequency and >95% Efficiency
- 30-ns Minimum Driver Dead-time and 99.5% Maximum Effective Duty Cycle
- High-Accuracy Voltage and Current Regulation
  - ±0.5% Charge Voltage Accuracy
  - ±3% Charge Current Accuracy
  - ±3% Adapter Current Accuracy
  - ±2% Input Current Sense Amp Accuracy
- Integration
  - Internal Loop Compensation
  - Internal Soft Start
- Safety
  - Input Overvoltage Protection (OVP)
  - Dynamic Power Management (DPM) with Status Indicator
  - Reverse-Conduction Protection Input FET
- Supports Two, Three, or Four Li+ Cells
- 5 – 24 V AC/DC-Adapter Operating Range
- Analog Inputs with Ratiometric Programming via Resistors or DAC/GPIO Host Control
  - Charge Voltage (4-4.512 V/cell)
  - Charge Current (up to 10 A, with 10-mΩ sense resistor)
  - Adapter Current Limit (DPM)
- Status and Monitoring Outputs
  - AC/DC Adapter Present with Programmable Voltage Threshold
  - Low Input-Power Detect with Adjustable Threshold and Hysteresis
  - DPM Loop Active
  - Current Drawn from Input Source
- Battery Discharge Current Sense with No Adapter, or Selectable Low-Iq mode
- Supports Any Battery Chemistry: Li+, NiCd, NiMH, Lead Acid, etc.
- Charge Enable
- 10-μA Off-State Current
- 28-pin, 5x5-mm QFN package

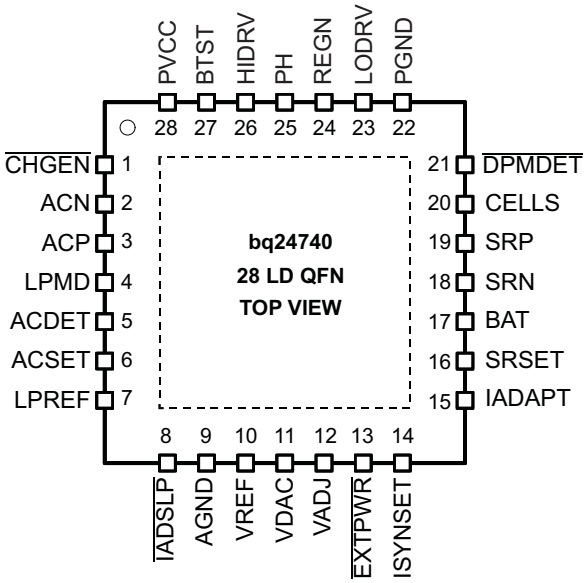
APPLICATIONS

- Notebook and Ultra-Mobile Computers
- Portable Data-Capture Terminals
- Portable Printers
- Medical Diagnostics Equipment
- Battery Bay Chargers
- Battery Back-up Systems

DESCRIPTION

The bq24740 is a high-efficiency, synchronous battery charger with integrated compensation and system power selector logic, offering low component count for space-constrained multi-chemistry battery charging applications. Ratiometric charge current and voltage programming allows very high regulation accuracies, and can be either hardwired with resistors or programmed by the system power-management microcontroller using a DAC or GPIOs.

The bq24740 charges two, three, or four series Li+ cells, supporting up to 10 A of charge current, and is available in a 28-pin, 5x5-mm thin QFN package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

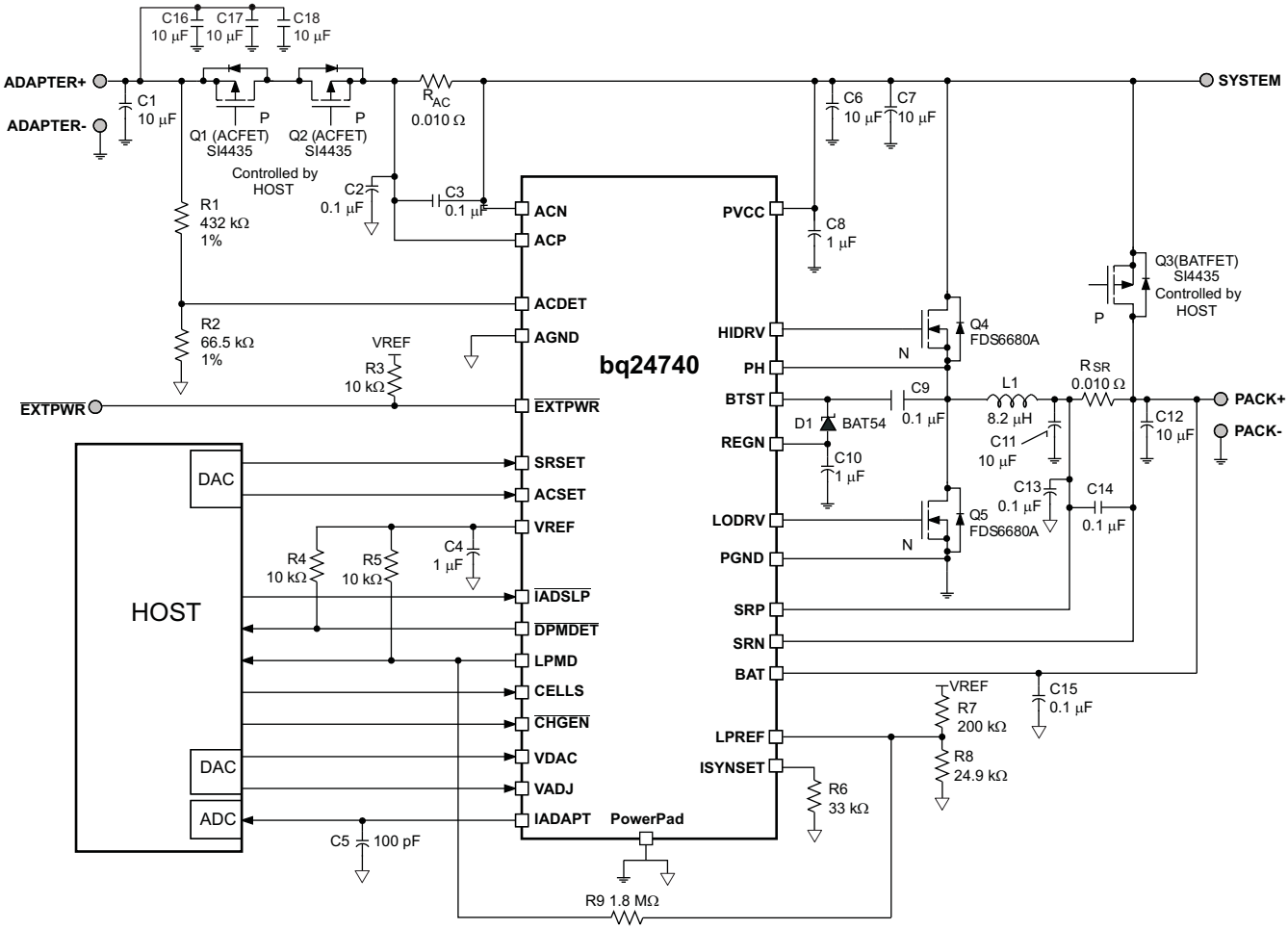
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The bq24740 features Dynamic Power Management (DPM) and input power limiting. These features reduce battery charge current when the input power limit is reached to avoid overloading the AC adapter when supplying the load and the battery charger simultaneously. A highly-accurate current-sense amplifier enables precise measurement of input current from the AC adapter to monitor the overall system power. If the adapter current is above the programmed low-power threshold, a signal is sent to host so that the system optimizes its power performance according to what is available from the adapter.

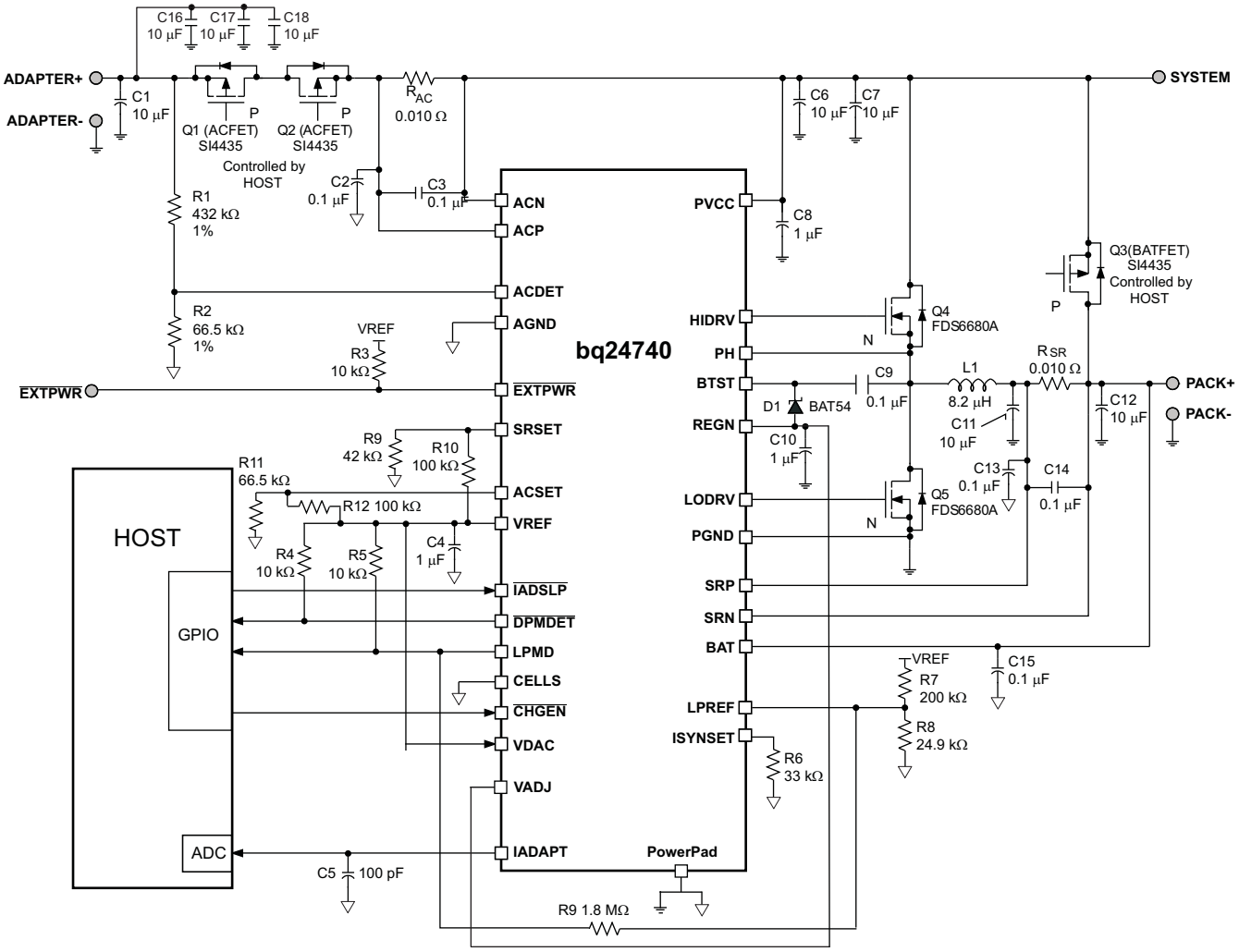
TYPICAL APPLICATION



(1) Pull-up rail could be either VREF or other system rail .
(2) SRSET/ACSET could come from either DAC or resistor dividers .

V_{IN} = 20 V, V_{BAT} = 3-cell Li-Ion, I_{CHARGE} = 3 A, $I_{ADAPTER_LIMIT}$ = 4 A

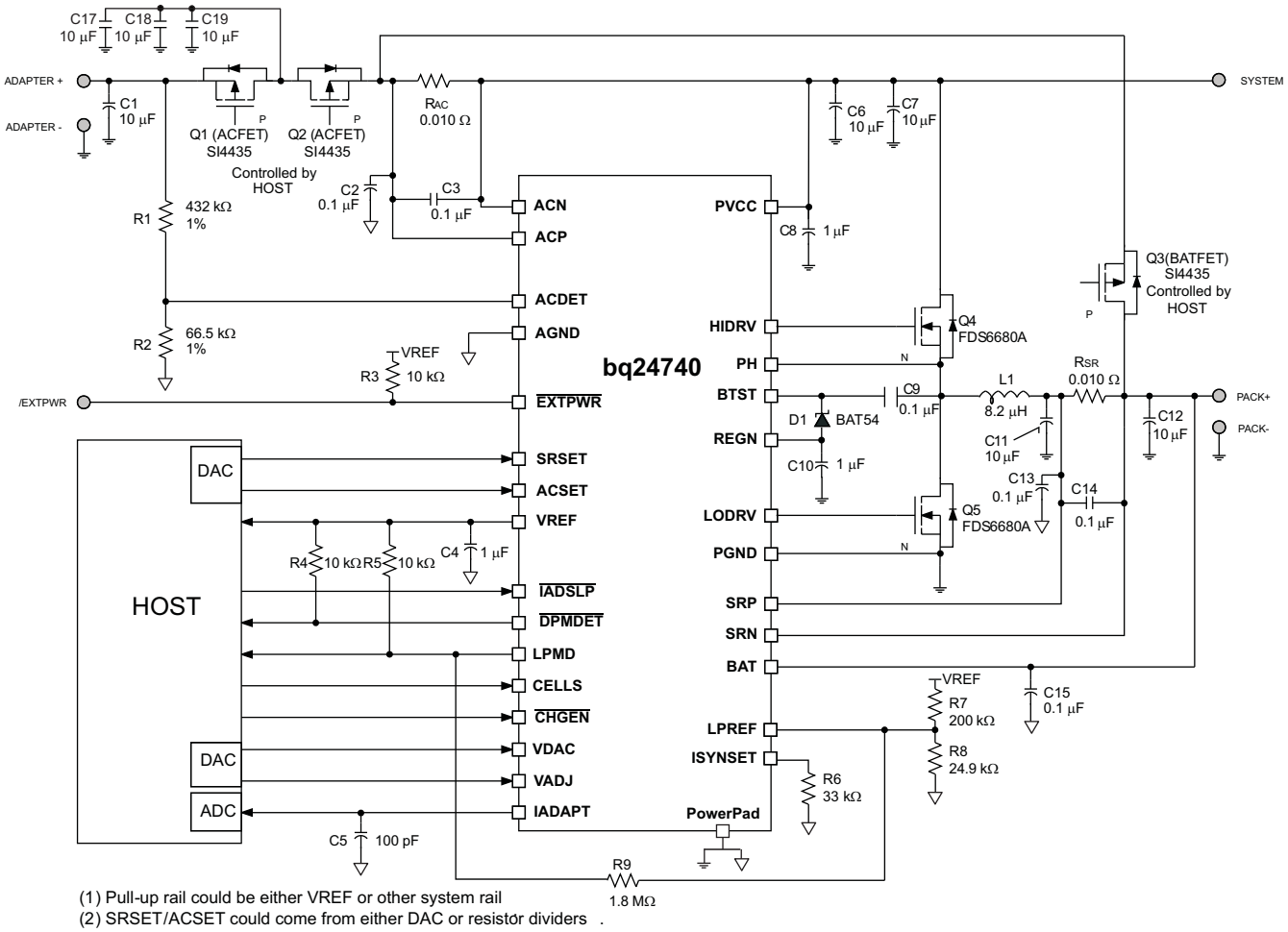
Figure 1. Typical System Schematic, Voltage and Current Programmed by DAC



(1) Pull-up rail could be either VREF or other system rail .
(2) SRSET/ACSET could come from either DAC or resistor dividers.

A. V_{IN} = 20 V, V_{BAT} = 3-cell Li-Ion, I_{CHARGE} = 3 A, $I_{ADAPTER_LIMIT}$ = 4 A

Figure 2. Typical System Schematic, Voltage and Current Programmed by Resistor



(1) Pull-up rail could be either VREF or other system rail
(2) SRSET/ACSET could come from either DAC or resistor dividers .

V_{IN} = 20 V, V_{BAT} = 3-cell Li-Ion, I_{CHARGE} = 3 A, $I_{ADAPTER_LIMIT}$ = 4 A

Figure 3. Typical System Schematic: Sensing Battery Discharge Current, When Adapter Removed. (Set $\overline{\text{IADSLP}}$ at logic high)

ORDERING INFORMATION

Part number	Package	Ordering Number (Tape and Reel)	Quantity
bq24740	28-PIN 5 x 5 mm QFN	bq24740RHDR	3000
		bq24740RHDT	250

PACKAGE THERMAL DATA

PACKAGE	θ_{JA}	T_A = 70°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C
QFN – RHD (1)(2)	39°C/W	2.36 W	0.028 W/°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. This is connected to the ground plane by a 2x3 via matrix.

Table 1. TERMINAL FUNCTIONS – 28-PIN QFN

TERMINAL		DESCRIPTION
NAME	NO.	
$\overline{\text{CHGEN}}$	1	Charge enable active-low logic input. LO enables charge. HI disables charge.
ACN	2	Adapter current sense resistor, negative input. An optional 0.1-µF ceramic capacitor is placed from ACN pin to AGND for common-mode filtering. An optional 0.1-µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering.
ACP	3	Adapter current sense resistor, positive input. (See comments with ACN description)
LPMD	4	Low power mode detect active-high open-drain logic output. Place a 10-kΩ pullup resistor from LPMD pin to the pullup-voltage rail. Place a positive-feedback resistor from LPMD pin to LPREF pin for programming hysteresis (see design example for calculation). The output is HI when IADAPT pin voltage is lower than LPREF pin voltage. The output is LO when IADAPT pin voltage is higher than LPREF pin voltage.
ACDET	5	Adapter detected voltage set input. Program the adapter detect threshold by connecting a resistor divider from adapter input to ACDET pin to AGND pin. Adapter voltage is detected if ACDET-pin voltage is greater than 2.4 V. The I_{ADAPT} current sense amplifier is active when the ACDET pin voltage is greater than 0.6 V. Input overvoltage, ACOV, disables charge and $\overline{\text{ACDRV}}$ when ACDET > 3.1 V. ACOV does not latch
ACSET	6	Adapter current set input. The voltage ratio of ACSET voltage versus VDAC voltage programs the input current regulation set-point during Dynamic Power Management (DPM). Program by connecting a resistor divider from VDAC to ACSET to AGND; or by connecting the output of an external DAC to the ACSET pin and connect the DAC supply to the VDAC pin.
LPREF	7	Low power voltage set input. Connect a resistor divider from VREF to LPREF and AGND to program the reference for the LOPWR comparator. The LPREF-pin voltage is compared to the IADAPT-pin voltage and the logic output is given on the LPMD open-drain pin. Connecting a positive-feedback resistor from LPREF pin to LPMD pin programs the hysteresis.
$\overline{\text{IADSLP}}$	8	Enable IADAPT to enter sleep mode; active-low logic input. Allows low I_q sleep mode when adapter not detected. Logic low turns off the Input Current Sense Amplifier (IADAPT) when adapter is not detected and ACDET pin is <0.6 V - allows lower battery discharge current. Logic high keeps IADAPT current-sense amplifier on when adapter is not detected and ACDET pin is <0.6 V - this allows measuring battery discharge current.
AGND	9	Analog ground. On PCB layout, connect to the analog ground plane, and only connect to PGND through the power pad underneath the IC.
VREF	10	3.3-V regulated voltage output. Place a 1-µF ceramic capacitor from VREF to AGND pin close to the IC. This voltage could be used for ratiometric programming of voltage and current regulation.
VDAC	11	Charge voltage set reference input. Connect the VREF or external DAC voltage source to the VDAC pin. Battery voltage, charge current, and input current are programmed as a ratio of the VDAC pin voltage versus the VADJ, SRSET, and ACSET pin voltages, respectively. Place resistor dividers from VDAC to VADJ, SRSET, and ACSET pins to AGND for programming. A DAC could be used by connecting the DAC supply to VDAC and connecting the output to VADJ, SRSET, or ACSET.
VADJ	12	Charge voltage set input. The voltage ratio of VADJ voltage versus VDAC voltage programs the battery voltage regulation set-point. Program by connecting a resistor divider from VDAC to VADJ, to AGND; or, by connecting the output of an external DAC to VADJ, and connect the DAC supply to VDAC. VADJ connected to REGN programs the default of 4.2 V per cell.
$\overline{\text{EXTPWR}}$	13	Valid adapter active-low detect logic open-drain output. Pulled low when input voltage is above ACDET programmed threshold, OR input current is greater than 1.25 A with 10-mΩ sense resistor. Connect a 10-kΩ pullup resistor from $\overline{\text{EXTPWR}}$ pin to pullup supply rail.
ISYNSET	14	Synchronous mode voltage set input. Place a resistor from ISYNSET to AGND to program the charge undercurrent threshold to force non-synchronous converter operation at low output current, and to prevent negative inductor current. Threshold should be set at greater than half of the maximum inductor ripple current (50% duty cycle).
IADAPT	15	Adapter current sense amplifier output. IADAPT voltage is 20 times the differential voltage across ACP-ACN. Place a 100-pF or less ceramic decoupling capacitor from IADAPT to AGND.
SRSET	16	Charge current set input. The voltage ratio of SRSET voltage versus VDAC voltage programs the charge current regulation set-point. Program by connecting a resistor divider from VDAC to SRSET to AGND; or by connecting the output of an external DAC to SRSET pin and connect the DAC supply to VDAC pin.
BAT	17	Battery voltage remote sense. Directly connect a kelvin sense trace from the battery pack positive terminal to the BAT pin to accurately sense the battery pack voltage. Place a 0.1-µF capacitor from BAT to AGND close to the IC to filter high-frequency noise.
SRN	18	Charge current sense resistor, negative input. An optional 0.1-µF ceramic capacitor is placed from SRN pin to AGND for common-mode filtering. An optional 0.1-µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering.
SRP	19	Charge current sense resistor, positive input. (See comments for SRN.)
CELLS	20	2, 3 or 4 cells selection logic input. Logic low programs 3 cell. Logic high programs 4 cell. Floating programs 2 cell.

Table 1. TERMINAL FUNCTIONS – 28-PIN QFN (continued)

TERMINAL		DESCRIPTION
NAME	NO.	
$\overline{\text{DPMDET}}$	21	Dynamic power management (DPM) input current loop active, open-drain output status. Logic low indicates input current is being limited by reducing the charge current. Connect 10-kΩ pullup resistor from $\overline{\text{DPMDET}}$ to VREF or a different pullup-supply rail.
PGND	22	Power ground. On PCB layout, connect directly to source of low-side power MOSFET, to ground connection of input and output capacitors of the charger. Only connect to AGND through the power pad underneath the IC.
LODRV	23	PWM low side driver output. Connect to the gate of the low-side power MOSFET with a short trace.
REGN	24	PWM low side driver positive 6-V supply output. Connect a 1-µF ceramic capacitor from REGN to PGND, close to the IC. Use for high-side driver bootstrap voltage by connecting a small-signal Schottky diode from REGN to BTST.
PH	25	PWM high side driver negative supply. Connect to the phase switching node (junction of the low-side power MOSFET drain, high-side power MOSFET source, and output inductor). Connect the 0.1-µF bootstrap capacitor from from PH to BTST.
HIDRV	26	PWM high side driver output. Connect to the gate of the high-side power MOSFET with a short trace.
BTST	27	PWM high side driver positive supply. Connect a 0.1-µF bootstrap ceramic capacitor from BTST to PH. Connect a small bootstrap Schottky diode from REGN to BTST.
PVCC	28	IC power positive supply. Connect to the common-source (diode-OR) point: source of high-side P-channel MOSFET and source of reverse-blocking power P-channel MOSFET. Place a 1-µF ceramic capacitor from PVCC to PGND pin close to the IC.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)(2)

		VALUE	UNIT
Voltage range	PVCC, ACP, ACN, SRP, SRN, BAT	–0.3 to 30	V
	PH	–1 to 30	
	REGN, LODRV, VADJ, ACSET, SRSET, ACDET, ISYNSET, LPMD, LPREF, $\overline{\text{CHGEN}}$, CELLS, $\overline{\text{EXTPWR}}$, $\overline{\text{DPMDET}}$	–0.3 to 7	
	VDAC	–0.3 to 5.5	
	VREF	–0.3 to 3.6	
	BTST, HIDRV with respect to AGND and PGND, IADAPT	–0.3 to 36	
Maximum difference voltage	ACP–ACN, SRP–SRN, AGND–PGND	–0.5 to 0.5	
Junction temperature range		–40 to 155	°C
Storage temperature range		–55 to 155	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage range	PH	–1		24	V
	PVCC, ACP, ACN, SRP, SRN, BAT	0		24	
	REGN, LODRV	0		6.5	
	VREF	0		3.3	
	VDAC, IADAPT	0		3.6	
	ACSET, SRSET, ACDET, ISYNSET, LPMD, LPREF, $\overline{\text{CHGEN}}$, CELLS, $\overline{\text{EXTPWR}}$, $\overline{\text{DPMDET}}$	0		5.5	
	VADJ	0		6.5	
	BTST, HIDRV with respect to AGND and PGND	0		30	
	AGND, PGND	–0.3		0.3	
Maximum difference voltage: ACP–ACN, SRP–SRN				5.5	
Junction temperature range		–40		125	°C
Storage temperature range		–55		150	

PACKAGE THERMAL DATA

PACKAGE	θ_{JA}	T_A = 70°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C
QFN– RHD(1)	39°C/W	2.36W	0.028 W/°C

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. This is connected to the ground plane by a 2x3 via matrix.

ELECTRICAL CHARACTERISTICS

7.0 V ≤ V_{PVCC} ≤ 24 V, 0°C < T_J < +125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CONDITIONS						
V_{PVCC_OP}	PVCC Input voltage operating range		5.0		24.0	V
CHARGE VOLTAGE REGULATION						
$V_{BAT_REG_RNG}$	BAT voltage regulation range	4V-4.512V per cell, times 2,3,4 cell	8		18	V
V_{VDAC_OP}	VDAC reference voltage range		2.6		3.6	V
V_{ADJ_OP}	VADJ voltage range		0		REGN	V
	Charge voltage regulation accuracy	8 V, 8.4 V, 9.024 V	–0.5		0.5	%
		12 V, 12.6 V, 13.536 V	–0.5		0.5	
		16 V, 16.8 V, 18.048 V	–0.5		0.5	
	Charge voltage regulation set to default to 4.2 V per cell	VADJ connected to REGN, 8.4 V, 12.6 V, 16.8 V	–0.5		0.5	%
CHARGE CURRENT REGULATION						
V_{IREG_CHG}	Charge current regulation differential voltage range	V_{IREG_CHG} = V_{SRP} – V_{SRN}	0		100	mV
V_{SRSET_OP}	SRSET voltage range		0		VDAC	V
	Charge current regulation accuracy	V_{IREG_CHG} = 40–100 mV	–3		3	%
		V_{IREG_CHG} = 20 mV	–5		5	
		V_{IREG_CHG} = 5 mV	–25		25	
		V_{IREG_CHG} = 1.5 mV	–33		33	

ELECTRICAL CHARACTERISTICS (continued)

7.0 V ≤ V_{PVCC} ≤ 24 V, 0°C < T_J < +125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENT REGULATION						
V_{IREG_DPM}	Adapter current regulation differential voltage range	$V_{IREG_DPM} = V_{ACP} – V_{ACN}$	0		200	mV
V_{ACSET_OP}	ACSET voltage range		0		2	V
	Input current regulation accuracy	V_{IREG_DPM} = 40–100 mV	–3		3	%
		V_{IREG_DPM} = 20 mV	–5		5	
		V_{IREG_DPM} = 5 mV	–25		25	
		V_{IREG_DPM} = 1.5 mV	–33		33	
VREF REGULATOR						
V_{VREF_REG}	VREF regulator voltage	V_{ACDET} > 0.6 V, 0-30 mA	3.267	3.3	3.333	V
I_{VREF_LIM}	VREF current limit	V_{VREF} = 0 V, V_{ACDET} > 0.6 V	35		75	mA
REGN REGULATOR						
V_{REGN_REG}	REGN regulator voltage	V_{ACDET} > 0.6 V, 0-75 mA, PVCC > 10 V	5.6	5.9	6.2	V
I_{REGN_LIM}	REGN current limit	V_{REGN} = 0 V, V_{ACDET} > 0.6 V	90		135	mA
ADAPTER CURRENT SENSE AMPLIFIER						
V_{ACP/N_OP}	Input common mode range	Voltage on ACP/SRN	0		24	V
V_{IADAPT}	IADAPT output voltage range		0		2	V
I_{IADAPT}	IADAPT output current		0		1	mA
A_{IADAPT}	Current sense amplifier voltage gain	$A_{IADAPT} = V_{IADAPT} / V_{IREG_DPM}$		20		V/V
	Adapter current sense accuracy	V_{IREG_DPM} = 40–100 mV	–2		2	%
		V_{IREG_DPM} = 20 mV	–3		3	
		V_{IREG_DPM} = 5 mV	–25		25	
		V_{IREG_DPM} = 1.5 mV	–30		30	
I_{IADAPT_LIM}	Output current limit	V_{IADAPT} = 0 V	1			mA
C_{IADAPT_MAX}	Maximum output load capacitance	For stability with 0 mA to 1 mA load			100	pF
ACDET COMPARATOR						
$V_{PVCC-BAT_OP}$	Differential Voltage from PVCC to BAT		–20		24	V
V_{ACDET_CHG}	ACDET adapter-detect rising threshold	Min voltage to enable charging, V_{ACDET} rising	2.376	2.40	2.424	V
$V_{ACDET_CHG_HYS}$	ACDET falling hysteresis	V_{ACDET} falling		40		mV
	ACDET rising deglitch (1)	VACDET rising	518	700	908	ms
	ACDET falling deglitch	VACDET falling		10		µs
V_{ACDET_BIAS}	ACDET enable-bias rising threshold	Min voltage to enable all bias, V_{ACDET} rising	0.56	0.62	0.68	V
$V_{ACDET_BIAS_HYS}$	Adapter present falling hysteresis	V_{ACDET} falling		20		mV
	ACDET rising deglitch (1)	V_{ACDET} rising		10		µs
	ACDET falling deglitch	V_{ACDET} falling		10		
INPUT OVERVOLTAGE COMPARATOR (ACOV)						
V_{ACOV}	AC Over-voltage rising threshold on ACDET (See ACDET in *erminal Functions*)		3.007	3.1	3.193	V
V_{ACOV_HYS}	AC Over-voltage rising deglitch			1.3		ms
	AC Over-voltage falling deglitch			1.3		

(1) Verified by design.

ELECTRICAL CHARACTERISTICS (continued)

7.0 V ≤ V_{PVCC} ≤ 24 V, 0°C < T_J < +125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC CURRENT DETECT COMPARATOR (INPUT UNDER_CURRENT)						
V_{ACIDET}	Adapter current detect rising threshold	V_{ACI} = I_{AC} × R_{AC} × 20, falling edge	200	250	300	mV
V_{ACIDET_HYS}	Adapter current detect hysteresis	Rising edge		50		mV
PVCC / BAT COMPARATOR (REVERSE DISCHARGING PROTECTION)						
$V_{PVCC-BAT_FALL}$	PVCC to BAT falling threshold	V_{PVCC} – V_{BAT} to turn off ACFET	140	185	240	mV
$V_{PVCC-BAT__HYS}$	PVCC to BAT hysteresis			50		mV
	PVCC to BAT Rising Deglitch	V_{PVCC} – V_{BAT} > $V_{PVCC-BAT_RISE}$		10		µs
	PVCC to BAT Falling Deglitch	V_{PVCC} – V_{BAT} < $V_{PVCC-BAT_FALL}$		6		
INPUT UNDERVOLTAGE LOCK-OUT COMPARATOR (UVLO)						
V_{UVLO}	AC Under-voltage rising threshold	Measure on PVCC	3.5	4	4.5	V
V_{UVLO_HYS}	AC Under-voltage hysteresis, falling			260		mV
BAT OVER-VOLTAGE COMPARATOR						
V_{OV_RISE}	Over-voltage rising threshold (2)	As percentage of V_{BAT_REG}		104		%
V_{OV_FALL}	Over-voltage falling threshold (2)			102		
CHARGE OVER-CURRENT COMPARATOR						
V_{OC}	Charge over-current falling threshold	As percentage of I_{REG_CHG}		145		%
	Minimum Current Limit (SRP-SRN)			50		mV
INPUT CURRENT LOW-POWER MODE COMPARATOR						
V_{ACLP_HYS}	AC low power hysteresis			2.8		mV
V_{ACLP_OFFSET}	AC low power rising threshold			1		
THERMAL SHUTDOWN COMPARATOR						
T_{SHUT}	Thermal shutdown rising temperature	Temperature Increasing		155		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis, falling			20		
PWM HIGH SIDE DRIVER (HIDRV)						
$R_{DS_HI_ON}$	High side driver turn-on resistance	V_{BTST} – V_{PH} = 5.5 V, tested at 100 mA		3	6	Ω
$R_{DS_HI_OFF}$	High side driver turn-off resistance	V_{BTST} – V_{PH} = 5.5 V, tested at 100 mA		0.7	1.4	
$V_{BTST_REFRESH}$	Bootstrap refresh comparator threshold voltage	V_{BTST} – V_{PH} when low side refresh pulse is requested	4			V
PWM LOW SIDE DRIVER (LODRV)						
$R_{DS_LO_ON}$	Low side driver turn-on resistance	REGN = 6 V, tested at 100 mA		3	6	Ω
$R_{DS_LO_OFF}$	Low side driver turn-off resistance	REGN = 6 V, tested at 100 mA		0.6	1.2	
PWM DRIVERS TIMING						
	Driver Dead Time — Dead time when switching between LODRV and HIDRV. No load at LODRV and HIDRV		30			ns
PWM OSCILLATOR						
F_{SW}	PWM switching frequency		240		360	kHz
V_{RAMP_HEIGHT}	PWM ramp height	As percentage of PVCC		6.6		%PVCC

(2) Verified by design.

ELECTRICAL CHARACTERISTICS (continued)

7.0 V ≤ V_{PVCC} ≤ 24 V, 0°C < T_J < +125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENT						
I_{OFF_STATE}	Total off-state battery current from SRP, SRN, BAT, VCC, BTST, PH, etc.	V_{BAT} = 16.8 V, V_{ACDET} < 0.6 V, V_{PVCC} > 5 V, T_J = 85°C		7	10	µA
		V_{BAT} = 16.8 V, V_{ACDET} < 0.6 V, V_{PVCC} > 5 V, T_J = 125°C		7	11	
I_{BAT_ON}	Battery on-state quiescent current	V_{BAT} = 16.8V, 0.6V < V_{ACDET} < 2.4V, V_{PVCC} > 5V		1		mA
$I_{BAT_LOAD_CD}$	Internal battery load current, charge disbled	Charge is disabled: V_{BAT} = 16.8 V, V_{ACDET} > 2.4 V, V_{PVCC} > 5 V		3	5	mA
$I_{BAT_LOAD_CE}$	Internal battery load current, charge enabled	Charge is enabled: V_{BAT} = 16.8 V, V_{ACDET} > 2.4 V, V_{PVCC} > 5 V	6	10	12	mA
I_{AC}	Adapter quiescent current	V_{PVCC} = 20 V, charge disabled		2.8	4	mA
I_{AC_SWITCH}	Adapter switching quiescent current	V_{PVCC} = 20 V, Charge enabled, converter running, total gate charge = 2 × 10 nC		25		mA
INTERNAL SOFT START (8 steps to regulation current)						
	Soft start steps			8		step
	Soft start step time			1.7		ms
CHARGER SECTION POWER-UP SEQUENCING						
	Charge-enable delay after power-up	Delay from when adapter is detected to when the charger is allowed to turn on	518	700	908	ms
ISYNSET AMPLIFIER AND COMPARATOR (SYNCHRONOUS TO NON-SYSNCHRONOUS TRANSITION)						
	Accuracy	5 mV	–20		20	%
$A_{ISYNSET}$	Gain	ISYNSET amplifier gain		250		V/I
$V_{ISYNSET}$	ISYNSET pin voltage			1		V
	ISYNSET rising deglitch			20		µs
	ISYNSET falling deglitch			640		µs
LOGIC IO PIN CHARACTERISTICS (CHGEN, IADSLP)						
V_{IN_LO}	Input low threshold voltage				0.8	V
V_{IN_HI}	Input high threshold voltage		2.1			
V_{BIAS}	Input bias current	$V_{\overline{CHGEN}}$ = 0 to V_{REGN}			1	µA
LOGIC INPUT PIN CHARACTERISTICS (CELLS)						
V_{IN_LO}	Input low threshold voltage, 3 cells	CELLS voltage falling edge			0.5	V
V_{IN_MID}	Input mid threshold voltage, 2 cells	CELLS voltage rising for MIN, CELLS voltage falling for MAX	0.8		1.8	
V_{IN_HI}	Input high threshold voltage, 4 cells	CELLS voltage rising	2.5			
I_{BIAS_FLOAT}	Input bias float current for 2-cell selection	V = 0 to V	–1		1	µA
OPEN-DRAIN LOGIC OUTPUT PIN CHARACTERISTICS (EXTPWR)						
V_{OUT_LO}	Output low saturation voltage	Sink Current = 4 mA			0.5	V
	Delay, EXTPWR falling		518	700	908	ms
	Delay, EXTPWR rising			10		µs
OPEN-DRAIN LOGIC OUTPUT PIN CHARACTERISTICS (DPMDET, LPMD)						
V_{OUT_LO}	Output low saturation voltage	Sink Current = 5 mA			0.5	V
	Delay, rising/falling			10		ms

TYPICAL CHARACTERISTICS

Table of Graphs(1)

Y	X	FIgure
VREF Load and Line Regulation	vs Load Current	Figure 4
REGN Load and Line Regulation	vs Load Current	Figure 5
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Input Current	vs ACSET/VDAC Ratio	Figure 8
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Continuous Conduction Mode (CCM) Switching Waveforms		Figure 26
Discontinuous Conduction Mode (DCM) Switching Waveforms		Figure 27

(1) Test results based on Figure 2 application schematic. V_{IN} = 20 V, V_{BAT} = 3-cell LiIon, I_{CHG} = 3 A, $I_{ADAPTER_LIMIT}$ = 4 A, T_A = 25°C, unless otherwise specified.

VREF LOAD AND LINE REGULATION vs Load Current

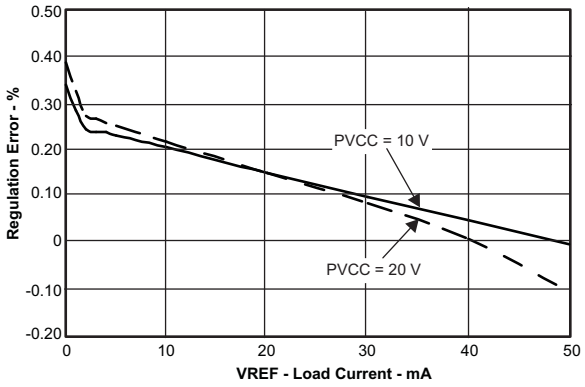


Figure 4.

REGN LOAD AND LINE REGULATION vs LOAD CURRENT

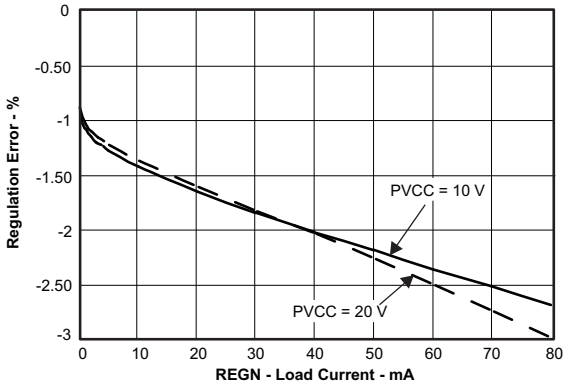


Figure 5.

BAT VOLTAGE vs VADJ/VDAC RATIO

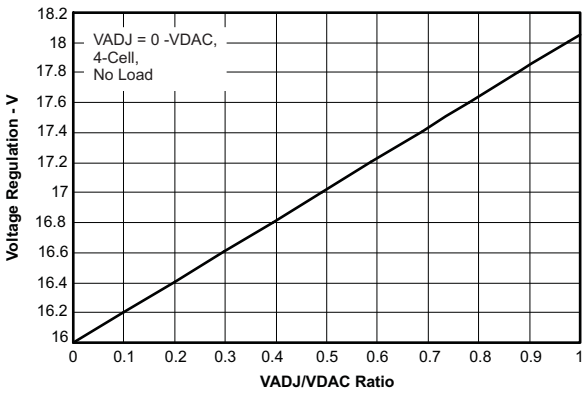


Figure 6.

CHARGE CURRENT vs SRSET/VDAC RATIO

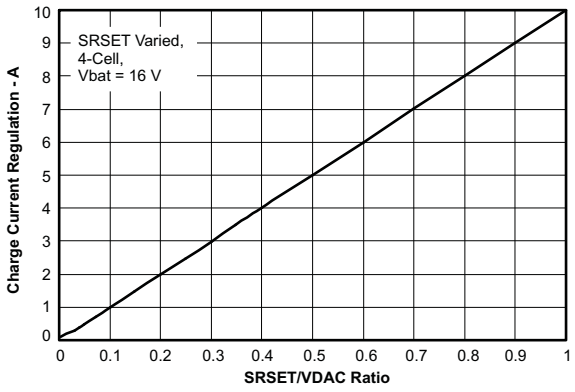


Figure 7.

INPUT CURRENT vs ACSET/VDAC RATIO

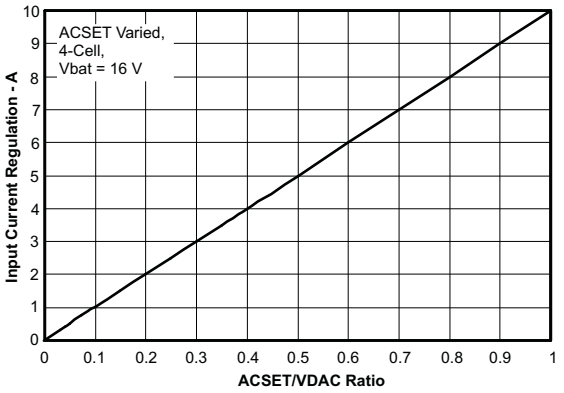


Figure 8.

BAT VOLTAGE REGULATION ACCURACY vs CHARGE CURRENT

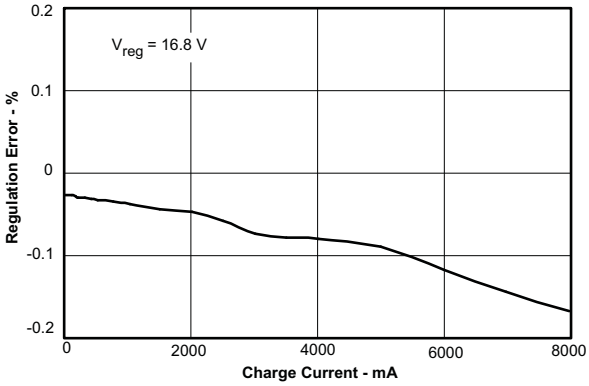


Figure 9.

BAT VOLTAGE REGULATION ACCURACY

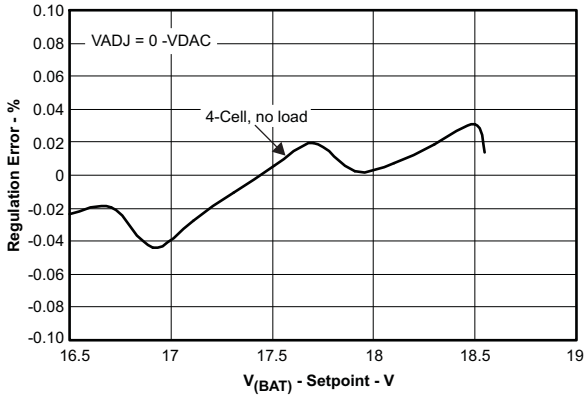


Figure 10.

CHARGE CURRENT REGULATION ACCURACY

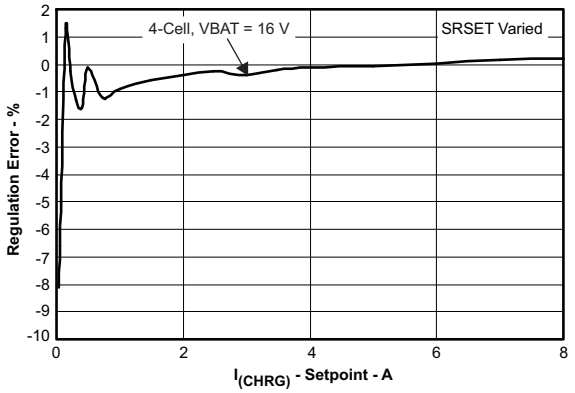


Figure 11.

INPUT CURRENT REGULATION (DPM) ACCURACY

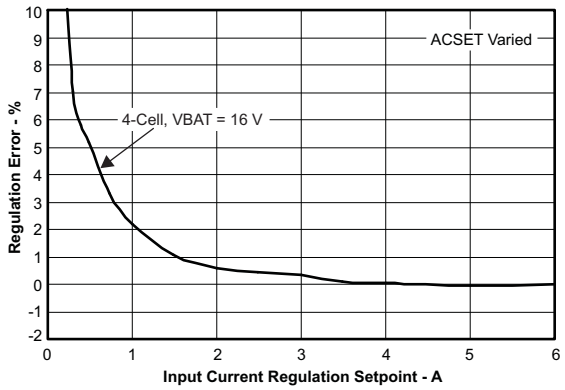


Figure 12.

V_{IADAPT} INPUT CURRENT SENSE AMPLIFIER ACCURACY

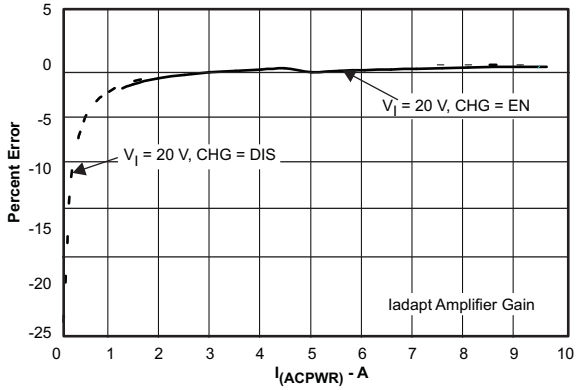


Figure 13.

INPUT REGULATION CURRENT (DPM), AND CHARGE CURRENT VS SYSTEM CURRENT

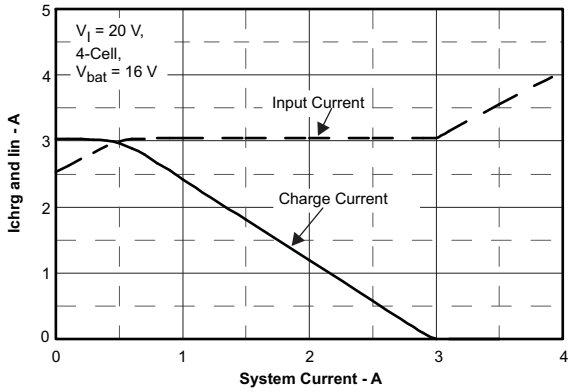


Figure 14.

TRANSIENT SYSTEM LOAD (DPM) RESPONSE

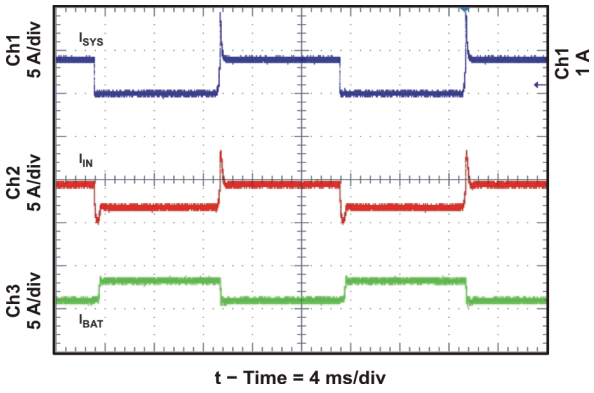


Figure 15.

CHARGE CURRENT REGULATION VS BAT VOLTAGE

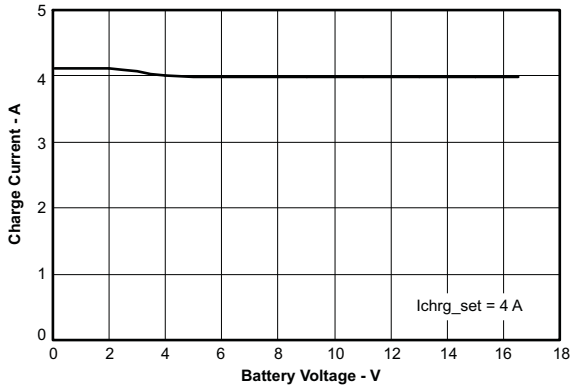


Figure 16.

EFFICIENCY VS BATTERY CHARGE CURRENT

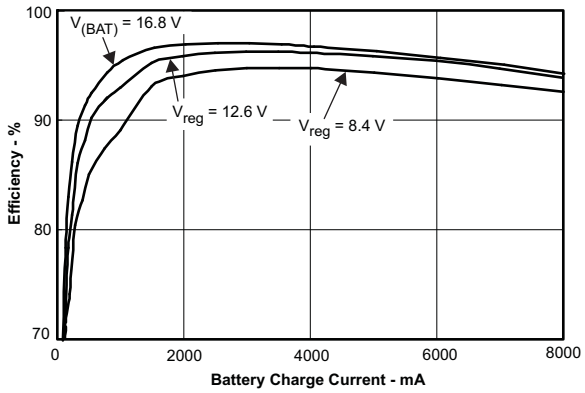
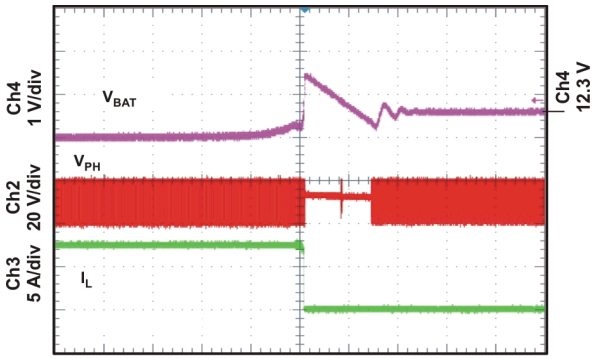


Figure 17.

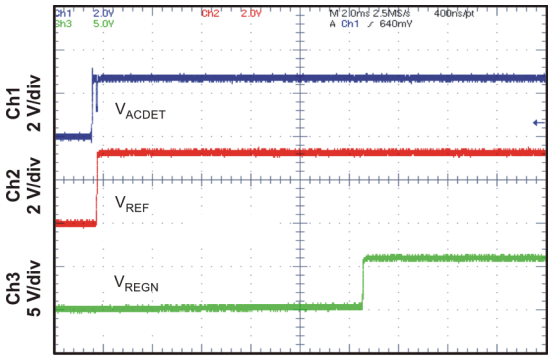
BATTERY REMOVAL



t – Time = 5 ms/div

Figure 18.

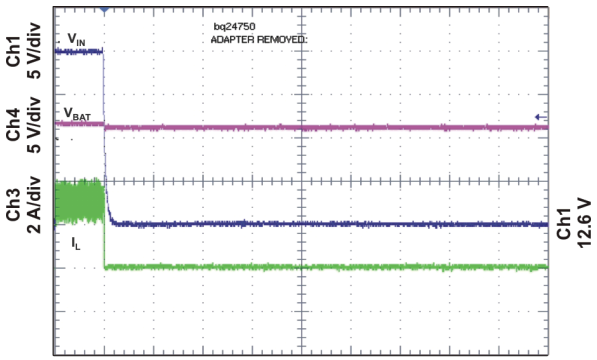
REF AND REGN STARTUP



t – Time = 2 ms/div

Figure 19.

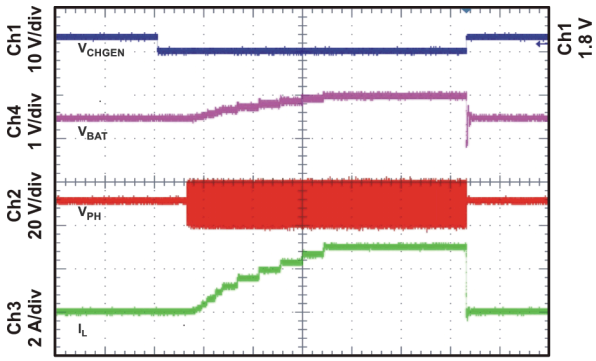
CHARGER ON ADAPTER REMOVAL



t – Time = 200 µs/div

Figure 20.

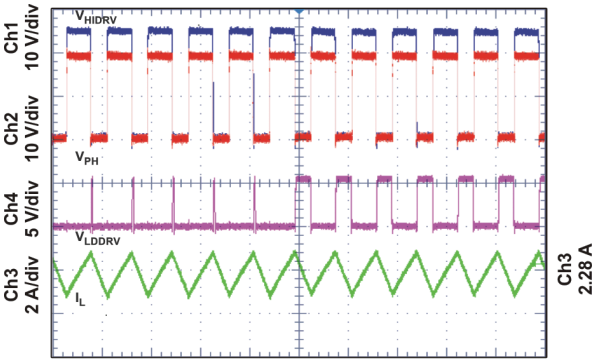
CHARGE ENABLE / DISABLE AND CURRENT SOFT-START



t – Time = 4 ms/div

Figure 21.

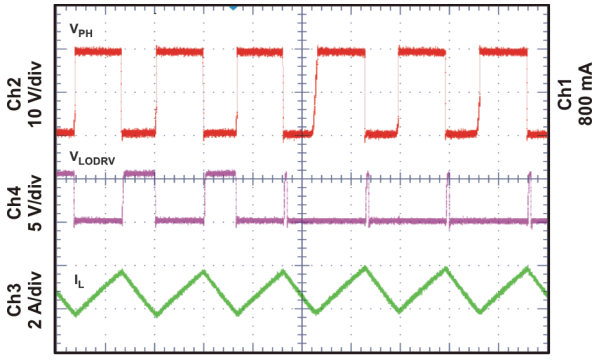
NONSYNCHRONOUS TO SYNCHRONOUS TRANSITION



t – Time = 4 µs/div

Figure 22.

SYNCHRONOUS TO NONSYNCHRONOUS TRANSITION



t – Time = 2 µs/div

Figure 23.

NEAR 100% DUTY CYCLE BOOTSTRAP RECHARGE PULSE

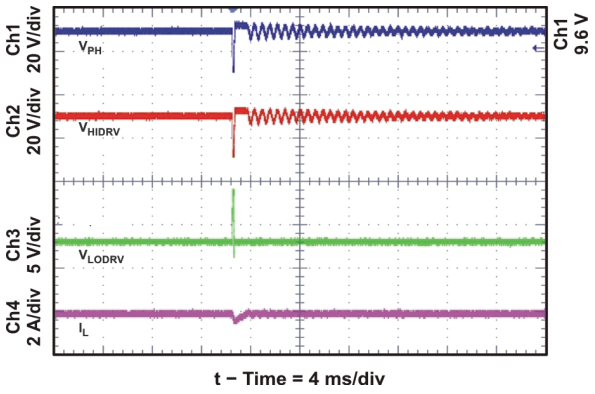


Figure 24.

BATTERY SHORTED CHARGER RESPONSE, OVERCURRENT PROTECTION (OCP) AND CHARGE CURRENT REGULATION

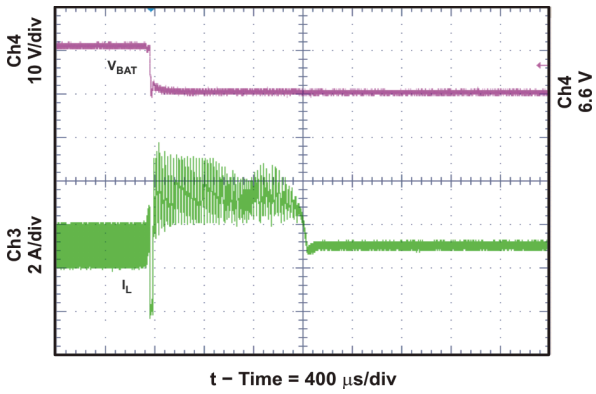


Figure 25.

CONTINUOUS CONDUCTION MODE (CCM) SWITCHING WAVEFORMS

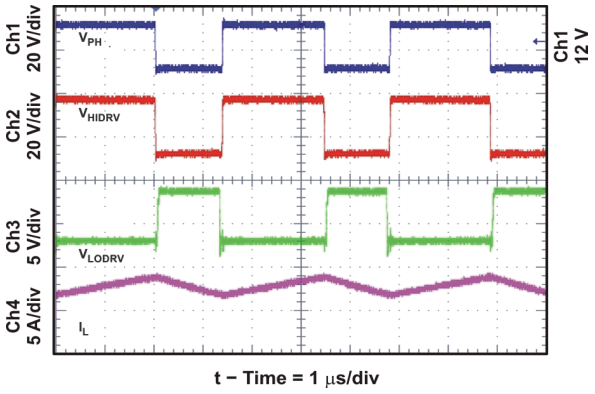


Figure 26.

DISCONTINUOUS CONDUCTION MODE (DCM) SWITCHING WAVEFORMS

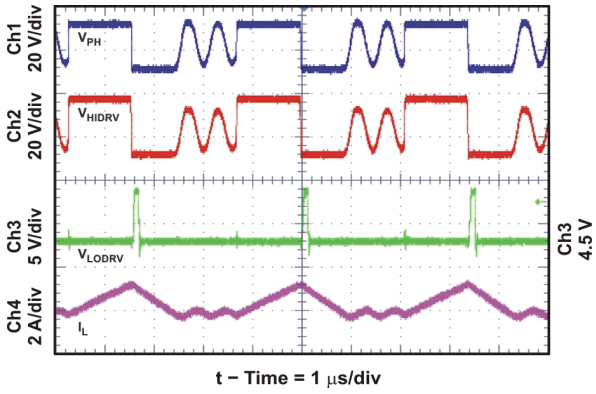
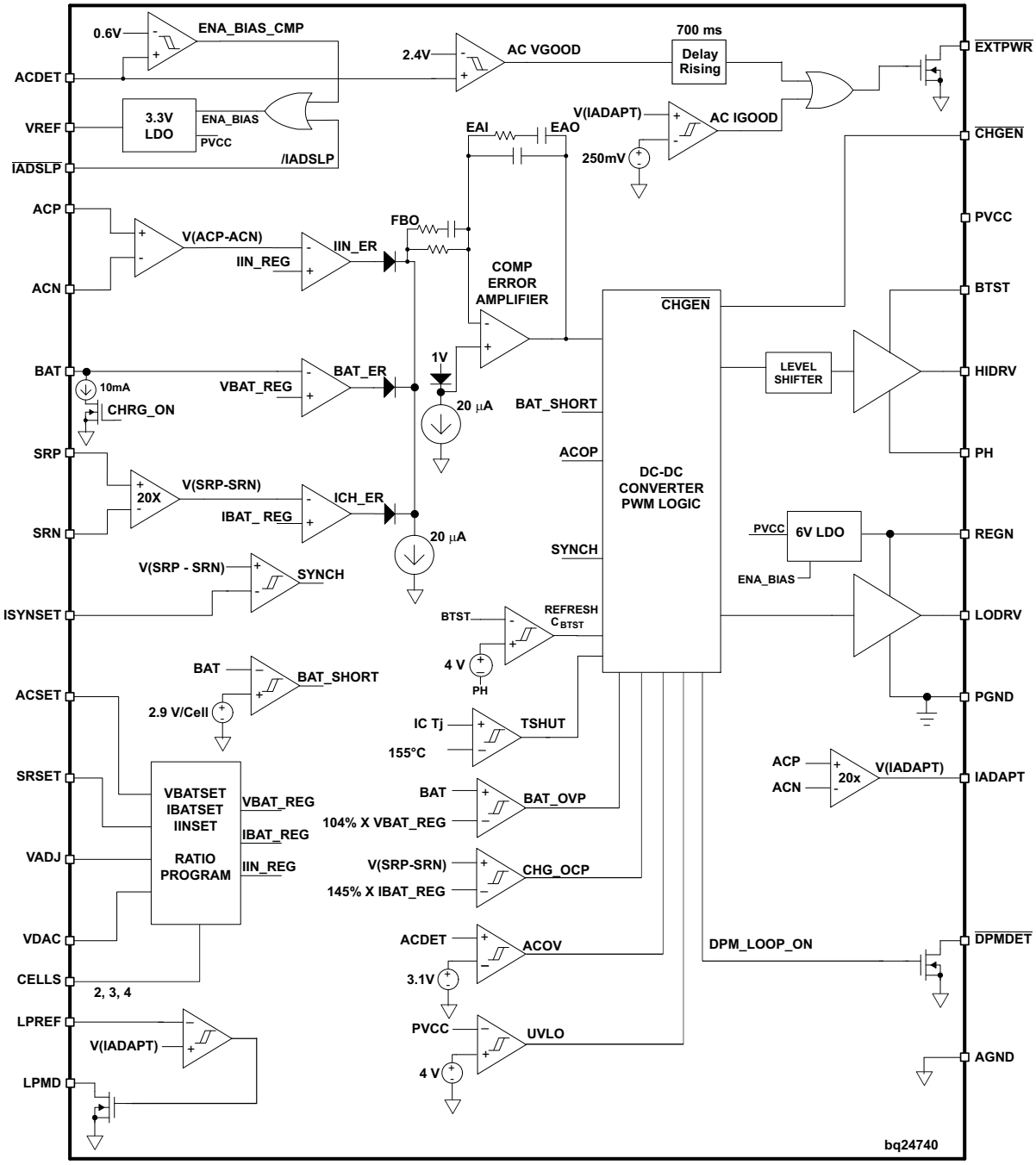


Figure 27.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATIONS

DETAILED DESCRIPTION

BATTERY VOLTAGE REGULATION

The bq24740 uses a high-accuracy voltage regulator for charging voltage. Internal default battery voltage setting V_{BATT}=4.2 V × cell count. The regulation voltage is ratio-metric with respect to VADC. The ratio of VADJ and VDAC provides extra 12.5% adjust range on V_{BATT} regulation voltage. By limiting the adjust range to 12.5% of the regulation voltage, the external resistor mismatch error is reduced from ±1% to ±0.1%. Therefore, an overall voltage accuracy as good as 0.5% is maintained, while using 1% mis-match resistors. Ratio-metric conversion also allows compatibility with D/As or microcontrollers (µC). The battery voltage is programmed through VADJ and VDAC using Equation 1.

$$V_{BATT} = \text{cell count} \times \left[4V + \left(0.5 \times \frac{V_{VADJ}}{V_{VDAC}} \right) \right] \quad (1)$$

The input voltage range of VDAC is between 2.6 V and 3.6 V. VADJ is set between 0 and VDAC. V_{BATT} defaults to 4.2 V × cell count when VADJ is connected to REGN.

CELLS pin is the logic input for selecting cell count. Connect CELLS to charge 2,3, or 4 Li+ cells. When charging other cell chemistries, use CELLS to select an output voltage range for the charger.

CELLS	CELL COUNT
Float	2
AGND	3
VREF	4

The per-cell battery termination voltage is function of the battery chemistry. Consult the battery manufacturer to determine this voltage.

The BAT pin is used to sense the battery voltage for voltage regulation and should be connected as close to the battery as possible, or directly on the output capacitor. A 0.1-µF ceramic capacitor from BAT to AGND is recommended to be as close to the BAT pin as possible to decouple high frequency noise.

BATTERY CURRENT REGULATION

The SRSET input sets the maximum charging current. Battery current is sensed by resistor R_{SR} connected between SRP and SRN. The full-scale differential voltage between SRP and SRN is 100 mV. Thus, for a 0.010 Ω sense resistor, the maximum charging current is 10 A. SRSET is ratio-metric with respect to VDAC using Equation 2:

$$I_{CHARGE} = \frac{V_{SRSET}}{V_{VDAC}} \times \frac{0.10}{R_{SR}} \quad (2)$$

The input voltage range of SRSET is between 0 and V_{DAC}, up to 3.6 V.

The SRP and SRN pins are used to sense across R_{SR} with default value of 10 mΩ. However, resistors of other values can also be used. For a larger the sense resistor, you get a larger sense voltage, and a higher regulation accuracy; but, at the expense of higher conduction loss.

INPUT ADAPTER CURRENT REGULATION

The total input from an AC adapter or other DC sources is a function of the system supply current and the battery charging current. System current normally fluctuates as portions of the systems are powered up or down. Without Dynamic Power Management (DPM), the source must be able to supply the maximum system current and the maximum charger input current simultaneously. By using DPM, the input current regulator reduces the charging current when the input current exceeds the input current limit set by ACSET. The current capability of the AC adapter can be lowered, reducing system cost.

Similar to setting battery regulation current, adapter current is sensed by resistor R_{AC} connected between ACP and ACN. Its maximum value is set ACSET, which is ratio-metric with respect to VDAC, using Equation 3.

$$I_{ADAPTER} = \frac{V_{ACSET}}{V_{VDAC}} \times \frac{0.10}{R_{AC}} \quad (3)$$

The input voltage range of ACSET is between 0 and V_{DAC}, up to 3.6 V.

The ACP and ACN pins are used to sense R_{AC} with default value of 10mΩ. However, resistors of other values can also be used. For a larger the sense resistor, you get a larger sense voltage, and a higher regulation accuracy; but, at the expense of higher conduction loss.

ADAPTER DETECT AND POWER UP

An external resistor voltage divider attenuates the adapter voltage before it goes to ACDET. The adapter detect threshold should typically be programmed to a value greater than the maximum battery voltage and lower than the minimum allowed adapter voltage. The ACDET divider should be placed before the ACFET in order to sense the true adapter input voltage whether the ACFET is on or off. Before adapter is detected, BATFET stays on and ACFET turns off.

If PVCC is below 5 V, the device is disabled, and both ACFET and BATFET turn off.

If ACDET is below 0.6 V but PVCC is above 5 V, part of the bias is enabled, including a crude bandgap reference, ACFET drive and BATFET drive. IADAPT is disabled and pulled down to GND. The total quiescent current is less than 10μA.

Once ACDET rises above 0.6 V and PVCC is above 5 V, all the bias circuits are enabled and REGN output goes to 6 V and VREF goes to 3.3 V. IADAPT becomes valid to proportionally reflect the adapter current.

When ACDET keeps rising and passes 2.4 V, a valid AC adapter is present. 500ms later, the following occurs:

- ACGOOD becomes high through external pull-up resistor to the host digital voltage rail;
- Charger turns on if all the conditions are satisfied and STAT becomes valid. (refer to *Enable and Disable Charging*)

ENABLE AND DISABLE CHARGING

The following conditions have to be valid before charge is enabled:

- $\overline{\text{CHGEN}}$ is LOW;
- Adapter is detected;
- Adapter is higher than PVCC-BAT threshold;
- Adapter is not over voltage;
- 500ms delay is complete after adapter detected;
- REGNGOOD and VREFGOOD are valid;
- Thermal Shut (TSHUT) is not valid;

One of the following conditions will stop on-going charging:

- $\overline{\text{CHGEN}}$ is HIGH;
- Adapter is removed;
- Adapter is less than 250mV above battery;
- Adapter is over voltage;
- Adapter is over current;
- TSHUT IC temperature threshold is reached (145°C on rising-edge with 15°C hysteresis).

AUTOMATIC INTERNAL SOFT-START CHARGER CURRENT

The charger automatically soft-starts the charger regulation current every time the charger is enabled to ensure there is no overshoot or stress on the output capacitors or the power converter. The soft-start consists of stepping-up the charge regulation current into 8 evenly divided steps up to the programmed charge current. Each step lasts around 1ms, for a typical rise time of 8 ms. No external components are needed for this function.

CONVERTER OPERATION

The synchronous buck PWM converter uses a fixed frequency (300 kHz) voltage mode with feed-forward control scheme. A type III compensation network allows using ceramic capacitors at the output of the converter. The compensation input stage is connected internally between the feedback output (FBO) and the error amplifier input (EAI). The feedback compensation stage is connected between the error amplifier input (EAI) and error amplifier output (EAO). The LC output filter is selected to give a resonant frequency of 8–12.5 kHz nominal.

Where resonant frequency, f_o, is given by: $$f_o = \frac{1}{2\pi\sqrt{L_o C_o}}$$ where (from Figure 1 schematic)

- C_O = C11 + C12
- L_O = L1

An internal saw-tooth ramp is compared to the internal EAO error control signal to vary the duty-cycle of the converter. The ramp height is one-fifteenth of the input adapter voltage making it always directly proportional to the input adapter voltage. This cancels out any loop gain variation due to a change in input voltage, and simplifies the loop compensation. The ramp is offset by 250 mV in order to allow zero percent duty-cycle, when the EAO signal is below the ramp. The EAO signal is also allowed to exceed the saw-tooth ramp signal in order to get a 100% duty-cycle PWM request. Internal gate drive logic allows achieving 99.98% duty-cycle while ensuring the N-channel upper device always has enough voltage to stay fully on. If the BTST pin to PH pin voltage falls below 4 V for more than 3 cycles, then the high-side n-channel power MOSFET is turned off and the low-side n-channel power MOSFET is turned on to pull the PH node down and recharge the BTST capacitor. Then the high-side driver returns to 100% duty-cycle operation until the (BTST-PH) voltage is detected to fall low again due to leakage current discharging the BTST capacitor below the 4 V, and the reset pulse is reissued.

The 300 kHz fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current, and temperature, simplifying output filter design and keeping it out of the audible noise region. The charge current sense resistor R_{SR} should be placed with at least half or more of the total output capacitance placed before the sense resistor contacting both sense resistor and the output inductor; and the other half or remaining capacitance placed after the sense resistor. The output capacitance should be divided and placed onto both sides of the charge current sense resistor. A ratio of 50:50 percent gives the best performance; but the node in which the output inductor and sense resistor connect should have a minimum of 50% of the total capacitance. This capacitance provides sufficient filtering to remove the switching noise and give better current sense accuracy. The type III compensation provides phase boost near the cross-over frequency, giving sufficient phase margin.

SYNCHRONOUS AND NON-SYNCHRONOUS OPERATION

The charger operates in non-synchronous mode when the sensed charge current is below the ISYNSET value. Otherwise, the charger operates in synchronous mode.

During synchronous mode, the low-side n-channel power MOSFET is on, when the high-side n-channel power MOSFET is off. The internal gate drive logic ensures there is break-before-make switching to prevent shoot-through currents. During the 30ns dead time where both FETs are off, the back-diode of the low-side power MOSFET conducts the inductor current. Having the low-side FET turn-on keeps the power dissipation low, and allows safely charging at high currents. During synchronous mode the inductor current is always flowing and operates in Continuous Conduction Mode (CCM), creating a fixed two-pole system.

During non-synchronous operation, after the high-side n-channel power MOSFET turns off, and after the break-before-make dead-time, the low-side n-channel power MOSFET will turn-on for around 80ns, then the low-side power MOSFET will turn-off and stay off until the beginning of the next cycle, where the high-side power MOSFET is turned on again. The 80ns low-side MOSFET on-time is required to ensure the bootstrap capacitor is always recharged and able to keep the high-side power MOSFET on during the next cycle. This is important for battery chargers, where unlike regular dc-dc converters, there is a battery load that maintains a voltage and can both source and sink current. The 80-ns low-side pulse pulls the PH node (connection between high and low-side MOSFET) down, allowing the bootstrap capacitor to recharge up to the REGN LDO value. After the 80 ns, the low-side MOSFET is kept off to prevent negative inductor current from occurring. The inductor current is blocked by the off low-side MOSFET, and the inductor current will become discontinuous. This mode is called Discontinuous Conduction Mode (DCM).

During the DCM mode the loop response automatically changes and has a single pole system at which the pole is proportional to the load current, because the converter does not sink current, and only the load provides a current sink. This means at very low currents the loop response is slower, as there is less sinking current available to discharge the output voltage. At very low currents during non-synchronous operation, there may be a small amount of negative inductor current during the 80 ns recharge pulse. The charge should be low enough to be absorbed by the input capacitance.

Whenever the converter goes into 0% duty-cycle mode, and BTST – PH < 4 V, the 80-ns recharge pulse occurs on LODRV, the high-side MOSFET does not turn on, and the low-side MOSFET does not turn on (no 80-ns recharge pulse), and there is no discharge from the battery.

ISYNSET CONTROL (CHARGE UNDER-CURRENT)

In bq24740, ISYN is internally set as the charge current threshold at which the charger changes from non-synchronous operation into synchronous operation. The low side driver turns on for only 80 ns to charge the boost cap. This is important to prevent negative inductor current, which may cause a boost effect in which the input voltage increases as power is transferred from the battery to the input capacitors. This can lead to an over-voltage on the PVCC node and potentially cause some damage to the system. This programmable value allows setting the current threshold for any inductor current ripple, and avoiding negative inductor current. The minimum synchronous threshold should be set from ½ the inductor current ripple to the full ripple current, where the inductor current ripple is given by

$$\frac{I_{RIPPLE_MAX}}{2} \le I_{SYN} \le I_{RIPPLE_MAX}$$

$$\text{and} \quad I_{RIPPLE_MAX} = \frac{\left(V_{IN_MAX} - V_{BAT_MIN}\right) \times \left(\frac{V_{BAT_MIN}}{V_{IN_MAX}}\right) \times \left(\frac{1}{f_S}\right)}{L_{MIN}} \tag{4}$$

where

V_{IN_MAX}: maximum adapter voltage
V_{BAT_MIN}: minimum BAT voltage
f_S: switching frequency
L_{MIN}: minimum output inductor

The ISYNSET comparator, or charge under-current comparator, compares the voltage between SRP-BAT and internal threshold on the cycle-to-cycle base. The threshold is set to 13 mV on the falling edge with 8 mV hysteresis on the rising edge with 10% variation.

HIGH ACCURACY IADAPT USING CURRENT SENSE AMPLIFIER (CSA)

An industry standard, high accuracy current sense amplifier (CSA) is used to monitor the input current by the host or some discrete logic through the analog voltage output of the IADAPT pin. The CSA amplifies the input sensed voltage of ACP – ACN by 20x through the IADAPT pin. The IADAPT output is a voltage source 20 times the input differential voltage. Once PVCC is above 5 V and ACDET is above 0.6V, IADAPT no longer stays at ground, but becomes active. If the user wants to lower the voltage, they could use a resistor divider from IOUT to AGND, and still achieve accuracy over temperature as the resistors can be matched their thermal coefficients.

A 200-pF capacitor connected on the output is recommended for decoupling high-frequency noise. An additional RC filter is optional, after the 200-pF capacitor, if additional filtering is desired. Note that adding filtering also adds additional response delay.

INPUT OVER VOLTAGE PROTECTION (ACOV)

ACOV provides protection to prevent system damage due to high input voltage. The controller enters ACOV when ACDET > 3.1 V. Charge is disabled, the adapter is disconnected from the system by turning off $\overline{\text{ACDRV}}$, and the battery is connected to the system by turning on $\overline{\text{BATDRV}}$. ACOV is not latched—normal operation resumes when the ACDET voltage returns below 3.1 V. ACOV threshold is 130% of the adapter-detect threshold.

INPUT UNDER VOLTAGE LOCK OUT (UVLO)

The system must have a minimum 5V PVCC voltage to allow proper operation. This PVCC voltage could come from either input adapter or battery, using a diode-OR input. When the PVCC voltage is below 5 V the bias circuits REGN and VREF stay inactive, even with ACDET above 0.6 V.

INPUT CURRENT LOW-POWER MODE DETECTION

In order to optimize the system performance, the HOST keeps an eye on the adapter current. Once the adapter current is above threshold set via LPREF, LPMD pin sends signal to HOST. The signal alarms the host that input power has exceeded the programmed limit, allowing the host to throttle back system power by reducing clock frequency, lowering rail voltages, or disabling certain parts of the system. The LPMD pin is an open-drain output. Connect a pull-up resistor to LPMD. The output is logic HI when the IADAPT output voltage (IADAPT = 20 x $V_{ACP-ACN}$) is lower than the LPREF input voltage. The LPREF threshold is set by an external resistor divider using VREF. A hysteresis can be programmed by a positive feedback resistor from LPMD pin to the LPREF pin.

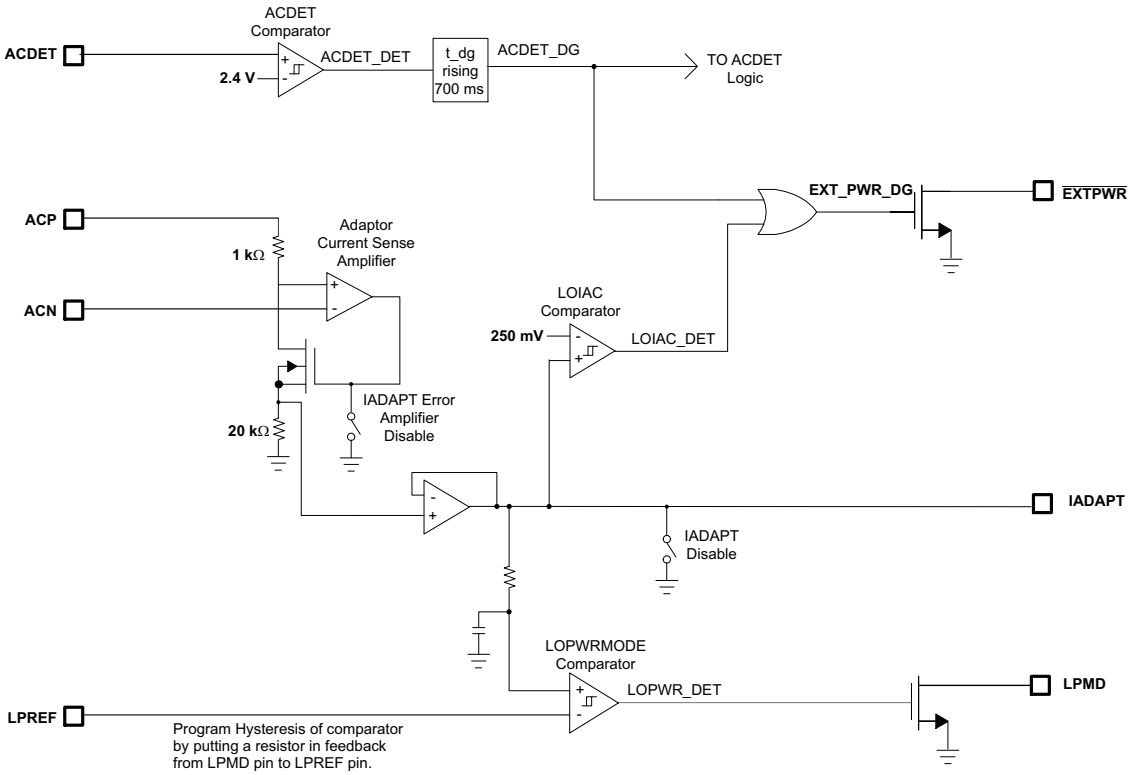


Figure 28. $\overline{\text{EXTPWR}}$, LPREF and LPMD Logic

BATTERY OVER-VOLTAGE PROTECTION

The converter stops switching when BAT voltage goes above 104% of the regulation voltage. The converter will not allow the high-side FET to turn on until the BAT voltage goes below 102% of the regulation voltage. This allows one-cycle response to an overvoltage condition, such as when the load is removed or the battery is disconnected. A 10-mA current sink from BAT to PGND is on only during charge, and allows discharging the stored output-inductor energy into the output capacitors.

CHARGE OVER-CURRENT PROTECTION

The charger has a secondary over-current protection. It monitors the charge current, and prevents the current from exceeding 145% of regulated charge current. The high-side gate drive turns off when the over-current is detected, and automatically resumes when the current falls below the over-current threshold.

THERMAL SHUTDOWN PROTECTION

The QFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junctions temperatures low. As added level of protection, the charger converter turns off and self-protects whenever the junction temperature exceeds the TSHUT threshold of 145°C. The charger stays off until the junction temperature falls below 130°C.

Status Outputs ($\overline{\text{EXTPWR}}$, LPMD, $\overline{\text{DPMDET}}$ pin)

Four status outputs are available, and they all, except for LPMD, require external pull up resistors to pull the pins to system digital rail for a high level.

$\overline{\text{EXTPWR}}$ open-drain output goes low under either of the two conditions:

1. ACDET is above 2.4 V
2. Adapter current is above 1.25 A using a 10-mΩ sense resistor (IADAPT voltage above 250 mV). Internally, the AC current detect comparator looks between IADAPT and an internal 250-mV threshold. It indicates a good adapter is connected because of valid voltage or current.

STAT open-drain output goes low when charging. A high level on STAT indicates the charger is not charging; therefore, either, $\overline{\text{CHGEN}}$ pin is not low, or the charger is not able to charge because input voltage is still powering up and the 700-ms delay has not finished, or because of a fault condition such as overcurrent, input over voltage, or TSHUT over temperature.

LPMD push-pull output goes low when the input current is higher than the programmed threshold via LPREF pin. Hysteresis can be programmed by putting a resistor from LPREF pin to LPMD pin.

$\overline{\text{DPMDET}}$ open-drain output goes low when the DPM loop is active to reduce the battery charge current (after a 10-ms delay).

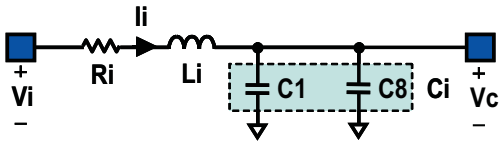
Table 2. Component List for Typical System Circuit of Figure 1

PART DESIGNATOR	QTY	DESCRIPTION
Q1, Q2, Q3	3	P-channel MOSFET, –30V,-6A, SO-8, Vishay-Siliconix, Si4435
Q4, Q2	2	N-channel MOSFET, 30V, 12.5A, SO-8, Fairchild, FDS6680A
D1	1	Diode, Dual Schottky, 30V, 200mA, SOT23, Fairchild, BAT54C
R_{AC}, R_{SR}	2	Sense Resistor, 10 mΩ, 1%, 1W, 2010, Vishay-Dale, WSL2010R0100F
L1	1	Inductor, 10µH, 7A, 31mΩ, Vishay-Dale, IHLP5050FD-01
C1, C6, C7, C11, C12	5	Capacitor, Ceramic, 10µF, 35V, 20%, X5R, 1206, Panasonic, ECJ-3YB1E106M
C4, C8, C10	3	Capacitor, Ceramic, 1µF, 25V, 10%, X7R, 2012, TDK, C2012X7R1E105K
C2, C3, C9, C13, C14, C15	6	Capacitor, Ceramic, 0.1µF, 50V, 10%, X7R, 0805, Kemet, C0805C104K5RACTU
R3, R4, R5	4	Resistor, Chip, 10 kΩ, 1/16W, 5%, 0402
R1	1	Resistor, Chip, 432 kΩ, 1/16W, 1%, 0402
R2	1	Resistor, Chip, 66.5 kΩ, 1/16W, 1%, 0402
R6	1	Resistor, Chip, 33 kΩ, 1/16W, 1%, 0402
R7	1	Resistor, Chip, 200 kΩ, 1/16W, 1%, 0402
R8	1	Resistor, Chip, 24.9 kΩ, 1/16W, 1%, 0402
R9	1	Resistor, Chip, 1.8 MΩ, 1/16W, 1%, 0402

APPLICATION INFORMATION

Input Capacitance Calculation

During the adapter hot plug-in, the $\overline{ACDRV}$ has not been enabled. The AC switch is off and the simplified equivalent circuit of the input is shown in Figure 29.



A. Ri and Li are the equivalent input inductance and resistance. C1 and C8 are the input capacitance.

Figure 29. Simplified Equivalent Circuit During Adapter Insertion

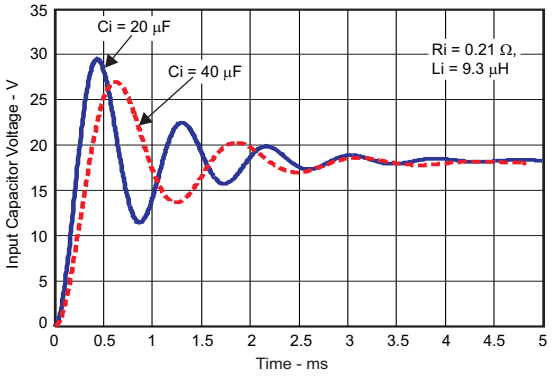
The voltage on the input capacitor(s) is given by:

$$V_C(t) = V_C(0) + \frac{V_i \cdot \omega}{Z_0 \cdot C_i \cdot \omega_0^2} + \frac{V_i}{Z_0 \cdot C_i \cdot \omega_0^2} e^{-\frac{R_i}{2L_i}t} \left(-\frac{R_i}{2L_i} \sin \omega t - \omega \cdot \cos \omega t \right) \quad (5)$$

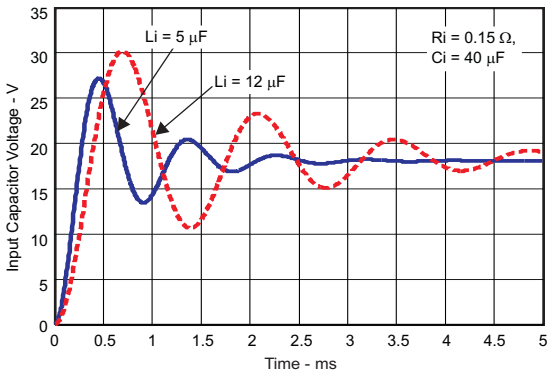
where $Z_0 = \sqrt{\frac{L_i}{C_i}}$, $\omega = \sqrt{\frac{1}{L_i C_i} - \left(\frac{R_i}{2L_i}\right)^2}$, and $\omega_0 = \sqrt{\frac{1}{L_i C_i}}$

APPLICATION INFORMATION (continued)

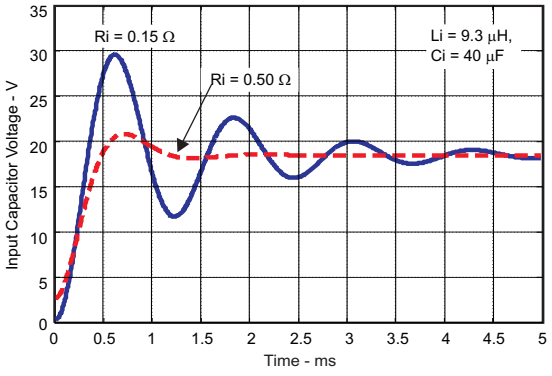
For a typical notebook charger application, the total stray inductance of the adapter output wire and the PCB connections is normally 5–12 µH, and the total effective resistance of the input connections is 0.15–0.5 Ω. Figure 30(a) demonstrates that a higher Ci helps to damp the voltage spike. Figure 30(b) demonstrates the effect of the input stray inductance Li on the input voltage spike. The dashed curve in Figure 30(b) represents the worst case for Ci=40 µF. Figure 30(c) shows how the resistance helps to suppress the input voltage spike.



(a) Vc with various Ci values



(b) Vc with various Li values



(c) Vc with various Ri values

Figure 30. Parametric Study Of The Input Voltage

Minimizing the input stray inductance, increasing the input capacitance and using high-ESR input capacitors helps to suppress the input voltage spike.

APPLICATION INFORMATION (continued)

Figure 31 shows the measured input voltages and currents with different input capacitances. The voltage spike drops by about 5 V after increasing Ci from 20 µF to 40 µF. The input voltage spike has been dramatically damped by using a 47 F electrolytic capacitor.

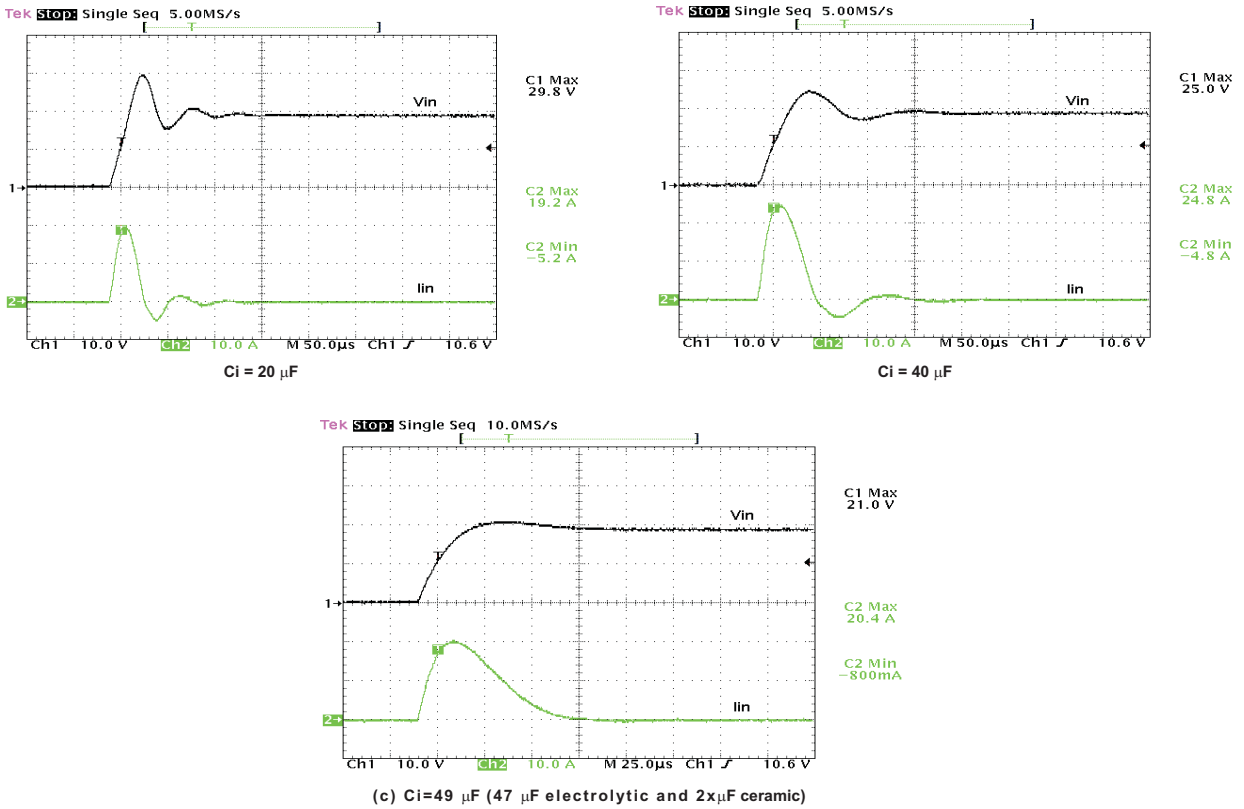


Figure 31. Adapter DC Side Hot Plug-In With Various Input Capacitances

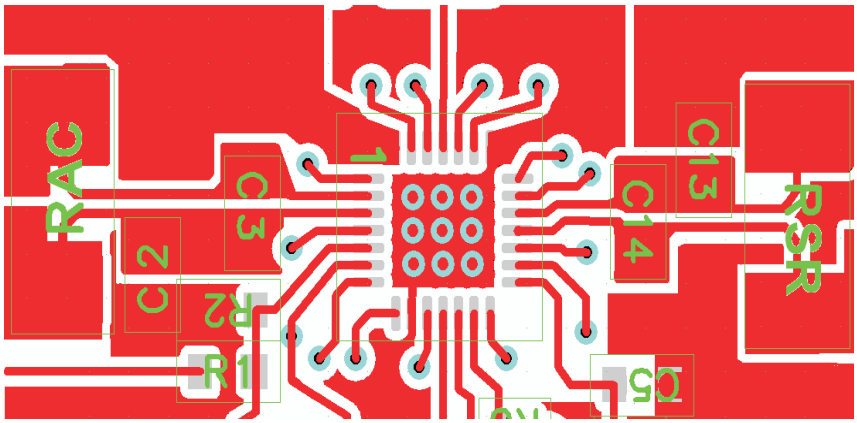
Since the input voltage to the IC is PVCC which is 0.7 V (diode voltage drop) lower than Vc during the adapter insertion, a 40-µF input capacitance is normally adequate to keep the PVCC voltage well below the maximum voltage rating under normal conditions. In case of a higher input stray inductance, the input capacitance may be increased accordingly. An electrolytic capacitor will help reduce the input voltage spike due to its high ESR.

APPLICATION INFORMATION (continued)

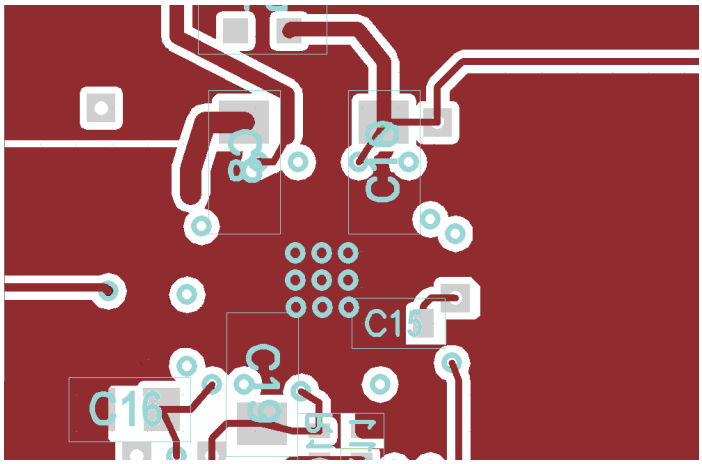
PCB Layout Design Guideline

1. It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
2. The control stage and the power stage should be routed separately. At each layer, the signal ground and the power ground are connected only at the power pad.
3. The AC current-sense resistor must be connected to ACP (pin 3) and ACN (pin 2) with a Kelvin contact. The area of this loop must be minimized. The decoupling capacitors for these pins should be placed as close to the IC as possible.
4. The charge-current sense resistor must be connected to SRP (pin 19), SRN (pin 18) with a Kelvin contact. The area of this loop must be minimized. The decoupling capacitors for these pins should be placed as close to the IC as possible.
5. Decoupling capacitors for PVCC (pin 28), VREF (pin 10), REGN (pin 24) should be placed underneath the IC (on the bottom layer) with the interconnections to the IC as short as possible.
6. Decoupling capacitors for BAT (pin 17), IADAPT (pin 15) must be placed close to the corresponding IC pins with the interconnections to the IC as short as possible.
7. Decoupling capacitor CX for the charger input must be placed very close to the Q4 drain and Q5 source.

Figure 32 shows the recommended component placement with trace and via locations.

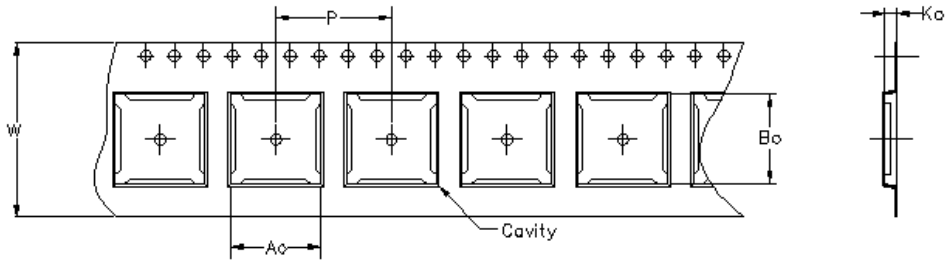


(a) Top Layer



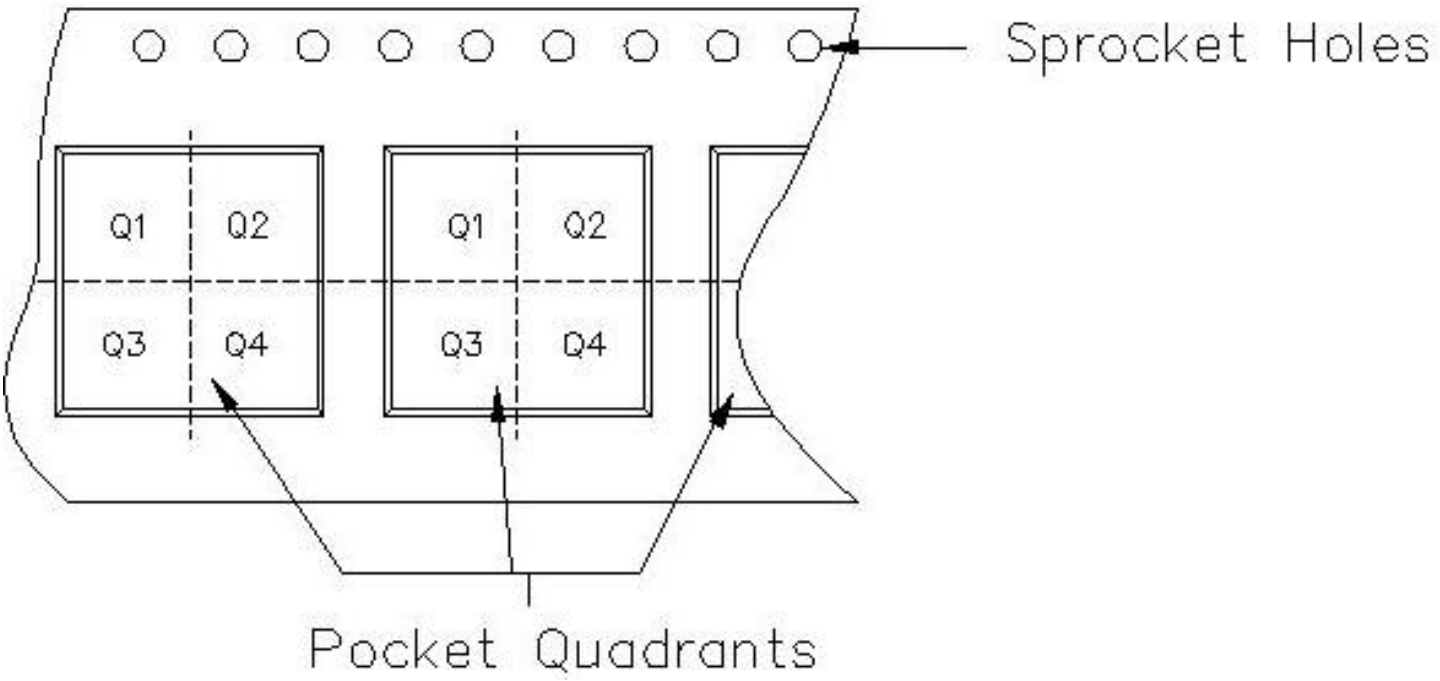
(b) Bottom Layer

Figure 32. Layout Example



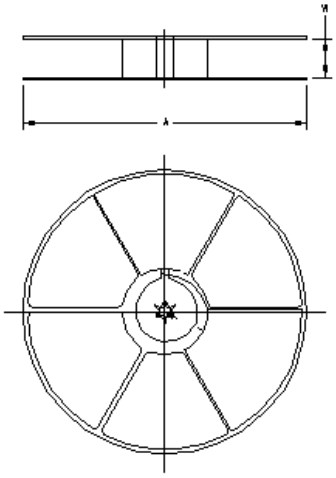
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



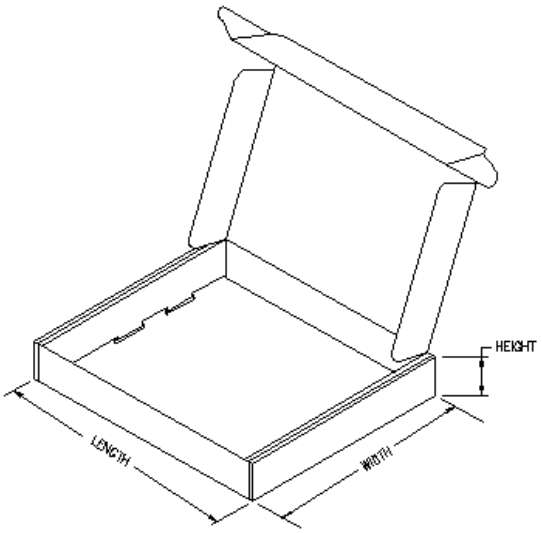
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24740RHDR	RHD	28	MLA	330	12	5.3	5.3	1.5	8	12	PKGORNT2TR-MSP
BQ24740RHDT	RHD	28	MLA	180	12	5.3	5.3	1.5	8	12	PKGORNT2TR-MSP

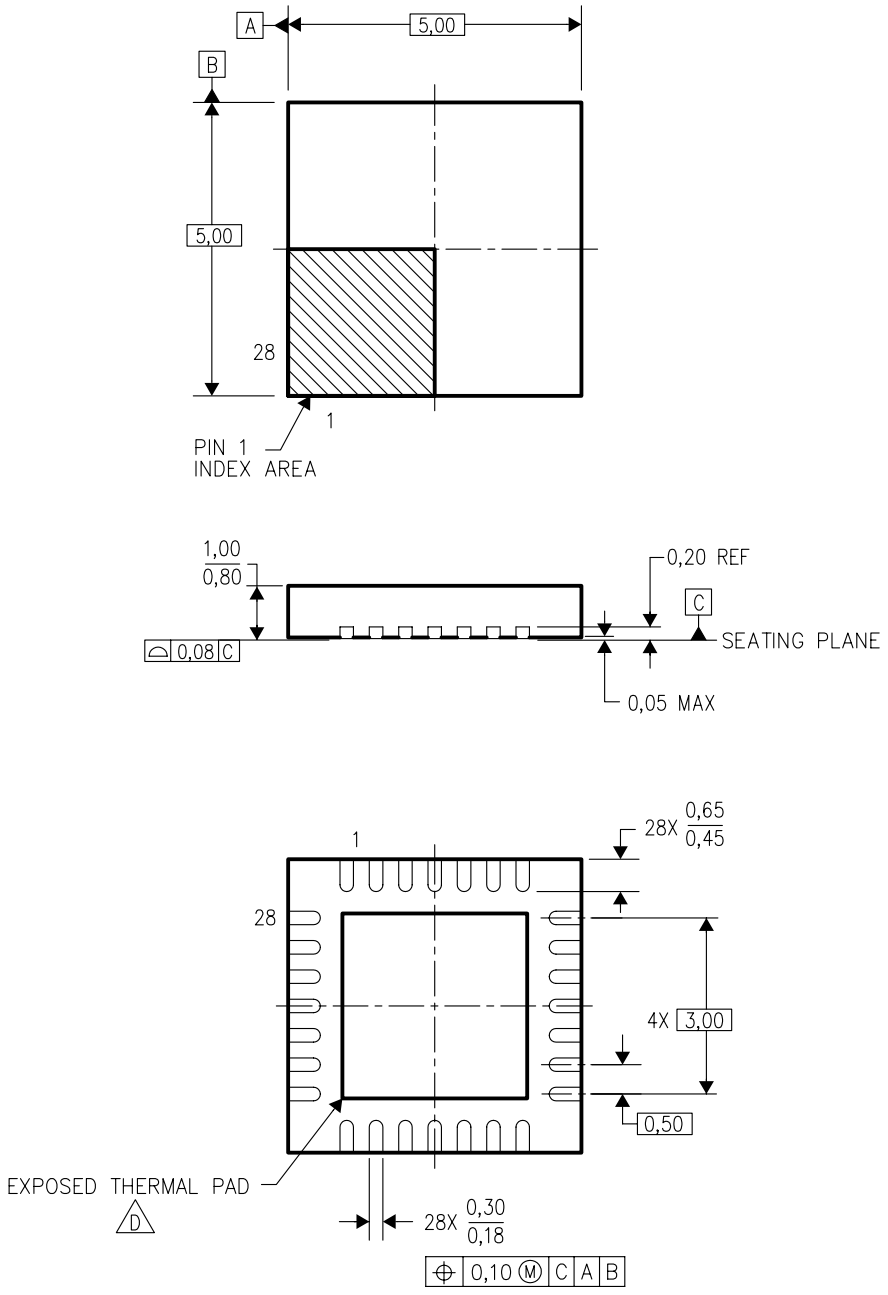


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
BQ24740RHDR	RHD	28	MLA	346.0	346.0	29.0
BQ24740RHDT	RHD	28	MLA	190.0	212.7	31.75


HEIGHT
LENGTH
WIDTH

RHD (S–PQFP–N28) PLASTIC QUAD FLATPACK



4204400/B 11/04

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

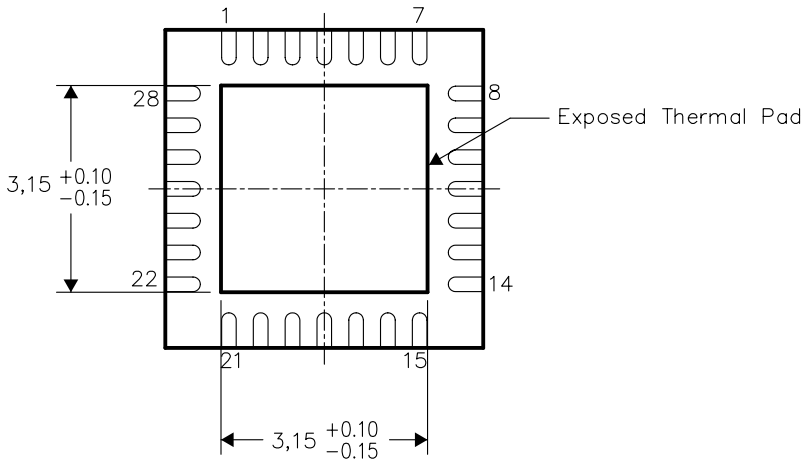
RHD (S–PQFP–N28)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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