MP2235S

High-Efficiency, 3 A, 16 V, 800 kHz Synchronous Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2235S is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a compact solution to achieve a 3 A continuous output current with excellent load and line regulation over a wide input supply range. The MP2235S has synchronous mode operation for higher efficiency over the output current load range.

Current mode operation provides fast transient response and eases loop stabilization.

Full protection features include over-current protection (OCP) and thermal shutdown (TSD).

The MP2235S requires a minimal number of readily available, standard, external components and is available in a space-saving 8-pin TSOT23 package.

FEATURES

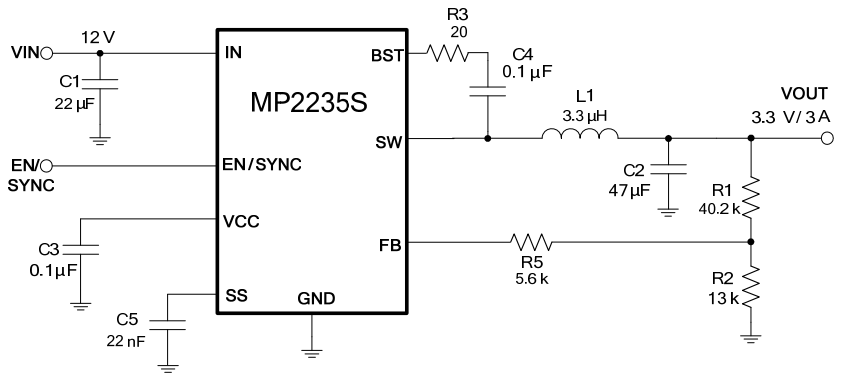
- Wide 4.5 V to 16 V Operating Input Range
- 120 mΩ/50 mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- High-Efficiency Synchronous Mode Operation
- Fixed 800 kHz Switching Frequency
- Synchronizes from a 300 kHz to a 2 MHz External Clock
- Power-Save Mode at Light Load
- External Soft-Start
- Over-Current Protection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.804 V
- Available in a 8-pin TSOT-23 Package

APPLICATIONS

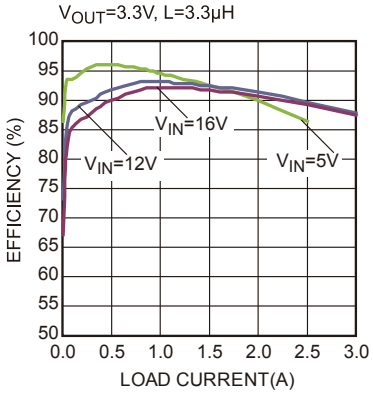
- Notebook Systems and I/O Power
- Digital Set-Top Boxes
- Flat-Panel Televisions and Monitors
- Distributed Power Systems

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.
"MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION



Efficiency vs. Load Current



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2235SGJ	TSOT23-8	*See Below*

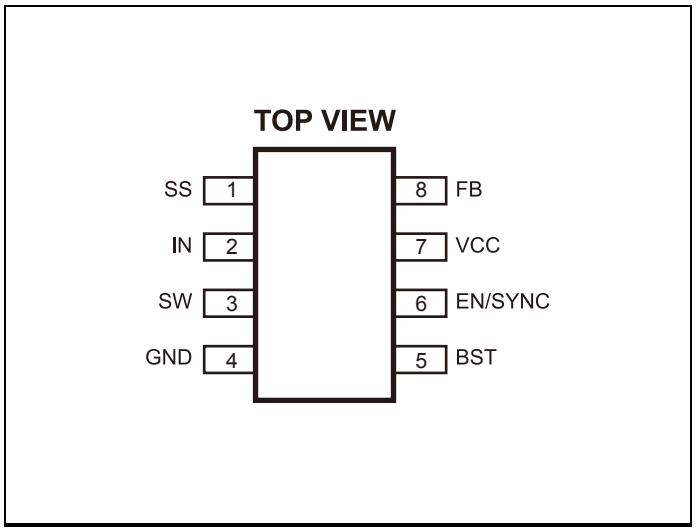
* For Tape & Reel, add suffix –Z (e.g. MP2235SGJ–Z)

TOP MARKING

AQAY

AQA: Product code of MP2235SGJ
Y: Year code

PACKAGE REFERENCE



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3 V to 17 V
V_{SW}.....-0.3 V (-5 V for <10 ns) to 17 V (19 V for < 10 ns)
V_{BST} ..... V_{SW} + 6 V
All other pins ..... -0.3 V to 6 V (2)
Continuous power dissipation (T_A = +25°C) (3)
..... 1.25 W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to 150°C

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) .....4.5 V to 16 V
Output voltage (V_{OUT}).....0.804 V to V_{IN} x D_{MAX}
Operating junction temp. (T_J).. -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

TSOT23-8	100	55 °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) For additional details on the absolute maximum rating of EN, please refer to the “Enable/SYNC Control” section on page 12.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12 V, T_J = -40°C to + 125°C[6], typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0 V, T_J= + 25°C			1	µA
		V_{EN} = 0 V, T_J = -40°C to + 125°C			5	µA
Supply current (quiescent)	I_q	V_{EN} = 2 V, V_{FB} = 1 V		0.5	1	mA
HS switch on resistance	HS_{RDS-ON}	V_{BST-SW} = 5 V		120		mΩ
LS switch on resistance	LS_{RDS-ON}	V_{CC} = 5 V		50		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0 V, V_{SW} = 12 V or 0 V			1	µA
Current limit	I_{LIMIT}	Under 40% duty cycle	4	5		A
Oscillator frequency	f_{SW}	V_{FB} = 0.75 V,T_J = + 25°C	620	800	900	kHz
		V_{FB} = 0.75 V, T_J = -40°C to +125°C	550	800	900	kHz
Foldback frequency	f_{FB}	V_{FB} < 400 mV		0.5		f_{SW}
Maximum duty cycle	D_{MAX}	V_{FB} = 700 mV		92		%
Minimum on time[7]	T_{ON_MIN}			40		ns
Sync frequency range	f_{SYNC}		0.3		2	MHz
Feedback voltage	V_{FB}	T_J = 25°C	788	804	820	mV
		T_J = -40°C to +125°C	784	804	824	mV
Feedback current	I_{FB}	V_{FB} = 830 mV		10	50	nA
EN rising threshold	V_{EN_RISING}		1	1.4	1.8	V
EN hysteresis	$V_{EN_Hysteresis}$			150		mV
EN input current	I_{EN}	V_{EN} = 2 V		2		µA
		V_{EN} = 0 V		0		µA
EN turn-off delay	EN_{td-off}			10		µs
VIN under-voltage lockout threshold—rising	$INUV_{Vth}$		3.5	3.9	4.3	V
VIN under-voltage lockout threshold—hysteresis	$INUV_{HYS}$			700		mV
VCC regulator	V_{CC}		4.6	5	5.4	V
VCC load regulation		I_{CC} = 5 mA		2		%
Soft-start current	I_{SS}		8	11	14	µA
Thermal shutdown [7]				150		°C
Thermal hysteresis [7]				20		°C

NOTES:

6) Not tested in production. Guaranteed by over-temperature correlation.

7) Guaranteed by design.

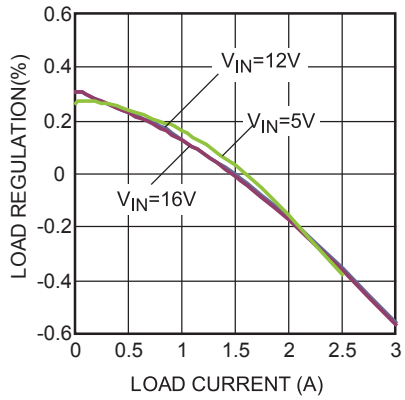
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the design example section.
V_{IN} = 12 V, V_{OUT} = 3.3 V, L = 3.3 µH, T_A = 25°C, unless otherwise noted.

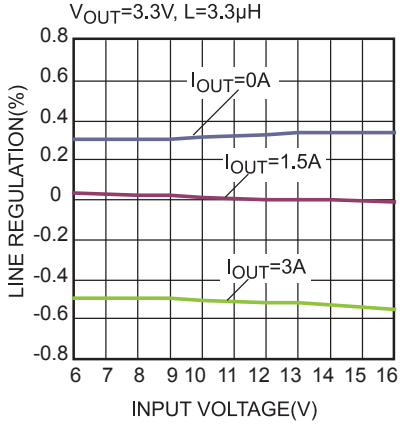
Load Regulation

V_{OUT}=3.3V, L=3.3µH

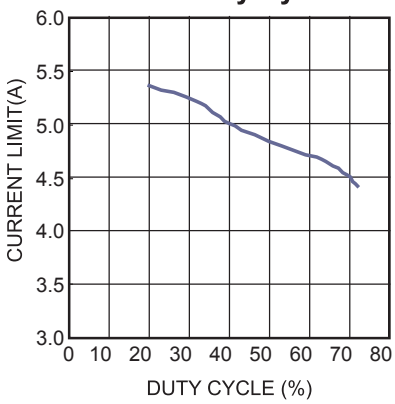


Line Regulation

V_{OUT}=3.3V, L=3.3µH

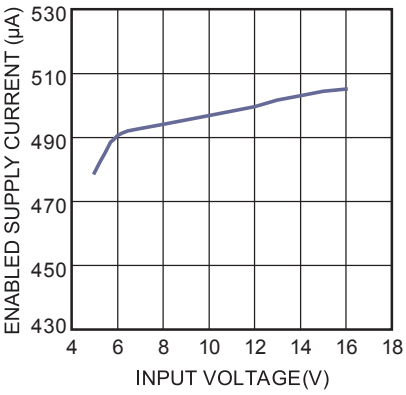


Inductor Peak Current Limit vs. Duty Cycle



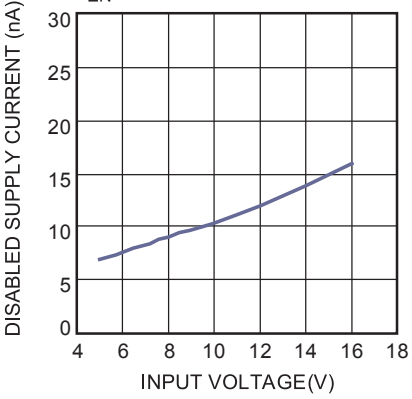
Enabled Supply Current vs. Input Voltage

V_{EN}=2V, V_{FB}=1V

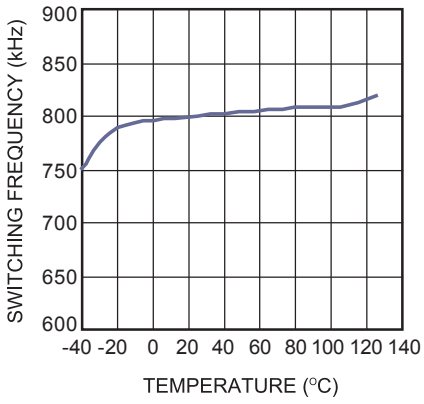


Disabled Supply Current vs. Input Voltage

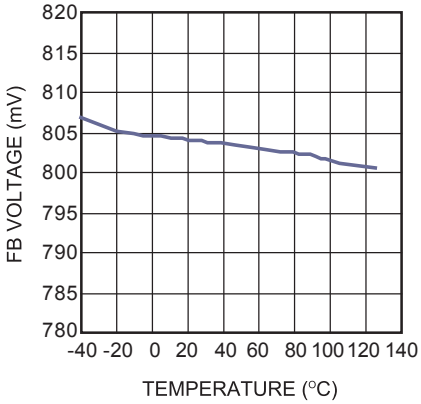
V_{EN}=0V



Switching Frequency vs. Temperature



FB Voltage vs. Temperature



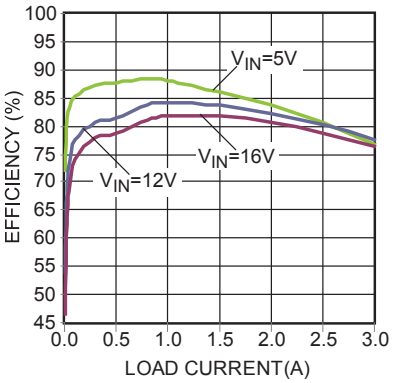
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the design example section. V_{IN} = 12 V, V_{OUT} = 3.3 V, L = 3.3 µH, T_A = 25°C, unless otherwise noted.

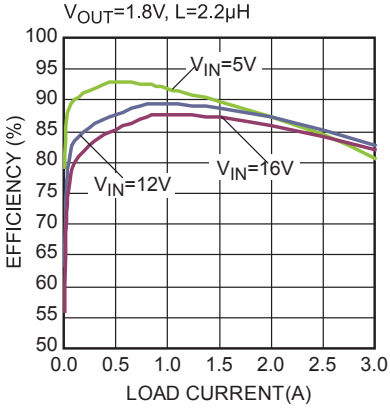
Efficiency vs. Load Current

V_{OUT}=1.2V, L=1µH



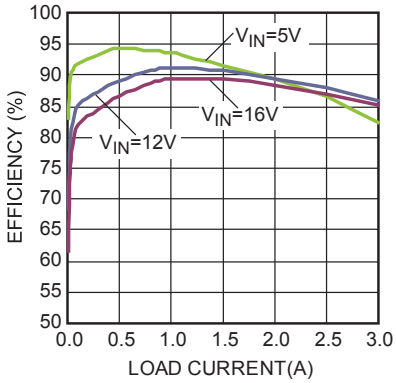
Efficiency vs. Load Current

V_{OUT}=1.8V, L=2.2µH



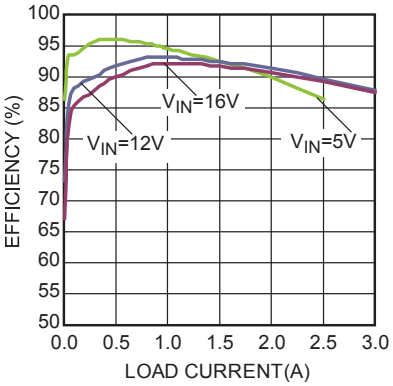
Efficiency vs. Load Current

V_{OUT}=2.5V, L=2.2µH



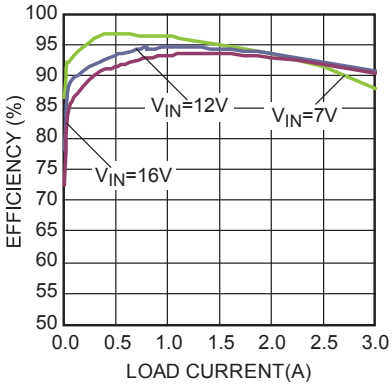
Efficiency vs. Load Current

V_{OUT}=3.3V, L=3.3µH



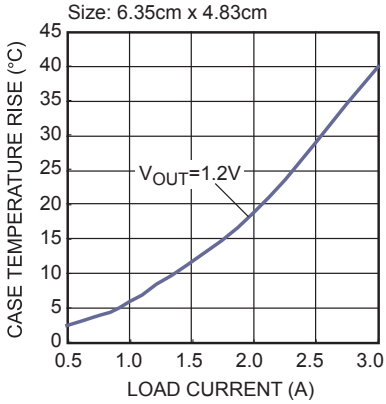
Efficiency vs. Load Current

V_{OUT}=5V, L=3.3µH



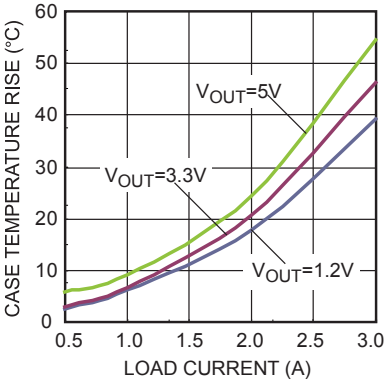
Case Temperature Rise vs. Load Current

V_{IN}=5V, 2 Layers PCB,
Size: 6.35cm x 4.83cm



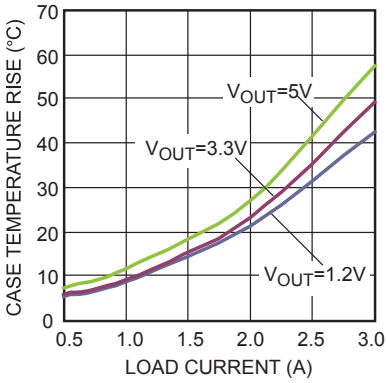
Case Temperature Rise vs. Load Current

V_{IN}=12V, 2 Layers PCB,
Size: 6.35cm x 4.83cm



Case Temperature Rise vs. Load Current

V_{IN}=16V, 2 Layers PCB,
Size: 6.35cm x 4.83cm

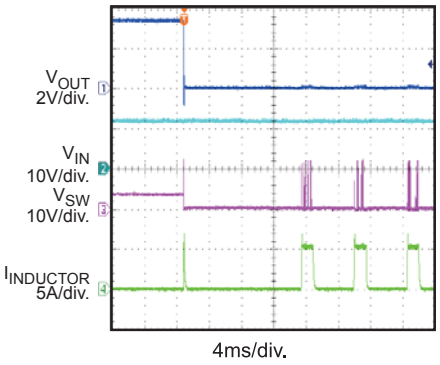


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

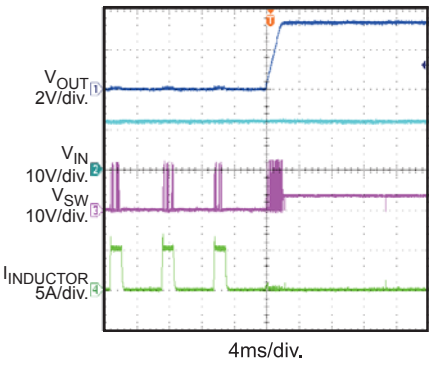
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the design example section.
V_{IN} = 12 V, V_{OUT} = 3.3 V, L = 3.3 µH, T_A = 25°C, unless otherwise noted.

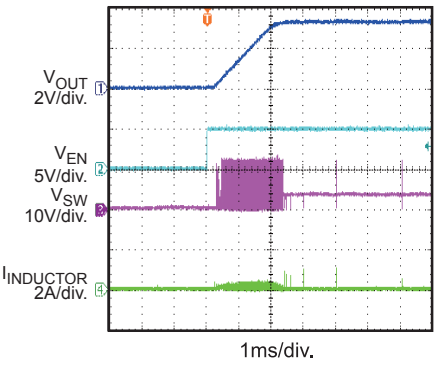
Short Entry
I_{OUT}=0A



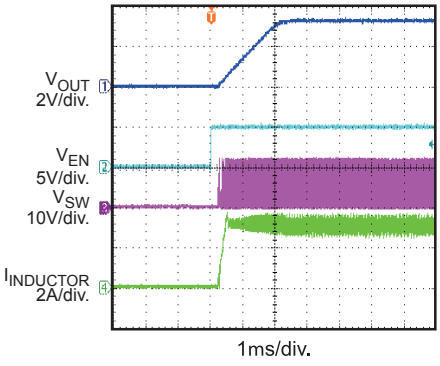
Short Recovery
I_{OUT}=0A



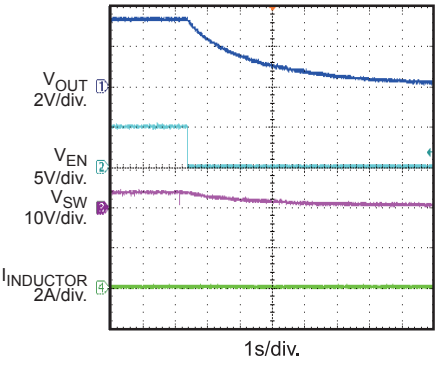
Start-Up through Enable
I_{OUT}=0A



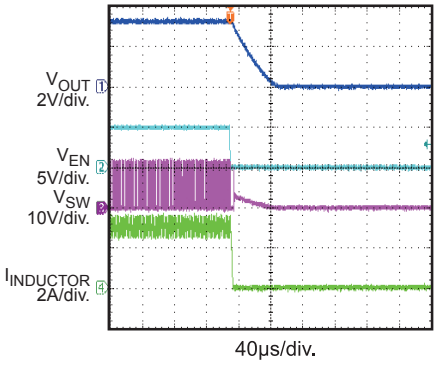
Start-Up through Enable
I_{OUT}=3A



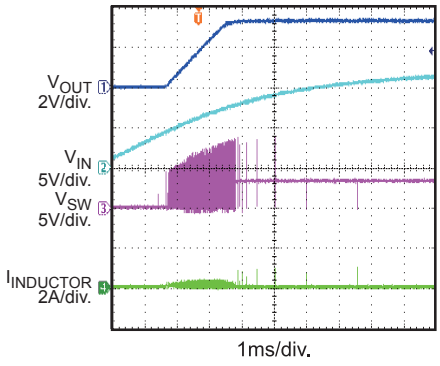
Shutdown through Enable
I_{OUT}=0A



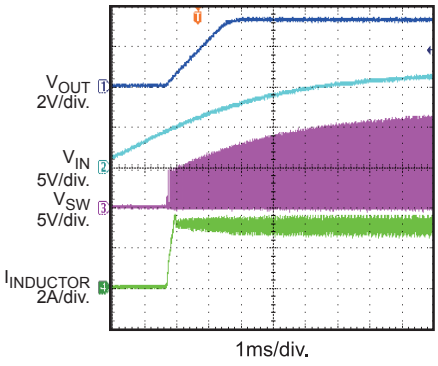
Shutdown through Enable
I_{OUT}=3A



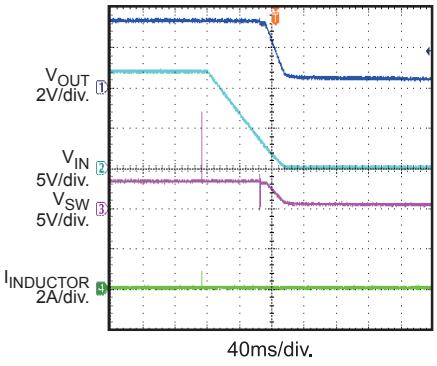
Start-Up through Input Voltage
I_{OUT}=0A



Start-Up through Input Voltage
I_{OUT}=3A



Shutdown through Input Voltage
I_{OUT}=0A

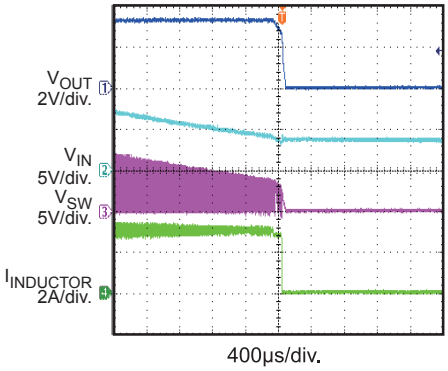


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

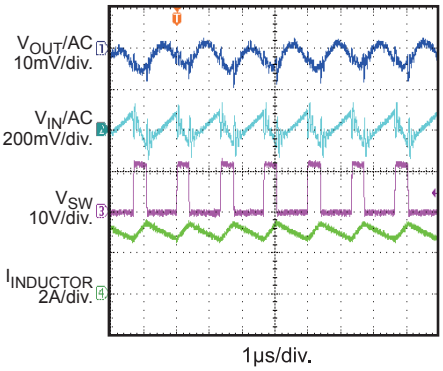
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the design example section.
V_{IN} = 12 V, V_{OUT} = 3.3 V, L = 3.3 µH, T_A = 25°C, unless otherwise noted.

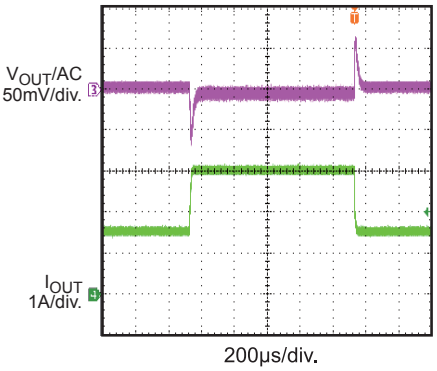
Shutdown through Input Voltage
I_{OUT}=3A



Input / Output Ripple
I_{OUT}=3A



Load Transient Reponse
I_{OUT}=1.5A to 3A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

PIN FUNCTIONS

Package Pin #	Name	Description
1	SS	**Soft start**. Connect an external capacitor to program the soft-start time for the switch mode regulator.
2	IN	**Supply voltage.** IN supplies power for the internal MOSFET and regulator. The MP2235S operates from a +4.5 V to +16 V input rail. IN requires a low ESR and low-inductance capacitor (C1) to decouple the input rail. Place the input capacitor very close to IN and connect it with wide PCB traces and multiple vias.
3	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to V_{IN} by the high-side switch during the PWM duty cycle on time. The inductor current drives SW negative during the off time. The on resistance of the low-side switch and the internal body diode fixes the negative voltage. Connect SW using wide PCB traces and multiple vias.
4	GND	**System ground.** GND is the reference ground of the regulated output voltage. PCB layout requires extra care. For best results, connect to GND with copper and vias.
5	BST	**Bootstrap.** Requires a capacitor connected between SW and BST to form a floating supply across the high-side switch driver.
6	EN/SYNC	**Enable.** EN=high to enable the MP2235S. Apply an external clock to change the switching frequency. For automatic start-up, connect EN to V_{IN} with a 100 kΩ resistor.
7	VCC	**Internal 5 V LDO output.** VCC powers the driver and control circuits. Decouple with a 0.1 µF to 0.22 µF capacitor. Do NOT use a capacitor ≥0.22 µF.
8	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 400 mV to prevent current limit runaway during a short-circuit fault. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

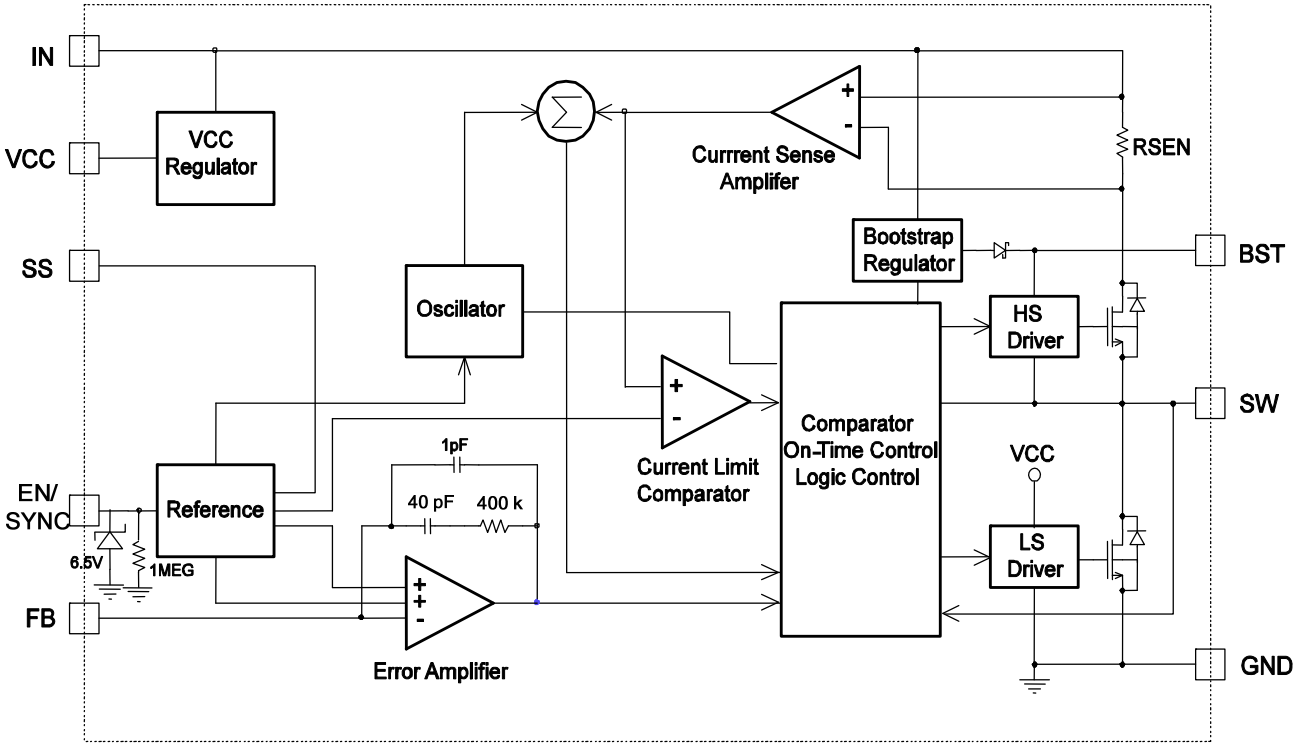


Figure 1—Functional block diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

OPERATION

The MP2235S is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a compact solution that achieves a 3 A continuous output current with excellent load and line regulation over a 4.5 V to 16 V input supply range.

The MP2235S has three working modes: advanced asynchronous modulation (AAM) mode, discontinuous conduction mode (DCM), and continuous conduction mode (CCM). The load current increases as the device transitions from AAM mode to DCM to CCM.

AAM Control Operation

In a light-load condition, the MP2235S works in advanced asynchronous modulation (AAM) mode (see Figure 2). The V_{AAM} is an internal fixed voltage when the input and output voltages are fixed. V_{COMP} is the error-amplifier output (which represents the peak inductor-current information). When V_{COMP} is lower than V_{AAM}, the internal clock is blocked. This causes the MP2235S to skip pulses, achieving the light-load power save. Refer to AN032 for additional details.

The internal clock re-sets every time V_{COMP} is higher than V_{AAM}. Simultaneously, the high-side MOSFET (HS-FET) turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}.

The light-load feature in this device is optimized for 12 V input applications.

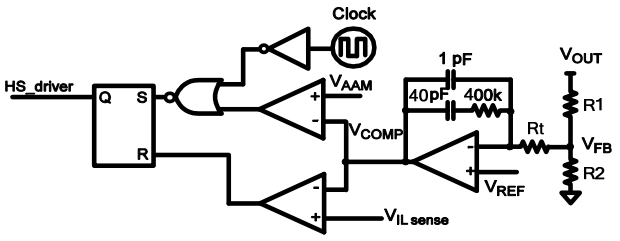


Figure 2—Simplified AAM control logic

DCM Control Operation

The V_{COMP} ramps up as the output current increases. When its minimum value exceeds V_{AAM}, the device enters discontinuous conduction mode (DCM). In DCM, the internal clock initiates the PWM cycle, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP} (after a period of dead time), and the low-side MOSFET (LS-FET) turns on and remains on until the inductor-current value decreases to zero. The device repeats the same operation in every clock cycle to regulate the output voltage (see Figure 3).

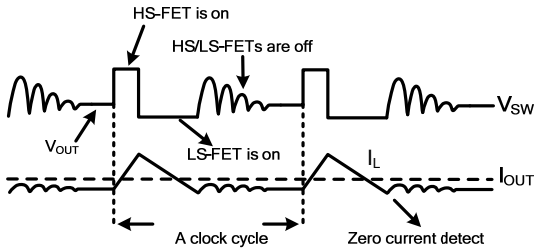


Figure 3—DCM control operation

CCM Control Operation

The device enters continuous conduction mode (CCM) from DCM once the inductor current no longer drops to zero in a clock cycle. In CCM, the internal clock initiates the PWM cycle, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP} (after a period of dead time), and the LS-FET turns on and remains on until the next clock cycle begins. The device repeats the same operation in every clock cycle to regulate the output voltage.

If $V_{ILsense}$ does not reach the value set by V_{COMP} within 92 percent of one PWM period, the HS-FET is forced off.

Internal Regulator

A 5 V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 5 V, the output of the regulator is in full regulation. When V_{IN} is less than 5 V, the output decreases, and the part requires a 0.1 µF ceramic decoupling capacitor.

Error Amplifier (EA)

The error amplifier compares the FB voltage to the internal 0.804 V reference (V_{REF}) and outputs a current proportional to the difference between the two. This output current then charges or discharges the internal compensation network to form the COMP

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

voltage, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Enable/SYNC Control

EN/SYNC is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator, drive EN low to turn off the regulator. An internal 1 MΩ resistor from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip. EN/SYNC is clamped internally using a 6.5 V Zener diode (see Figure 4). Connecting the EN input pin through a pull-up resistor to the voltage on IN limits the EN input current to less than 100 µA.

For example, with 12 V connected to IN, $R_{PULLUP} \geq (12\ V - 6.5\ V) \div 100\ \mu A = 55\ k\Omega$.

Connecting EN directly to a voltage source without a pull-up resistor requires limiting the amplitude of the voltage source to ≤6 V to prevent damage to the Zener diode (see Figure 4).

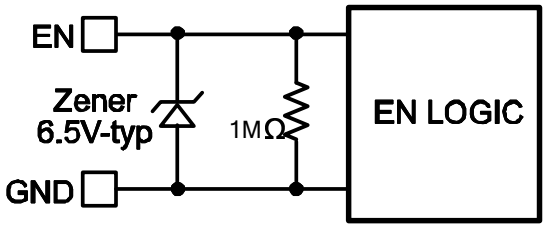


Figure 4—6.5 V Zener diode connection

For external clock synchronization, connect a clock with a frequency range between 300 kHz and 2 MHz 2 ms after the output voltage is set: The internal clock rising edge synchronizes with the external clock rising edge. Select an external clock signal with a pulse width less than 1 µs.

Under-Voltage Lockout (UVLO)

The MP2235S has under-voltage lockout protection (UVLO). When the VCC voltage exceeds the UVLO rising threshold voltage, the device begins to power-up. It shuts off when the VCC voltage drops below the UVLO falling threshold voltage. This is non-latch protection.

The MP2235S is disabled when the input voltage falls below 3.2 V, typically. If an application requires a higher under-voltage lockout (UVLO) threshold, use EN to adjust the input voltage UVLO by using two external resistors (see Figure 5). For best results, set the UVLO falling threshold (VSTOP) above 4.5 V using the enable resistors. Set the rising threshold (VSTART) to provide enough hysteresis to allow for input-supply variations.

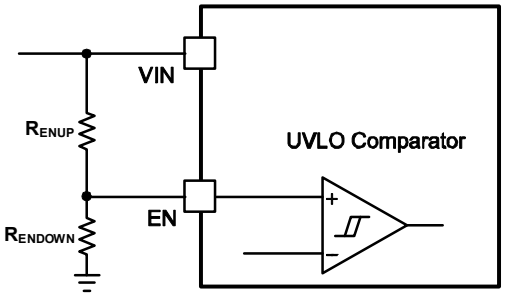


Figure 5—Adjustable UVLO

Soft-Start (SS)

Adjust the soft-start time by connecting a capacitor from SS to ground. When the soft-start begins, an internal 11 µA current source charges the external capacitor. The soft-start capacitor connects to the non-inverting input of the error amplifier. The soft-start period continues until the voltage on the soft-start capacitor exceeds the 0.804 V reference. Then the non-inverting amplifier takes the reference voltage as the input. Use Equation (1) to calculate the soft-start time:

$$t_{SS}(ms) = \frac{0.804V \times Css(nF)}{11\mu A} \quad (1)$$

Over-Current-Protection (OCP) and Hiccup

The MP2235S has a cycle-by-cycle over-current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, the output voltage drops until V_{FB} is below the under-voltage (UV) threshold (50 percent below the reference, typically). Once UV is triggered, the MP2235S enters hiccup mode to re-start the part periodically. This protection mode is useful when the output is dead shorted to ground, greatly reducing the average short-circuit current to alleviate thermal issues and protect the regulator. The MP2235S exits hiccup mode once the over-current condition is removed.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the die temperature exceeds 150°C, the entire chip shuts down. When the temperature drops below its lower threshold (130°C, typically), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2 V with a hysteresis of 150 mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, R3, C4, L1, and C2 (see Figure 6). If V_{IN}- V_{SW} exceeds 5 V, U1 regulates M1 to maintain a 5 V BST voltage across C4. A 20 Ω resistor placed between the SW and BST capacitors is strongly recommended to reduce SW spike voltage.

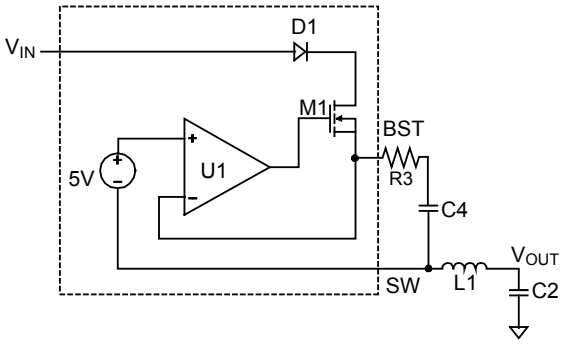


Figure 6—Internal bootstrap charging circuit

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: V_{EN} low, V_{IN} low, and thermal shutdown. During the shutdown procedure, the signal path is blocked first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see Typical Application on page 1).

Choose R1 around 40 kΩ for V_{OUT} > 1.2 V, R2 is then given using Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.804V} - 1} \quad (2)$$

The T-type network is highly recommended (see Figure 7).

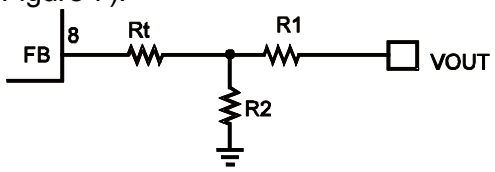


Figure 7—T-type network

Table 1 lists the recommended resistor and compensation values for common output voltages.

Table 1—Resistor selection for common output voltages(8)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Rt (kΩ)
1	20.5	84.5	34
1.2	30.1	61.9	24
1.8	40.2	32.4	15
2.5	40.2	19.1	6.8
3.3	40.2	13	5.6
5	40.2	7.68	2

NOTES:

8) The recommended parameters are based on an 800 kHz switching frequency; a different input voltage, output inductor value, and output capacitor value may affect the selection of R1, R2, and Rt. For additional component parameters, please refer to the “Typical Application Circuits” section on page 17 and page 18.

Selecting the Inductor

Use an inductor (1 µH to 22 µH) with a DC current rating at least 25 percent higher than the maximum load current for most applications. For highest efficiency, use an inductor with a DC resistance less than 15 mΩ. For most designs, the inductance value can be derived from Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30 percent of the maximum load current. The maximum inductor peak current is calculated using Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Use a larger inductor for improved efficiency under light-load conditions—below 100 mA.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Use ceramic capacitors with X5R or X7R dielectrics for best results because of their low ESR and small temperature coefficients. For most applications, use a 22 µF capacitor.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated using Equation (5) and Equation (6):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1 µF) placed as close to the IC as possible. When using ceramic capacitors,

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

make sure that they have enough capacitance to provide sufficient charge in order to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated using Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (8)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

The characteristics of the output capacitor affect the stability of the regulation system. The MP2235S can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

In particular conditions, the BST voltage may become insufficient. During these conditions, an external bootstrap diode can enhance the efficiency of the regulator and avoid insufficient BST voltage at light-load PFM operation. Insufficient BST voltage is more likely to occur during either of the following conditions:

- V_{OUT} is 5 V or 3.3 V; or
- the duty cycle is high: D= $\frac{V_{OUT}}{V_{IN}}$ >65%

If the BST voltage is insufficient, the output ripple voltage may become extremely large during a light-load condition. If this occurs, add an external BST diode from VCC to BST (see Figure 8).

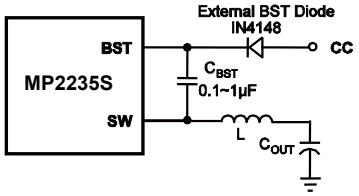


Figure 8—Optional external bootstrap diode to enhance efficiency

The recommended external BST diode is IN4148, and the BST capacitor value is 0.1 μF to 1 μF.

PCB Layout Guidelines [9]

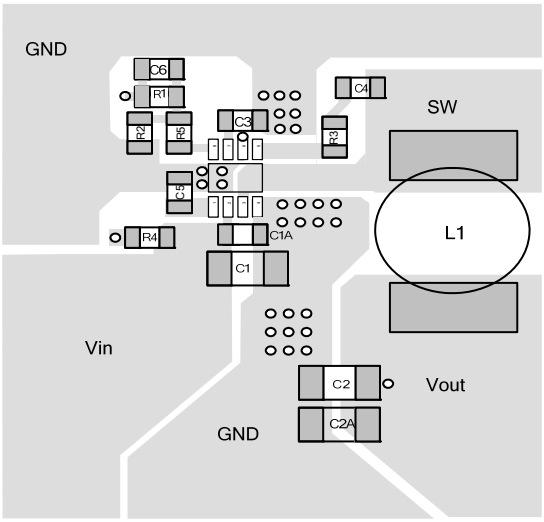
Efficient PCB layout is critical to achieve stable operation, especially for VCC capacitor and input capacitor placement. For best results, refer to Figure 9 and follow the guidelines below:

1. Use a large ground plane directly connected to GND. Add vias near GND if the bottom layer is ground plane.
2. Place the VCC capacitor as close as possible to the chip VCC and GND. Make the trace length of VCC pin to the VCC capacitor anode to the VCC capacitor cathode to the chip GND as short as possible.
3. Place the ceramic input capacitor close to IN and GND. Keep the connection of the input capacitor and IN as short and wide as possible.
4. Route SW and BST away from sensitive analog areas such as FB.
5. Place the T-type feedback resistor (R5) close to the chip to ensure the trace (which connects to FB) is as short as possible.

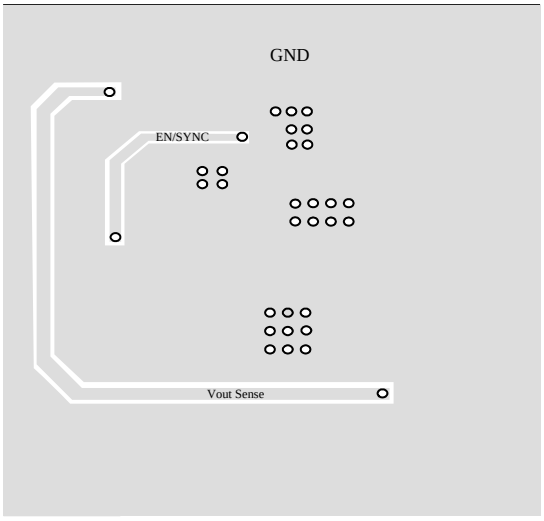
NOTES:

9) The recommended layout is based on Figure 10 on page 17.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.



Top Layer



Bottom Layer

Figure 9—Recommended PCB layout

Design Example

Table 2 is a design example following the application guidelines for the following specifications:

Table 2—Design example

V_{IN}	12 V
V_{OUT}	3.3 V
I_{OUT}	3 A

The detailed application schematic is shown in Figure 11. The typical performance and circuit waveforms have been shown in the “Typical Performance Characteristics” section. For more device applications, please refer to the related evaluation board datasheets.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

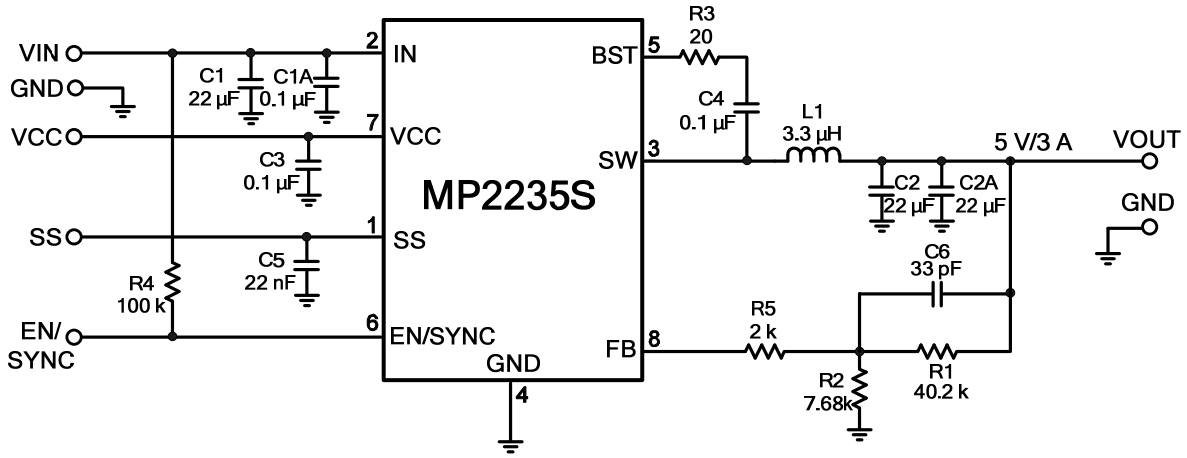


Figure 10—12V_{IN}, 5 V/3 A output

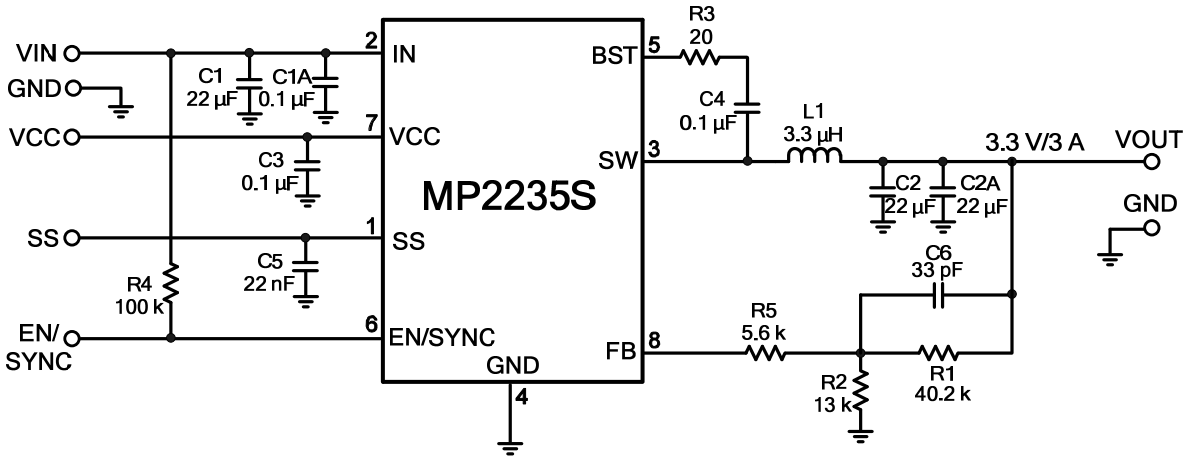


Figure 11—12V_{IN}, 3.3 V/3 A output

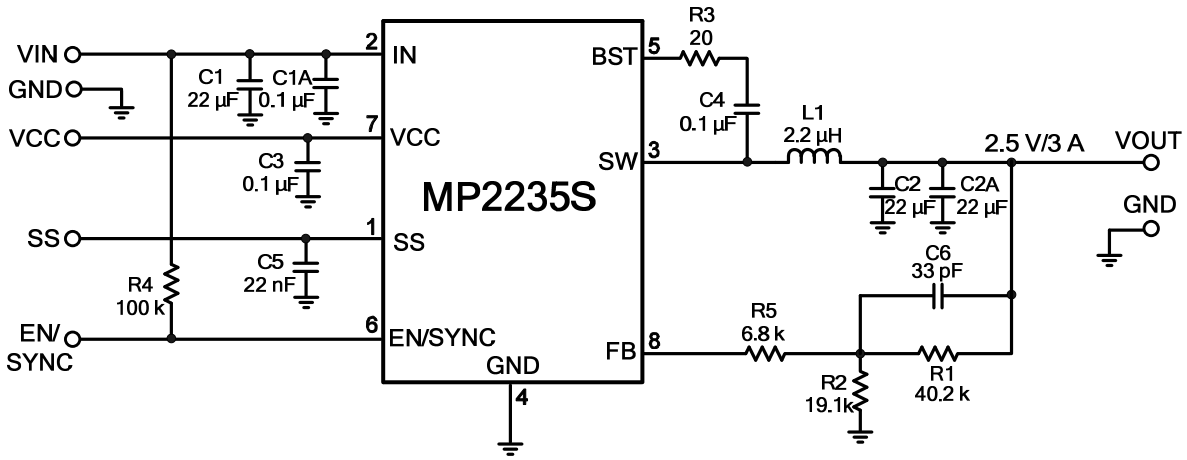


Figure 12—12V_{IN}, 2.5 V/3 A output

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

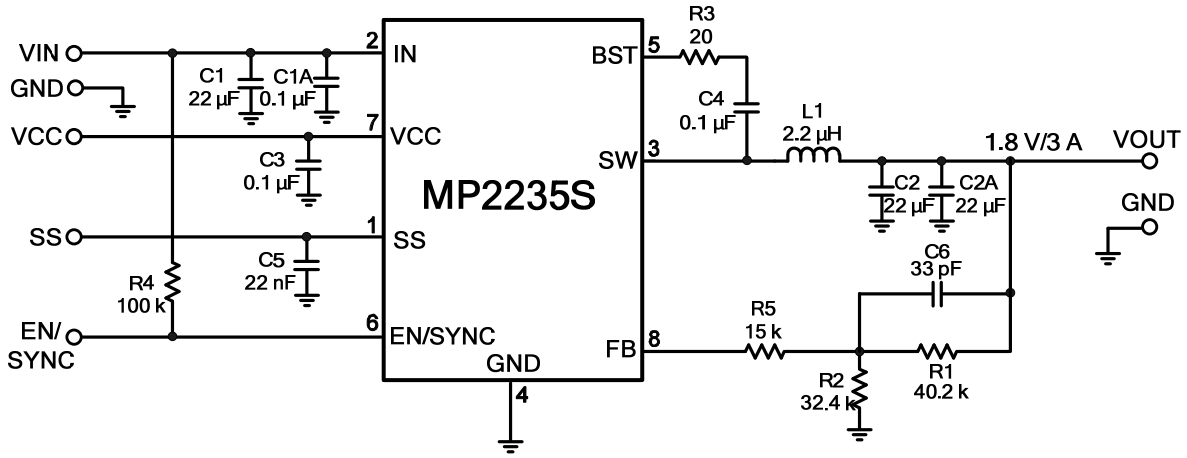


Figure 13—12V_{IN}, 1.8 V/3 A output

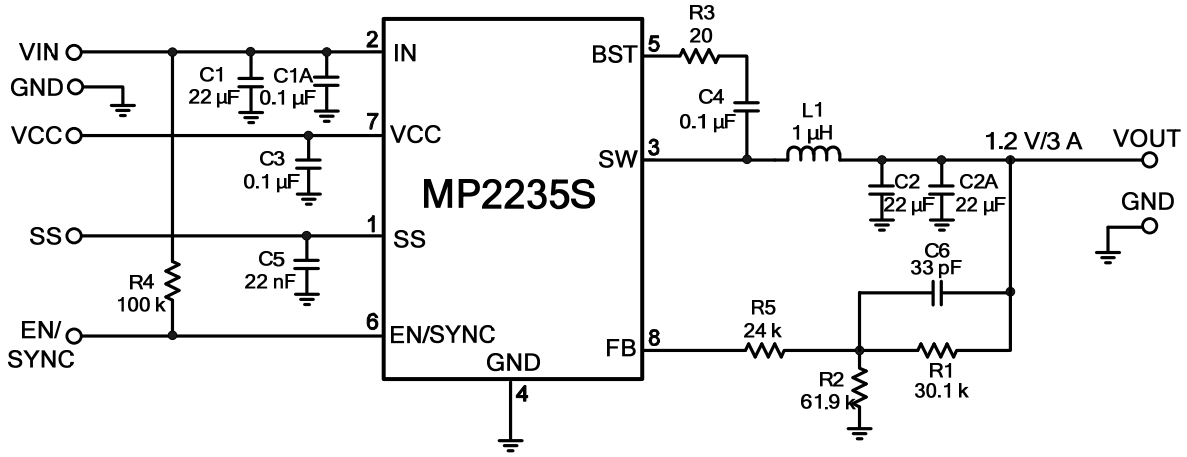


Figure 14—12V_{IN}, 1.2 V/3 A output

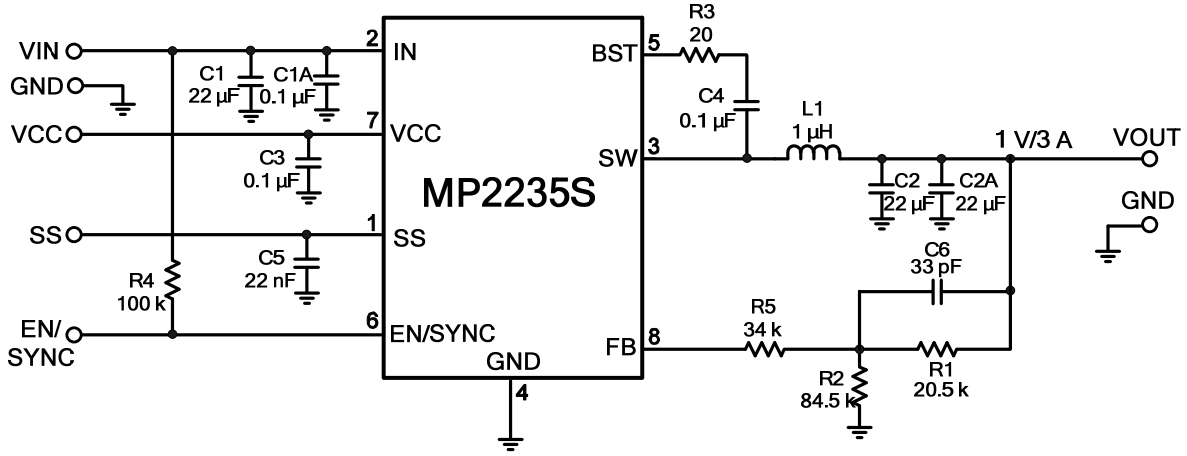
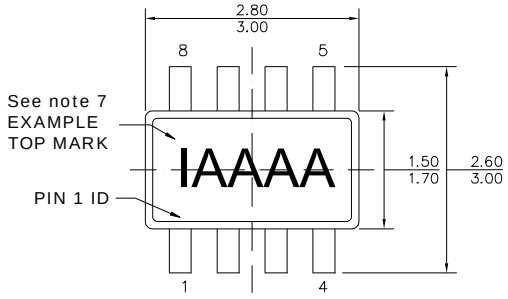


Figure 15—12V_{IN}, 1 V/3 A output

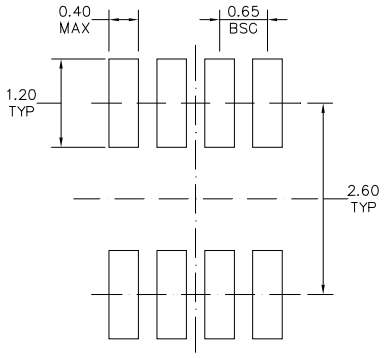
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

PACKAGE INFORMATION

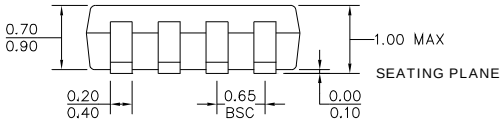
TSOT23-8



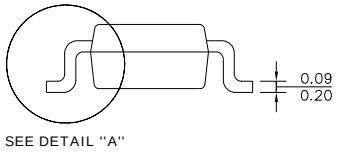
TOP VIEW



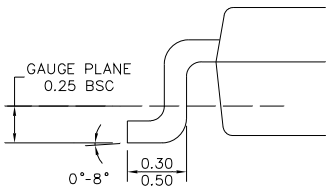
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.