OPA4277-SP High-Precision Operational Amplifier

1 Features

- QMLV (QML Class V) MIL-PRF-38535 Qualified and Radiation Hardness Assured (RHA), SMD 5962-16209
- 5962**L**16209:
  - Radiation Hardness Assurance (RHA) up to Total Ionizing Dose (TID) 50 krad(Si)
  - Single Event Latchup (SEL) Immune to LET = 85 MeV-cm^2/mg
- Ultra-Low Offset Voltage: 20 µV
- Ultra-Low Drift: ±0.15 µV/°C
- High Open-Loop Gain: 134 dB
- High Common-Mode Rejection: 140 dB
- High-Power Supply Rejection: 130 dB
- Wide Supply Range: ±2 to ±18 V
- Low-Quiescent Current: 800 µA/Amplifier

2 Applications

- Space Satellite Temperature and Position Sensing
- High-Accuracy Space Instrumentation
- Space Precision and Scientific Applications
  - Transducer Amplifier
  - Bridge Amplifier
  - Strain Gage Amplifier
  - Precision Integrator

3 Description

The OPA4277-SP precision operational amplifier replaces the industry standard LM124-SP. It offers improved noise and two orders of magnitude lower input offset voltage. Features include ultra-low offset voltage and drift, low-bias current, high common-mode rejection, and high-power supply rejection.

The OPA4277-SP operates from ±2- to ±18-V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA4277-SP precision operational amplifier is specified for real-world applications; a single limit applies over the ±5- to ±15-V supply range. High performance is maintained as the amplifier swings to the specified limits.

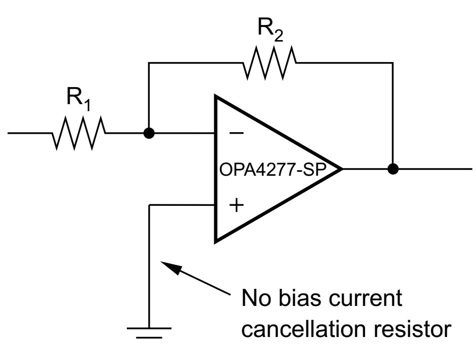
The OPA4277-SP is easy to use and free from phase inversion and overload problems found in some operational amplifiers. It is stable in unity gain and provides excellent dynamic behavior over a wide range of load conditions. The OPA4277-SP features completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA4277-SP	KGD(2)	—

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) KGD = known good die.

Simplified Schematic



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4 Revision History

DATE	REVISION	NOTES
December 2016	*	Initial release.

5 Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	Negative (lower) Power Supply	AlCu (0.5%)	990 to 1210 nm

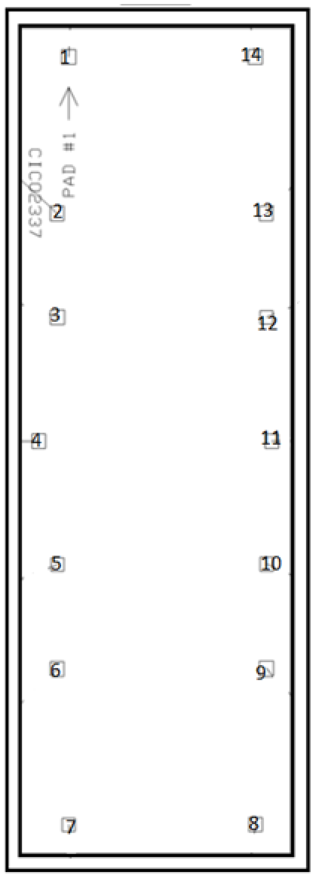


Table 1. Bond Pad Coordinates in Microns(1)

PAD		I/O	DESCRIPTION	X MIN	Y MIN	X MAX	Y MAX
NO.	NAME						
1	OUT A	O	Output channel A.	1791.042	7290.340	1901.751	7401.049
2	–IN A	I	Inverting input channel A.	1701.719	6111.536	1807.397	6217.213
3	+IN A	I	Noninverting input channel A.	1701.719	5326.505	1812.429	5437.215
4	V+	—	Positive (higher) power supply.	1555.784	4390.507	1661.461	4498.700
5	+IN B	I	Noninverting input channel B.	1706.752	3462.057	1807.397	3562.702
6	–IN B	I	Inverting input channel B.	1701.719	2671.994	1807.397	2777.671
7	OUT B	O	Output channel B.	1796.074	1498.222	1896.719	1598.867
8	OUT C	O	Output channel C.	3278.071	1498.222	3383.748	1603.900
9	–IN C	I	Inverting input channel C.	3362.361	2671.994	3473.071	2782.704
10	+IN C	I	Noninverting input channel C.	3367.393	3462.057	3473.071	3567.734
11	V–	—	Negative (lower) power supply.	3407.651	4391.765	3513.329	4497.442
12	+IN D	I	Noninverting input channel D.	3367.393	5331.537	3468.038	5432.182
13	–IN D	I	Inverting input channel D.	3362.361	6111.536	3468.038	6217.213
14	OUT D	O	Output channel D.	3273.039	7290.340	3383.748	7401.049

(1) Substrate must be biased to V–, negative (lower) power supply.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage = (V+) – (V–)		36	V
Input voltage	(V–) – 0.7	(V+) + 0.7	V
Output short circuit	Continuous		
Operating temperature	–55	125	°C
Junction temperature		150	°C
Lead temperature (soldering, 10 s)		300	°C
Storage temperature, T_{stg}	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Machine model (MM)	±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	Dual supply voltage	±5	±15	V
T_J	Operating junction temperature	–55	125	°C

6.4 Electrical Characteristics

At T_J = 25°C, V_S = ±5 V to ±15 V, and R_L = 2 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_J = 25°C, pre- and post-irradiated		±20	±65	µV
		T_J = –55°C to 125°C, pre-irradiated			±140	
dV_{OS}/d_T	Input offset voltage temperature drift	T_J = –55°C to 125°C, pre-irradiated		±0.15		µV/°C
PSRR	Input offset voltage	vs time		0.2		µV/mo
		vs power supply, V_S = ±2 V to ±18 V, T_J = 25°C, pre- and post-irradiated		±0.3	±1	µV/V
		V_S = ±2 V to ±18 V, T_J = –55°C to 125°C			±1	µV/V
	Channel separation	dc		0.1		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	T_J = –55°C to 125°C			±17.5	nA
		T_J = 25°C, pre- and post-irradiated			±17.5	
I_{OS}	Input offset current	T_J = –55°C to 125°C			±17.5	nA
		T_J = 25°C, pre- and post-irradiated			±17.5	
NOISE						
	Input voltage noise	f = 0.1 to 10 Hz		0.22		$µV_{pp}$
	Input voltage noise density	f = 10 Hz		12		nV/√Hz
		f = 100 Hz		8		
		f = 1 kHz		8		
		f = 10 kHz		8		
i_n	Input noise current density	f = 1 kHz		0.2		fA/√Hz
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range	T_J = 25°C, pre- and post-irradiated	(V–) + 2		(V+) – 2	V
CMRR	Common-mode rejection ratio	(V–) + 2 V < V_{CM} < (V+) – 2 V, T_J = 25°C, post-irradiated	114	140		dB
		(V–) + 2 V < V_{CM} < (V+) – 2 V, T_J = –55°C to 125°C	114			
INPUT IMPEDANCE						
	Differential			100 || 3		MΩ || pF
	Common mode	(V–) + 2 V < V_{CM} < (V+) – 2 V		250 || 3		GΩ || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_O = (V_O–) + 0.5 V to (V_O+) – 1.2 V, R_L = 10 kΩ		140		dB
		V_O = (V_O–) + 1.5 V to (V_O+) – 1.5 V, R_L = 2 kΩ, T_J = –55°C to 125°C	118	134		
		V_O = (V_O–) + 1.5 V to (V_O+) – 1.5 V, R_L = 2 kΩ, T_J = 25°C, pre- and post-irradiated	118	134		
		V_O = (V_O–) + 3.4 V to (V_O+) – 3.4 V, R_L = 600 Ω, V_S = ±7 V, T_J = –55°C to 125°C	118	134		
		V_O = (V_O–) + 3.4 V to (V_O+) – 3.4 V, R_L = 600 Ω, V_S = ±7 V, T_J = 25°C, pre- and post-irradiated	118	134		

Electrical Characteristics (continued)

At T_J = 25°C, V_S = ±5 V to ±15 V, and R_L = 2 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			1		MHz
SR	Slew rate			0.8		V/µs
	Settling time	0.1%, 10-V step, V_S = ±15 V, G = 1		14		µs
		0.01%, 10-V step, V_S = ±15 V, G = 1		16		
THD + N	Total harmonic distortion + noise	1 kHz, G = 1, V_O = 3.5 Vrms		0.002%		
OUTPUT						
V_O	Output voltage	R_L = 10 kΩ, T_J = 25°C, pre- and post-irradiated	(V–) + 0.5		(V+) – 1.2	V
		R_L = 10 kΩ, T_J = –55°C to 125°C	(V–) + 0.5		(V+) – 1.2	
		R_L = 2 kΩ, T_J = 25°C, pre- and post-irradiated	(V–) + 1.5		(V+) – 1.5	
		R_L = 2 kΩ, T_J = –55°C to 125°C	(V–) + 1.5		(V+) – 1.5	
		T_J = 25°C, R_L = 600 Ω, pre- and post-irradiated	(V–) + 3.4		(V+) – 3.4	
		R_L = 600 Ω, V_S = ±7 V, T_J = –55°C to 125°C	(V–) + 3.4		(V+) – 3.4	
I_{SC}	Short-circuit current			±35		mA
C_{LOAD}	Capacitive load drive	f = 350 kHz, I_O = 0		See *Typical Characteristics*		
POWER SUPPLY						
V_S	Specified voltage	T_J = –55°C to 125°C	±5	±7	±15	V
		T_J = 25°C, pre- and post-irradiated	±5	±7	±15	
V_S	Operating voltage	T_J = –55°C to 125°C	±2	±7	±18	V
		T_J = 25°C, pre- and post-irradiated	±2	±7	±18	
I_Q	Quiescent current per amplifier	I_O = 0, T_J = 25°C, pre- and post-irradiated		±790	±850	µA
		I_O = 0, T_J = –55°C to 125°C			±900	

6.5 Typical Characteristics

At T_J = 25°C, V_S = ±15 V, and R_L = 2 kΩ, pre-irradiated (unless otherwise noted).

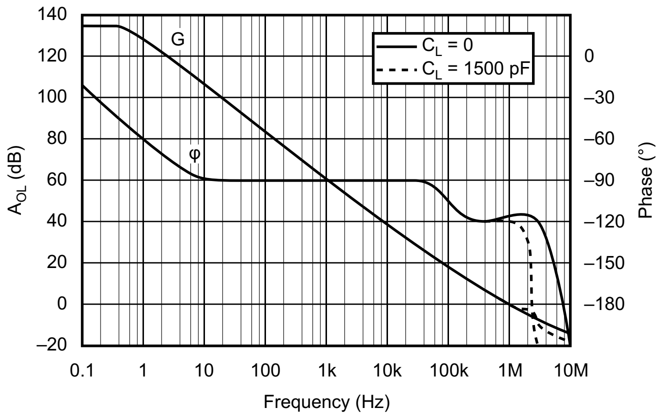


Figure 1. Open-Loop Gain/Phase vs Frequency

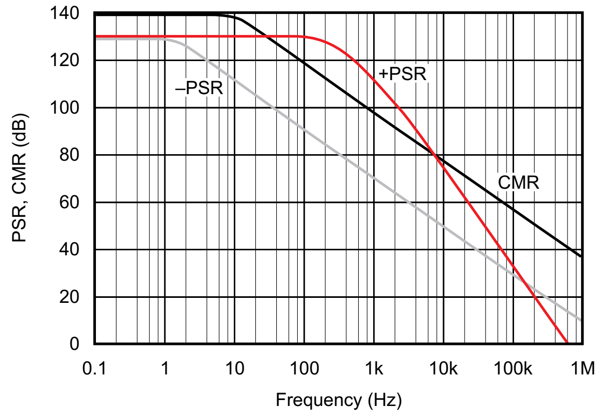


Figure 2. Power Supply and Common-Mode Rejection vs Frequency

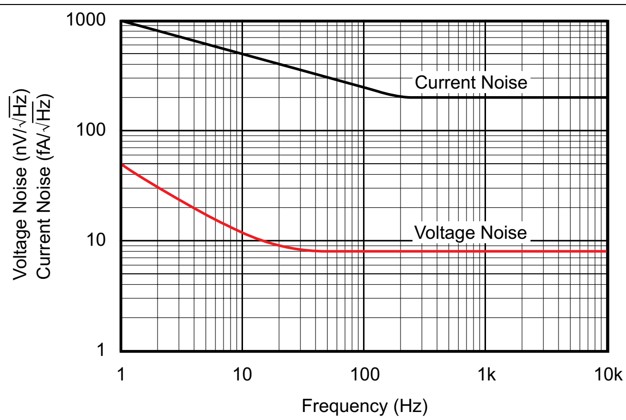
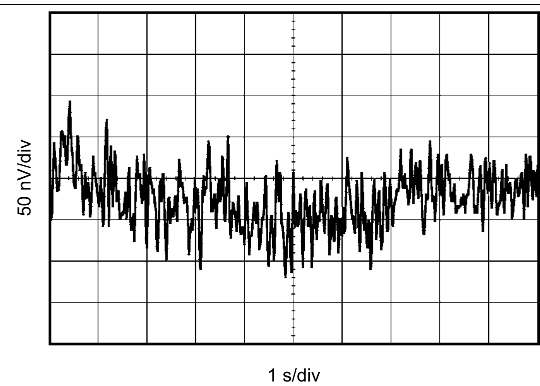
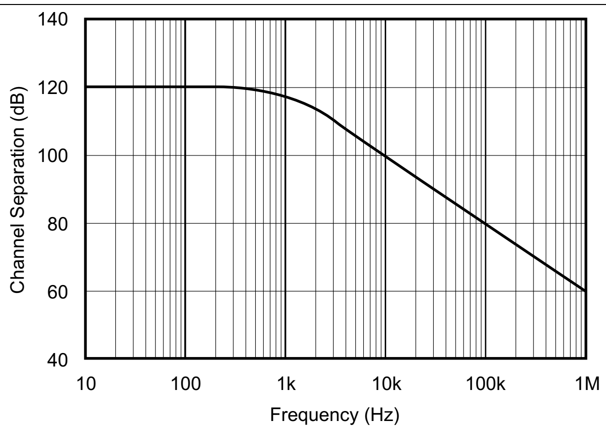


Figure 3. Input Noise and Current Noise Spectral Density vs Frequency



Noise signal is bandwidth limited to lie between 0.1 Hz and 10 Hz.

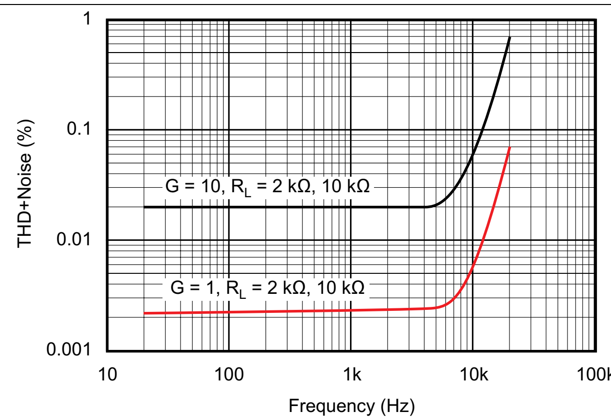
Figure 4. Input Noise Voltage vs Time



G = 1, measured channel A to D or B to C.

Other combinations yield similar or improved rejection.

Figure 5. Channel Separation vs Frequency



V_{OUT} = 3.5 Vrms

Figure 6. Total Harmonic Distortion + Noise vs Frequency

Typical Characteristics (continued)

At T_J = 25°C, V_S = ±15 V, and R_L = 2 kΩ, pre-irradiated (unless otherwise noted).

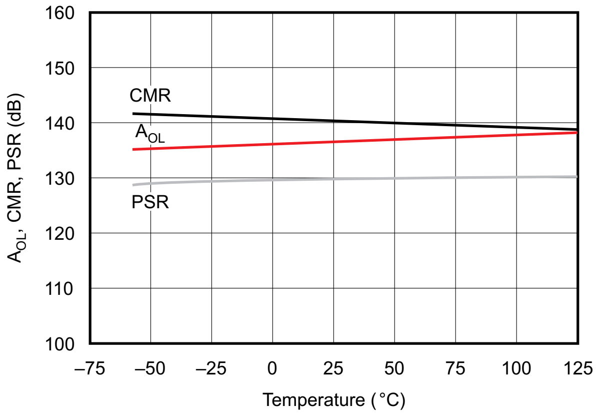
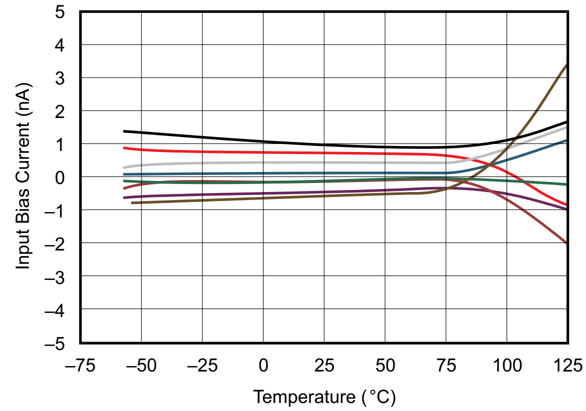


Figure 7. A_{OL}, CMR, PSR vs Temperature



Curves represent typical production units.

Figure 8. Input Bias Current vs Temperature

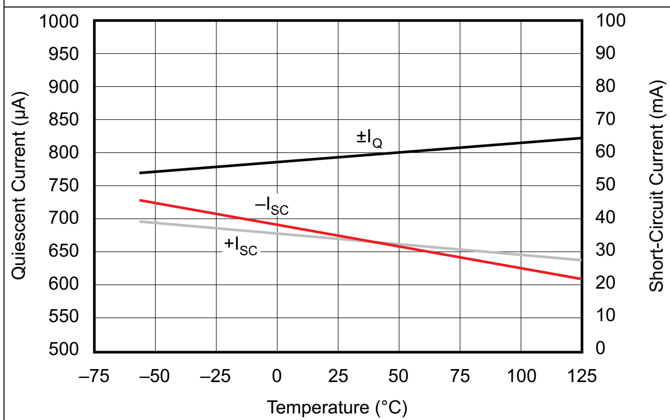
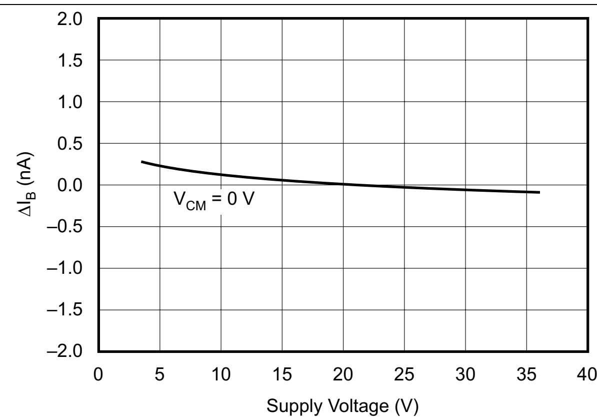
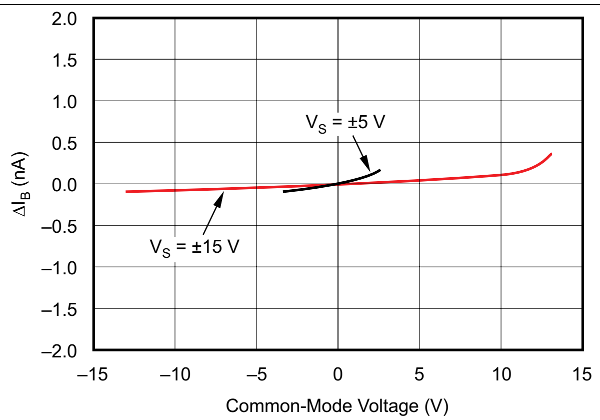


Figure 9. Quiescent Current and Short-Circuit Current vs Temperature



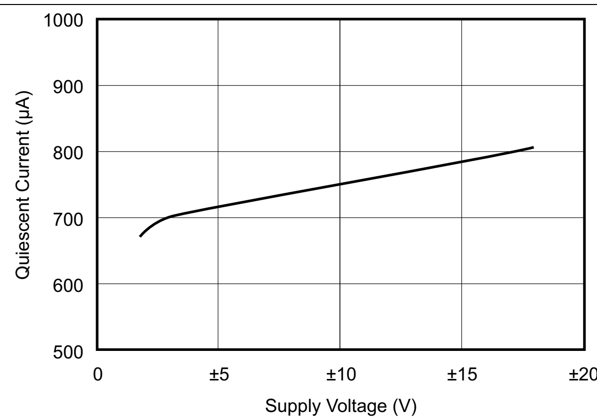
Curve shows normalized change in bias current with respect to V_S = ±10 V (+20 V). Typical I_B may range from –0.5 nA to 0.5 nA at V_S = ±10 V.

Figure 10. Change in Input Bias Current vs Power Supply Voltage



Curve shows normalized change in bias current with respect to V_{CM} = 0 V. Typical I_B may range from –0.5 nA to 0.5 nA at V_{CM} = 0 V.

Figure 11. Change in Input Bias Current vs Common-Mode Voltage



Per amplifier

Figure 12. Quiescent Current vs Supply Voltage

Typical Characteristics (continued)

At T_J = 25°C, V_S = ±15 V, and R_L = 2 kΩ, pre-irradiated (unless otherwise noted).

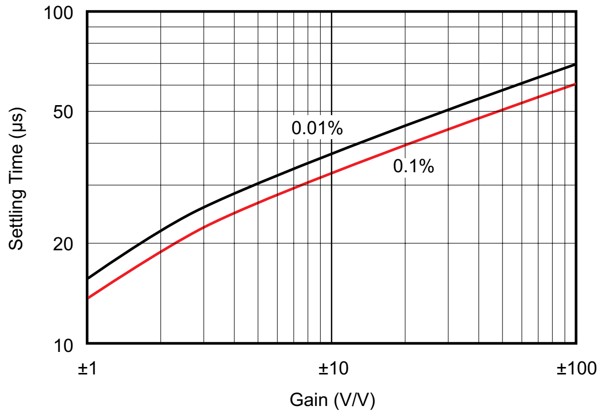


Figure 13. Settling Time vs Closed-Loop Gain

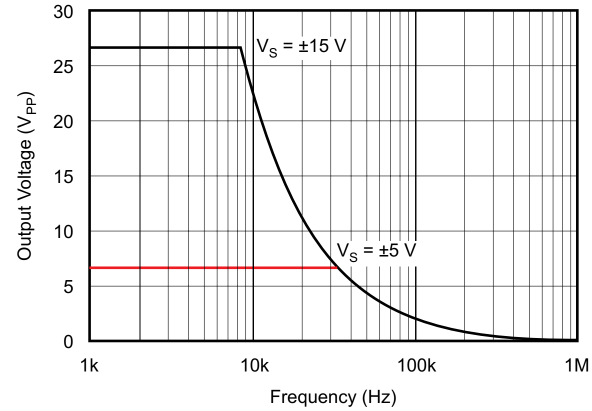


Figure 14. Maximum Output Voltage vs Frequency

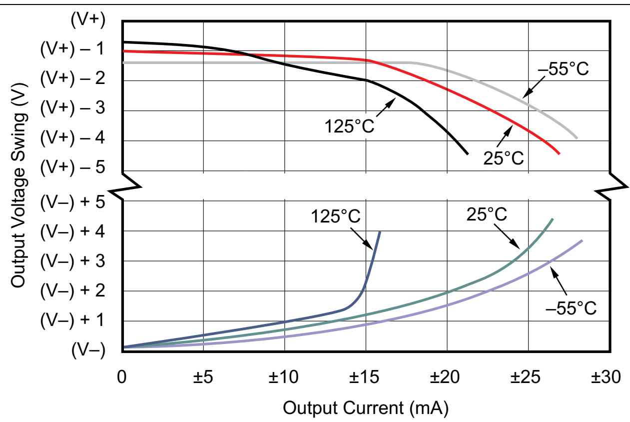


Figure 15. Output Voltage Swing vs Output Current

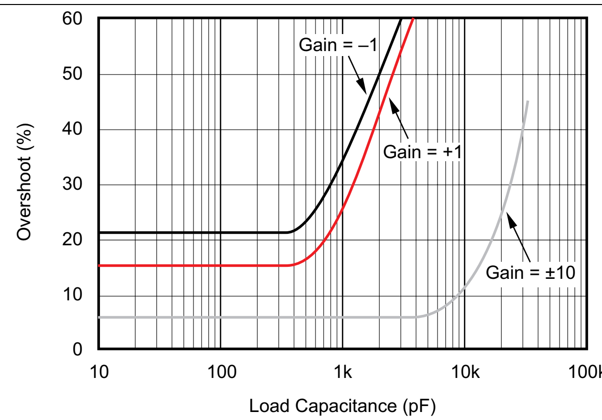


Figure 16. Small-Signal Overshoot vs Load Capacitance

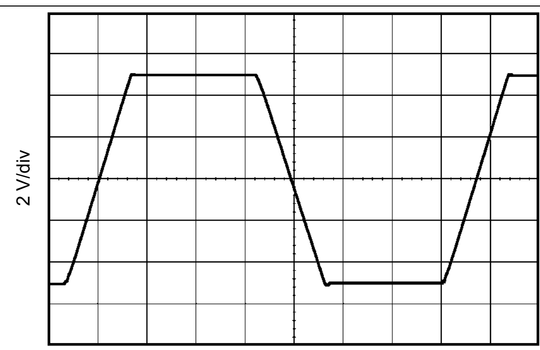


Figure 17. Large-Signal Step Response

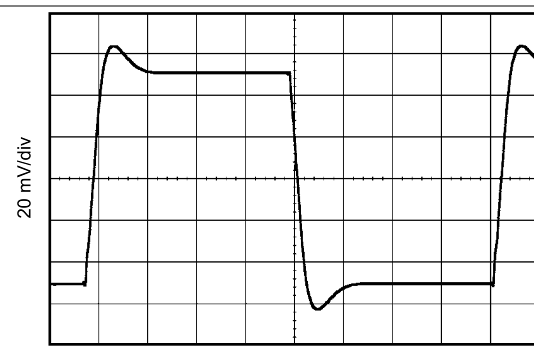
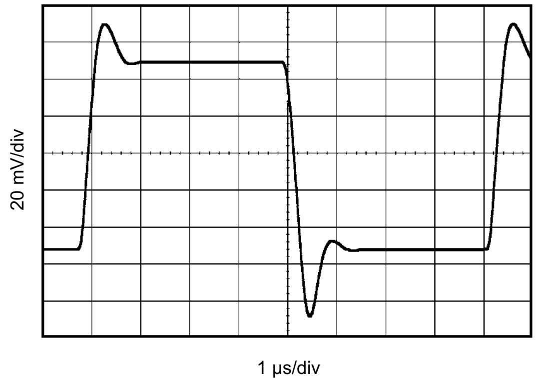


Figure 18. Small-Signal Step Response

Typical Characteristics (continued)

At T_J = 25°C, V_S = ±15 V, and R_L = 2 kΩ, pre-irradiated (unless otherwise noted).



G = 1 C_L = 1500 pF V_S = ±15 V

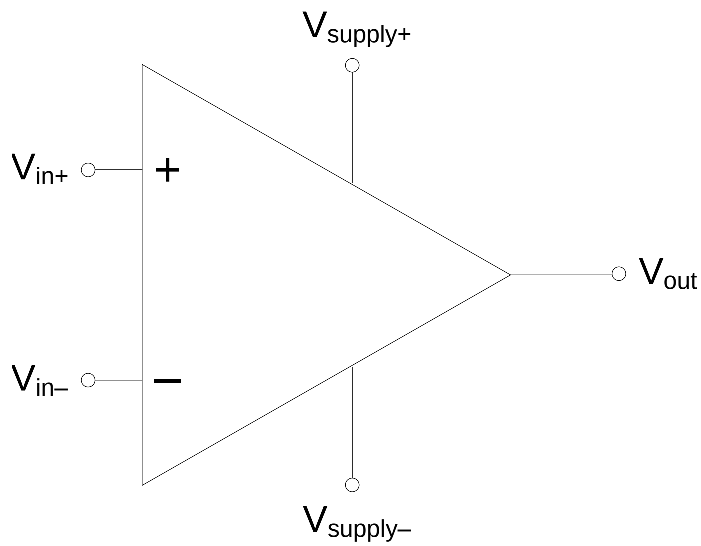
Figure 19. Small-Signal Step Response

7 Detailed Description

7.1 Overview

The OPA4277-SP precision operational amplifier replaces the industry standard LM124-SP. It offers improved noise, wider output voltage swing, and is twice as fast with half the quiescent current. Features include ultra-low offset voltage and drift, low bias current, high common-mode rejection, and high power supply rejection.

7.2 Functional Block Diagram



7.3 Feature Description

The OPA4277-SP operates from ±2- to ±18-V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA4277-SP precision operational amplifier is specified for real-world applications; a single limit applies over the ±5- to ±15-V supply range. High performance is maintained as the amplifier swings to the specified limits. Because the initial offset voltage (±50 μV max) is so low, user adjustment is usually not required.

7.3.1 Input Protection

The inputs of the OPA4277-SP are protected with 1-kΩ series input resistors and diode clamps. The inputs can withstand ±30-V differential inputs without damage. The protection diodes conduct current when the inputs are overdriven. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the operational amplifier.

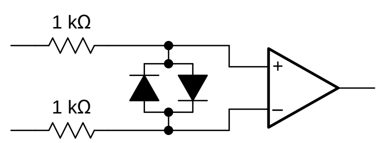


Figure 20. OPA4277-SP Input Protection

7.3.2 Input Bias Current Cancellation

The input stage base current of the OPA4277-SP is internally compensated with an equal and opposite cancellation circuit. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

Feature Description (continued)

When the bias current is canceled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to use a bias current cancellation resistor, as is often done with other operational amplifiers (see Figure 21). A resistor added to cancel input bias current errors may actually increase offset voltage and noise.

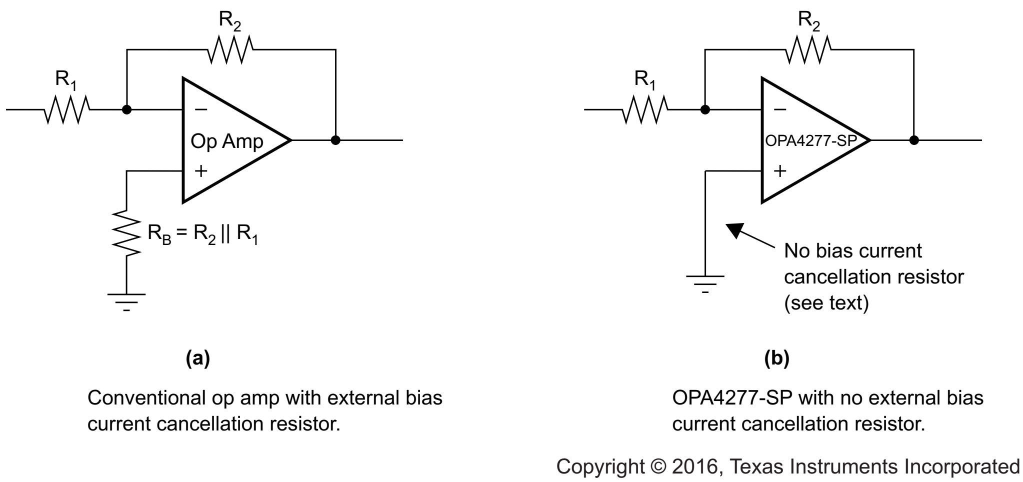


Figure 21. Input Bias Current Cancellation

7.4 Device Functional Modes

The OPA4277-SP has a single functional mode and is operational when the power-supply voltage, (V+) – (V–), is less than 36 V.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA4277-SP is unity-gain stable and free from unexpected output phase reversal, making it easy to use in a wide range of applications. Applications with noisy or high-impedance power supplies may require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.2 Typical Application

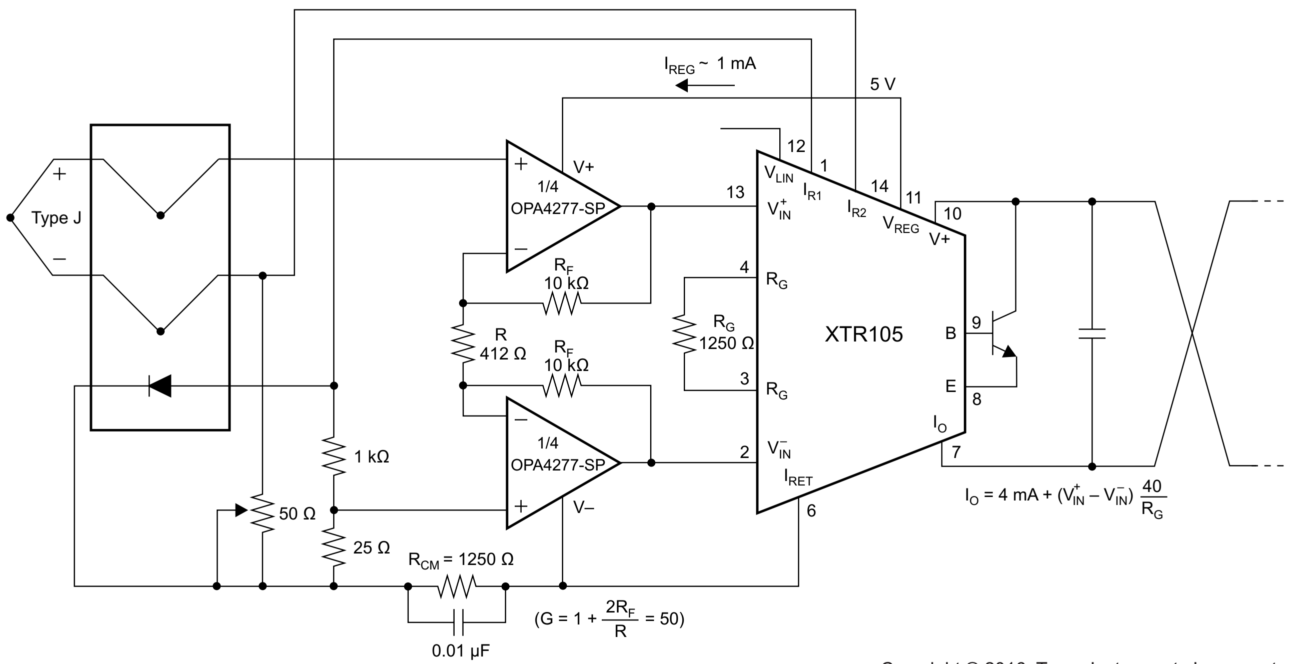


Figure 22. Thermocouple Low-Offset, Low-Drift Loop Measurement With Diode Cold Junction Compensation

8.2.1 Design Requirements

For the thermocouple low-offset, low-drift loop measurement with diode cold junction compensation shown in Figure 22, a gain of 50 is desired.

Typical Application (continued)

8.2.2 Detailed Design Procedure

Equation 1 shows the equation used to determine the resistor values needed for a gain of 50. Table 2 lists the design parameters.

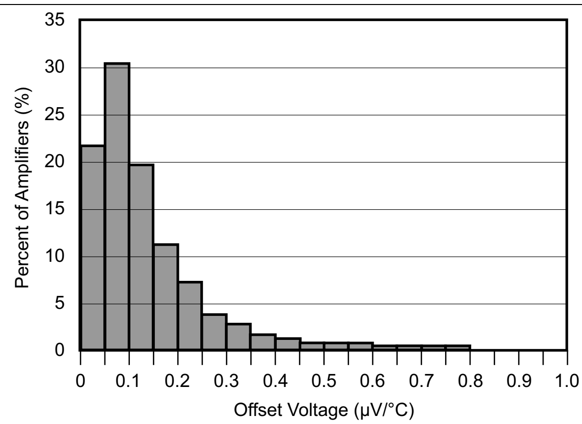
$$G = 1 + \frac{2R_F}{R} = 50 \quad (1)$$

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
R_F	10 kΩ
R	412 Ω

8.2.3 Application Curve

At T_J = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.



Typical distribution of packaged units. Single, dual, and quad included.

Figure 23. Warm-Up Offset Voltage Drift

9 Power Supply Recommendations

OPA4277-SP operates from ±2- to ±18-V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA4277-SP is specified for real-world applications; a single limit applies over the ±5- to ±15-V supply range. This allows a customer operating at V_S = ±10 V to have the same assured performance as a customer using ±15-V supplies. In addition, key parameters are assured over the specified temperature range, –55°C to 125°C. Most behavior remains unchanged through the full operating voltage range (±2 to ±18 V). Parameters which vary significantly with operating voltage or temperature are shown in the typical performance curves.

10 Layout

10.1 Layout Guidelines

The leadframe die pad should be soldered to a thermal pad on the PCB. Mechanical drawings located in *Mechanical, Packaging, and Orderable Information* show the physical dimensions for the package and pad.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

The OPA4277-SP has very-low offset voltage and drift. To achieve highest performance, optimize circuit layout and mechanical conditions. Offset voltage and drift can be degraded by small thermoelectric potentials at the operational amplifier inputs. Connections of dissimilar metals generate thermal potential, which can degrade the ultimate performance of the OPA4277-SP. Cancel these thermal potentials by assuring that they are equal in both input terminals.

- Keep the thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield operational amplifier and input circuitry from air currents such as cooling fans.

10.2 Layout Example

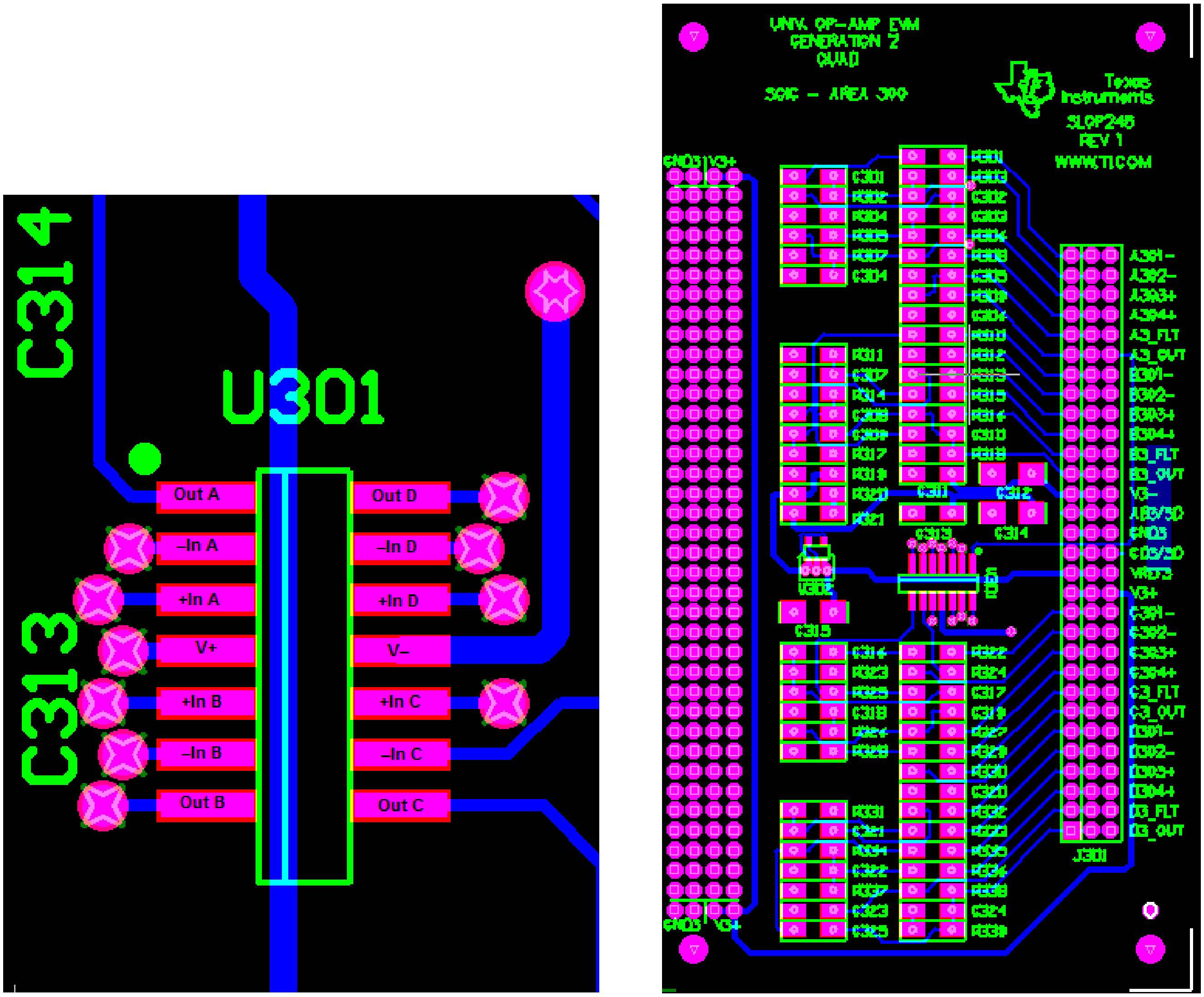


Figure 24. Board Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962R1620901V9A	PREVIEW	XCEPT	KGD			TBD	Call TI	Call TI	-55 to 125		

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA4277-SP :

- Catalog: OPA4277
- Enhanced Product: OPA4277-EP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications