EPSON
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S1C33401

CMOS 32-bit Single Chip Microcomputer

- **32-bit C33 ADV RISC Core with 8K-byte Cache**
- **Low Power Consumption**
- **Multiply Accumulation**
- **Built-in 32K-byte + 1K-byte RAM**
- **10-bit ADC**
- **4-ch. SIO**
- **10-ch. PWM Timer with DA16 Mode**
- **Card Interfaces**
- **High-speed DMA, Intelligent DMA**

■ DESCRIPTIONS

The S1C33401 is a 32-bit RISC-type microcomputer originally developed for embedded applications by Seiko Epson. The S1C33401 is built around the C33 ADV core block that includes the CPU, MMU, cache, and modules that allow various external memory and I/O devices to be connected directly, and incorporates a bus block that includes the DMA controller and other control units. In addition to these primary units, the S1C33401 incorporates a basic peripheral circuit block that includes an interrupt controller, timers, serial interfaces, card interfaces, input/output ports, and A/D converter, and an extended peripheral circuit block that includes a chip ID register, RTC, and other components.
The S1C33401 is manufactured by a 0.18 µm fine-pattern CMOS process, backed by sophisticated clock control functions, and can operate at higher speed with less power than ever before. In addition to its use as an embedded-type processor in various portable systems, the S1C33401 features a built-in C33 ADV CPU to provide enhanced functionality for multimedia support while retaining upward compatibility with the conventional C33 STD CPU, making it an ideal solution to the requirements of mobile multimedia applications.

Product Lineup

Model No.	Package
S1C33401F00A∗∗∗	QFP20-184pin
S1C33401B00A∗∗∗	PFBGA-160pin

■ FEATURES

CORE

● CPU

- Original Seiko Epson 32-bit RISC-type CPU – C33 ADV
- Internal 32-bit data processing
- 4GB address space
- Powerful instruction set
  - Code length: 16 bits per instruction
  - Number of instructions: 164
  - Main instructions executable in 1 cycle (including immediate-extended instructions, each consisting of two to three instructions)
  - 15.15 ns per instruction (when operating at 66 MHz, max.)
- Multimedia support functions
  - Built-in 32-bit × 16-bit multiplier
  - 16 × 16, 32 × 16 and 32 × 32-bit multiplication
  - 16 × 16, 32 × 16 and 32 × 32-bit multiply-accumulate operations
  - Repeated execution by loop and repeat instructions
  - Rounding to minimum/maximum values by saturation instruction
  - ALU instruction execution with post-shift

● High-speed Bus Control Unit (HBCU)

- Controls memory access by the CPU by dividing 4GB logical space into eight 512MB blocks.
- Manages MMU, CCU, and ASID processing in each block.
- Capable of multiplexing logical space using ASID and mirroring physical space.
- Can simultaneously process A0RAM data read/write operations and instruction fetching from cache.

● Memory Management Unit (MMU)

- Converts logical space into physical space in page units (4KB or 64KB per page).
- Supports 16 entries per way for a total of 64 entries, due to 4-way set associative method.
- Can protect memory for each page.
- Allows optional selection of using cache for each page.
- Supports five causes of MMU exception.

● Cache Control Unit (CCU)

- Physical address-based instruction/data coexisting type of cache
- Contains 8KB cache.
- Supports 128 entries per way for a total of 512 lines, due to 4-way set associative method (4 words per line).
- Allows selection of write-through or write-back mode for writing to cache.
- Can lock a specified way and interrupt handler routine.
- Forwarding function to allow immediate instruction/data transfer even during refill.

● Clock Management Unit (CMU)

- Controls reset and NMI input.
- System clock control
  - Selects clock source, turns clock on/off, and divides operating clock.
  - Controls clock according to standby mode (SLEEP, HALT, or HALT2).
- Controls clock supply for each module (manual/auto).

● Debug Unit (DBG)

- Supports on-chip trace/break and other debugging functions at the chip level.
- Provides an advanced debugging environment in conjunction with the ICD (in-circuit debugger) and debugger.

INTERNAL MEMORY

● High-speed RAM Incorporated in Area 0 (A0RAM)

- 32KB
- High-speed access with zero wait state

● RAM Incorporated in Area 3 (A3RAM)

- 1KB
- Access with one wait state
- Also usable as IDMA control information table

BUS CONTROL UNITS AND DMA CONTROLLER

● Basic Bus Control Unit (BBCU)

- Controls external address space by dividing it into 19 areas (Areas 4 to 22).
- Allows selection of external/internal access, endian mode, interface mode, device type, device size, and number of access cycles for each area.
- Outputs 8 chip-enable signals (#CE4–#CE11) corresponding to each external area.
- Supports two interface modes: A0 and BSL (with BSL mode for external memory only).
- Allows direct connection of SRAM, ROM, burst ROM, or flash memory to external bus.
- Allows insertion of wait state from external #WAIT pin (for SRAM type only).
- Arbitrates bus contention with external bus masters.

● Extended Bus Control Unit (EBCU)

- Allows direct connection of SDRAM (in one of Areas 4 to 22 selected).
- Data bus width: 16 bits
- Bank address: Up to four banks accommodated.
- Burst length: Fixed to 1 (with burst read/write executed by issuing successive commands).
- CAS latency: 1, 2, or 3
- Write mode: Single write
- Supports self-refresh and auto-refresh.
- Programmable refresh cycle
- Allows selection of bank active mode (with or without auto-precharge).

● High-speed DMA Controller (HSDMA)

- Up to four channels
- Capable of high-speed DMA transfer because of no need to read/write transfer conditions, etc. from/to memory.
- Supports dual-address and single-address transfers.
- Activated by DMA request input, interrupt cause, or software trigger.
- Can generate interrupt upon completion of transfer.

● Intelligent DMA Controller (IDMA)

- Up to 128 channels
- Supports dual-address transfers.
- Programmable DMA transfer control information in RAM (except A0RAM)
- Activated by a specific interrupt cause or software trigger.
- Can be linked from one IDMA channel to another.
- Can generate an interrupt upon completion of transfer.

INTERNAL PERIPHERAL CIRCUITS

● OSC3 Oscillator Circuit

- Generates the main system clock.
- Crystal/ceramic oscillator: 5 MHz (min.) to 33 MHz (max.)
- External clock input: 2 MHz (min.) to 33 MHz (max.)

● PLL

- Allows selection of whether to use ×1 to ×16 OSC3 oscillation frequency.
- PLL input frequency: 5 MHz (min.) to 33 MHz (max.)
- PLL output frequency: 20 MHz (min.) to 66 MHz (max.)

● SSCG (Spread Spectrum Clock Generator)

- SS-modulation circuit for system source clock (OSC3, PLL, or OSC1) to reduce Electromagnetic Interference (EMI) noise

● Interrupt Controller (ITC)

- Branches to interrupt handling routine via interrupt vector table.
- Can activate intelligent DMA.
- Handles 9 exceptions:
  - Reset exception (1)
  - Divide by zero exception (1)
  - Address misaligned exception (1)
  - NMI (1)
  - Software exceptions (4)
  - MMU exception (1)
- Handles 64 maskable interrupts:
  - Port/key input interrupts (18)
  - DMA controller interrupts (5)
  - 16-bit timer interrupts (20)
  - 8-bit timer interrupts (6)
  - Serial interface interrupts (12)
  - A/D converter interrupts (2)
  - RTC interrupt (1)

● Prescaler (PSC)

- Programmable 8-bit and 16-bit timers, and A/D converter clock settings

● 8-bit Timer (T8)

- 6-channel, 8-bit programmable timers
- Can generate an interrupt upon underflow.
- Can output the clock generated by underflow to external devices.
- Generates serial interface clock as programmed.
- Can output a trigger to A/D converter at specified intervals.

● 16-bit Timer (T16)
- 10-channel, 16-bit programmable timers
- Can be used as PWM timer.
- Supports DA16 mode.
- Can generate two interrupts per channel upon underflow or when matching compared value.
- Can output clock generated by underflow or when matching compared value to external devices.

● Watchdog Timer (WDT)
- 30-bit watchdog timer capable of generating NMI
- Programmable setting of NMI generation cycle

● Serial Interface (SIO)
- 4 channels
- Contains 4-byte receive data buffer (FIFO) and 2-byte transmit data buffer (FIFO) for each channel.
- Supports full-duplex communication.
- Selectable between 8-bit clock-synchronous and 8-bit or 7-bit asynchronous modes.
- Supports IrDA 1.0 interface.
- Can generate transmit buffer empty, receive buffer full, and receive error interrupts.

● Card Interface (CARD)
- Supports SmartMedia card (NAND flash).
- Supports CompactFlash card.
- Supports PC card (2 channels).

● I/O Ports (PORT)
- Up to 71 ports
- Can be used as general-purpose I/O pins when not used for peripheral functions.
- Programmable port input and key input interrupts

● A/D Converter (ADC)
- 4-channel, 10-bit A/D converters
- Can generate an interrupt upon completion of conversion.
- Can generate an interrupt when converted value is outside specified upper and lower limits.

● RTC
- Contains BCD time (second, minute, and hour) counters and calendar (day, days of the week, month, and year) counters.
- Allows selection between 24-hour and 12-hour modes.
- Equipped with function for 30-second correction in software.
- Can periodically generate interrupts (at intervals of 1/64 or 1 second, 1 minute, or 1 hour).
- Powered independently of other modules, and can operate even when system power is turned off.
- Contains an OSC1 oscillator circuit to generate 32.768 kHz (typ.) clock.

OPERATING CONDITIONS AND POWER CONSUMPTION

● Power Supply Voltage
- Core power supply voltages (V_{DD}, $PLLV_{DD}$, $RTCV_{DD}$): 1.65 V to 1.95 V (1.8 V ± 0.15 V)
- I/O power supply voltages (V_{DDE}, TMV_{DD}, AV_{DD}): 2.70 V to 3.60 V (3.0/3.3 V ± 0.3 V)

● Input Voltage
- High-level input voltage: 2.20 V (min.) to V_{DDE} (max.)
- Low-level input voltage: V_{SS} (min.) to 0.80 V (max.)

● Operating Clock Frequency
- CPU: 66 MHz (max.)
- Bus (BBCU, EBCU): 66 MHz (max.)

● Operating Temperature
- -40°C to 85°C

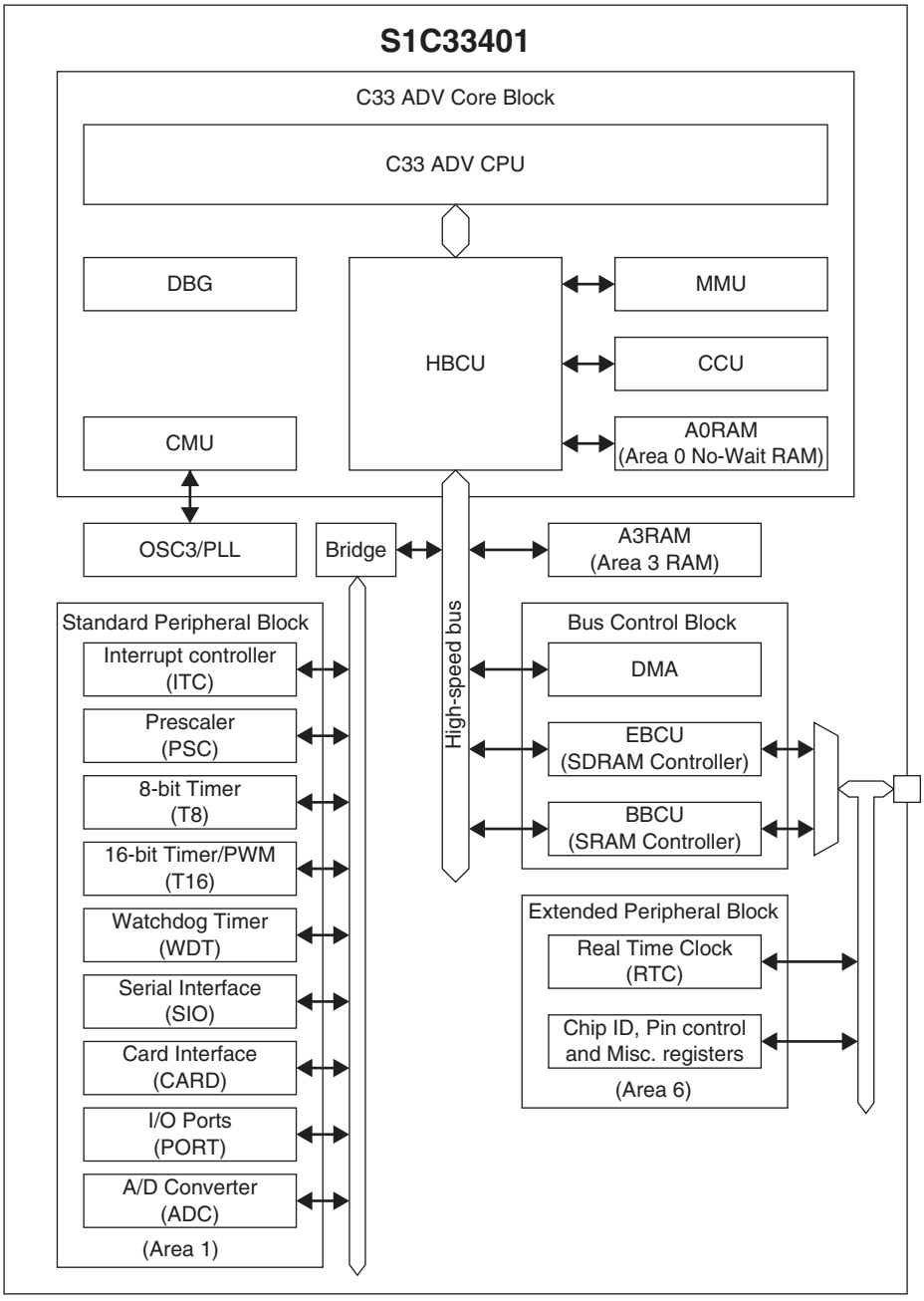
● **Power Consumption**

- In SLEEP mode: 25 µW (typ.)
- In HALT mode: 36 mW (typ., 66 MHz)
- During operation: 65 mW (typ., 66 MHz, cache off)

FORM OF SHIPMENT

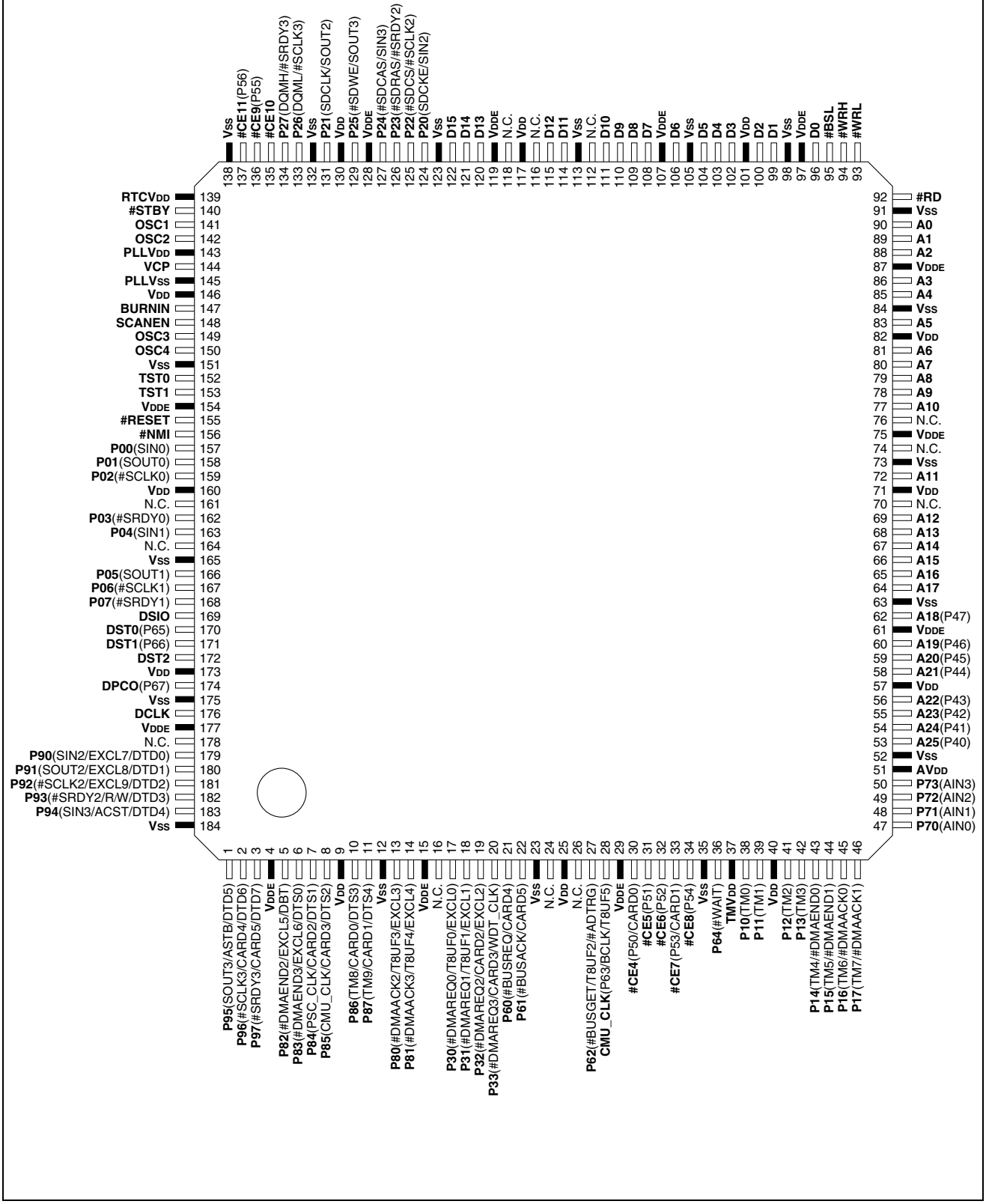
- PFBGA 160-pin plastic package (10 mm × 10 mm × 1.2 mm, 0.65 mm pitch)
- QFP20 184-pin plastic package (20 mm × 20 mm × 1.7 mm, 0.40 mm pitch)

■ BLOCK DIAGRAM

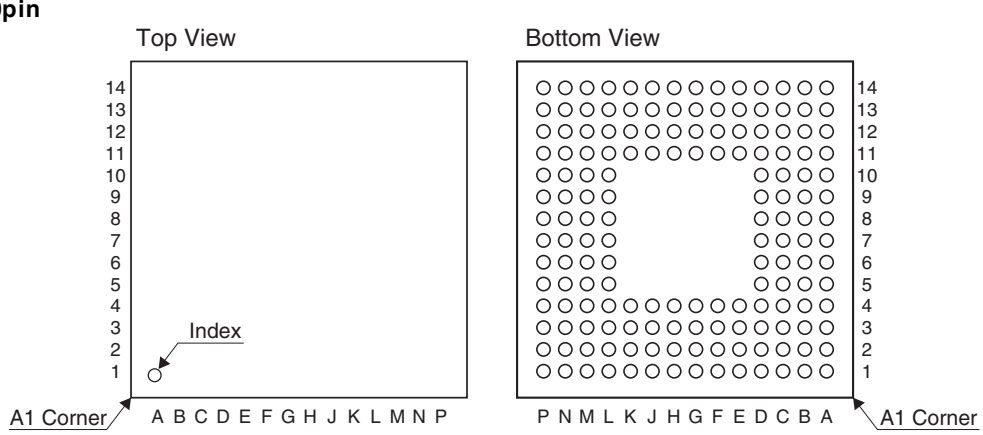


■ PIN LAYOUT DIAGRAM

QFP20-184pin



PFBGA-160pin



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	N.C.	**P92** #SCLK2 EXCL9 DTD2	**P90** SIN2 EXCL7 DTD0	**DCLK**	**P66** DST1	**P06** #SCLK1	**P03** #SRDY0	**P00** SIN0	**OSC4**	**OSC3**	**VSS**	**OSC2**	**OSC1**	N.C.	A
B	**P95** SOUT3 ASTB DTD5	**P93** #SRDY2 R/W DTD3	**P91** SOUT2 EXCL8 DTD1	**P67** DPCO	**P65** DST0	**P05** SOUT1	**VDD**	**#NMI**	**TST1**	**SCANEN**	**VDD**	**RTCVDD**	**#STBY**	**VSS**	B
C	**P97** #SRDY3 CARD5 DTD7	**P96** #SCLK3 CARD4 DTD6	**VSS**	**P94** SIN3 ACST DTD4	**DSIO**	**P07** #SRDY1	**P04** SIN1	**P01** SOUT0	**TST0**	**BURNIN**	**VCP**	**PLLVDD**	**#CE10**	**P27** DQMH #SRDY3	C
D	**P84** PSC_CLK CARD2 DTS1	**P83** #DMAEND3 EXCL6 DTS0	**P82** #DMAEND2 EXCL5 DBT	**VDDE**	**DST2**	**VSS**	**P02** #SCLK0	**#RESET**	**VDDE**	**#CE11** P56	**PLLVSS**	**P26** DQML #SCLK3	**VSS**	**P21** SDCLK SOUT2	D
E	**P86** TM8 CARD0 DTS3	**VSS**	**P85** CMU_CLK CARD3 DTS2	**VDD**							**#CE9** P55	**P25** #SDWE SOUT3	**P24** #SDCAS SIN3	**VDDE**	E
F	**P81** #DMAACK3 T8UF4 EXCL4	**P30** #DMAREQ0 T8UF0 EXCL0	**P87** TM9 CARD1 DTS4	**P80** #DMAACK2 T8UF3 EXCL3							**VDD**	**P23** #SDRAS #SRDY2	**D15**	**P20** SDCKE SIN2	F
G	**P32** #DMAREQ2 CARD2 EXCL2	**P61** #BUSACK CARD5	**P31** #DMAREQ1 T8UF1 EXCL1	**P33** #DMAREQ3 CARD3 WDT_CLK							**P22** #SDCS #SCLK2	**D13**	**D14**	**VDD**	G
H	**CMU_CLK** P63 BCLK T8UF5	**P62** #BUSGET T8UF2 #ADTRG	**P60** #BUSREQ CARD4	**VDDE**							**VDDE**	**D11**	**D12**	**VSS**	H
J	**#CE6** P52	**#CE5** P51	**#CE7** P53 CARD1	**#CE4** P50 CARD0							**D9**	**D8**	**D10**	**D7**	J
K	**P64** #WAIT	**TMVDD**	**VSS**	**#CE8** P54							**VSS**	**D4**	**D6**	**D5**	K
L	**P11** TM1	**P12** TM2	**P13** TM3	**P10** TM0	**VDD**	**A21** P44	**A16**	**VSS**	**A6**	**A4**	**D3**	**VDD**	**D2**	**D1**	L
M	**P14** TM4 #DMAEND0	**P16** TM6 #DMAACK0	**P17** TM7 #DMAACK1	**P15** TM5 #DMAEND1	**A23** P42	**VDDE**	**A14**	**A11**	**A9**	**VSS**	**#WRL**	**#WRH**	**#BSL**	**D0**	M
N	**P70** AIN0	**P71** AIN1	**AVDD**	**A25** P40	**A22** P43	**A19** P46	**A17**	**A13**	**A8**	**A5**	**VDDE**	**A1**	**VSS**	**#RD**	N
P	N.C.	**P72** AIN2	**P73** AIN3	**A24** P41	**A20** P45	**A18** P47	**A15**	**A12**	**A10**	**A7**	**A3**	**A2**	**A0**	N.C.	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Top View

■ PIN DESCRIPTION

Power Supply Pin List

Pin name	Pin No.		Function
	QFP	PFBGA	
V_{DD}	9,25,40,57,71,82,101, 117,130,146,160,173	B7,B11,E4,F11,G14, L5,L12	Power supply (+) for the internal logic circuits (1.65 V to 1.95 V)
V_{SS}	12,23,35,52,63,73,84,91,98, 105,113,123,132,138,151, 165,175,184	A11,B14,C3,D6,D13,E2, H14,K3,K11,L8,M10,N13	Power supply (–); GND
$PLLV_{DD}$	143	C12	Power supply (+) for the PLL ($PLLV_{DD} = V_{DD}$)
$PLLV_{SS}$	145	D11	Power supply (–) for the PLL ($PLLV_{SS} = V_{SS}$)
$RTCV_{DD}$	139	B12	Power supply (+) for the RTC ($RTCV_{DD} = V_{DD}$)
V_{DDE}	4,15,29,61,75,87,97,107, 119,128,154,177	D4,D9,E14,H4,H11,M6,N11	Power supply (+) for the I/O block (2.7 V to 3.6 V)
TMV_{DD}	37	K2	Power supply (+) for PWM timer outputs (P1*x* port) ($TMV_{DD} = V_{DDE}$)
AV_{DD}	51	N3	Power supply (+) for the analog system and AIN0–AIN3 ($AV_{DD} = V_{DDE}$)

External Bus Pin List

Pin name	Pin No.		I/O	Pull-up	Function	Module
	QFP	PFBGA				
D[15:0]	122–120, 115,114, 111–108, 106, 104–102, 100,99, 96	F13,G13, G12,H13, H12,J13, J11,J12, J14,K13, K14,K12, L11,L13, L14,M14	I/O	∗2	Data bus (D15–D0)	BBCU EBCU
#BSL	95	M13	**O**	∗1	Bus strobe (low byte) signal in BSL mode	BBCU
#RD	92	N14	**O**	∗1	Read signal	BBCU
#WRL	93	M11	**O**	∗1	Write (low byte) signal in A0 mode or write signal in BSL mode	BBCU
#WRH	94	M12	**O**	∗1	Write (high byte) signal in A0 mode or Bus strobe (high byte) signal in BSL mode	BBCU
A[17:0]	64–69, 72, 77–81, 83,85, 86, 88–90	N7,L7, P7,M7, N8,P8, M8,P9, M9,N9, P10,L9, N10,L10, P11,P12, N12,P13	**O**	∗1	Address bus (A17–A0)	BBCU EBCU
A18	62	P6	I/**O**	∗1	A18: Address bus (A18) (default)	BBCU
P47					P47: General-purpose I/O port	PORT
A19	60	N6	I/**O**	∗1	A19: Address bus (A19) (default)	BBCU
P46					P46: General-purpose I/O port	PORT
A20	59	P5	I/**O**	∗1	A20: Address bus (A20) (default)	BBCU
P45					P45: General-purpose I/O port	PORT
A21	58	L6	I/**O**	∗1	A21: Address bus (A21) (default)	BBCU
P44					P44: General-purpose I/O port	PORT
A22	56	N5	I/**O**	∗1	A22: Address bus (A22) (default)	BBCU
P43					P43: General-purpose I/O port	PORT
A23	55	M5	I/**O**	∗1	A23: Address bus (A23) (default)	BBCU
P42					P42: General-purpose I/O port	PORT
A24	54	P4	I/**O**	∗1	A24: Address bus (A24) (default)	BBCU
P41					P41: General-purpose I/O port	PORT
A25	53	N4	I/**O**	∗1	A25: Address bus (A25) (default)	BBCU
P40					P40: General-purpose I/O port	PORT
#CE11	137	D10	I/**O**	∗1	#CE11: Chip enable signal for areas 11 and 12 (default)	BBCU
P56					P56: General-purpose I/O port	PORT
#CE10	135	C13	I/**O**	∗1	Chip enable signal for areas 10, 13 and 20	BBCU
#CE9	136	E11	I/**O**	∗1	#CE9: Chip enable signal for areas 9 and 22 (default)	BBCU
P55					P55: General-purpose I/O port	PORT
#CE8	34	K4	I/**O**	∗1	#CE8: Chip enable signal for areas 8 and 21 (default)	BBCU
P54					P54: General-purpose I/O port	PORT

Pin name	Pin No.		I/O	Pull-up	Function	Module
	QFP	PFBGA				
#CE7	33	J3	I/**O**	∗1	#CE7: Chip enable signal for areas 7 and 19 (default)	BBCU
P53					P53: General-purpose I/O port	PORT
CARD1					CARD1: Card I/F signal 1 output (#SMWR or #CFCE2)	CARD
#CE6	32	J1	I/**O**	∗1	#CE6: Chip enable signal for areas 6, 17 and 18 (default)	BBCU
P52					P52: General-purpose I/O port	PORT
#CE5	31	J2	I/**O**	∗1	#CE5: Chip enable signal for areas 5, 15 and 16 (default)	BBCU
P51					P51: General-purpose I/O port	PORT
#CE4	30	J4	I/**O**	∗1	#CE4: Chip enable signal for areas 4 and 14 (default)	BBCU
P50					P50: General-purpose I/O port	PORT
CARD0					CARD0: Card I/F signal 0 output (#SMRD or #CFCE1)	CARD

Input/Output Port and Peripheral Circuit Pin List

Pin name	Pin No.		I/O	Pull-up	Function	Module
	QFP	PFBGA				
P00	157	A8	**I**/O	∗1	P00: General-purpose I/O port (default)	PORT
SIN0					SIN0: Serial I/F Ch.0 data input	SIO
P01	158	C8	**I**/O	∗1	P01: General-purpose I/O port (default)	PORT
SOUT0					SOUT0: Serial I/F Ch.0 data output	SIO
P02	159	D7	**I**/O	∗1	P02: General-purpose I/O port (default)	PORT
#SCLK0					#SCLK0: Serial I/F Ch.0 clock input/output	SIO
P03	162	A7	**I**/O	∗1	P03: General-purpose I/O port (default)	PORT
#SRDY0					#SRDY0: Serial I/F Ch.0 ready signal input/output	SIO
P04	163	C7	**I**/O	∗1	P04: General-purpose I/O port (default)	PORT
SIN1					SIN1: Serial I/F Ch.1 data input	SIO
P05	166	B6	**I**/O	∗1	P05: General-purpose I/O port (default)	PORT
SOUT1					SOUT1: Serial I/F Ch.1 data output	SIO
P06	167	A6	**I**/O	∗1	P06: General-purpose I/O port (default)	PORT
#SCLK1					#SCLK1: Serial I/F Ch.1 clock input/output	SIO
P07	168	C6	**I**/O	∗1	P07: General-purpose I/O port (default)	PORT
#SRDY1					#SRDY1: Serial I/F Ch.1 ready signal input/output	SIO
P10	38	L4	**I**/O	∗1	P10: General-purpose I/O port (default)	PORT
TM0					TM0: 16-bit timer 0 output	T16
P11	39	L1	**I**/O	∗1	P11: General-purpose I/O port (default)	PORT
TM1					TM1: 16-bit timer 1 output	T16
P12	41	L2	**I**/O	∗1	P12: General-purpose I/O port (default)	PORT
TM2					TM2: 16-bit timer 2 output	T16
P13	42	L3	**I**/O	∗1	P13: General-purpose I/O port (default)	PORT
TM3					TM3: 16-bit timer 3 output	T16
P14	43	M1	**I**/O	∗1	P14: General-purpose I/O port (default)	PORT
TM4					TM4: 16-bit timer 4 output	T16
#DMAEND0					#DMAEND0: HSDMA Ch.0 end-of-transfer signal output	HSDMA
P15	44	M4	**I**/O	∗1	P15: General-purpose I/O port (default)	PORT
TM5					TM5: 16-bit timer 5 output	T16
#DMAEND1					#DMAEND1: HSDMA Ch.1 end-of-transfer signal output	HSDMA
P16	45	M2	**I**/O	∗1	P16: General-purpose I/O port (default)	PORT
TM6					TM6: 16-bit timer 6 output	T16
#DMAACK0					#DMAACK0: HSDMA Ch.0 acknowledge signal output	HSDMA
P17	46	M3	**I**/O	∗1	P17: General-purpose I/O port (default)	PORT
TM7					TM7: 16-bit timer 7 output	T16
#DMAACK1					#DMAACK1: HSDMA Ch.1 acknowledge signal output	HSDMA
P20	124	F14	**I**/O	∗1	P20: General-purpose I/O port (default)	PORT
SDCKE					SDCKE: SDRAM clock enable signal output	EBCU
SIN2					SIN2: Serial I/F Ch.2 data input	SIO
P21	131	D14	**I**/O	∗1	P21: General-purpose I/O port (default)	PORT
SDCLK					SDCLK: SDRAM clock output	EBCU
SOUT2					SOUT2: Serial I/F Ch.2 data output	SIO
P22	125	G11	**I**/O	∗1	P22: General-purpose I/O port (default)	PORT
#SDCS					#SDCS: SDRAM chip enable signal output	EBCU
#SCLK2					#SCLK2: Serial I/F Ch.2 clock input/output	SIO
P23	126	F12	**I**/O	∗1	P23: General-purpose I/O port (default)	PORT
#SDRAS					#SDRAS: SDRAM row address strobe signal output	EBCU
#SRDY2					#SRDY2: Serial I/F Ch.2 ready signal input/output	SIO
P24	127	E13	**I**/O	∗1	P24: General-purpose I/O port (default)	PORT
#SDCAS					#SDCAS: SDRAM column address strobe signal output	EBCU
SIN3					SIN3: Serial I/F Ch.3 data input	SIO

Pin name	Pin No.		I/O	Pull-up	Function		Module
	QFP	PFBGA					
P25	129	E12	I/O	*1	P25:	General-purpose I/O port (default)	PORT
#SDWE					#SDWE:	SDRAM write signal output	EBCU
SOUT3					SOUT3:	Serial I/F Ch.3 data output	SIO
P26	133	D12	I/O	*1	P26:	General-purpose I/O port (default)	PORT
DQML					DQML:	SDRAM data (low byte) input/output mask signal output	EBCU
#SCLK3					#SCLK3:	Serial I/F Ch.3 clock input/output	SIO
P27	134	C14	I/O	*1	P27:	General-purpose I/O port (default)	PORT
DQMH					DQMH:	SDRAM data (high byte) input/output mask signal output	EBCU
#SRDY3					#SRDY3:	Serial I/F Ch.3 ready signal input/output	SIO
P30	17	F2	I/O	*1	P30:	General-purpose I/O port (default)	PORT
#DMAREQ0					#DMAREQ0:	HSDMA Ch.0 request input	HSDMA
T8UF0					T8UF0:	8-bit timer 0 output	T8
EXCL0					EXCL0:	16-bit timer 0 event counter input	T16
P31	18	G3	I/O	*1	P31:	General-purpose I/O port (default)	PORT
#DMAREQ1					#DMAREQ1:	HSDMA Ch.1 request input	HSDMA
T8UF1					T8UF1:	8-bit timer 1 output	T8
EXCL1					EXCL1:	16-bit timer 1 event counter input	T16
P32	19	G1	I/O	*1	P32:	General-purpose I/O port (default)	PORT
#DMAREQ2					#DMAREQ2:	HSDMA Ch.2 request input	HSDMA
CARD2					CARD2:	Card I/F signal 2 output (#IORD or #SMRD)	CARD
EXCL2					EXCL2:	16-bit timer 2 event counter input	T16
P33	20	G4	I/O	*1	P33:	General-purpose I/O port (default)	PORT
#DMAREQ3					#DMAREQ3:	HSDMA Ch.3 request input	HSDMA
CARD3					CARD3:	Card I/F signal 3 output (#IOWR or #SMWR)	CARD
WDT_CLK					WDT_CLK:	Watchdog timer output	WDT
P60	21	H3	I/O	*1	P60:	General-purpose I/O port (default)	PORT
#BUSREQ					#BUSREQ:	Bus release request input	BBCU
CARD4					CARD4:	Card I/F signal 4 output (#OE or #CFCE1)	CARD
P61	22	G2	I/O	*1	P61:	General-purpose I/O port (default)	PORT
#BUSACK					#BUSACK:	Bus acknowledge output	BBCU
CARD5					CARD5:	Card I/F signal 5 output (#WE or #CFCE2)	CARD
P62	27	H2	I/O	*1	P62:	General-purpose I/O port (default)	PORT
#BUSGET					#BUSGET:	Bus status monitor signal output	BBCU
T8UF2					T8UF2:	8-bit timer 2 output	T8
#ADTRG					#ADTRG:	A/D converter trigger input	ADC
P64	36	K1	I/O	*1	P64:	General-purpose I/O port (default)	PORT
#WAIT					#WAIT:	Wait cycle request input	BBCU
P70	47	N1	I	*1	P70:	General-purpose I/O port (default)	PORT
AIN0					AIN0:	A/D converter Ch.0 input	ADC
P71	48	N2	I	*1	P71:	General-purpose I/O port (default)	PORT
AIN1					AIN1:	A/D converter Ch.1 input	ADC
P72	49	P2	I	*1	P72:	General-purpose I/O port (default)	PORT
AIN2					AIN2:	A/D converter Ch.2 input	ADC
P73	50	P3	I	*1	P73:	General-purpose I/O port (default)	PORT
AIN3					AIN3:	A/D converter Ch.3 input	ADC
P80	13	F4	I/O	*1	P80:	General-purpose I/O port (default)	PORT
#DMAACK2					#DMAACK2:	HSDMA Ch.2 acknowledge signal output	HSDMA
T8UF3					T8UF3:	8-bit timer 3 output	T8
EXCL3					EXCL3:	16-bit timer 3 event counter input	T16
P81	14	F1	I/O	*1	P81:	General-purpose I/O port (default)	PORT
#DMAACK3					#DMAACK3:	HSDMA Ch.3 acknowledge signal output	HSDMA
T8UF4					T8UF4:	8-bit timer 4 output	T8
EXCL4					EXCL4:	16-bit timer 4 event counter input	T16
P82	5	D3	I/O	*1	P82:	General-purpose I/O port (default)	PORT
#DMAEND2					#DMAEND2:	HSDMA Ch.2 end-of-transfer signal output	HSDMA
EXCL5					EXCL5:	16-bit timer 5 event counter input	T16
DBT					DBT:	DBT signal output for debugging	DBG
P83	6	D2	I/O	*1	P83:	General-purpose I/O port (default)	PORT
#DMAEND3					#DMAEND3:	HSDMA Ch.3 end-of-transfer signal output	HSDMA
EXCL6					EXCL6:	16-bit timer 6 event counter input	T16
DTS0					DTS0:	DTS0 signal output for debugging	DBG
P84	7	D1	I/O	*1	P84:	General-purpose I/O port (default)	PORT
PSC_CLK					PSC_CLK:	Prescaler clock output	PSC
CARD2					CARD2:	Card I/F signal 2 output (#IORD or #SMRD)	CARD
DTS1					DTS1:	DTS1 signal output for debugging	DBG

Pin name	Pin No.		I/O	Pull-up	Function		Module
	QFP	PFBGA					
P85	8	E3	**I**/O	∗1	P85:	General-purpose I/O port (default)	PORT
CMU_CLK					CMU_CLK:	CMU external clock output	CMU
CARD3					CARD3:	Card I/F signal 3 output (#IOWR or #SMWR)	CARD
DTS2					DTS2:	DTS2 signal output for debugging	DBG
P86	10	E1	**I**/O	∗1	P86:	General-purpose I/O port (default)	PORT
TM8					TM8:	16-bit timer 8 output	T16
CARD0					CARD0:	Card I/F signal 0 output (#SMRD or #CFCE1)	CARD
DTS3					DTS3:	DTS3 signal output for debugging	DBG
P87	11	F3	**I**/O	∗1	P87:	General-purpose I/O port (default)	PORT
TM9					TM9:	16-bit timer 9 output	T16
CARD1					CARD1:	Card I/F signal 1 output (#SMWR or #CFCE2)	CARD
DTS4					DTS4:	DTS4 signal output for debugging	DBG
P90	179	A3	**I**/O	∗1	P90:	General-purpose I/O port (default)	PORT
SIN2					SIN2:	Serial I/F Ch.2 data input	SIO
EXCL7					EXCL7:	16-bit timer 7 event counter input	T16
DTD0					DTD0:	DTD0 signal output for debugging	DBG
P91	180	B3	**I**/O	∗1	P91:	General-purpose I/O port (default)	PORT
SOUT2					SOUT2:	Serial I/F Ch.2 data output	SIO
EXCL8					EXCL8:	16-bit timer 8 event counter input	T16
DTD1					DTD1:	DTD1 signal output for debugging	DBG
P92	181	A2	**I**/O	∗1	P92:	General-purpose I/O port (default)	PORT
#SCLK2					#SCLK2:	Serial I/F Ch.2 clock input/output	SIO
EXCL9					EXCL9:	16-bit timer 9 event counter input	T16
DTD2					DTD2:	DTD2 signal output for debugging	DBG
P93	182	B2	**I**/O	∗1	P93:	General-purpose I/O port (default)	PORT
#SRDY2					#SRDY2:	Serial I/F Ch.2 ready signal input/output	SIO
R/W					R/W:	Read/Write status output	BBCU
DTD3					DTD3:	DTD3 signal output for debugging	DBG
P94	183	C4	**I**/O	∗1	P94:	General-purpose I/O port (default)	PORT
SIN3					SIN3:	Serial I/F Ch.3 data input	SIO
ACST					ACST:	Bus access status output	BBCU
DTD4					DTD4:	DTD4 signal output for debugging	DBG
P95	1	B1	**I**/O	∗1	P95:	General-purpose I/O port (default)	PORT
SOUT3					SOUT3:	Serial I/F Ch.3 data output	SIO
ASTB					ASTB:	Address strobe output	BBCU
DTD5					DTD5:	DTD5 signal output for debugging	DBG
P96	2	C2	**I**/O	∗1	P96:	General-purpose I/O port (default)	PORT
#SCLK3					#SCLK3:	Serial I/F Ch.3 clock input/output	SIO
CARD4					CARD4:	Card I/F signal 4 output (#OE or #CFCE1)	CARD
DTD6					DTD6:	DTD6 signal output for debugging	DBG
P97	3	C1	**I**/O	∗1	P97:	General-purpose I/O port (default)	PORT
#SRDY3					#SRDY3:	Serial I/F Ch.3 ready signal input/output	SIO
CARD5					CARD5:	Card I/F signal 5 output (#WE or #CFCE2)	CARD
DTD7					DTD7:	DTD7 signal output for debugging	DBG

Debug Pin List

Pin name	Pin No.		I/O	Pull-up	Function		Module
	QFP	PFBGA					
DSIO	169	C5	**I**/O	Pull-up	Serial input/output for debugging		DBG
DCLK	176	A4	**O** (H)	–	DCLK signal output for debugging		DBG
DST2	172	D5	**O** (L)	–	DST2 signal output for debugging		DBG
DST0	170	B5	I/**O**	∗1	DST0:	DST0 signal output for debugging (default)	DBG
P65			(H)		P65:	General-purpose I/O port	PORT
DST1	171	A5	I/**O**	∗1	DST1:	DST1 signal output for debugging (default)	DBG
P66			(H)		P66:	General-purpose I/O port	PORT
DPCO	174	B4	I/**O**	∗1	DPCO:	DPCO signal output for debugging (default)	DBG
P67			(H)		P67:	General-purpose I/O port	PORT

Other Pin List

Pin name	Pin No.		I/O	Pull-up/down	Function	Module
	QFP	PFBGA				
OSC1	141	A13	**I**	–	Low speed (OSC1) oscillator input (32 kHz crystal or external clock input with V_{DD} level)	OSC
OSC2	142	A12	**O**	–	Low speed (OSC1) oscillator output	OSC
OSC3	149	A10	**I**	–	High speed (OSC3) oscillator input (crystal/ceramic or external clock input with V_{DD} level)	OSC
OSC4	150	A9	**O**	–	High speed (OSC3) oscillator output	OSC
VCP	144	C11	**O**	–	PLL analog monitor (used for current monitor)	CMU
CMU_CLK P63 BCLK T8UF5	28	H1	I/**O**	*1	CMU_CLK: CMU external clock output (default) P63: General-purpose I/O port BCLK: Bus clock output T8UF5: 8-bit timer 5 output	CMU PORT BBCU T8
#RESET	155	D8	**I**	Pull-up	Initial reset input pin	CMU
#NMI	156	B8	**I**	Pull-up	NMI request input pin	CMU
TST0	152	C9	**I**	Pull-down	Test input pin 0 (Connect to V_{SS} during normal operation)	–
TST1	153	B9	**I**	Pull-down	Test input pin 1 (Connect to V_{SS} during normal operation)	–
BURNIN	147	C10	**I**	–	Wafer level burn-in test enable input	–
SCANEN	148	B10	**I**	Pull-down	Scan test enable input	–
#STBY	140	B13	**I**	–	Standby input for disabling C33 operation (except RTC)	RTC

*1: These pins can have pull-ups enabled or disabled by setting the pin control registers. (Pull-ups are enabled by default.)

*2: These pins come with a bus hold latch.

Notes:
- The # prefixed to pin names indicates that input/output signals of the pin are active low.
- The pin names and I/O printed in boldface denote the default pin (signal) name and default input/output direction.
- (H) and (L) for I/O indicate the default output level. This is only indicated for signals whose level is fixed high or low when the chip is initially reset.
- The input level must be V_{DD} only for the OSC1 and OSC3 pins. Input levels for other pins should be V_{DDE} (AV_{DD}, TMV_{DD}) level.

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SEMICONDUCTOR OPERATIONS DIVISION

■ EPSON Electronic Devices Website
http://www.epson.jp/device/semicon_e

IC Sales Dept.
IC International Sales Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117

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