

Document Title**1M x 8bit 2.7 ~ 3.6V Super low Power FCMOS Slow SRAM**Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
00	Initial Draft	Jan.19.2002	Preliminary

DESCRIPTION

The HY62KF08802B is a high speed, super low power and 8Mbit full CMOS SRAM organized as 1M words by 8bits. The HY62KF08802B uses high performance full CMOS process technology and is designed for high speed and low power circuit technology. It is particularly well-suited for the high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 1.2V.

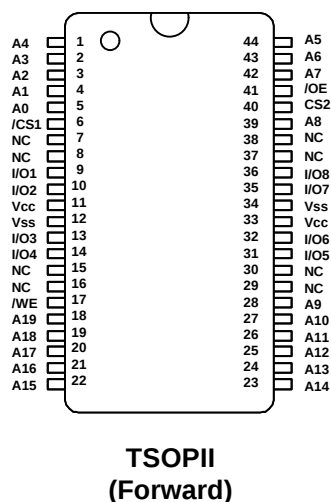
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup
 - 1.2V(min) data retention
- Standard pin configuration
 - 44pin 400mil TSOP-II (Forward)

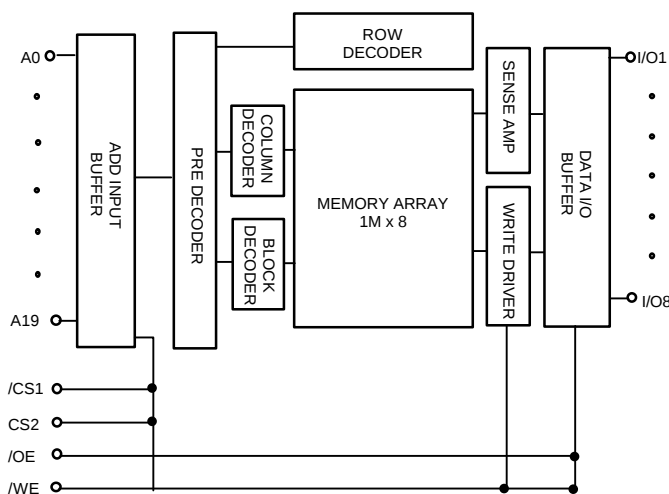
Product No.	Voltage (V)	Speed (ns)	Operation Current/I _{cc} (mA)	Standby Current(μA)		Temperature (°C)
				SL	LL	
HY62KF08802B-I	2.7~3.6	55/70	2	12	30	-40~85

Note 1. I : Industrial
2. Current value is max.

PIN CONNECTION



BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Function	Pin Name	Pin Function
/CS1, CS2	Chip Select	A0~A19	Address Inputs
/WE	Write Enable	Vcc	Power (2.7~3.6V)
/OE	Output Enable	Vss	Ground
I/O1~I/O8	Data Inputs/Outputs	NC	No Connection

ORDERING INFORMATION

Part No.	Speed	Power	Temp	Package
HY62KF08802B-SD(I)	55/70	SL-part	I	TSOP-II
HY62KF08802B-DD(I)	55/70	LL-part	I	TSOP-II

Note 1. I : Industrial

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating	Unit	Remark
V _{IN} , V _{OUT}	Input/Output Voltage	-0.3 to V _{CC} +0.3V	V	
V _{CC}	Power Supply	-0.3 to 4.6	V	
T _A	Operating Temperature	-40 to 85	°C	HY62KF08802B-I
T _{STG}	Storage Temperature	-55 to 150	°C	
P _D	Power Dissipation	1.0	W	
T _{SOLDER}	Ball Soldering Temperature & Time	260 • 10	°C•sec	

Note

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

TRUTH TABLE

/CS1	CS2	/WE	/OE	Mode	I/O Pin (/I/O1~/I/O8)	Power
H	X	X	X	Deselected	High-Z	Standby
X	L	X	X	Deselected	High-Z	
L	H	H	H	Output Disabled	High-Z	Active
L	H	H	L	Read	DOUT	Active
L	H	L	X	Write	DIN	Active

Note:

- H=V_{IH}, L=V_{IL}, X=don't care (V_{IL} or V_{IH})

RECOMMENDED DC OPERATING CONDITION

Symbol	Parameter	Min.	Typ	Max.	Unit
V _{CC}	Supply Voltage	2.7	3.0 or 3.3	3.6	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	-	V _{CC} +0.3	V
V _{IL}	Input Low Voltage	-0.3 ¹	-	0.6	V

Note : 1. Undershoot : V_{IL} = -1.5V for pulse width less than 30ns
 2. Undershoot is sampled, not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = -40°C to 85°C

Sym	Parameter	Test Condition	Min	Typ ¹	Max	Unit
I _{LI}	Input Leakage Current	V _{SS} ≤ V _{IN} ≤ V _{CC}	-1	-	1	uA
I _{LO}	Output Leakage Current	V _{SS} ≤ V _{OUT} ≤ V _{CC} , /CS1 = V _{IH} or CS2 = V _{IL} or /OE = V _{IH} or /WE = V _{IL}	-1	-	1	uA
I _{CC}	Operating Power Supply Current	/CS1 = V _{IL} , CS2 = V _{IH} V _{IN} = V _{IH} or V _{IL} , I _{I/O} = 0mA			4	mA
I _{CC1}	Average Operating Current	/CS1 = V _{IL} , CS2 = V _{IH} V _{IN} = V _{IH} or V _{IL} , Cycle Time = Min, 100% Duty, I _{I/O} = 0mA	3.0~	55ns	25	mA
			3.6V	70ns	20	mA
			2.7~	55ns	20	mA
			3.3V	70ns	15	mA
		/CS1 ≤ 0.2V, CS2 ≥ V _{CC} -0.2V V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} -0.2V, Cycle Time = 1us, 100% Duty, I _{I/O} = 0mA			3	mA
I _{SB}	Standby Current (TTL Input)	/CS1 = V _{IH} , CS2 = V _{IL} V _{IN} = V _{IH} or V _{IL}			300	uA
I _{SB1}	Standby Current (CMOS Input)	/CS1 ≥ V _{CC} - 0.2V, CS2 ≤ V _{SS} + 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ V _{SS} + 0.2V	3.0~	SL	0.2	12 uA
			3.6V	LL	0.2	30 uA
			2.7~	SL	0.2	12 uA
			3.3V	LL	0.2	25 uA
V _{OL}	Output Low	I _{OL} = 2.1mA	-	-	0.4	V
V _{OH}	Output High	I _{OH} = -1.0mA	2.4	-	-	V

Note

1. Typical values are at V_{CC} = 3.0V T_A = 25°C
2. Typical values are not 100% tested

CAPACITANCE

(Temp = 25°C, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C _{IN}	Input Capacitance (Add, /CS1, CS2, /WE, /OE)	V _{IN} = 0V	8	pF
C _{OUT}	Output Capacitance (I/O)	V _{I/O} = 0V	10	pF

Note : These parameters are sampled and not 100% tested

AC CHARACTERISTICS

T_A = -40°C to 85°C, unless otherwise specified

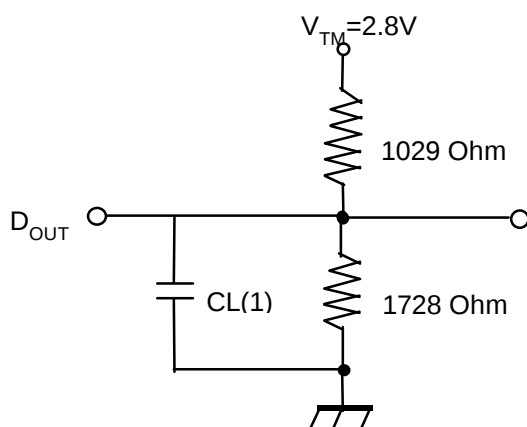
#	Symbol	Parameter	55ns		70ns		Unit
			Min.	Max.	Min.	Max.	
READ CYCLE							
1	tRC	Read Cycle Time	55	-	70	-	ns
2	tAA	Address Access Time	-	55	-	70	ns
3	tACS	Chip Select Access Time	-	55	-	70	ns
4	tOE	Output Enable to Output Valid	-	30	-	35	ns
5	tCLZ	Chip Select to Output in Low Z	10	-	10	-	ns
6	tOLZ	Output Enable to Output in Low Z	5	-	5	-	ns
7	tCHZ	Chip Deselection to Output in High Z	0	20	0	25	ns
8	tOHZ	Out Disable to Output in High Z	0	20	0	25	ns
9	tOH	Output Hold from Address Change	10	-	10	-	ns
WRITE CYCLE							
10	tWC	Write Cycle Time	55	-	70	-	ns
11	tCW	Chip Selection to End of Write	50	-	60	-	ns
12	tAW	Address Valid to End of Write	50	-	60	-	ns
13	tAS	Address Set-up Time	0	-	0	-	ns
14	tWP	Write Pulse Width	45	-	50	-	ns
15	tWR	Write Recovery Time	0	-	0	-	ns
16	tWHZ	Write to Output in High Z	0	20	0	20	ns
17	tDW	Data to Write Time Overlap	25	-	30	-	ns
18	tDH	Data Hold from Write Time	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	ns

AC TEST CONDITIONS

T_A = -40°C to 85°C, unless otherwise specified

Parameter		Value
Input Pulse Level		0.4V to 2.2V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Level		1.5V
Output Load	t _{CLZ} , t _{OLZ} , t _{CHZ} , t _{OHZ} , t _{WHZ} , t _{OW}	CL = 5pF + 1TTL Load
	Others	CL = 30pF + 1TTL Load

AC TEST LOADS

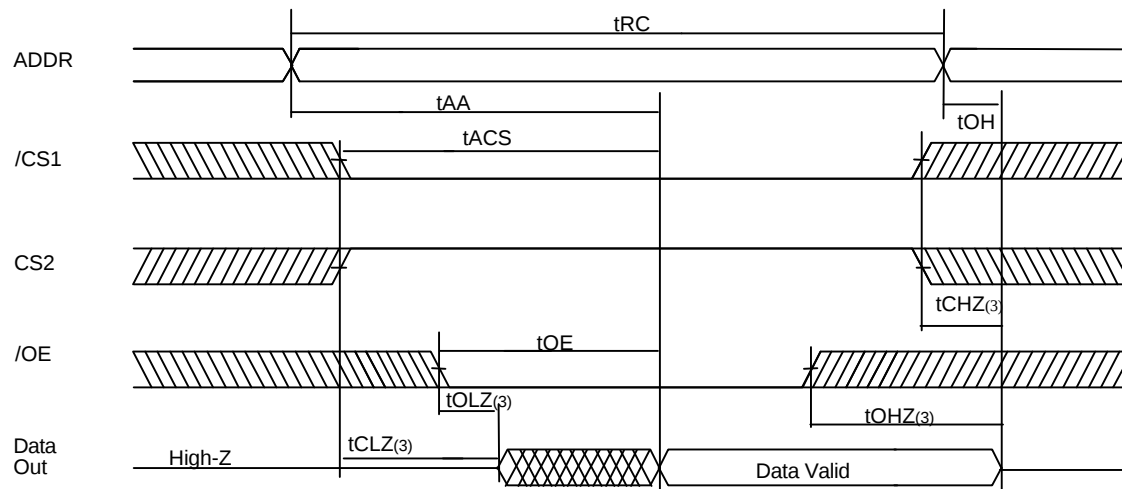


Note

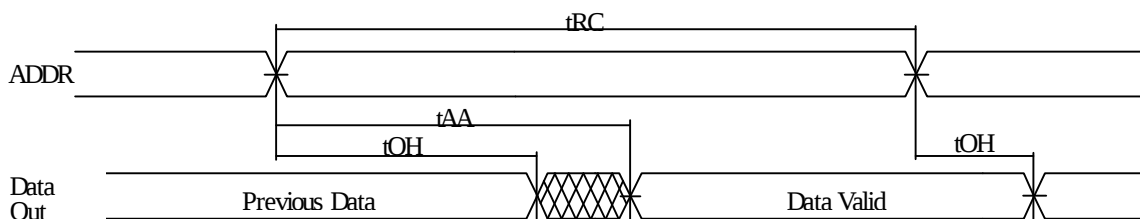
1. Including jig and scope capacitance

TIMING DIAGRAM

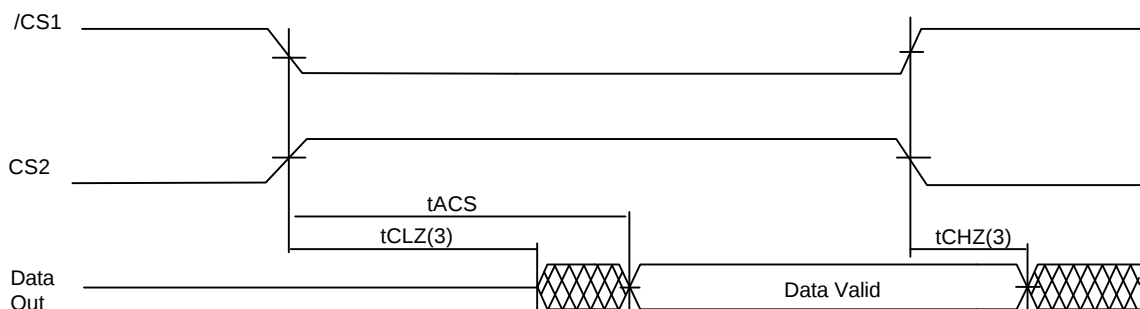
READ CYCLE 1 (Note 1,4)



READ CYCLE 2 (Note 1,2,4)



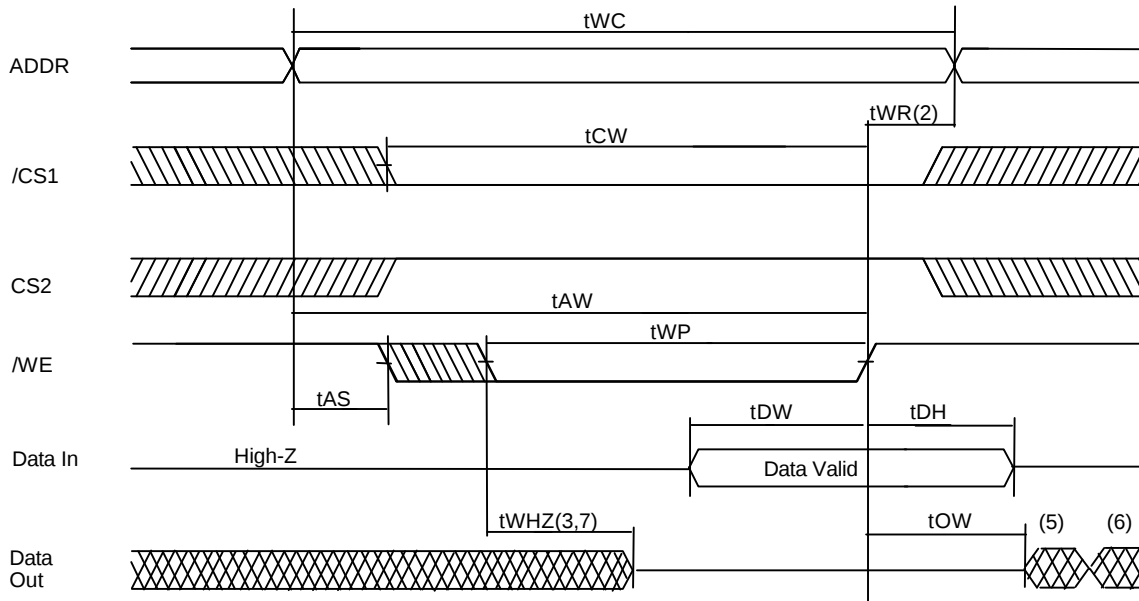
READ CYCLE 3 (Note 1,2,4)



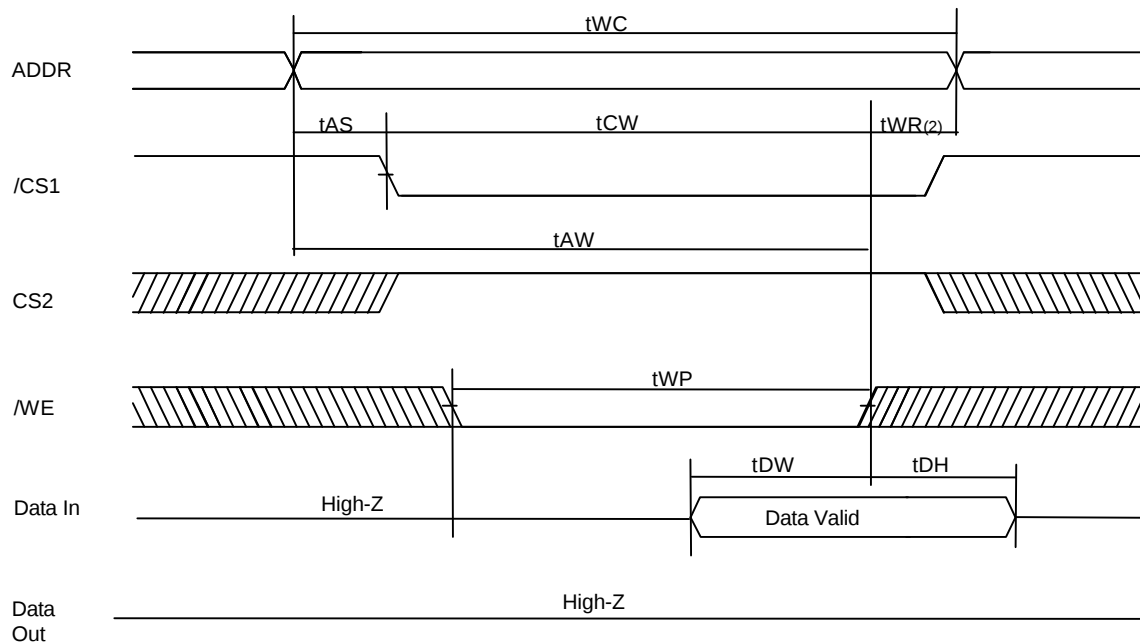
Notes:

1. Read Cycle occurs whenever a high on the /WE and /OE is low, while /CS1 and CS2 are in active status.
2. /OE = V_{IL}
3. Transition is measured $\pm 200\text{mV}$ from steady state voltage.
This parameter is sampled and not 100% tested.
4. /CS1 in high for the standby, low for active
CS2 in low for the standby, high for active.

WRITE CYCLE 1 (1,4,8) (/WE Controlled)



WRITE CYCLE 2 (Note 1,4,8) (/CS1, CS2 Controlled)



Notes:

1. A write occurs during the overlap of a low /WE, a low /CS1, a high CS2.
2. tWR is measured from the earlier of /CS1 or /WE going high or CS2 going low to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the /CS1, CS2 high transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. Q(data out) is the same phase with the write data of this write cycle.
6. Q(data out) is the read data of the next address.
7. Transition is measured $\pm 200\text{mV}$ from steady state. This parameter is sampled and not 100% tested.
8. /CS1 in high for the standby, low for active. CS2 in low for the standby, high for active.

DATA RETENTION ELECTRIC CHARACTERISTIC

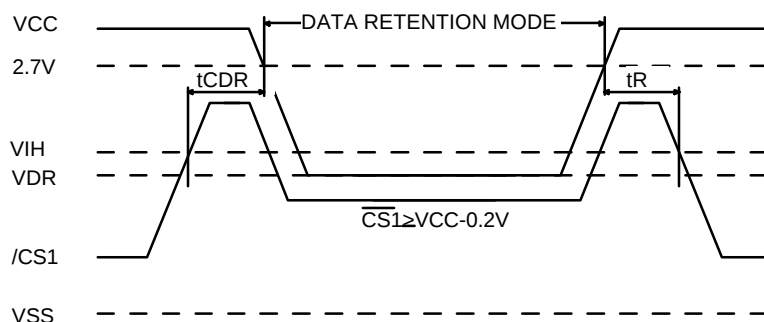
T_A = -40°C to 85°C

Symbol	Parameter	Test Condition	Min	Typ ¹	Max	Unit
V _{DR}	V _{CC} for Data Retention	$V_{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq V_{SS} + 0.2V$	1.2	-	3.6	V
I _{ccdr}	Data Retention Current	$V_{CC}=1.5V$, $V_{CS} \geq V_{CC} - 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq V_{SS} + 0.2V$				
		SL	-	0.1	6	uA
		LL	-	0.1	20	uA
t _{CDR}	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram	0	-	-	ns
t _R	Operating Recovery Time		t _{RC}	-	-	ns

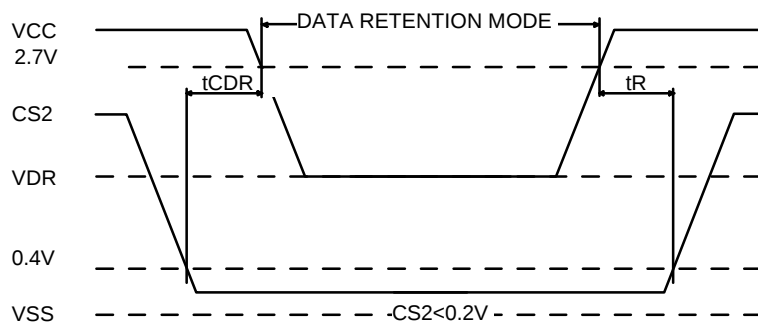
Notes:

1. Typical values are under the condition of T_A = 25°C.
2. Typical value are sampled and not 100% tested

DATA RETENTION TIMING DIAGRAM 1

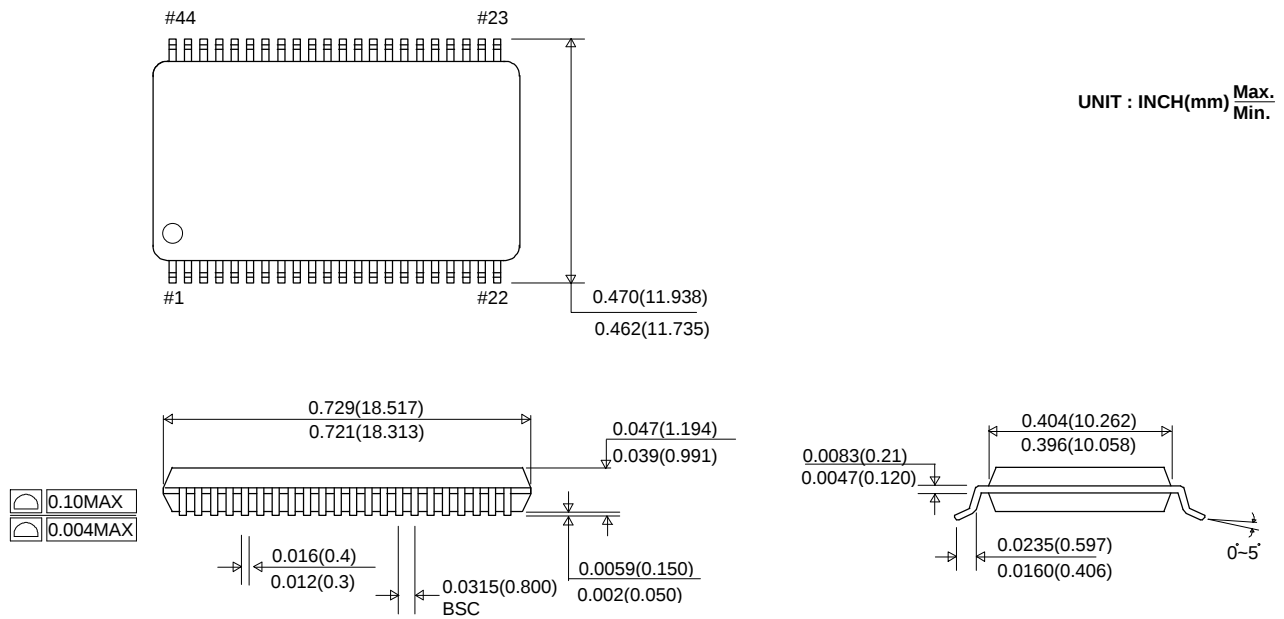


DATA RETENTION TIMING DIAGRAM 2



PACKAGE INFORMATION

44pin 400mil Thin Small Outline Package Forward (D)



MARKING INFORMATION

The diagram illustrates the marking scheme for a TSOP-II (Forward) package. It consists of three rows of markings:

- Row 1:** h y n i x [] [] [] [] y y w w p
- Row 2:** H Y 6 2 K F 8 8 0 2 B c s s t
- Row 3:** K O R E A [] [] [] [] [] [] [] []

A bracket on the left side groups the first two rows of markings.

Index

• hynix	: hynix Logo
• yy	: Year (ex : 02 = year 2002, 03 = year 2002)
• ww	: Work Week (ex : 12 = ww12)
• p	: Process Code
• HY62KF8802B	: Part Name
• c	: Power Consumption
	- D : Low Low Power
	- S : Super Low Power
• ss	: Speed
	- 55 : 55ns
	- 70 : 70ns
• t	: Temperature
	- I : Industrial (-40 ~ 85 °C)
• KOREA	: Origin Country
Note	
- Capital Letter	: Fixed Item
- Small Letter	: Non-fixed Item (Except hynix)