



## CTL130PS10-T52

### P-Channel Enhancement MOSFET

#### Features

- Drain-Source Breakdown Voltage  $V_{DSS}$ -100V
- Drain-Source On-Resistance  
 $R_{DS(ON)}$  160m $\Omega$ , at  $V_{GS} = -10V$ ,  $I_D = -3.6A$   
 $R_{DS(ON)}$  170m $\Omega$ , at  $V_{GS} = -4.5V$ ,  $I_D = -3.4A$
- *Continuous Drain Current* at  $T_C=25^\circ C$   $I_D = -11A$
- Advanced high cell density Trench Technology
- RoHS Compliance & Halogen Free

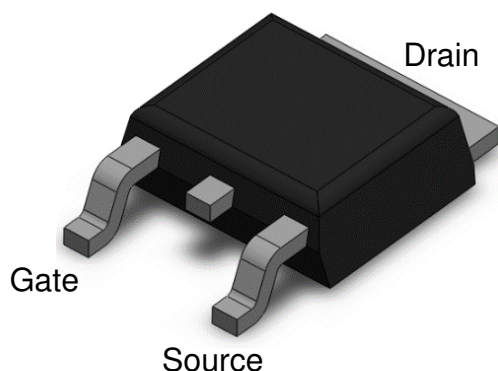
#### Applications

- Power Management in Note book
- DC/DC Converter
- Load Switch

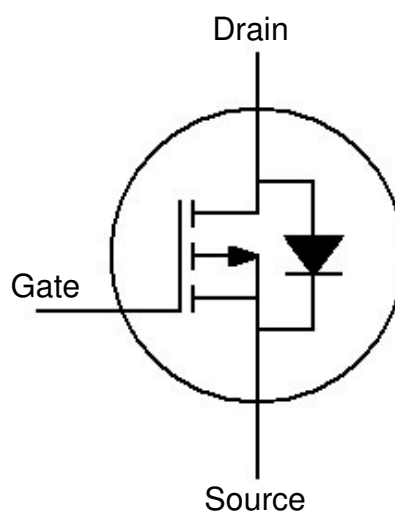
#### Description

The CTL130PS10-T52 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits , and low in-line power loss are needed in a very small outline surface mount package.

#### Package Outline



#### Schematic





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### Absolute Maximum Rating at 25°C

Symbol	Parameters	Test Conditions	Min	Note
V <sub>DS</sub>	Drain-Source Voltage	-100	V	
V <sub>GS</sub>	Gate-Source Voltage	±20	V	
I <sub>D</sub>	Continuous Drain Current @T <sub>C</sub> =25°C	-11	A	1
I <sub>DM</sub>	Pulsed Drain Current	-44	A	1
P <sub>D</sub>	Total Power Dissipation @T <sub>C</sub> =25°C	39	W	2
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C	
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C	

### Thermal Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
R <sub>θJC</sub>	Thermal Resistance Junction-Case		--	--	3.2	°C /W	1,4



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### Electrical Characteristics $T_A = 25^\circ\text{C}$ (unless otherwise specified)

#### Static Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$B_{VDSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-100	-	-	V	
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS} = -100V, V_{GS} = 0V$	-	-	-1	$\mu A$	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	$\pm 100$	nA	

#### On Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS} = -10V, I_D = -3.6A$	-	160	195	m $\Omega$	3
		$V_{GS} = -4.5V, I_D = -3.4A$	-	170	210	m $\Omega$	3
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu A$	1.0		3.0	V	3

#### Dynamic Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$C_{ISS}$	Input Capacitance	$V_{GS} = 0V,$ $V_{DS} = -15V$ $f = 1MHz$	-	1240	-	pF	
$C_{OSS}$	Output Capacitance		-	947	-		
$C_{RSS}$	Reverse Transfer Capacitance		-	30	-		

#### Switching Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$T_{D(ON)}$	Turn-On Delay Time	$V_{DS} = -50V,$ $V_{GS} = -10V,$ $R_G = 1\Omega,$ $R_L = -25\Omega$	-	35	-	ns	
$T_R$	Rise Time		-	12	-		
$T_{D(OFF)}$	Turn-Off Delay Time		-	58	-		
$T_F$	Fall Time		-	5	-		
$Q_G$	Total Gate Charge	$V_{DS} = -50V,$ $V_{GS} = -4.5V,$ $I_D = -3.6A$	-	14	-	nC	
$Q_{GS}$	Gate-Source Charge		-	5.3	-		
$Q_{GD}$	Gate-Drain (Miller) Charge		-	5.9	-		



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### Drain-Source Diode Characteristics

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$V_{SD}$	Body Diode Forward Voltage	$V_{GS} = 0V, I_{SD} = -2.9A$	-	-0.8	-1.2	V	1
$I_{SD}$	Body Diode Continuous Current		-	-	-1	A	1

Note:

1. The power dissipation is limited by 150°C junction temperature.
2. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
3. Thermal Resistance follow JESD51-3.



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### Typical Characteristic Curves

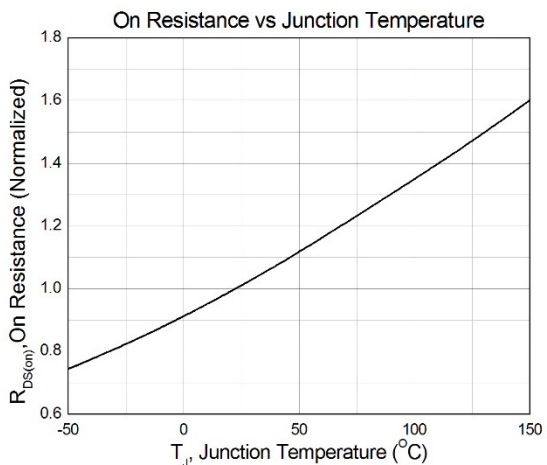


Figure 1

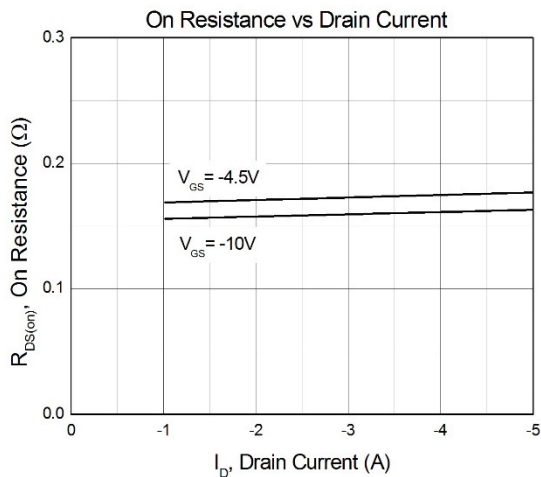


Figure 2

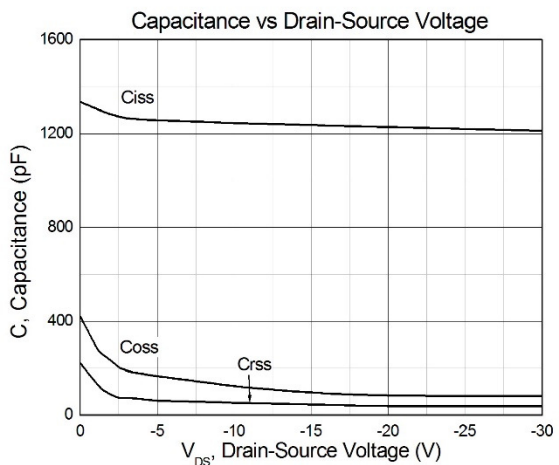


Figure 3

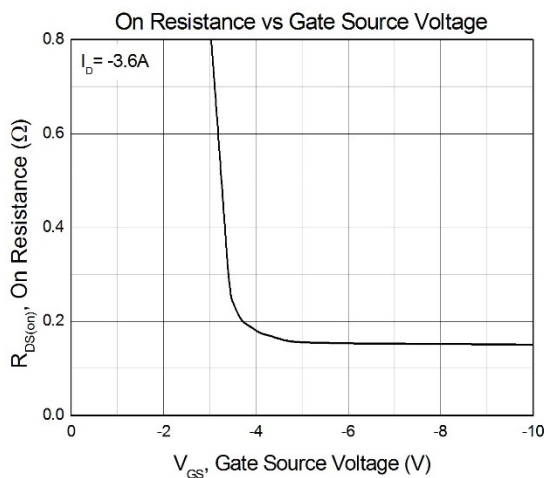


Figure 4

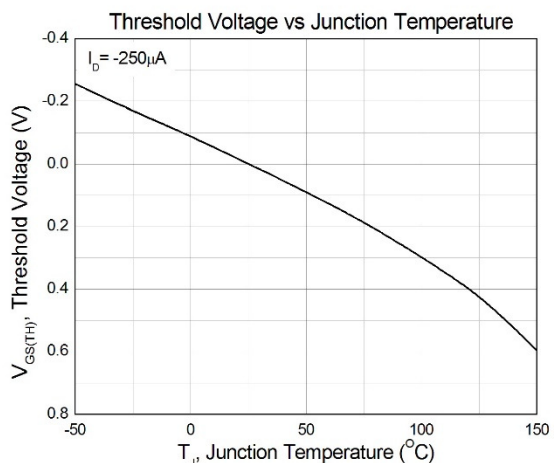


Figure 5

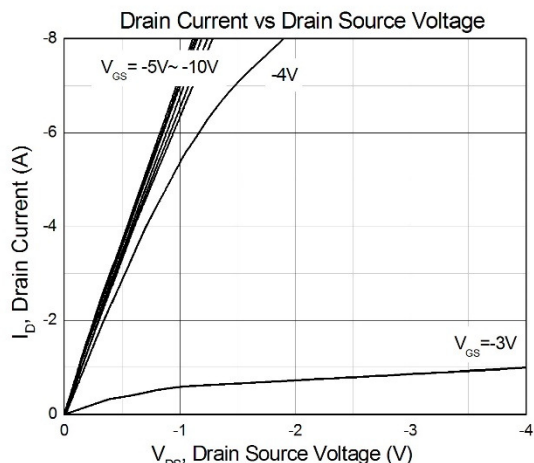
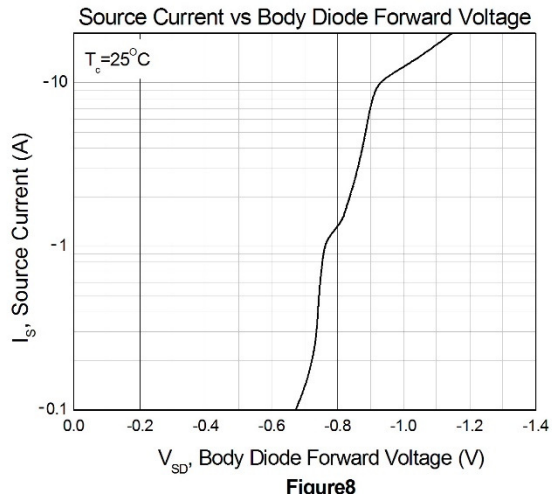
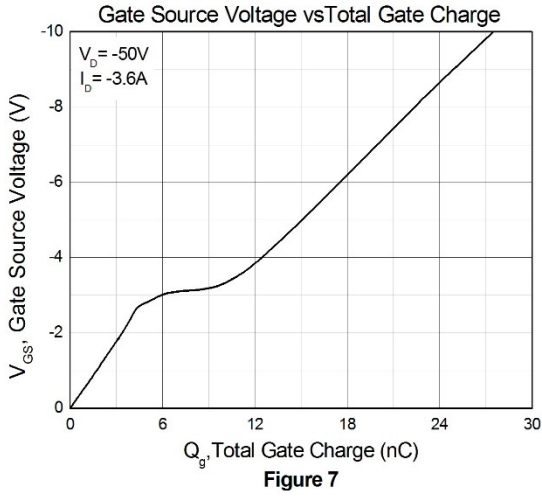


Figure 6



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### Test Circuits & Waveforms

Figure 9: Gate Charge Test Circuit

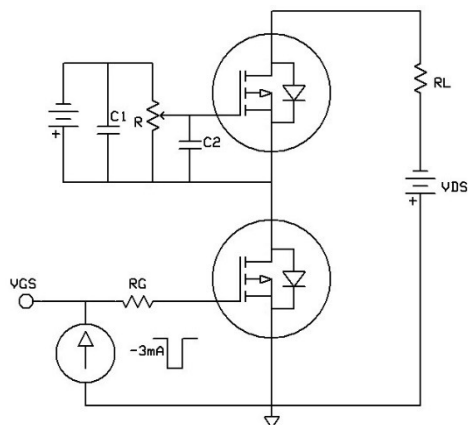


Figure 10: Gate Charge Waveform

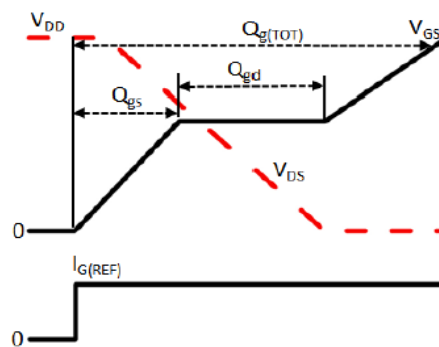


Figure 11: Switching Time Test Circuit

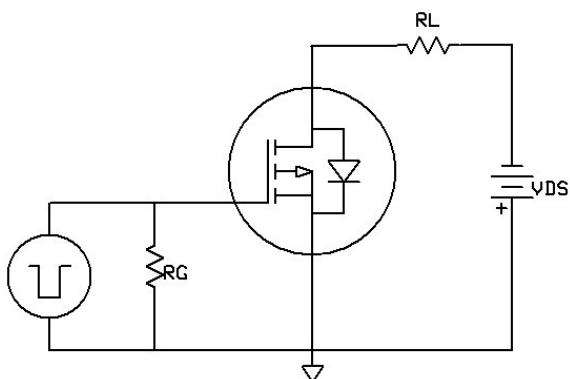
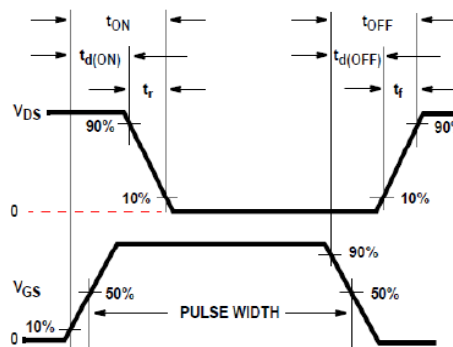


Figure 12: Switching Time Waveform

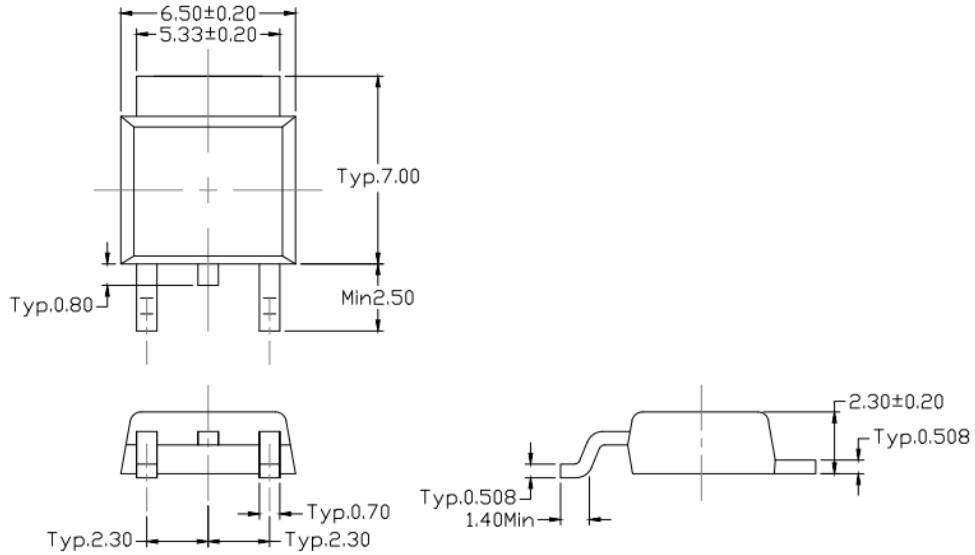




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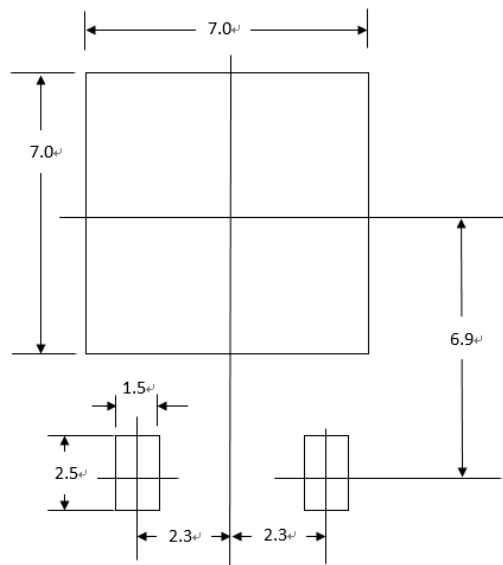
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### Package Dimension (TO-252)



Dimensions in mm unless otherwise stated

### Recommended pad layout for surface mount leadform



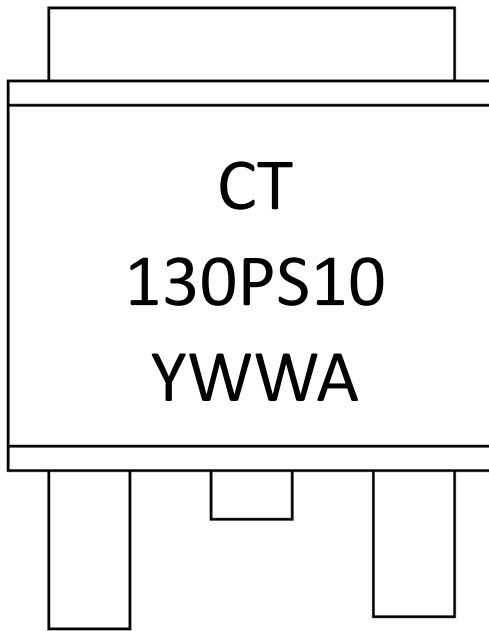
Dimensions in mm unless otherwise stated



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CT : Denotes "CT M  
130PS10 : Device Numbe  
Y : Fiscal Year  
WW : Work Week  
A : Production Coc

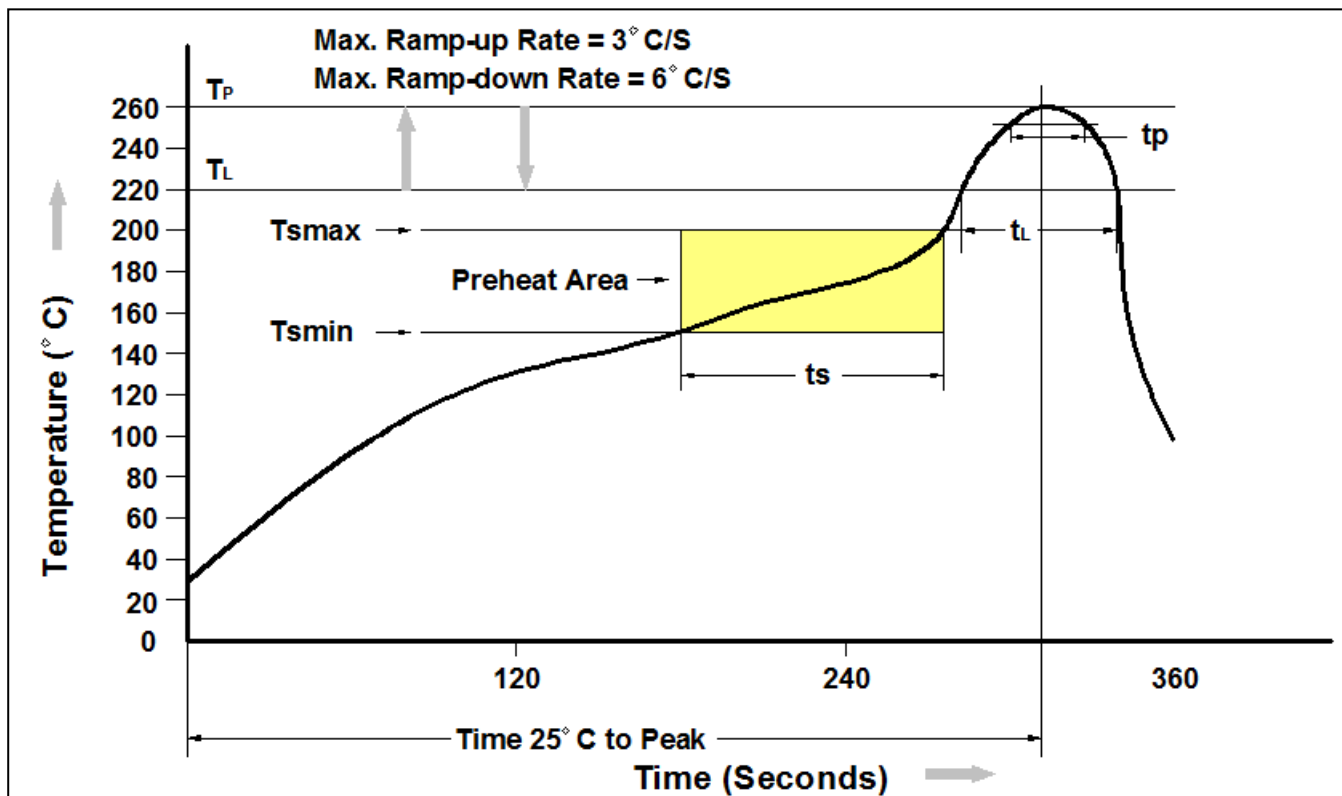


**Ordering Information**

<b>Part Number</b>	<b>Description</b>	<b>Quantity</b>
CTL130PS10-T52	TO-252 Reel	2500 pcs



Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (T Amin)	150 °C
Temperature Max. (Tsmax)	200 °C
Time (ts) from (T Amin to Tsmax)	60-120 seconds
Ramp-up Rate (tL to tP)	3 °C/second max.
Liquidous Temperature (TL)	217 °C
Time (tL) Maintained Above (TL)	60 – 150 seconds
Peak Body Package Temperature	260 °C +0 °C / -5 °C
Time (tP) within 5 °C of 260 °C	30 seconds
Ramp-down Rate (TP to TL)	6 °C/second max
Time 25 °C to Peak Temperature	8 minutes max.



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