Datasheet

Middle Power Class-D Speaker Amplifier series

20W+20W Full Digital Speaker Amplifier with built-in DSP

BM28720MUV

General Description

BM28720MUV is a Full Digital Speaker Amplifier with built-in DSP (Digital Sound Processor) designed for Flat-panel TVs in particular for space-saving and low-power consumption, delivers an output power of 20W+20W. This IC employs Bipolar, CMOS, and DMOS (BCD) process technology that eliminates turn-on resistance in the output power stage and internal loss due to line resistances up to an ultimate level. With this technology, the IC can achieve high efficiency. In addition, the IC is packaged in a compact reverse heat radiation type power package to achieve low power consumption and low heat generation and eliminates necessity of external heat-sink up to a total output power of 40W. This product satisfies both needs for drastic downsizing, low-profile structures and many function, high quality playback of sound system.

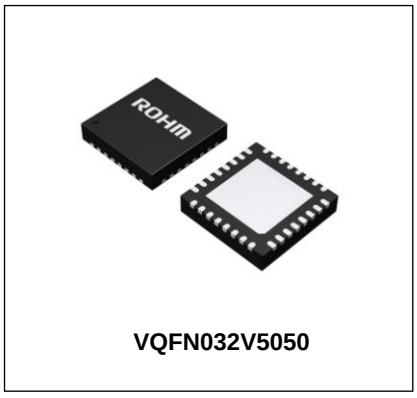
Key Specifications

- Supply voltage (VCC) 10V to 24V
- Speaker output power (VCC=18.5V, R_L=8Ω) 20W+20W (Typ.)
- THD+N 0.07 [%] (Typ.)

Applications

- Flat Panel TVs (LCD, OEL)
- Home Audio
- Desktop PC
- Amusement equipments
- Electronic Music equipments, etc.

Package W(Typ) x D(Typ) x H(Max)
VQFN032V5050 5.00mm x 5.00mm x 1.00mm



VQFN032V5050

Features

- This IC includes the DSP (digital sound processor) for Audio signal processing for Flat TVs.
  12 Band/ch BQ, 3 Band DRC, Pre-Scaler, Channel Mixer, Fine Master Volume, Hard Clipper, Level Meter etc.
- This IC has one input systems of digital audio interface. (No needs of Master Clock)
  - I^2S / LJ / RJ format
  - LRCLK: 32k/44.1k/48KHz
  - BCLK: 32fs / 48fs / 64fs
  - SDATA: 16 / 20 / 24bit
- This IC has one output systems of digital audio interface.
  - I^2S format
  - SDATA: 16 / 20 / 24bit
- With wide range of power supply voltage.
- The monaural output that can reduce the number of external parts can be used.
- With high efficiency and low heat dissipation contributing to miniaturization, slim design, and also power saving of the system.
- Eliminates pop-noise generated during the power supply on/off. High quality muting performance is realized by using the soft-muting technology.
- This IC is built-in with various protection functions for highly reliability design.
  - High temperature protection
  - Under voltage protection
  - Output short protection
  - DC voltage protection
  - Clock stop protection
- Small package

Typical Application Circuit

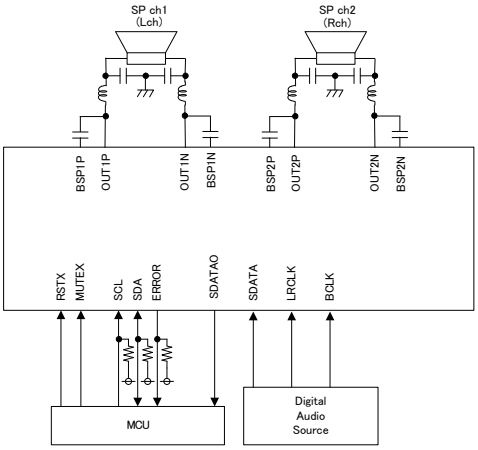


Figure 1. Typical application circuits

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Pin configuration and Block diagram

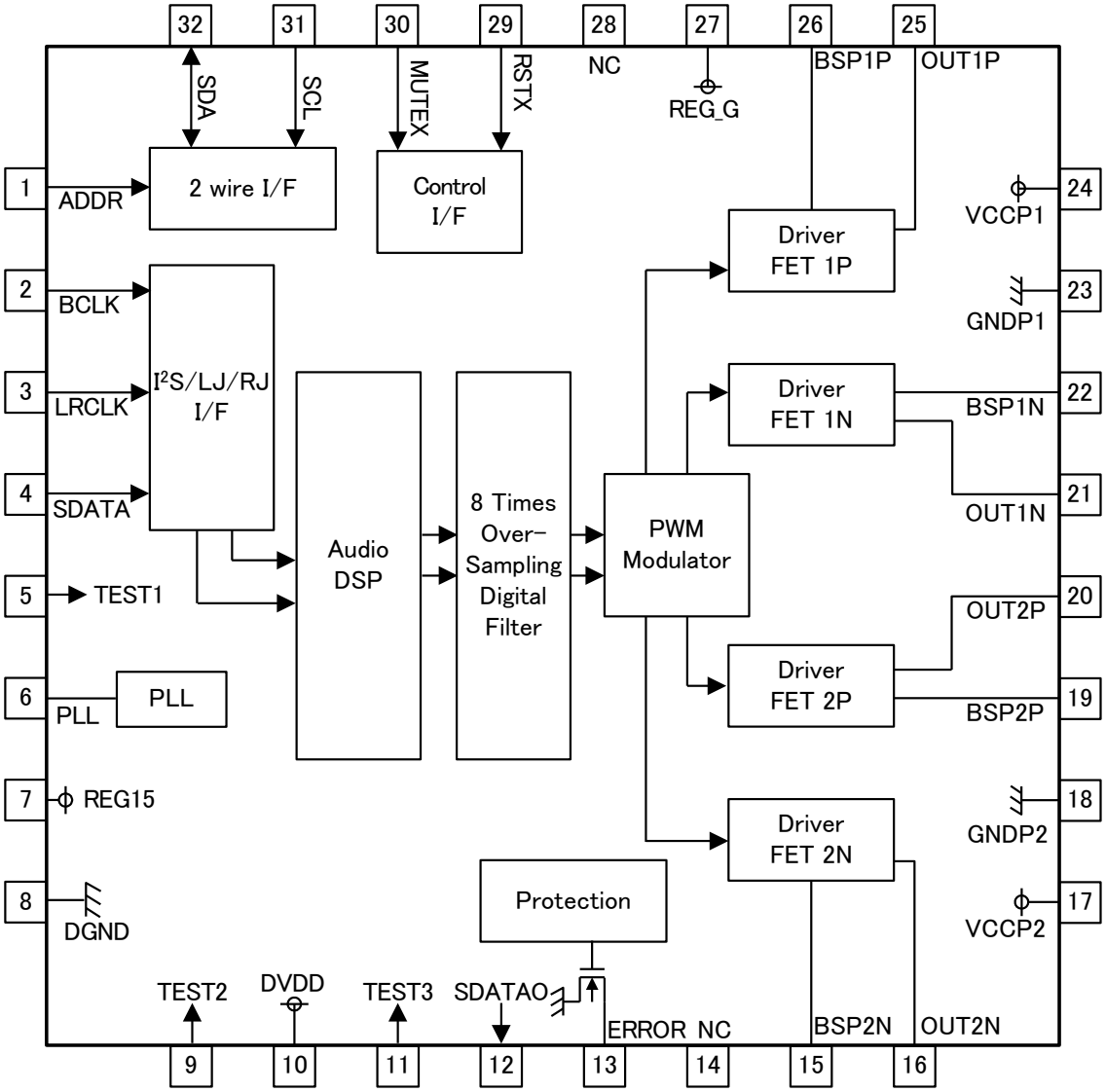


Figure 2. Pin configurations and Block diagram (Top View)

Pin Description

No.	Name	I/O	No.	Name	I/O	No.	Name	I/O	No.	Name	I/O
1	ADDR	I	9	TEST2	I	17	VCCP2	-	25	OUT1P	O
2	BCLK	I	10	DVDD	-	18	GNDP2	-	26	BSP1P	I
3	LRCK	I	11	TEST3	I	19	BSP2P	I	27	REG_G	O
4	SDATA	I	12	SDATAO	O	20	OUT2P	O	28	NC	-
5	TEST1	I	13	ERROR	O	21	OUT1N	O	29	RSTX	I
6	PLL	-	14	NC	-	22	BSP1N	I	30	MUTEX	I
7	REG15	O	15	BSP2N	I	23	GNDP1	-	31	SCL	I
8	DGND	-	16	OUT2N	O	24	VCCP1	-	32	SDA	I/O

I = input; O = output; - = others

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Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Limit	Unit	Conditions
Supply voltage	VCC	-0.3 to 34	V	Pin 17, 24 (Note 1) (Note 2)
	DVDD	-0.3 to 4.5	V	Pin 10 (Note 1)
Power dissipation	Pd	3.26	W	(Note 3)
		4.56	W	(Note 4)
Input voltage 1	VIN1	-0.3 to DVDD+0.3	V	Pin 1 - 5, 9, 11, 12, 13, 29 -32 (Note 1)
Terminal voltage 1	VPIN1	-0.3 to 7.0	V	Pin 27 (Note 1)
Terminal voltage 2	VPIN2	-0.3 to 29	V	Pin 16, 20, 21, 25 (Note 1)(Note 5)
Terminal voltage 3	VPIN3	OUTxx+6.0	V	Pin 15, 19, 22, 26 (Note 1)
Operating temperature range	Topr	-25 to +85	℃	
Storage temperature range	Tstg	-55 to +150	℃	
Maximum junction temperature	Tjmax	+150	℃	

(Note 1) The voltage that can be applied reference to GND (Pin 8, 18, 23).
(Note 2) Do not exceed Pd and Tjmax=150℃.
(Note 3) 74.2mm × 74.2mm × 1.6mm, FR4, 4-layer glass epoxy board
(Top and bottom layer back copper foil size: 20.2mm^2, 2nd and 3rd layer back copper foil size: 5505mm^2)
Derating in done at 26.1 mW/℃ for operating above Ta＝25℃. There are thermal via on the board.
(Note 4) 74.2mm × 74.2mm × 1.6mm, FR4, 4-layer glass epoxy board (Copper area 5505mm^2)
Derating in done at 36.5 mW/℃ for operating above Ta＝25℃. There are thermal via on the board.

(Note 5) It should use it below this ratings limit including the AC peak waveform (overshoot) for all conditions.
At only undershoot, it is admitted using at ≦10ns and ≦29V by the VCC reference. (Please refer following figure.)

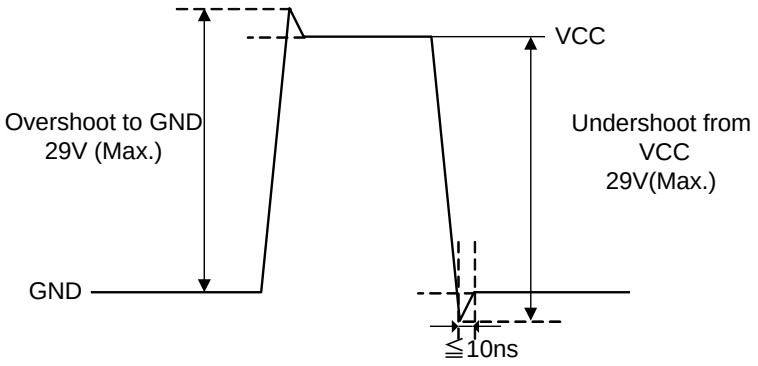


Figure 3.

Recommended Operating Ratings (Ta=25℃)

Item	Symbol	Limit	Unit	Conditions
Supply voltage	VCC	10 to 24	V	Pin 17, 24 (Note 1) (Note 2)
	DVDD	3 to 3.6	V	Pin 10 (Note 1)
Minimum load impedance	R_L	5.4	Ω	Pin 16, 20, 21, 25 VCC = 18V to 24V (Note 6)
		3.6	Ω	Pin 16, 20, 21, 25 VCC < 18V (Note 6)

(Note 6) Do not exceed Pd.

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Electrical Characteristics

(Unless otherwise specified Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz, R_L=8Ω, DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)

Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Total circuit						
Circuit current 1 (Normal mode)	I_{CC1}	-	45	90	mA	Pin 17, 24, No load
	I_{DD1}	-	9	19	mA	Pin 10, -infinity dBFS input, No load
Circuit current 2 (Reset mode)	I_{CC2}	-	10	40	μA	Pin 17, 24, No load RSTX=0V, MUTEX=0V
	I_{DD2}	-	2.5	7.0	mA	Pin 10, -infinity dBFS input, No load RSTX=0V, MUTEX=0V
Open-drain terminal Low level voltage	V_{ERR}	-	-	0.8	V	Pin 13, I_O=0.5mA
Regulator output voltage 1	V_{REG_G}	4.9	5.7	6.5	V	Pin 27
Regulator output voltage 2	V_{REG15}	1.3	1.5	1.7	V	Pin 7
High level input voltage	V_{IH}	2.5	-	3.3	V	Pin 1 - 5, 9, 11, 29 -32
Low level input voltage	V_{IL}	0	-	0.8	V	Pin 1 - 5, 9, 11, 29 -32
Input current (Input pull-up terminal)	I_{UP}	-150	-100	-50	μA	Pin 2 – 4 VIN = 0V
Input current (Input pull-down terminal)	I_{DN}	35	70	105	μA	Pin 1, 29, 30, VIN = 3.3V
Input current (SCL, SDA terminal)	I_{IL}	-1	0	-	μA	Pin 31, 32, VIN = 0V
Input current (SCL, SDA terminal)	I_{IH}	-	0	1	μA	Pin 31, 32, VIN = 3.3V
Speaker amplifier output						
Maximum output power 1	P_{O1}	-	10	-	W	VCC=13V,THD+N=10% (Note 7)
Maximum output power 2	P_{O2}	-	20	-	W	VCC=18.5V,THD+N=10% (Note 7)
Total harmonic distortion 1	THD1	-	0.07	-	%	P_O=1W, AES17 (Note 7)
Crosstalk 1	CT1	60	80	-	dB	VCC=13V, P_O=1W, A-weighted (Note 7)
Output noise voltage 1	V_{NO1}	-	80	-	μVrms	-infinity dBFS input, A-weighted (Note 7)
PWM sampling frequency	f_{PWM1}	-	256	-	kHz	fs=32 kHz
	f_{PWM2}	-	352.8	-	kHz	fs=44.1 kHz
	f_{PWM3}	-	384	-	kHz	fs=48 kHz

(Note 7) These items show the typical performance of device and depend on board layout, parts, and power supply.
The standard value is in mounting device and parts on surface of ROHM's board directly.

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Typical Performance Curves

Speaker output(Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=0V/3.3V, MUTEX=0V/3.3V, f=1kHz,
DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)
Measured by ROHM designed 4 layer board.

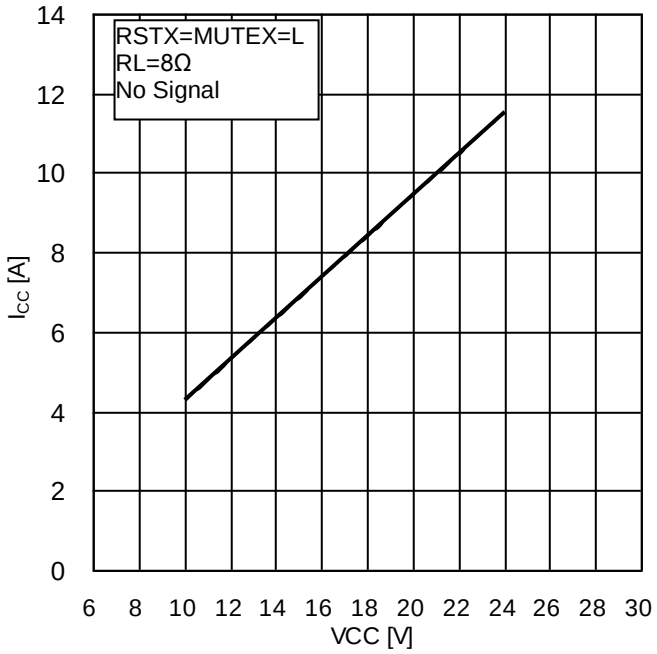


Figure 4.
Power supply voltage- Current consumption

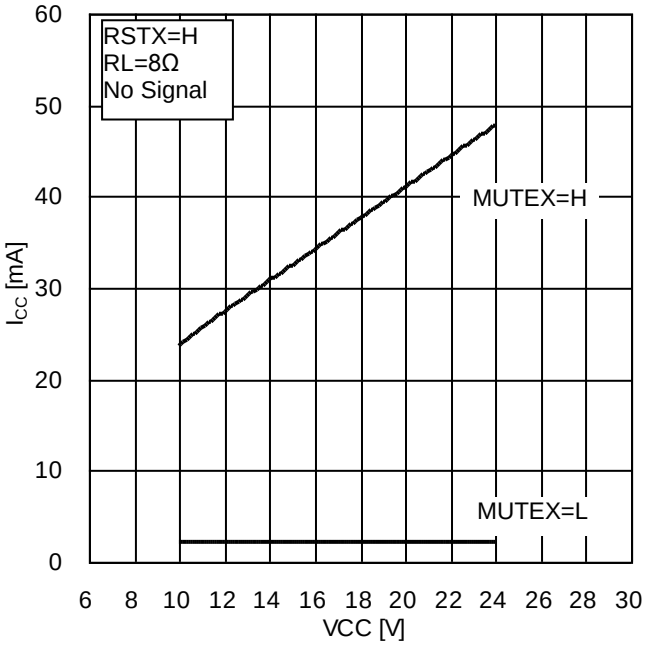


Figure 5.
Power supply voltage- Current consumption

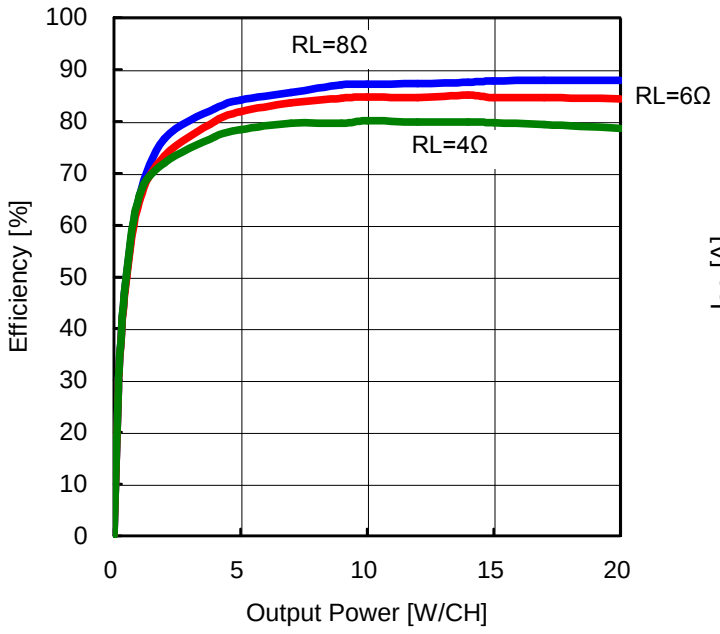


Figure 6.
Output power - Efficiency

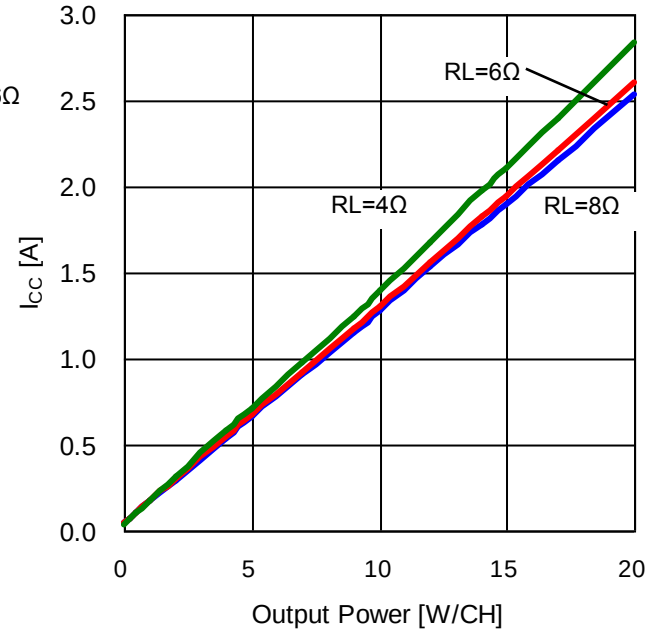


Figure 7.
Output power - Current consumption

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Typical Performance Curves

Speaker output(Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz,
DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)
Measured by ROHM designed 4 layer board.

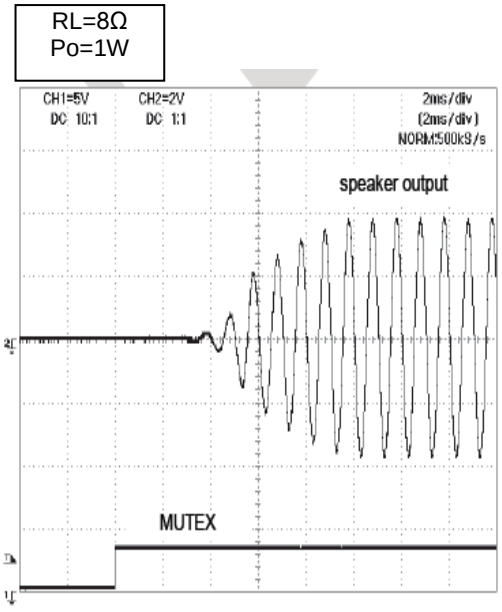


Figure 8.
Waveform at soft start

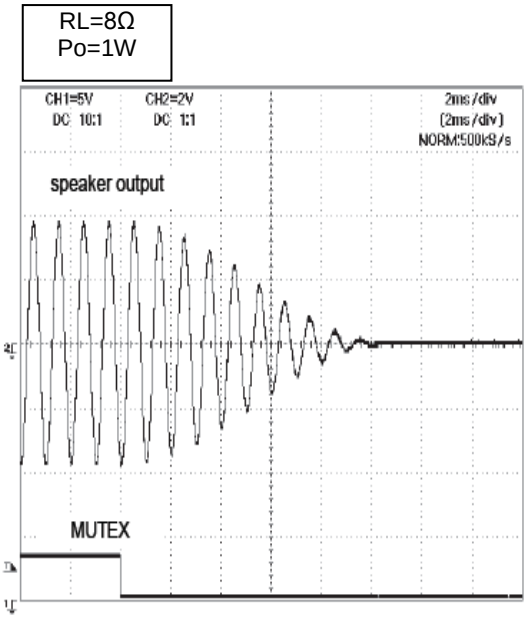


Figure 9.
Waveform at soft mute

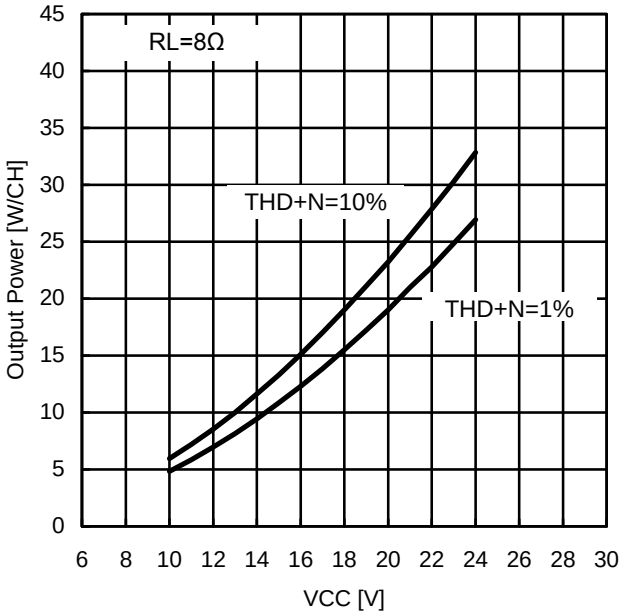


Figure 10.
Output voltage - Power voltage (R_L=8Ω)

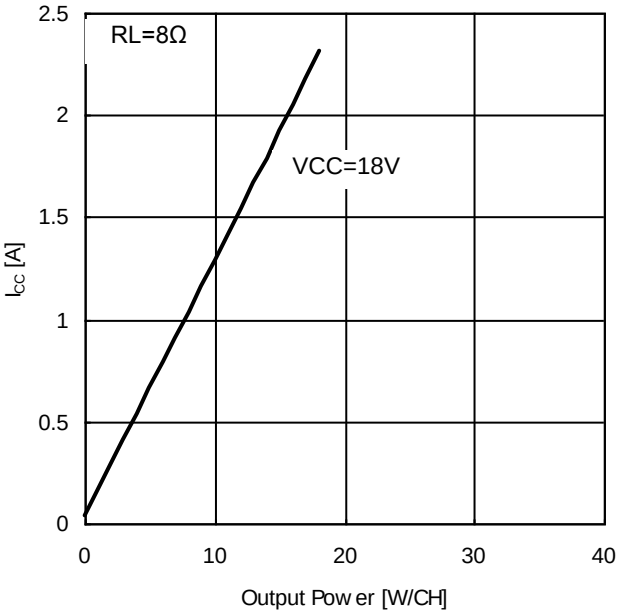


Figure 11.
Output power - Current consumption (R_L=8Ω)

※Dotted line means internal dissipation is over package power.

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Typical Performance Curves

Speaker output(Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz,
DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)
Measured by ROHM designed 4 layer board.

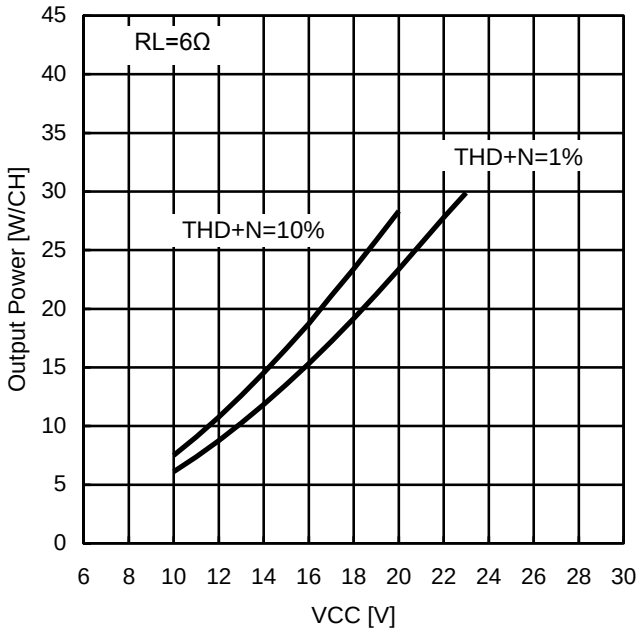


Figure 12.
Output voltage - Power voltage (R_L=6Ω)

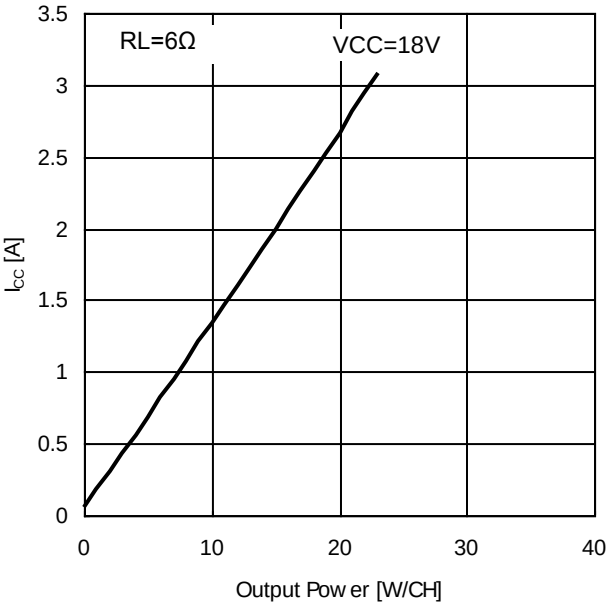


Figure 13.
Output power - Current consumption (R_L=6Ω)

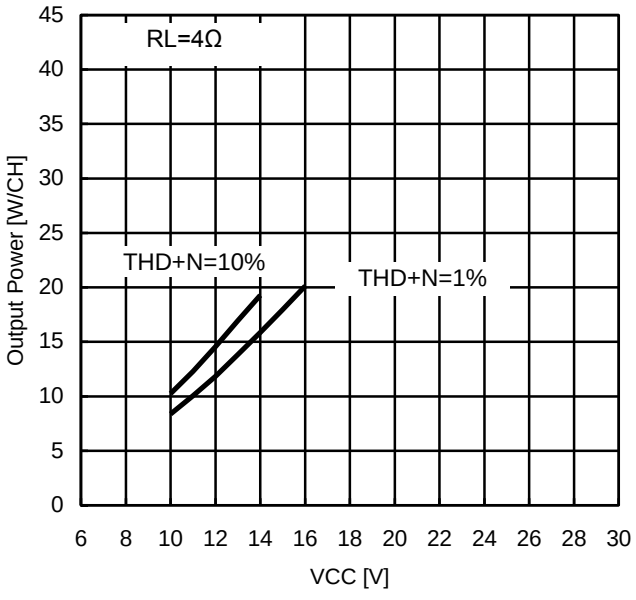


Figure 14.
Output Voltage – Power Voltage (R_L=4Ω)

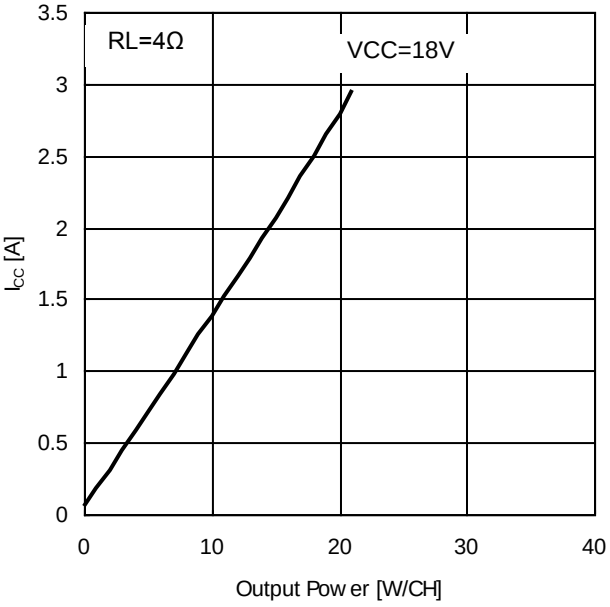


Figure 15.
Output power - Current consumption (R_L=4Ω)

※Dotted line means internal dissipation is over package power.

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Typical Performance Curves

Speaker output(R_L=8Ω, Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz,
DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)
Measured by ROHM designed 4 layer board.

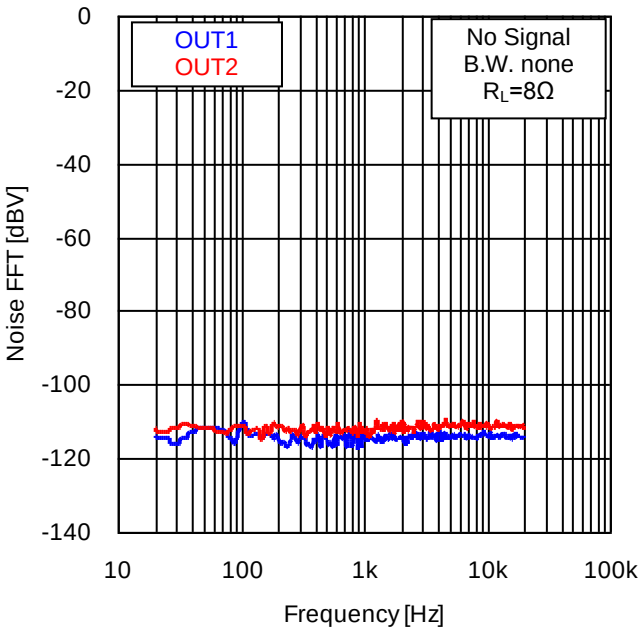


Figure 16.
FFT of output noise voltage

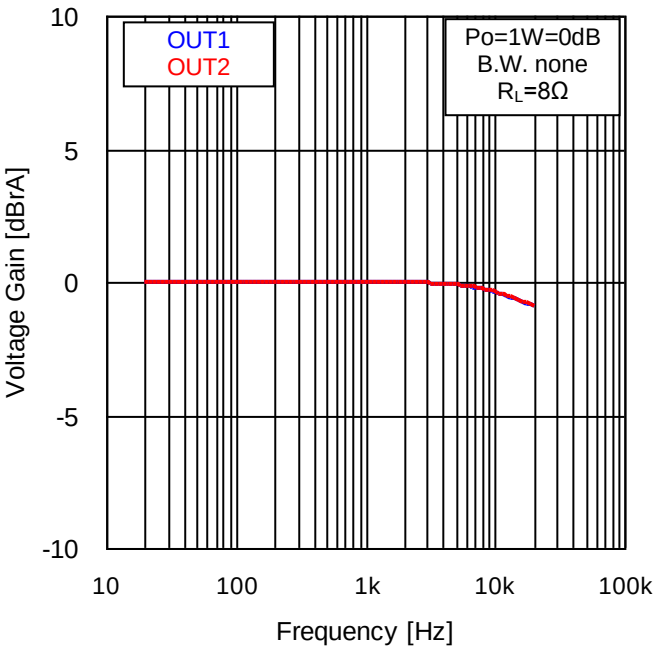


Figure 17.
Frequency – Output power

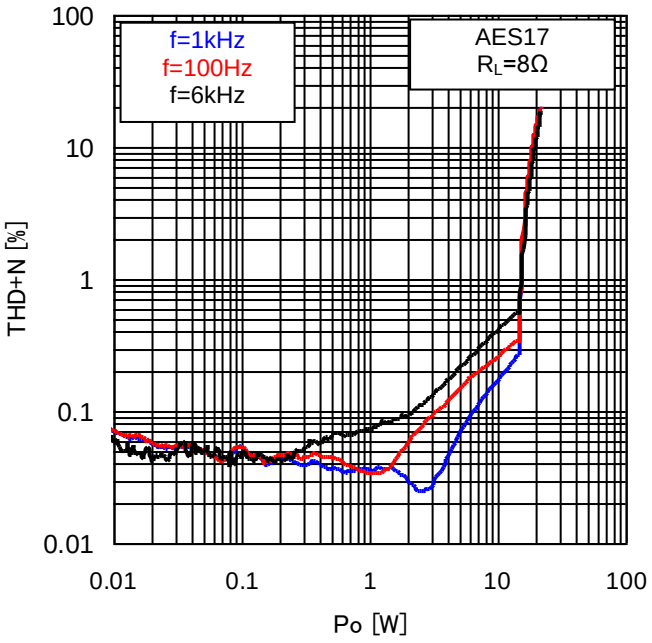


Figure 18.
Output Power - THD+N

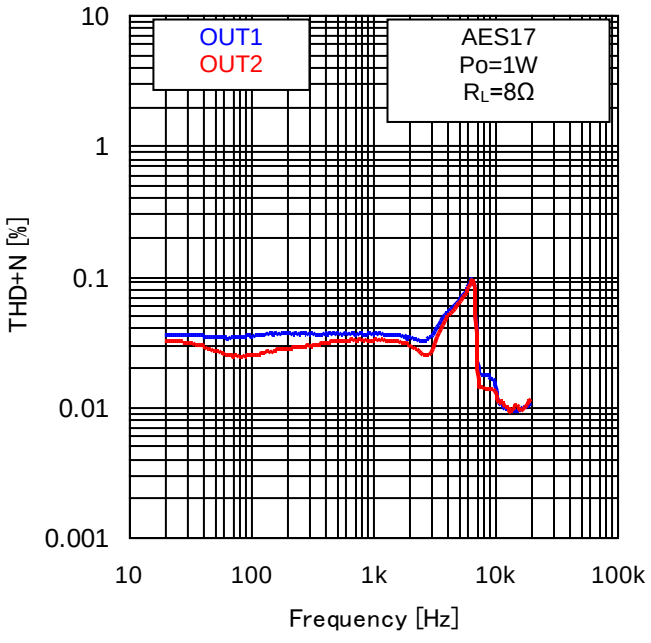


Figure 19.
Frequency - THD+N

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Typical Performance Curves

Speaker output(R_L=8Ω, Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz, DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)
Measured by ROHM designed 4 layer board.

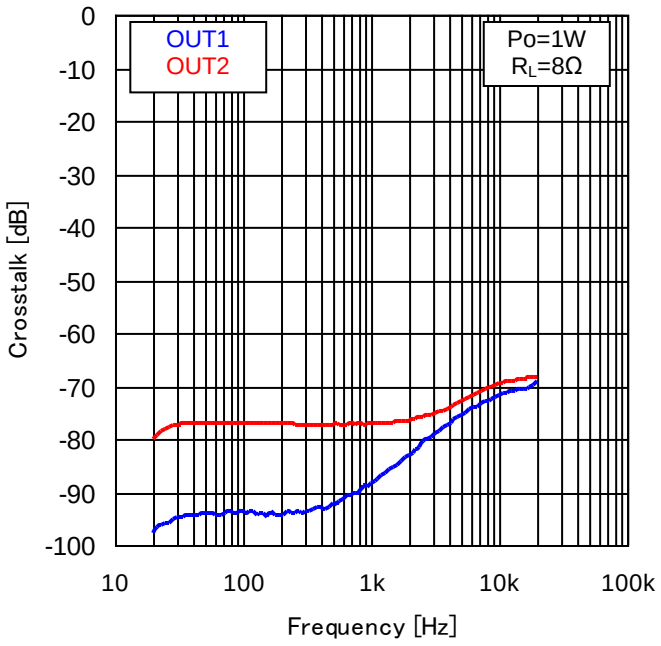


Figure 20.

Frequency - Crosstalk

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Typical Performance Curves

Speaker output(R_L=6Ω, Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz,
DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)
Measured by ROHM designed 4 layer board.

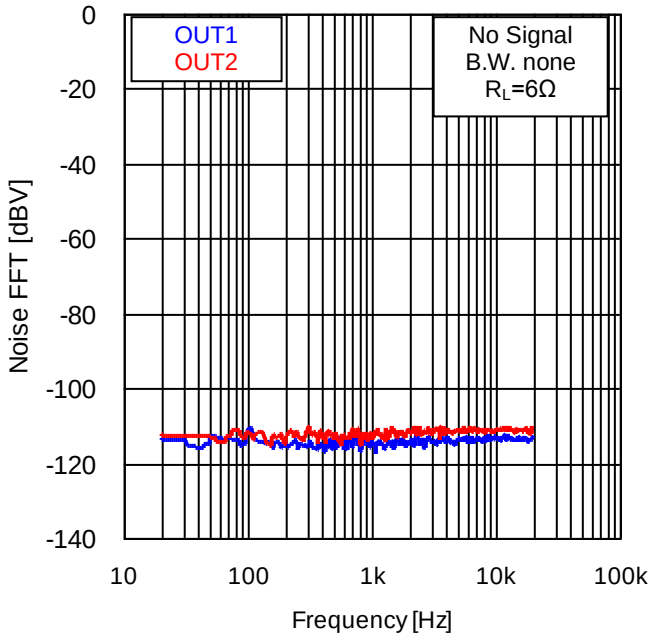


Figure 21.
FFT of output noise voltage

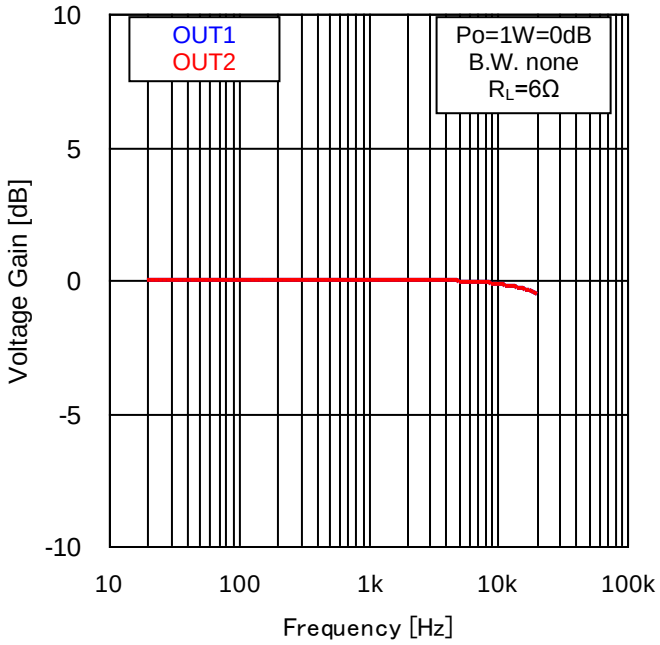


Figure 22.
Frequency – Output power

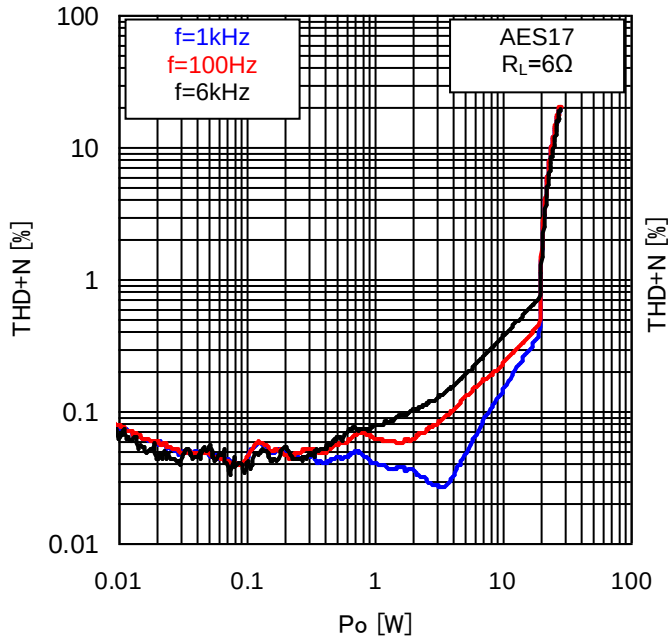


Figure 23.
Output Power - THD+N

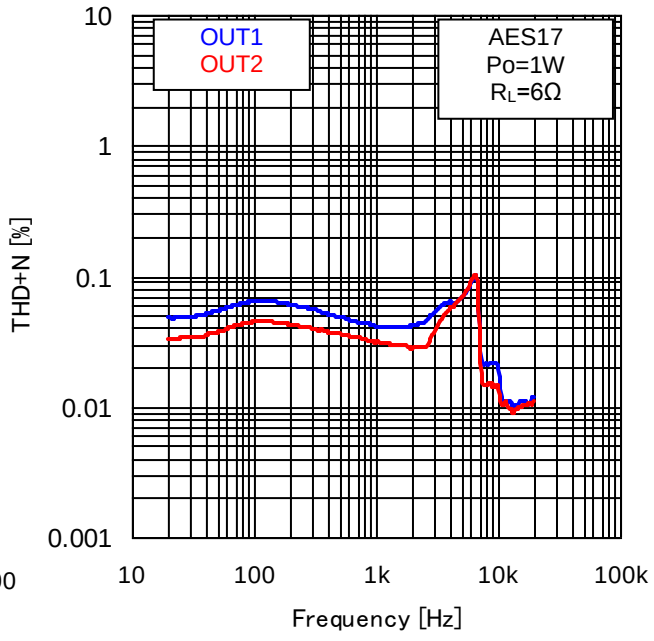


Figure 24.
Frequency - THD+N

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Typical Performance Curves

Speaker output R_L=6Ω, Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz,
DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)
Measured by ROHM designed 4 layer board.

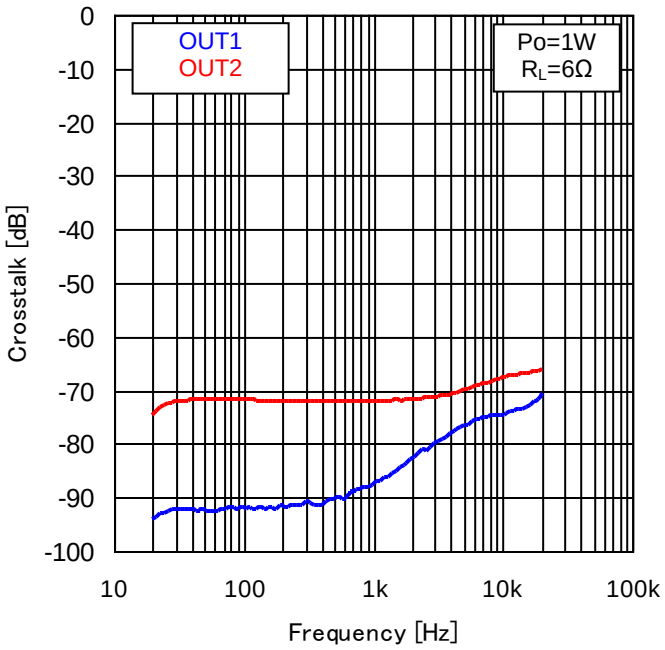


Figure 25.
Frequency - Crosstalk

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Typical Performance Curves

Speaker output(R_L=4Ω, Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz,
DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)
Measured by ROHM designed 4 layer board.

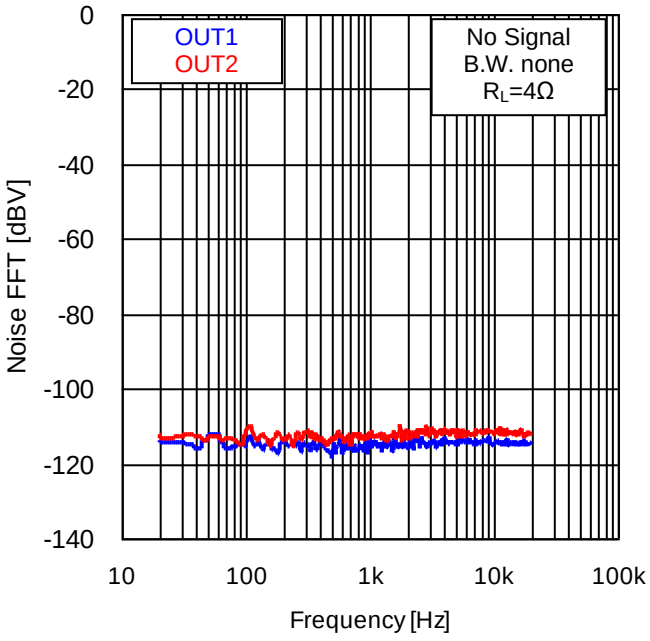


Figure 26.
FFT of output noise voltage

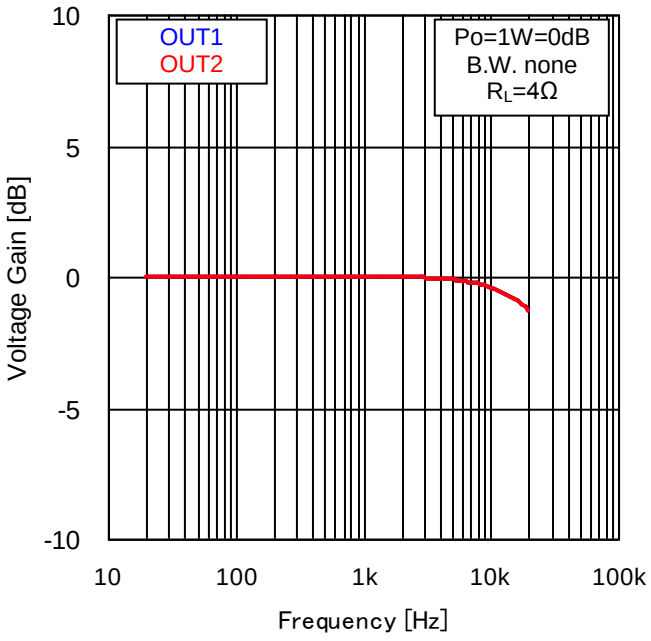


Figure 27.
Frequency – Output power

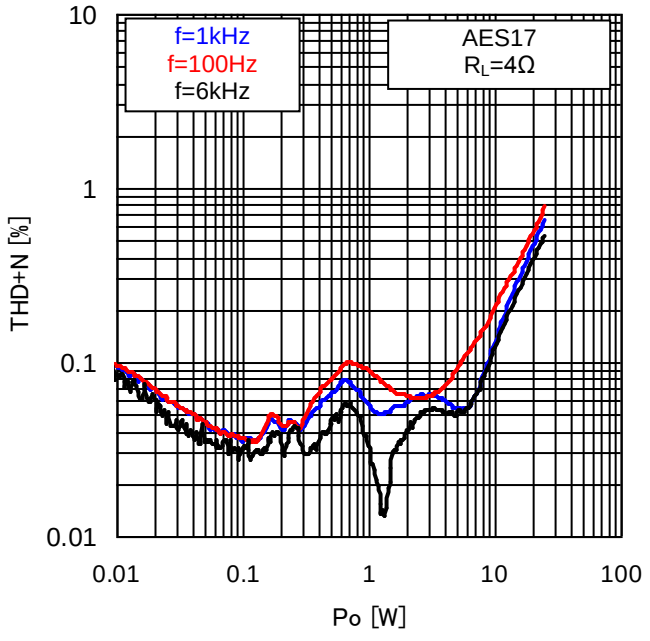


Figure 28.
Output Power - THD+N

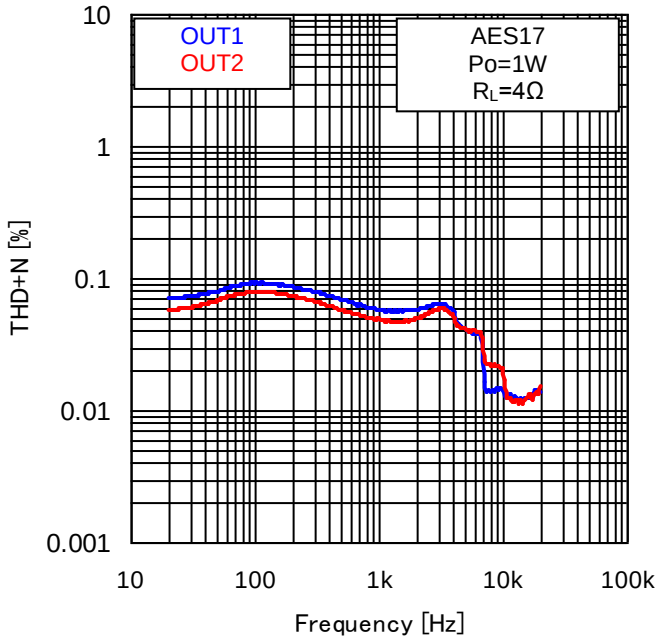


Figure 29.
Frequency - THD+N

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Typical Performance Curves

Speaker output(R_L=4Ω, Ta=25℃, VCC=18V, DVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, f=1kHz, DSP : Through, fs=48kHz, Snubber circuit for output terminal : R_{snb}=5.6Ω, C_{snb}=680pF)
Measured by ROHM designed 4 layer board.

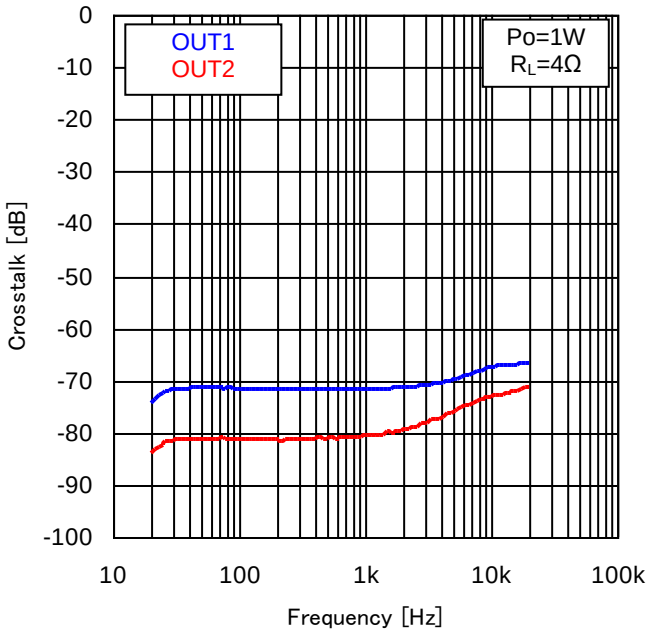


Figure 30.
Frequency - Crosstalk

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Digital Block Functional Overview

No.	Function	Specification
1	Pre-Scaler	・Lch / Rch become same set point. ・+48dB to -79dB (0.5dB step),-∞dB
2	Channel Mixer	・Lch <= Mute, Lch(default), Rch, (L+R)/2, L-R ・Rch <= Mute, Lch, Rch(default), (L+R)/2, L-R ・Lch/Rch are independent phase reversal control available
3	12 Band BQ	・12 Band biquad type filter ・Only 5 coefficient is required.(b0,b1,b2,a1,a2) ・The Filter types which can be realized is Peaking/Low-shelf/High-shelf/Low-pass/High-pass/All-pass/Notch. ・Lch/Rch become same set point or independent set. There is soft transition function.
4	Fine Master Volume	・Lch / Rch become same set point or independent set. ・+24dB to -103dB (0.125dB step),-∞dB ・There is soft transition function
5	3 Band DRC	・Non clip output is achieved ・Available three band operation ・Threshold level : +12dB to -32dB (0.5dB step)
6	Post-Scaler	・Lch / Rch become same set point ・+48dB to -79dB (0.5dB step),-∞dB
7	Fine Post-Scaler	・Lch / Rch become independent set point ・+0.7dB to -0.8dB (0.1dB step)
8	DC Cut HPF	・Fc : 1Hz
9	Clipper	・Lch / Rch become same set point ・Clip level : +3dB to -22.5dB (-0.1dB step)

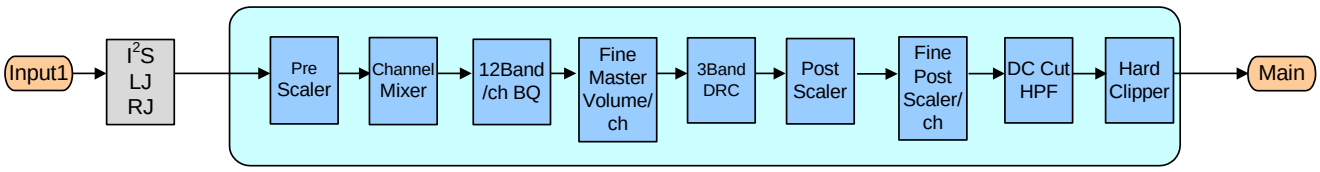


Figure 31. DSP Block diagram

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RSTX pin, MUTEX pin function

RSTX (29pin)	MUTEX (30pin)	DSP block condition	Speaker output condition
Low	Low	Reset ON	HiZ_low (Low consumption)
High	Low	Normal operation (Mute ON)	HiZ_low(Note 4) (Mute ON)
High	High	Normal operation (Mute OFF)	Normal operation (Mute OFF)
Low	High	Don't use.	

(Note 1) RSTX is set to low, internal registers are initialized.
(Note 2) VCCP1, VCCP2< 2.5V, IC latched by protection circuit and ERROR terminal condition are initialized.
(Note 3) If DVDD is under 3V, RSTX is set to low once for 10ms(min), and set high again. Then DSP is needed to set parameter again.
(Note 4) Speaker output becomes HiZ-low after elapse of PWM stop time after setting MUTEX low. Please refer to PWM sampling frequency.

PWM sampling frequency

PWM sampling frequency of Speaker output and Soft-mute transition time depends on sampling frequency (fs) of the digital sound input. These transition times are changed by sending select address 0x15[1:0].

Sampling frequency (fs)	PWM frequency	0x15[1:0] value	Soft mute transition time		PWM stop time
			Mute ON	Mute OFF	
48kHz	384kHz	0x0	10.7ms	10.7ms	86ms
		0x1	21.4ms	10.7ms	106ms
		0x2	42.7ms	10.7ms	125ms
		0x3	85.4ms	10.7ms	162ms
44.1kHz	352.8kHz	0x0	11.7ms	11.7ms	93ms
		0x1	23.3ms	11.7ms	113ms
		0x2	46.5ms	11.7ms	135ms
		0x3	92.9ms	11.7ms	177ms
32 kHz	256kHz	0x0	16.1ms	16.1ms	116ms
		0x1	32.1ms	16.1ms	148ms
		0x2	64.1ms	16.1ms	178ms
		0x3	128.1ms	16.1ms	241ms

Wait time(Twait) rules from releasing RSTX to releasing MUTEX.

When the time from releasing RSTX to releasing MUTEX prescribes **Twait**, please secure **Twait** by all means more than 450ms.

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2 wire Bus control signal specification

1) Electrical characteristics and Timing of Bus line and I/O stage

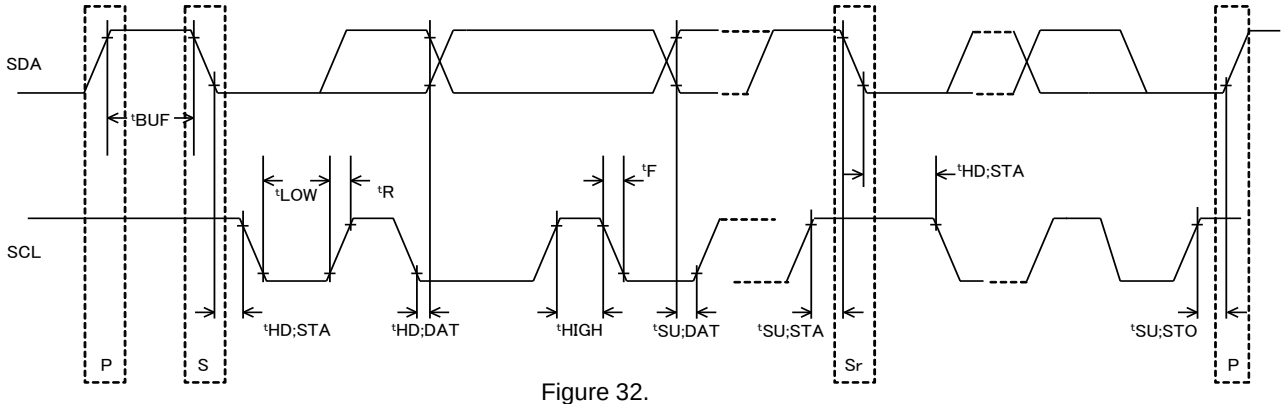


Figure 32.

SDA and SCL bus line characteristics(Unless otherwise specified Ta=25℃, VDD=3.3V)

	Parameter	Symbol	High speed mode		Unit
			Min.	Max.	
1	SCL clock frequency	fSCL	0	400	kHz
2	Bus free time between「Stop」condition and「Start」condition	tBUF	1.3	—	μs
3	Hold-time of (sending again)「Start」condition. After this period the first clock pulse is generated.	tHD;STA	0.6	—	μs
4	SCL clock's LOW state Hold-time	tLOW	1.3	—	μs
5	SCL clock's HIGH state Hold-time	tHIGH	0.6	—	μs
6	Set-up time of sending again「Start」condition	tSU;STA	0.6	—	μs
7	Data hold time	tHD;DAT	0 (Note 1)	—	μs
8	Data set-up time	tSU;DAT	250	—	ns
9	Rise-time of SDA and SCL signal	tR	20+0.1Cb	300	ns
10	Fall-time of SDA and SCL signal	tF	20+0.1Cb	300	ns
11	Set-up time of 「Stop」condition	tSU;STO	0.6	—	μs
12	Capacitive load of each bus line	Cb	—	400	pF

The above-mentioned numerical values are all the values corresponding to VIH min and the VIL max level.

(Note 1) To exceed an undefined area on the fall-edge of SCL (VIH min of the SCL signal), the transmitting set should internally offer the holding time of 300ns or more for the SDA signal.

(Note 2) SCL and SDA pin is not corresponding to threshold tolerance of 5V.
Please use it within 4.5V of the absolute maximum rating.

2)Command interface

2 wire Bus control is used for command interface. It not only writes but also it is possible to read it excluding a part of register. In addition to "Slave Address " , set and write 1 byte of "Select Address " to read out the data. 2 wire Bus Slave mode format is illustrated below.

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P

Figure 33.

S : Start Condition

Slave Address : The data of eight bits in total is sent putting up bit of Read mode (high) or Write mode (low) after slave address (7bit) set with the terminal ADDR. (MSB first)

A : The acknowledge bit adds to data that the acknowledge is sent and received in each byte.
When data is correctly sent and received, "low" is sent and received.
There was no acknowledgement for "high".

Select Address : The select address in one byte is used.(MSB first)

Data : Data byte is sent and received data(MSB first)

P : Stop Condition

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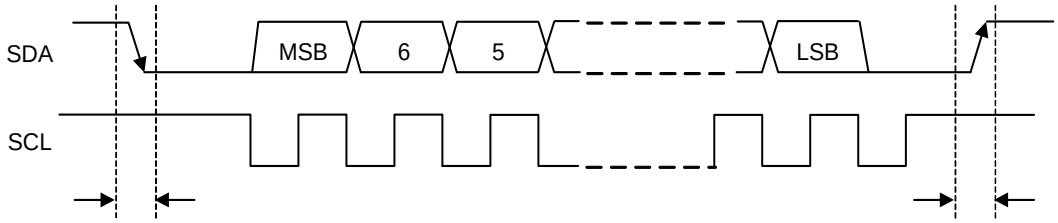


Figure 34.

3)Slave Address

・While ADDR pin is "low"

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	0	1/0

・While ADDR pin is "high"

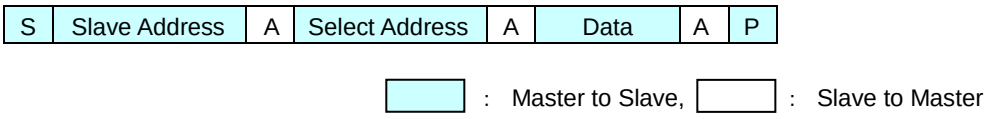
MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	1	1/0

Figure 35.

4) Writing of data

・Basic format



・Auto-increment format

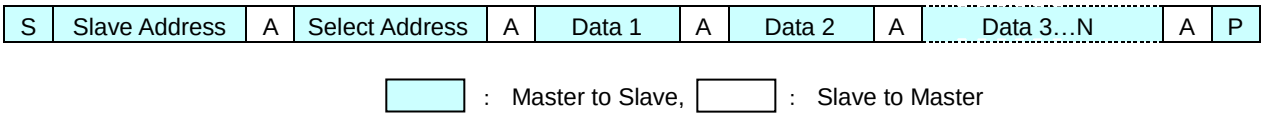


Figure 36.

5)Reading of data

First of all, the destination address (0x20 in the example) for reading is written in the register of the 0xD0 address at the time of reading. In the following stream, data is read after the slave address. Please do not return acknowledge when you end the reception.

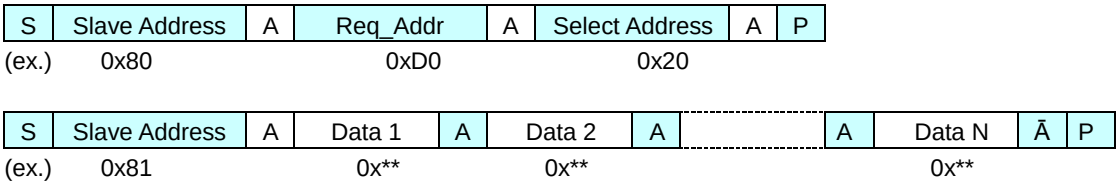


Figure 37.

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Format of digital audio input

- LRCLK: It is L/R clock input signal.
  It corresponds to 32kHz/44.1kHz/48kHz and that is same as the sampling frequency (fs).
  This signal shows left or right of audio data.

- BCLK: It is Bit Clock input signal.
  It is used for the latch of data in rising edge. Frequency of BCLK is 64 times of sampling frequency (64fs) or 48 times (48fs) or 32 times (32fs). If BCLK frequency is 32fs, only 16 bit data width is available.

- SDATA: It is data input signal.
  It is amplitude data. The data length is different according to the resolution of the input digital data.
  Data width is selectable as 16 bit, 20 bit or 24 bit.

  The digital input has I2S, Left-justified and Right-justified formats.
  The figure below shows the timing chart of each transmission mode.

- SDATAO: Audio data after DSP processing.
  Data is audio data after DSP processing.
  This output is synchronous to LRCK and BCLK.
  Output supports only I2S format.

BCLK clock 64fs

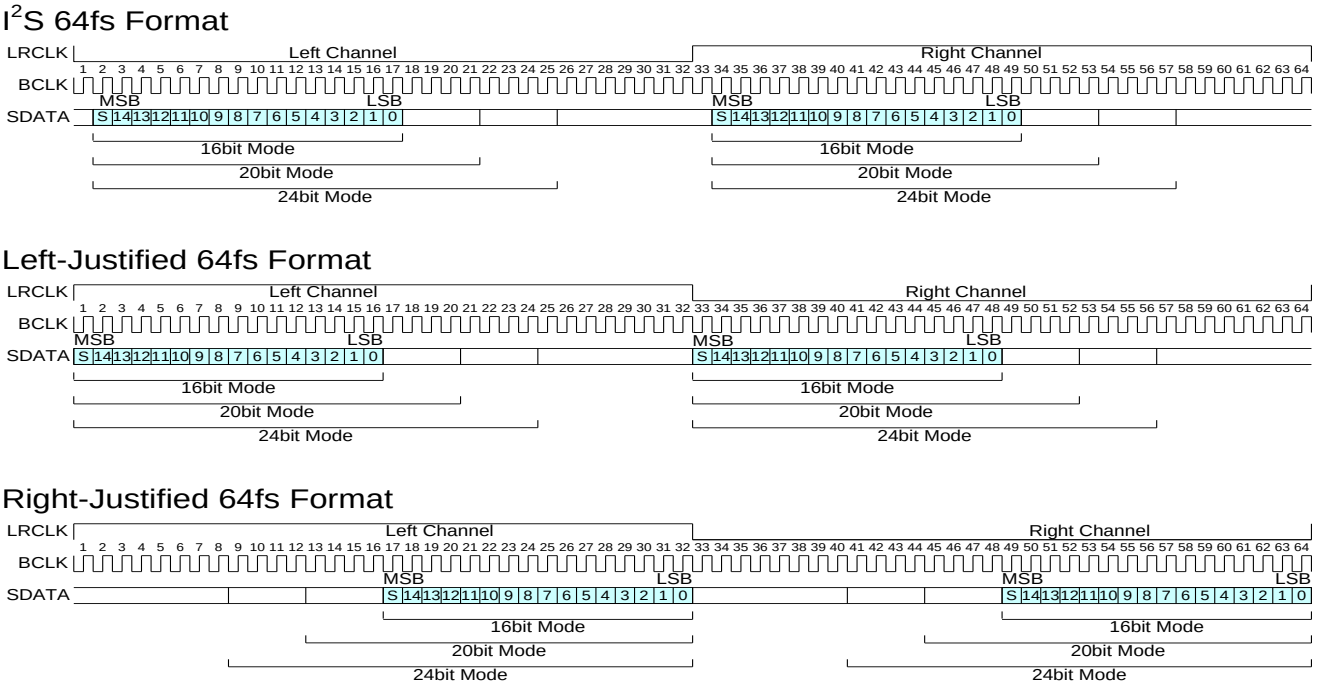
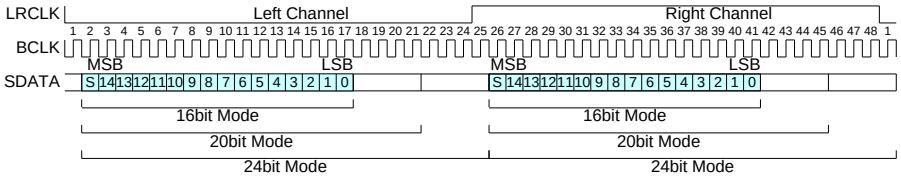


Figure 38.

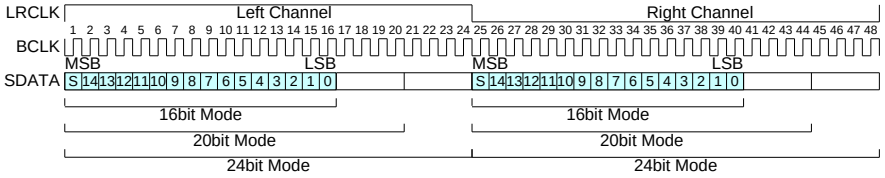
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BCLK clock 48fs

I²S 48fs Format



Left-Justified 48fs Format



Right-Justified 48fs Format

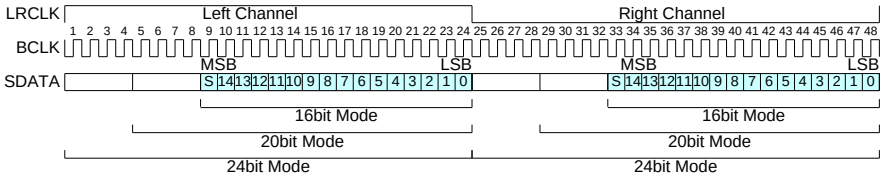
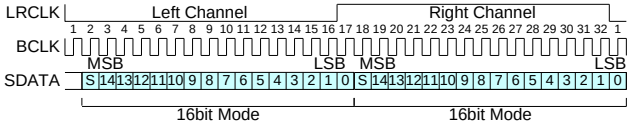


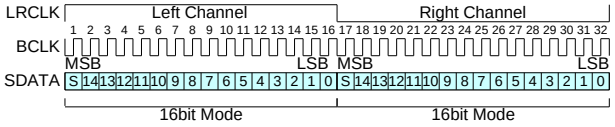
Figure 39.

BCLK clock 32fs

I²S 32fs Format



Left-Justified 32fs Format



Right-Justified 32fs Format

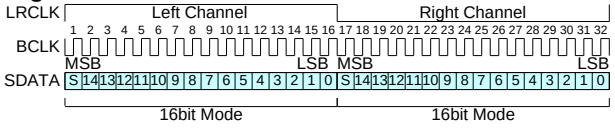


Figure 40.

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Format setting for Digital Audio Interface

Please set BCLK clock fs, Data length and Format by transmitting command according to inputted Digital Serial Audio signal.

SDATAO output data bit width is able to be set independently.

Output supports only I^2S format.

BCLK clock

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x03[5:4]	0x0	64fs
	0x1	48fs
	0x2	32fs
	0x3	Don't use

Data format

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x03[3:2]	0x0	I^2S format
	0x1	Left-justified format
	0x2	Right-justified format
	0x3	Don't use

Data width

Default = 0x2 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x03[1:0]	0x0	16 bit
	0x1	20 bit
	0x2	24 bit
	0x3	Don't use

SDATAO output data width

Default = 0x2 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x78[1:0]	0x0	16 bit
	0x1	20 bit
	0x2	24 bit
	0x3	Don't use

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Audio Interface format and timing

Recommended timing and operating conditions (BCLK, LRCLK, SDATA)

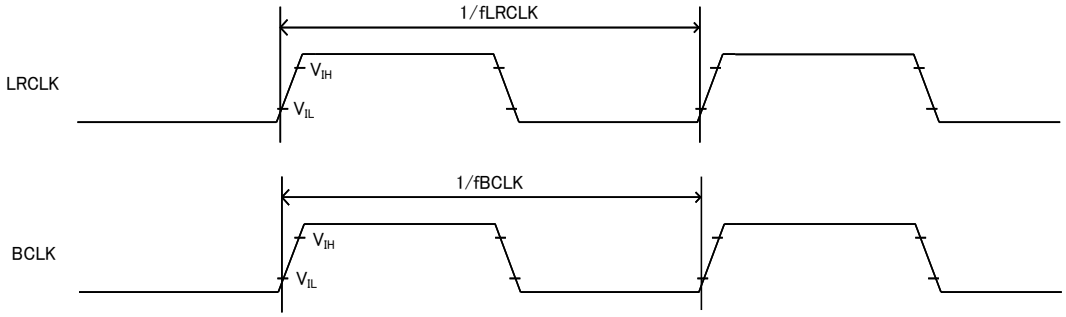


Figure 41. Clock timing

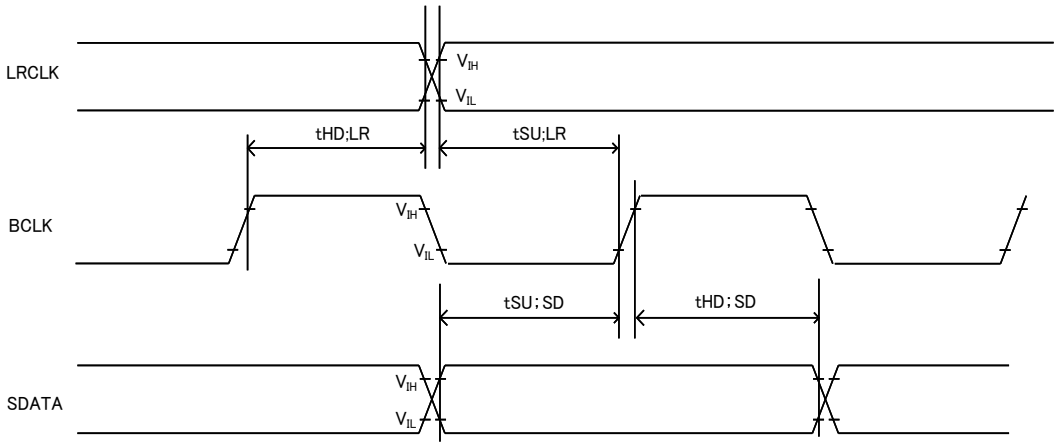


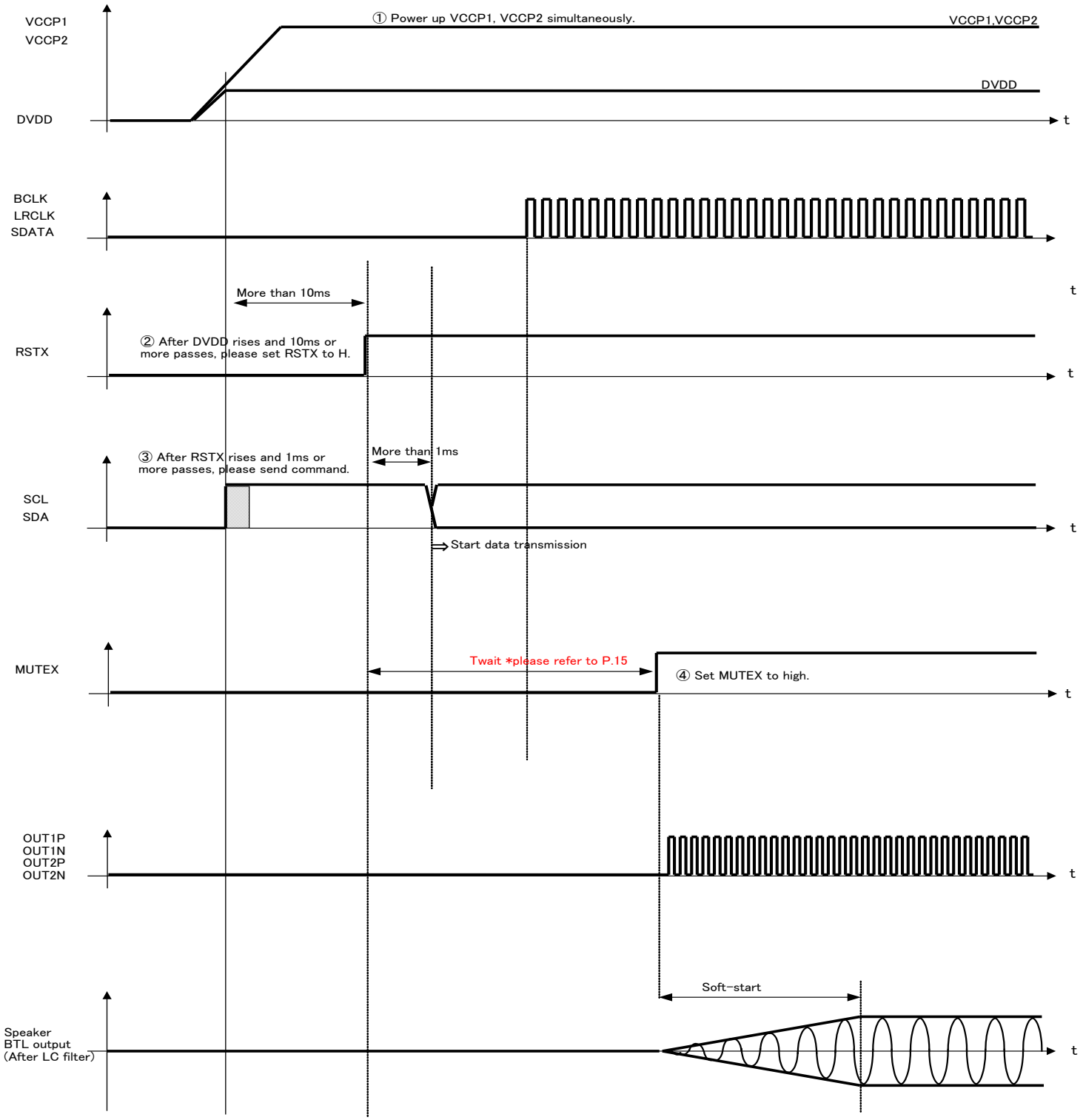
Figure 42. Audio Interface timing

No.	Parameter	Symbol	Limit		Unit
			Min.	Max.	
1	LRCLK frequency	fLRCLK	32	48	kHz
2	BCLK frequency	fBCLK	2.048	3.072	MHz
3	Setup time, LRCLK(Note 1)	tSU;LR	20	–	ns
4	Hold time, LRCLK(Note 1)	tHD;LR	20	–	ns
5	Setup time, SDATA	tSU;SD	20	–	ns
6	Hold time, SDATA	tHD;SD	20	–	ns
7	LRCLK, DUTY	dLRCLK	40	60	%
8	BCLK, DUTY	dBCLK	40	60	%

(Note 1) This regulation is to keep rising edge of LRCK and rising edge of BCLK from overlapping.

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Power supply start-up sequence

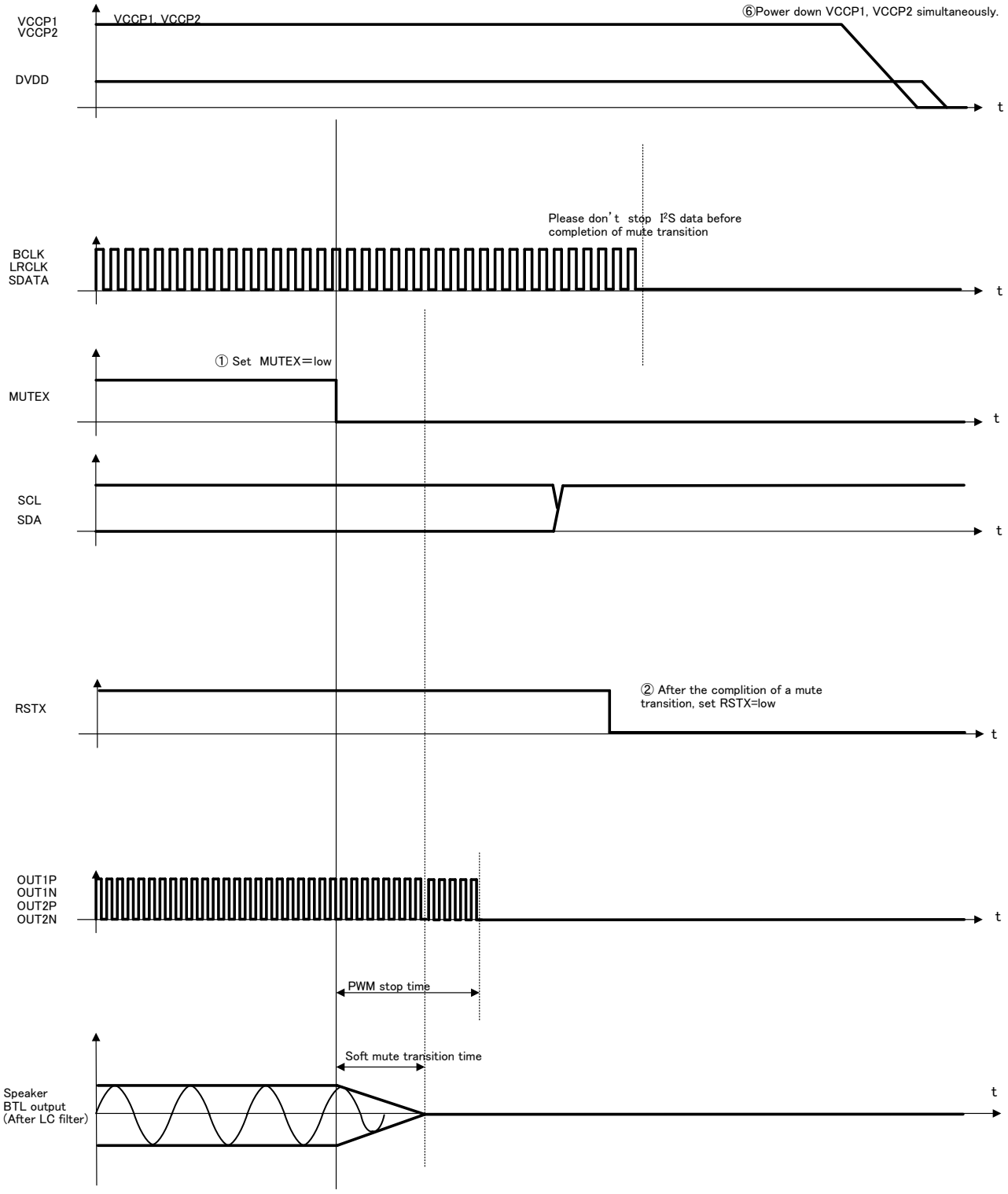


*Please make sure to input low to RSTX terminal from external at the time power up DVDD.
*Please refer to [7. The wake-up Procedure of power-up].

Figure 43.

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Power supply shut-down sequence



※Please make sure to input low to RSTX terminal when DVDD is powered down.

Figure 44.

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About the protection function

Protection function	Detecting & Releasing condition		Speaker PWM output	ERROR(Note 1) output
Output short protection	Detecting condition	Detecting current = 7.2A (TYP.)	HiZ_low (latch) (Note 2)	Low (latch)
DC voltage protection	Detecting condition	PWM output Duty=0% or 100% for 12μs(TYP)and over	HiZ_low (latch) (Note 2)	Low (latch)
High temperature protection	Detecting condition	Chip temperature to be above 150℃ (TYP.)	HiZ_low	Low
	Releasing condition	Chip temperature to be below 120℃ (TYP.)	Normal operation	
Under voltage protection	Detecting condition	Power supply voltage to be below 7.0V (TYP.)	HiZ_low	High
	Releasing condition	Power supply voltage to be above 7.5V (TYP.)	Normal operation	
Clock stop protection	Detecting condition	BCLK signal have stopped among constant period. LRCLK signal have stopped among constant period. BCLK frequency is under constant value. BCLK frequency is over constant value. Please refer to P.55-58 about constant value.	HiZ_low	High
	Releasing condition	LRCLK signal haven't stopped among constant period and BCLK continues maximum 60ms or more of continuous appropriate frequency. Please refer to P.55-58 about constant value.	Normal operation	

(Note 1) The ERROR pin is Nch open-drain output.
(Note 2) Once an IC is latched, the circuit is not released automatically even after an abnormal status is removed.
The following procedures ① or ② is available for recovery.
①After MUTEX pin is made low once over PWM stop time, MUTEX pin is returned to high again.
②Turning on the power supply again (VCCP1, VCCP2<2.5V, 10ms(min)).

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1) Output short protection (Short to the power supply)

This IC has the output short protection circuit that stops the PWM output when the PWM output is short-circuited to the power supply due to abnormality.

Detecting condition - It will detect when MUTEX pin is set high and the current that flows in the PWM output pin becomes 7.2A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-low if detected, and IC does the latch.

Releasing method - ①After MUTEX pin is set low once over the PWM stop time(see page 15), MUTEX pin is returned to high again.

②Turning on the power supply again (VCCP1, VCCP2<2.5V, 10ms(min)).

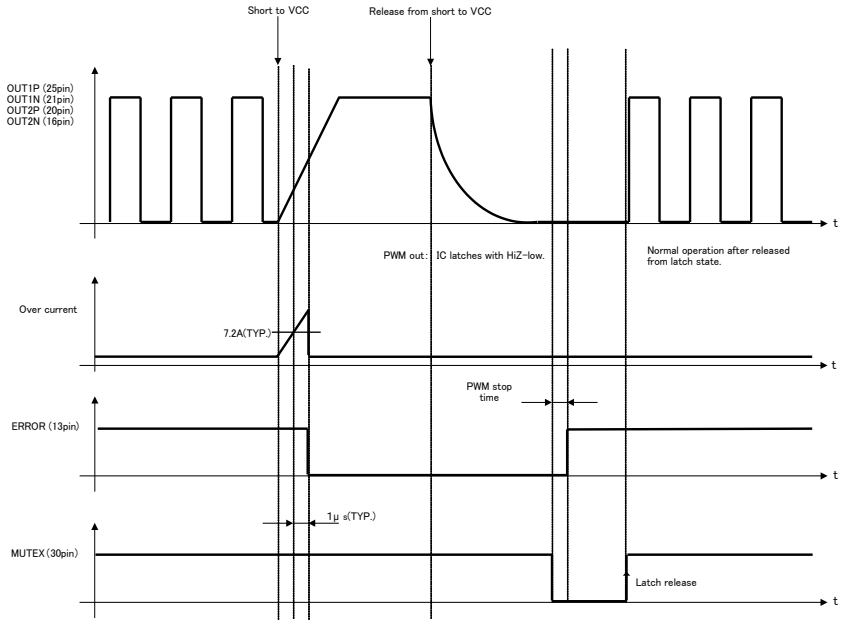


Figure 45.

2) Output short protection (Short to GND)

This IC has the output short protection circuit that stops the PWM output when the PWM output is short-circuited to GND due to abnormality.

Detecting condition - It will detect when MUTEX pin is set high and the current that flows in the PWM output terminal becomes 7.2A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-low if detected, and IC does the latch.

Releasing method – ①After MUTEX pin is set low once over the PWM stop time(see page 15), MUTEX pin is returned to high again.

②Turning on the power supply again (VCCP1, VCCP2<2.5V, 10ms(min)).

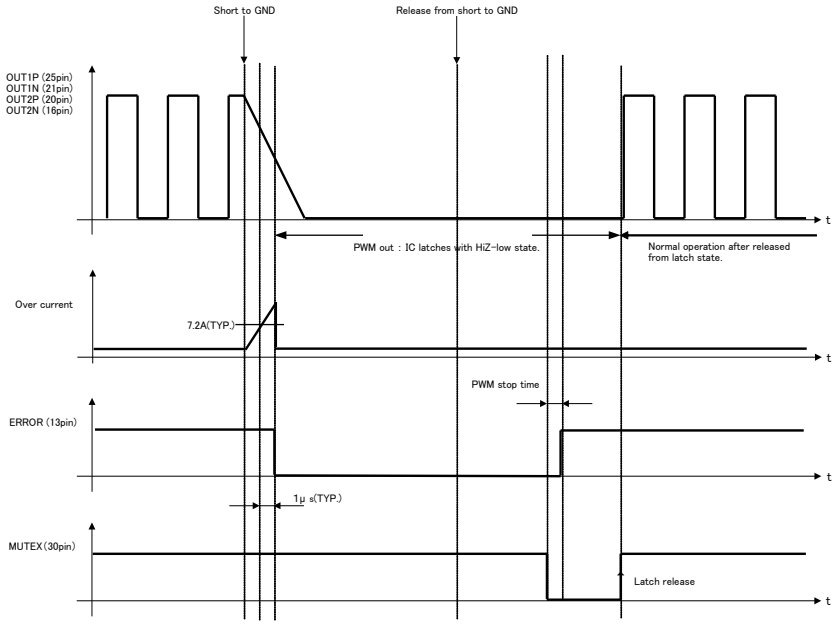


Figure 46.

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3) DC voltage protection in the speaker

When the DC voltage in the speaker is impressed due to abnormality, this IC has the protection circuit where the speaker is defended from destruction.

Detecting condition - It will detect when MUTEX pin is set high and PWM output Duty=0% or 100% over 12μs.(fs=48kHz) Once detected, The PWM output instantaneously enters the state of HiZ-low, and IC does the latch.

Releasing method – ①After MUTEX pin is set low once over the PWM stop time(see page 15), MUTEX pin is returned to high again.

②Turning on the power supply again (VCCP1, VCCP2<2.5V, 10ms(min)).

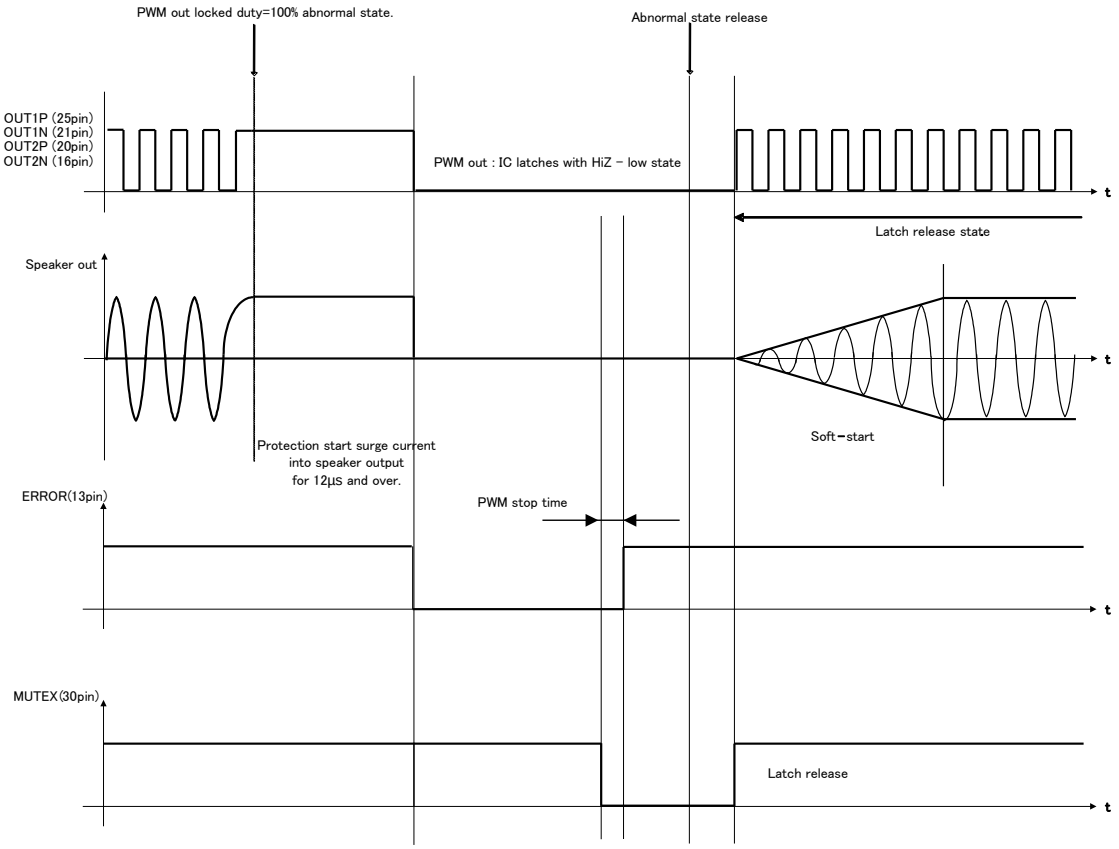


Figure 47.

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4) High temperature protection

This IC has the high temperature protection circuit that prevents thermal reckless driving under an abnormal state for the temperature of the chip to exceed Tjmax=150℃.

Detecting condition - It will detect when MUTEX pin is set high and the temperature of the chip becomes 150℃(TYP.) or more. The speaker output is muted when detected.

Releasing condition - It will release when MUTEX pin is set high and the temperature of the chip becomes 120℃(TYP.) or less. The speaker output is outputted when released.

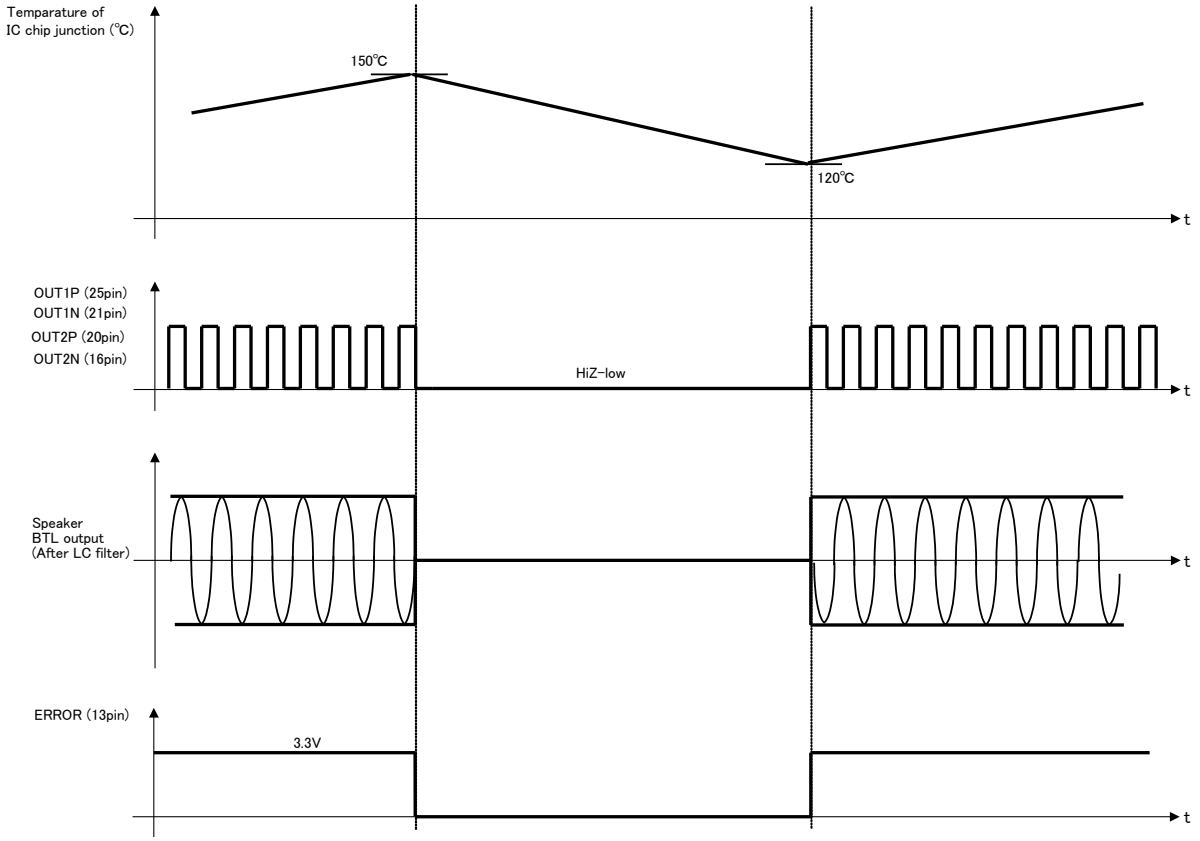


Figure 48.

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5) Under voltage protection

This IC has the under voltage protection circuit that make speaker output mute once detecting extreme drop of the power supply voltage.

Detecting condition – It will detect when MUTEX pin is set high and the power supply voltage becomes lower than 7.0V. The speaker output is muted when detected.

Releasing condition – It will release when MUTEX pin is set high and the power supply voltage becomes more than 7.5V. The speaker output is outputted when released.

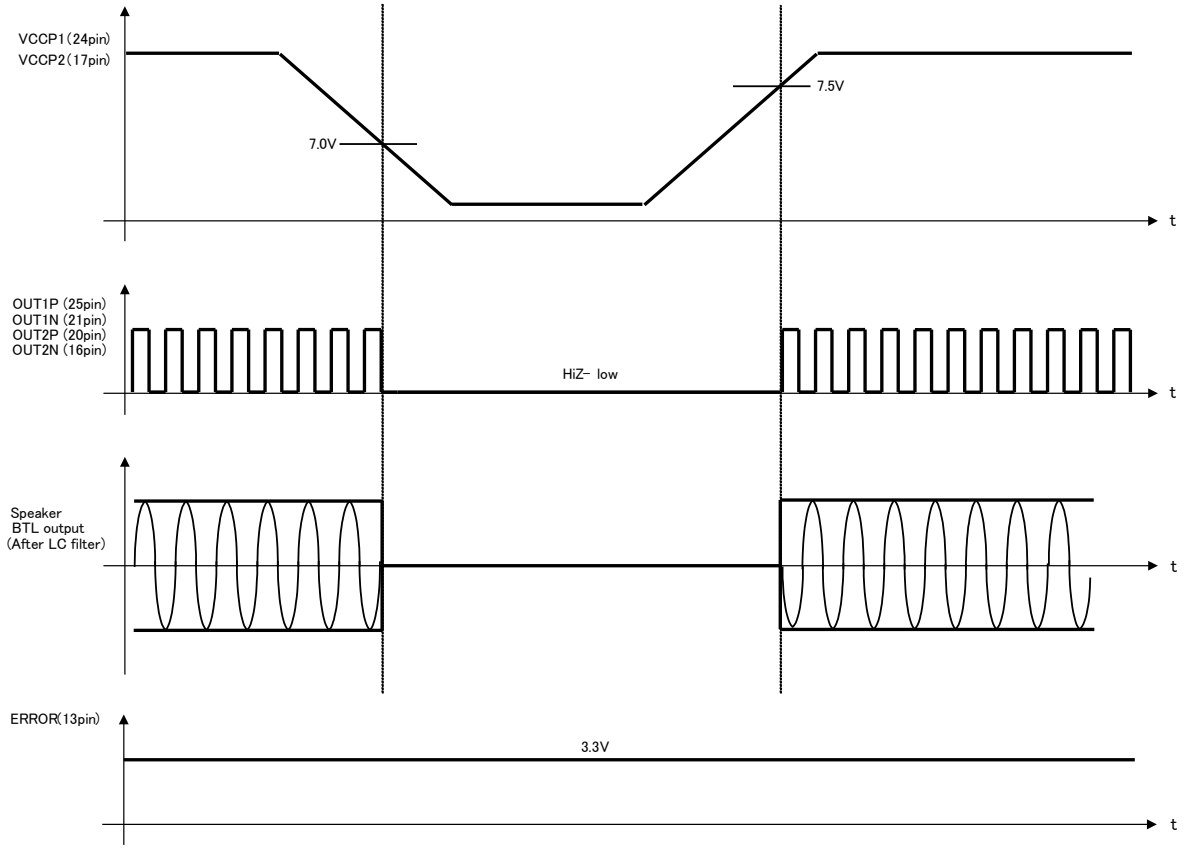


Figure 49.

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6) Clock stop protection

This IC has the clock stop protection circuits that make the speaker output mute when the BCLK and LRCLK frequency of the digital sound input are decreased or low frequency.

Detecting condition - BCLK frequency is low or stop, LRCLK frequency is stop. Speaker output is muted.

Releasing condition - Mute is released when it passes more than 60ms after an internal error state was removed. (max).

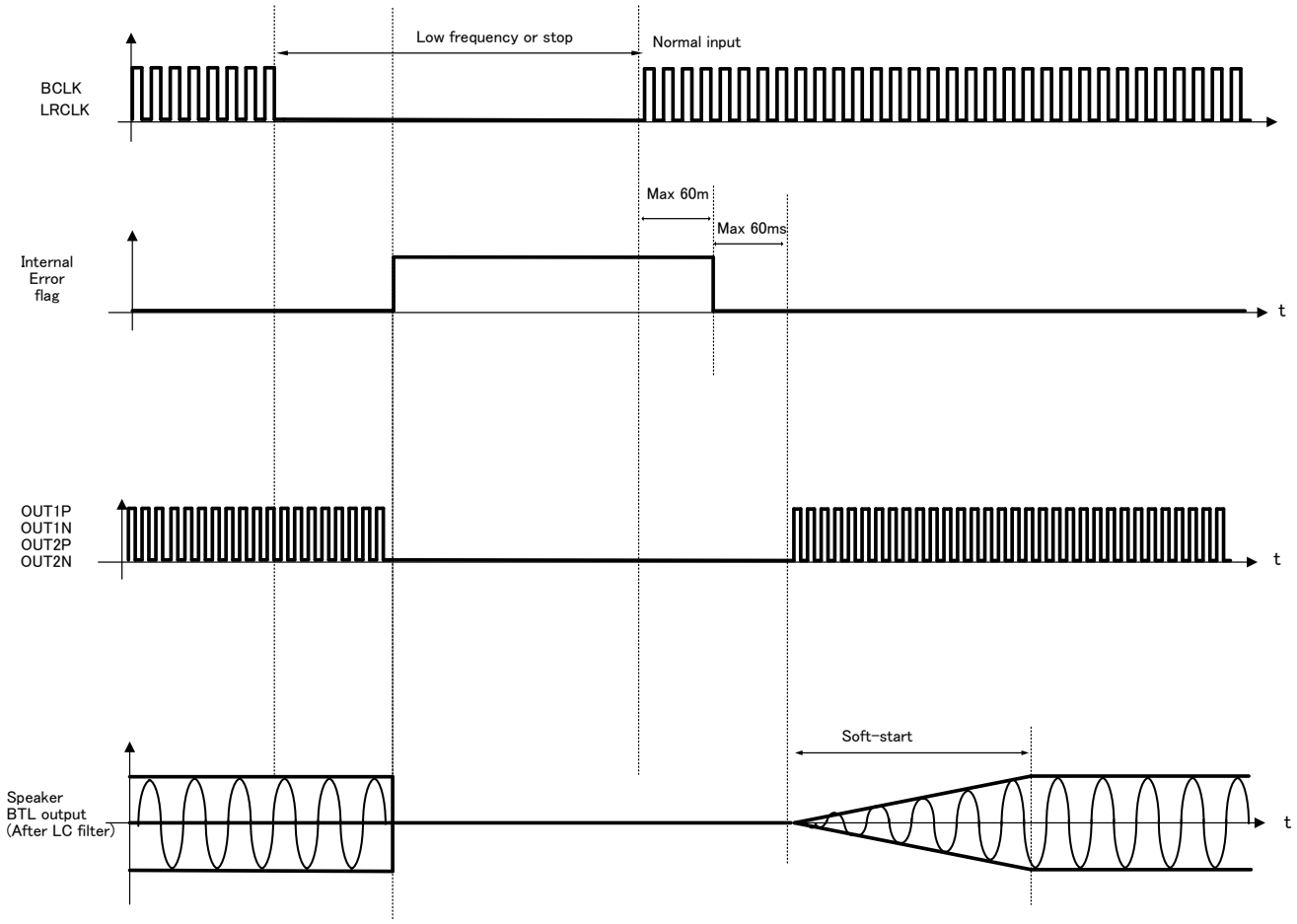


Figure 50.

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Functional descriptions of DSP Block

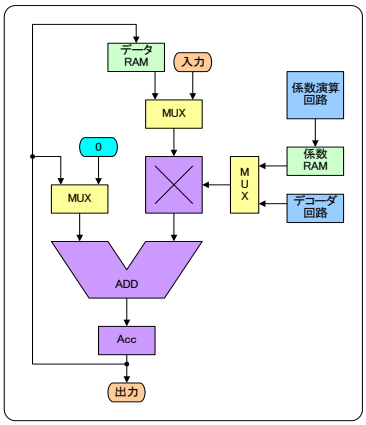
1. Digital Sound Processing(DSP)

The digital sound processing (DSP) part of BM28720 is composed of the special hardware which is the optimal for FPD-TV, the Mini/Micro Compo. BM28720MUV does the following processing using this special DSP.

Pre-Scaler, Channel Mixer, 12 Band BQ, Fine Master Volume, 3 Band DRC, Fine Post-Scaler, DC Cut HPF, Hard Clipper

The outline and signal flow of the DSP part

Data width:	32 bit (DATA RAM)
Machine cycle:	20.3ns (1024fs, fs=48kHz)
Multiplier:	32×24 → 56 bit
Adder:	56+56 → 56 bit
Data RAM:	512×32 bit
Coefficient RAM:	512×24 bit
Sampling frequency :	fs=32k,44.1k,48kHz



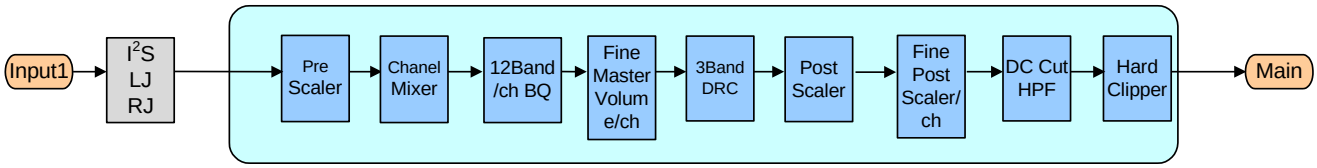


Figure 51.

The digital signal from 16 bits to 24 bits is inputted to the DSP but extends 8bit(+48dB) as the overflow margin to the upper side. When doing the processing which exceeds this range, it processes a clip in the DSP. Incidentally, in case of the 2nd IIR-type (BQ) filter which is often used generally as the digital filter, because it consumes a lot of overflow margins, the output of the multiplier and the adder inside needs note.

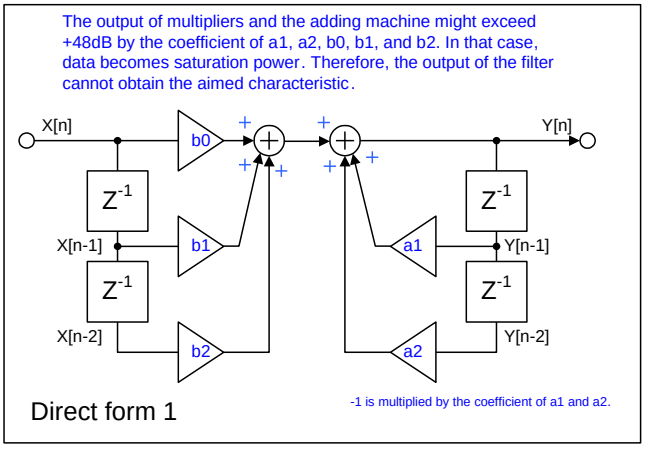


Figure 52.

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The management of audio data is as follows by each block.

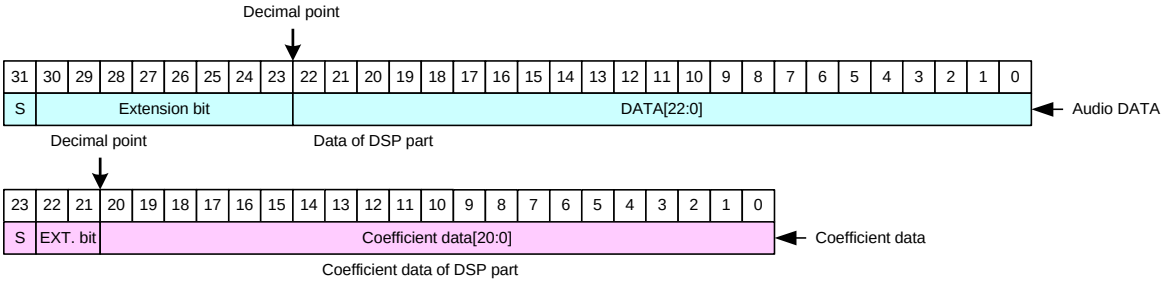


Figure 53.

1-1. Bypass

It enable pass the some function of the DSP. By using it, it left the set value of the each function and can be passed that function. it is possible to make ON/OFF of the sound effect easily.
1) 12 Band BQ, 2) 3 Band DRC and the 3) whole DSP can be passed.

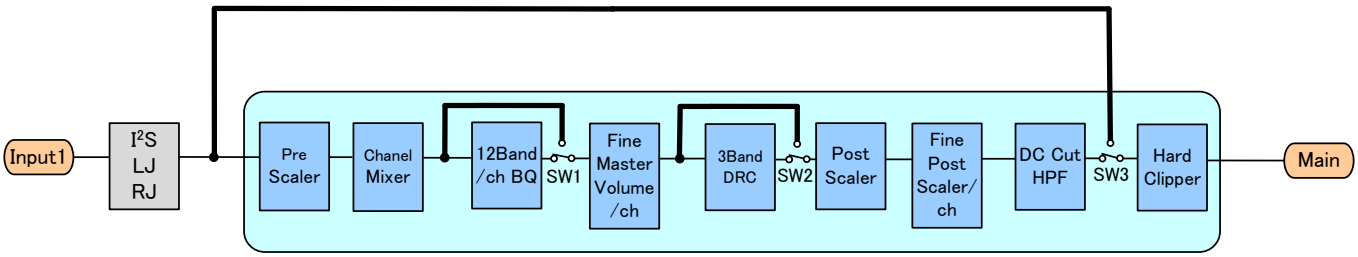


Figure 54.

Default = 0x00 *Blue square means initial value.

Select Address	bit	Explanation of operation
0x02 [2:0]	2	Bypass of 12 Band BQ (SW1) 0:Normal 1:Bypass
	1	Bypass of 3 Band DRC (SW2) 0:Normal 1:Bypass
	0	Bypass of DSP (SW3) 0:Normal 1:Bypass

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1-2. Pre-Scaler

Pre-Scaler adjusts gain of input audio data. The adjustable-range can be set from +48 dB to -79 dB with the 0.5-dB step. (Lch/Rch use same value)
Pre-Scaler doesn't have a soft transfer feature.

Default = 0x60 *Blue square means initial value.

Select Address	Explanation of operation
0x16 [7:0]	

Command Value	Gain
0x00	+48dB
0x01	+47.5dB
⋮	⋮
0x60	0dB
0x61	-0.5dB
0x62	-1dB
⋮	⋮
0xFE	-79dB
0xFF	-∞

1-3. Channel setup with a phase inversion function (Channel Mixer 1)

It sets a mixing in the sound on the left channel and the right channel of the digital signal which was inputted to the DSP. It makes a stereo signal a monaural here. Also, the phase-inversion, the mute on each channel can be set.

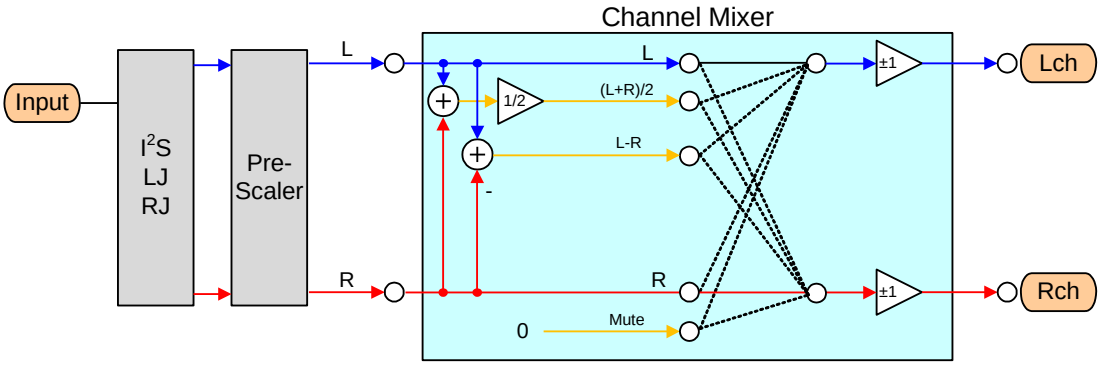


Figure 55.

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DSP input: The data inputted into Lch of DSP is inverted.

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x17[7]	0x0	Normal
	0x1	Invert

DSP input: The data inputted into Lch of DSP is mixed.

Default = 0x1 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x17 [6:4]	0x0	Mute
	0x1	Lch data input
	0x2	Rch data input
	0x3	(Lch + Rch) / 2
	0x4	Lch-Rch

DSP input: The data inputted into Rch of DSP is inverted.

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x17 [3]	0x0	Normal
	0x1	Invert

DSP input: The data inputted into Rch of DSP is mixed.

Default = 0x2 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x17 [2:0]	0x0	Mute
	0x1	Lch data input
	0x2	Rch data input
	0x3	(Lch + Rch) / 2
	0x4	Lch-Rch

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1-4. Biquad filter

In this IC, the following block has the biquad type filter(BQ).
There are 12 Band BQ, Crossover filter of 3 Band DRC block and BQ of the smooth transition.
The shape is used as peaking filter, low shelf filter, high shelf filter, low-pass filter, high-pass filter, notch filter and all path filters.
Setting the coefficient of the digital filter in the IC by transmit to the coefficient RAM via command. 12 Band BQ have the soft transfer feature. About the detailed order of the parameter setting, please refers to the following BQ setting method.

Select of BQ independence or synchronous setting

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x60 [4]*	0x0	L/R common setting
	0x1	L/R independence setting

*0x60[4] setting note.
Please re-set all BQ when you change the setting of 0x60[4].
Total 18 BQ needs to be set again. (BQ1-12, DRC1, DRC2 and DRC3).

BQ soft transition destination band

Default = 0x0 *Blue square means initial value.

Select Address	Explanation of operation
0x51 [4:0]*	

Value	Destination	Value	Destination
0x00	12BAND(1)	0x0A	12BAND(11)
0x01	12BAND(2)	0x0B	12BAND(12)
0x02	12BAND(3)		
0x03	12BAND(4)		
0x04	12BAND(5)		
0x05	12BAND(6)		
0x06	12BAND(7)		
0x07	12BAND(8)		
0x08	12BAND(9)		
0x09	12BAND(10)		

Select of smooth transition

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x53 [6]	0x0	Use smooth transition
	0x1	Not use smooth transition

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Select the destination channel of smooth transition

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x53 [5:4]	0x0	Lch と Rch
	0x1	Lch
	0x2	Rch
	0x3	Don't use

Setting of smooth transition time

Default = 0x3 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x53 [3:2]	0x0	2.7ms
	0x1	5.3ms
	0x2	10.7ms
	0x3	21.3ms

Setting of smooth transition wait time

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x53 [1:0]	0x0	2.7ms
	0x1	5.3ms
	0x2	10.7ms
	0x3	21.3ms

Setting of smooth transition start

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x58 [0]	0x0	Stop the smooth transition operation
	0x1	Start the smooth transition operation (After the transition is completed, it becomes 0 automatically)

This register is write only.

Read-out smooth transition status

Read only

Select Address	Explanation of operation
0x59 [0]	1 : Executing soft transition 0 : Not during soft transition

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1-5. Volume

Volume is from+24dB to -103dB, and can be selected by the step of 0.125dB. And it is possible to be setting of -∞dB, too. At the time of switching of Volume, smooth transition is performed. Soft transition duration is optional with the command.
L/R synchronous or L/R independent can be selected by 0x10[7].
It becomes the following formula at the transition from AdB to BdB. C is smooth transition duration selected by 0x15[7:6] command.

$$\text{Transition time} = \left| \left(10^{\frac{A}{20}} - 10^{\frac{B}{20}}\right) * C \right| \text{ ms}$$

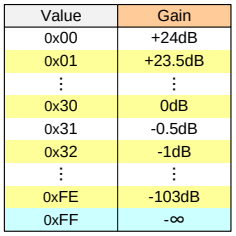
Setting of soft transition time

Default = 0x0 *Blue square means initial value.

Select Address	Value	動作説明
0x15 [7:6]	0x0	21.3ms
	0x1	42.7ms
	0x2	85.3ms
	0x3	Don't use

Lch/common volume setting

Default = 0xFF *Blue square means initial value.

Select Address	Explanation of operation
0x11 [7:0]	

Value	Gain
0x00	+24dB
0x01	+23.5dB
⋮	⋮
0x30	0dB
0x31	-0.5dB
0x32	-1dB
⋮	⋮
0xFE	-103dB
0xFF	-∞

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Setting of fine volume
This command becomes effective by sending the following command after setting.
When using this command, it is possible to set a volume in 0.125dB carving.
When L/R synchronous volume setting, 0x11[7:0] is enable.
When L/R independent volume setting, 0x11[7:0] is the volume setting of Lch.

Lch/common fine volume setting

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x10 [1:0]	0x0	0dB
	0x1	-0.125dB
	0x2	-0.25dB
	0x3	-0.375dB

【Note1】
It is possible to use with the 0.5-dB step in changing only 0x11[7:0] when 0x10[1:0]=0x0.

The Lch/Rch independent volume setting and the synchronous volume setting can be selected by 0x10[7] command.
When Lch/Rch independent volume set, the volume setting of Lch is the setting of 0x10[1:0] and 0x11, and the volume setting of Rch is the settings of 0x10[5:4] and 0x12.

Setting of Lch/Rch independent volume

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x10[7]	0x0	Lch/Rch common volume setting
	0x1	Lch/Rch independent volume setting

Setting of volume (Setting of Rch volume, It is enable only to set an independent volume.)

Default = 0xFF *Blue square means initial value.

Select Address	Explanation of operation
0x12 [7:0]	

Value	Gain
0x00	+24dB
0x01	+23.5dB
⋮	⋮
0x30	0dB
0x31	-0.5dB
0x32	-1dB
⋮	⋮
0xFE	-103dB
0xFF	-∞

Setting of fine volume
This command becomes effective by sending the following command after setting.
When using this command, it is possible to set a volume in 0.125dB carving.

Setting of fine volume (Setting of Rch fine volume, It is enable only to set an independent volume.)

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x10 [5:4]	0x0	0dB
	0x1	-0.125dB
	0x2	-0.25dB
	0x3	-0.375dB

【Note2】
It is possible to use with the 0.5-dB step in changing only 0x12[7:0] when 0x10[5:4]=0.

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【Note3】
It is possible to use with the 0.125-dB step in setting both 0x10[1:0] and 0x11[7:0].
In case of 0x10[1:0] = 0x0, it becomes the set value of 0x11[7:0].
In case of 0x10[1:0] = 0x1, it becomes the -0.125dB set value of 0x11[7:0].
In case of 0x10[1:0] = 0x2, it becomes the -0.25dB set value of 0x11[7:0].
In case of 0x10[1:0] = 0x3, it becomes the -0.375dB set value of 0x11[7:0].
Because it is fixed by the transfer of 0x11 in any case, the soft transfer can be beforehand begun in the set value for the direct following of the purpose in setting 0x11 after setting in 0x10.
0x10[5:4] is the same function as 0x10[1:0], 0x12 is the same function as 0x11 when Lch/Rch independently set for Rch.

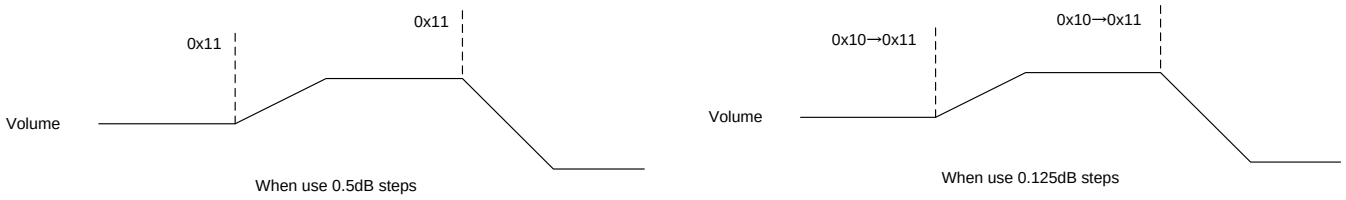


Figure 56.

1-6. 3 band DRC

This DRC is used in order to prevent clip output of a large audio signal.
There are three kinds of DRC (DRC1, DRC2, and DRC3), and non clip output can be achieved at each band.
DRC1, DRC2 and DRC3 can set up two threshold value levels. Moreover, it is possible to also change slope.

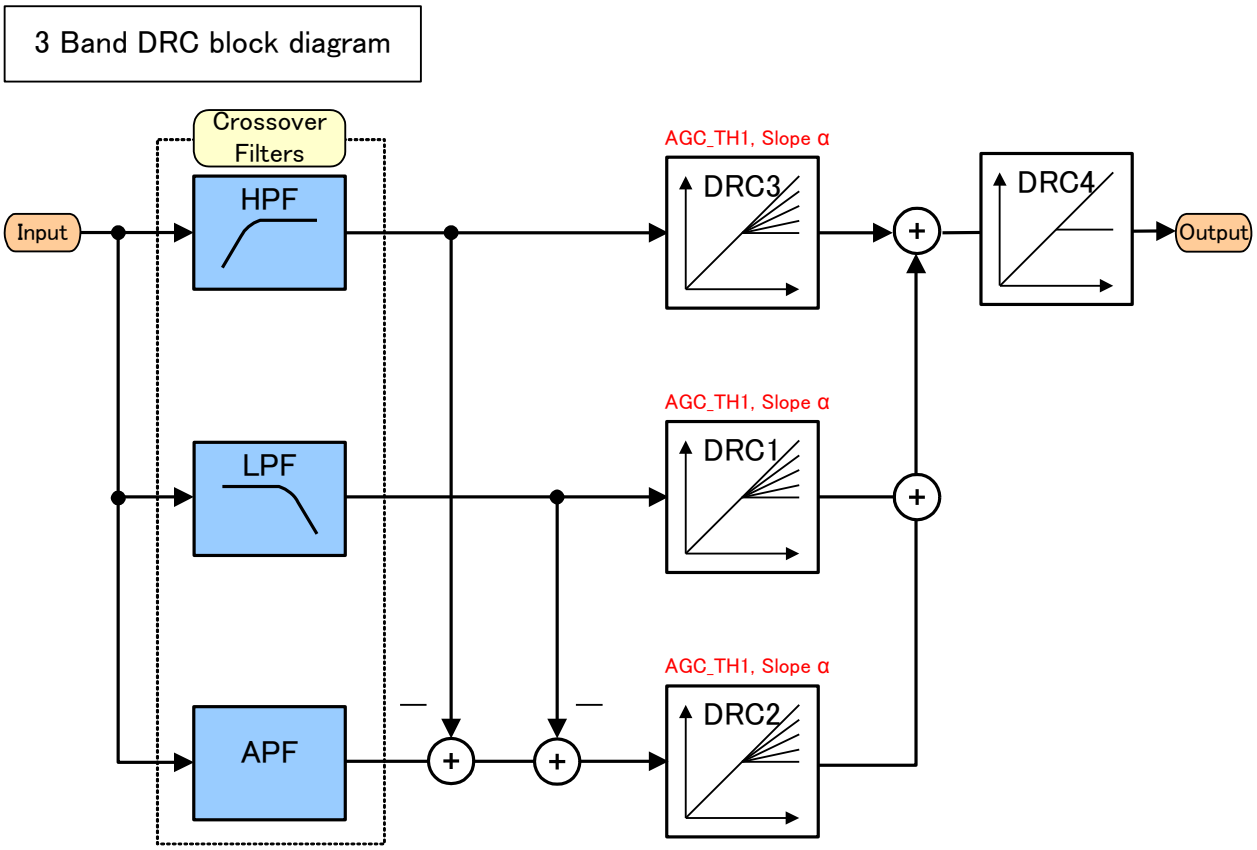
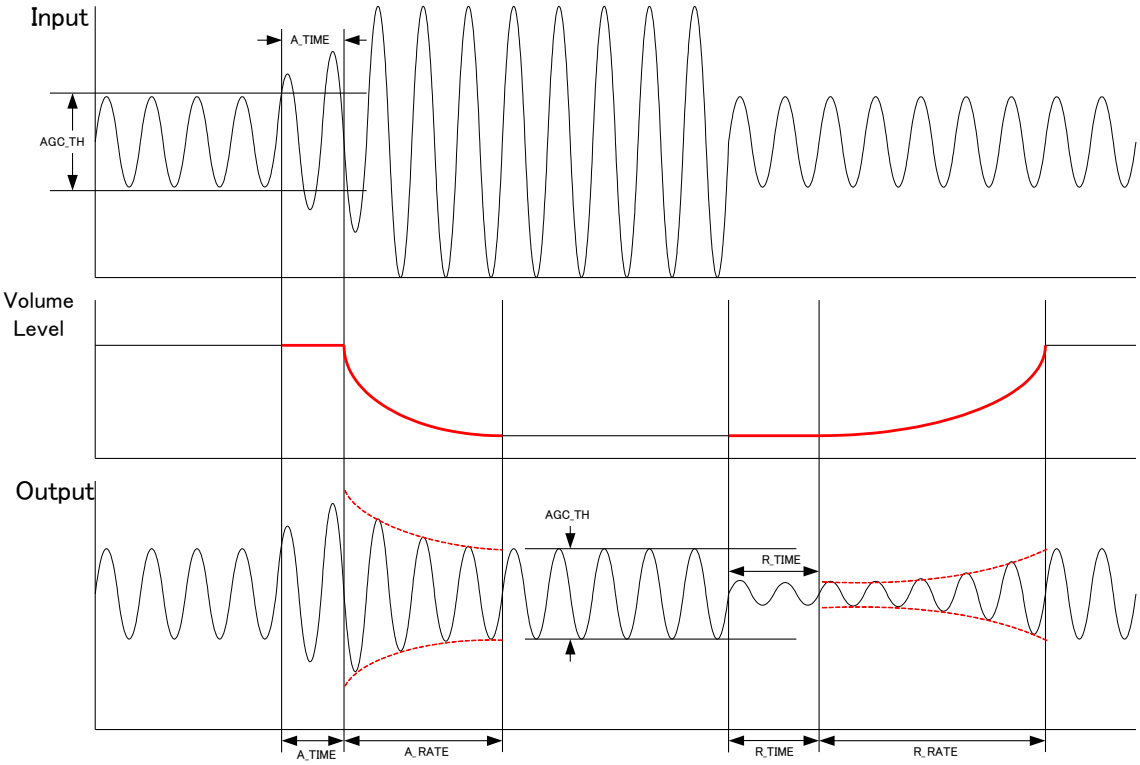


Figure 57.

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DRC transition figure



In here A_TIME is the time for detecting time before starting gain down operation. And A_RATE decides the slope of gain compression.

On the other hand R_TIME is the time for detecting before starting to release gain operation. And R_RATE decides slope of release gain.

Figure 58.

DRC1, DRC2, DRC3 can be set AGC_TH1 and AGC_TH2 as shown in below. If output is in between AGC_TH1 and AGC_TH2, a slant for output gain can be made. If input become bigger and output over AGC_TH2, output gain don't have slant and become constant level. Value for slant setting (α) is calculated by AGC_TH1, AGC_TH2 and the value of input gain for reaching AGC_TH2 (xdB).

The operation between AGC_TH1 and AGC_TH2 is decided as $DRC1_{slope}$ and $DRC2_{slope}$ and $DRC3_{slope}$.

And the operation over AGC_TH2 is decided as $DRC1_{comp}$ and $DRC2_{comp}$ and $DRC3_{comp}$.

Each operation can be set ON/OFF, A_TIME, A_RATE, R_TIME, R_RATE respectively.

DRC input-and-output gain characteristics

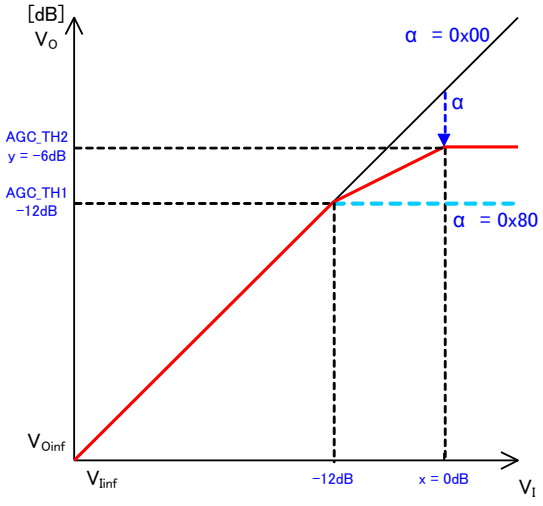


Figure 59.

The formula which asks for Slope alpha is described below.

Alpha changes into 8bit Hex data of the complement of 2 the value calculated by calculation.

$$\alpha = \frac{10^{\frac{y}{20}} - 10^{\frac{x}{20}}}{10^{\frac{TH}{20}} - 10^{\frac{x}{20}}} \times 128$$

TH is AGC_TH1. x is input level. y is output level.

Ex) It asks for alpha at the time of AGC_TH1 = −12dB, x = 0dB y = −6dB

$$\alpha = \frac{10^{\frac{-6}{20}} - 10^{\frac{0}{20}}}{10^{\frac{-12}{20}} - 10^{\frac{0}{20}}} \times 128$$

α = 85.266 → 0x55

0x55 calculated is set as 0x29, 0x31 or 0x39.

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Volume Curve

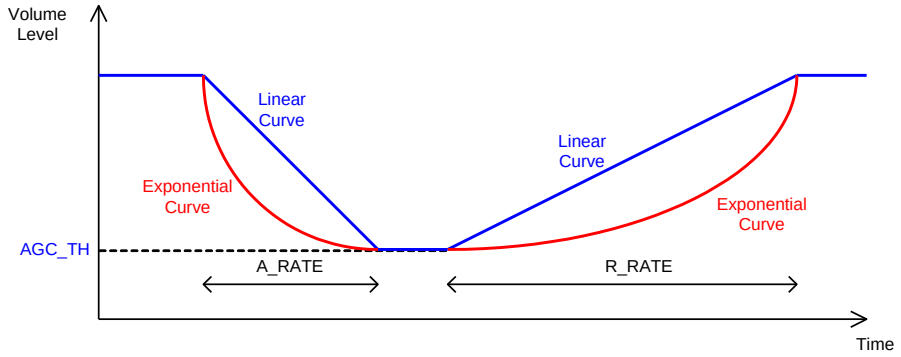


Figure 60.

DRC1$_{slope}$ ON/OFF setting

OFF is through output.

Default = 0x1 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x20 [7]	0x0	Not use
	0x1	Use

DRC1$_{comp}$ ON/OFF setting

OFF is through output.

Default = 0x1 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x20 [6]	0x0	Not use
	0x1	Use

DRC2$_{slope}$ ON/OFF setting

OFF is through output.

Default = 0x1 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x20 [5]	0x0	Not use
	0x1	Use

DRC2$_{comp}$ ON/OFF setting

OFF is through output.

Default = 0x1 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x20 [4]	0x0	Not use
	0x1	Use

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DRC3$_{slope}$ ON/OFF setting

OFF is through output.

Default = 0x1 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x20 [3]	0x0	Not use
	0x1	Use

DRC3$_{comp}$ ON/OFF setting of compressor

OFF is through output.

Default = 0x1 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x20 [2]	0x0	Not use
	0x1	Use

DRC4 ON/OFF setting

DRC4 have only compression function. DRC4 don't have slope function.

OFF is through output.

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x3F [4]	0x0	Not use
	0x1	Use

The volume curve at the time of an attack (A_RATE) is selected.

Default = 0x1 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x21[7]	0x0	Linear curve
	0x1	Exponential curve

The volume curve at the time of a release (R_RATE) is selected.

Default = 0x1 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x21 [6]	0x0	Linear curve
	0x1	Exponential curve

DRC is 1 Band setting at initial state.

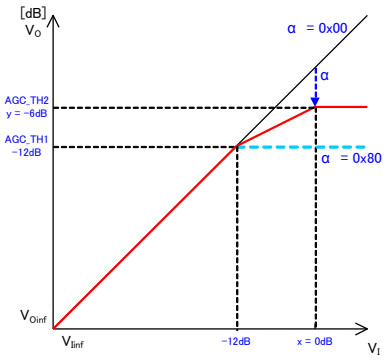
To set the crossover filter (HPF, LPF and APF) which divides the frequency band of 3 Band DRC, therefore, it is referred to the 1-4.

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Slope (α) setting of $DRC1_{slope}$, $DRC2_{slope}$, and $DRC3_{slope}$

$DRC1_{slope}$, $DRC2_{slope}$ and $DRC3_{slope}$ can be set individually.

Default = 0x80 *Blue square means initial value.

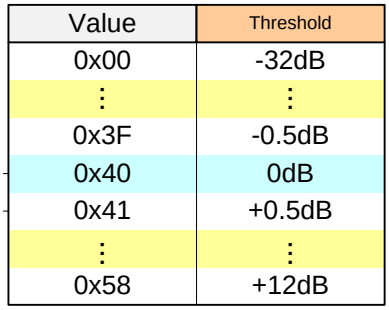
Select Address	Explanation of operation
$DRC1_{slope}$ 0x29 [7:0] $DRC2_{slope}$ 0x31 [7:0] $DRC3_{slope}$ 0x39 [7:0]	 The formula which asks for Slope alpha is described below. Alpha changes into 8bit Hex data of the complement of 2 the value calculated by calculation. $\alpha = \frac{10^{\frac{y}{20}} - 10^{\frac{x}{20}}}{10^{\frac{TH}{20}} - 10^{\frac{x}{20}}} \times 128$ TH is AGC_TH1. x is input level. y is output level. Ex) It asks for alpha at the time of AGC_TH1 = −12dB, x = 0dB y = −6dB $\alpha = \frac{10^{\frac{-6}{20}} - 10^{\frac{0}{20}}}{10^{\frac{-12}{20}} - 10^{\frac{0}{20}}} \times 128$ α = 85.266 → 0x55 0x55 calculated is set as 0x29, 0x31 or 0x39.

AGC_TH1 setting of $DRC1_{slope}$, $DRC2_{slope}$, and $DRC3_{slope}$

$DRC1_{slope}$, $DRC2_{slope}$ and $DRC3_{slope}$ can be set individually.

Please set this value is smaller than the value of AGC_TH2.

Default = 0x40 *Blue square means initial value.

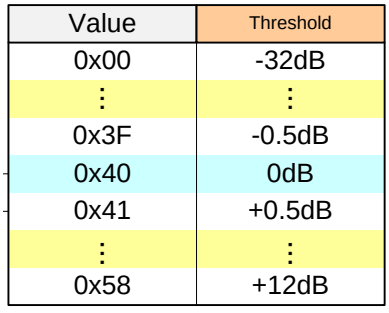
Select Address	Explanation of operation
$DRC1_{slope}$ 0x28 [6:0] $DRC2_{slope}$ 0x30 [6:0] $DRC3_{slope}$ 0x38 [6:0]	

Value	Threshold
0x00	-32dB
⋮	⋮
0x3F	-0.5dB
0x40	0dB
0x41	+0.5dB
⋮	⋮
0x58	+12dB

AGC_TH2 setting of $DRC1_{comp}$, $DRC2_{comp}$, $DRC3_{comp}$, and DRC4

$DRC1_{comp}$, $DRC2_{comp}$, $DRC3_{comp}$ and DRC4 can be set individually.

Default = 0x40 *Blue square means initial value.

Select Address	Explanation of operation
$DRC1_{comp}$ 0x2C [6:0] $DRC2_{comp}$ 0x34 [6:0] $DRC3_{comp}$ 0x3C [6:0] DRC4 0x40 [6:0]	

Value	Threshold
0x00	-32dB
⋮	⋮
0x3F	-0.5dB
0x40	0dB
0x41	+0.5dB
⋮	⋮
0x58	+12dB

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A_RATE setting of $DRC1_{slope}$, $DRC2_{slope}$, $DRC3_{slope}$, $DRC1_{comp}$, $DRC2_{comp}$, $DRC3_{comp}$, DRC4
$DRC1_{slope}$, $DRC2_{slope}$, $DRC3_{slope}$, $DRC1_{comp}$, $DRC2_{comp}$, $DRC3_{comp}$, DRC4 can be set individually.

Default = 0x3 *Blue square means initial value.

Select Address	Explanation of operation
$DRC1_{slope}$ 0x2A [6:4] $DRC2_{slope}$ 0x32 [6:4] $DRC3_{slope}$ 0x3A [6:4] $DRC1_{comp}$ 0x2E [6:4] $DRC2_{comp}$ 0x36 [6:4] $DRC3_{comp}$ 0x3D [6:4] DRC4 0x41 [6:4]	

Value	A_RATE	Value	A_RATE
0x0	1ms	0x4	5ms
0x1	2ms	0x5	10ms
0x2	3ms	0x6	20ms
0x3	4ms	0x7	40ms

R_RATE setting of $DRC1_{slope}$, $DRC2_{slope}$, $DRC3_{slope}$, $DRC1_{comp}$, $DRC2_{comp}$, $DRC3_{comp}$, DRC4
$DRC1_{slope}$, $DRC2_{slope}$, $DRC3_{slope}$, $DRC1_{comp}$, $DRC2_{comp}$, $DRC3_{comp}$, DRC4 can be set individually.

Default = 0xB *Blue square means initial value.

Select Address	Explanation of operation
$DRC1_{slope}$ 0x2A [3:0] $DRC2_{slope}$ 0x32 [3:0] $DRC3_{slope}$ 0x3A [3:0] $DRC1_{comp}$ 0x2E [3:0] $DRC2_{comp}$ 0x36 [3:0] $DRC3_{comp}$ 0x3D [3:0] DRC4 0x41 [3:0]	

Value	R_RATE	Value	R_RATE
0x0	0.125s	0x8	2s
0x1	0.1825s	0x9	2.5s
0x2	0.25s	0xA	3s
0x3	0.5s	0xB	4s
0x4	0.75s	0xC	5s
0x5	1s	0xD	6s
0x6	1.25s	0xE	7s
0x7	1.5s	0xF	8s

A_TIME setting of $DRC1_{slope}$, $DRC2_{slope}$, $DRC3_{slope}$, $DRC1_{comp}$, $DRC2_{comp}$, $DRC3_{comp}$, DRC4
$DRC1_{slope}$, $DRC2_{slope}$, $DRC3_{slope}$, $DRC1_{comp}$, $DRC2_{comp}$, $DRC3_{comp}$, DRC4 can be set individually.

Default = 0x1 *Blue square means initial value.

Select Address	Explanation of operation
$DRC1_{slope}$ 0x2B [7:4] $DRC2_{slope}$ 0x33 [7:4] $DRC3_{slope}$ 0x3B [7:4] $DRC1_{comp}$ 0x2F [7:4] $DRC2_{comp}$ 0x37 [7:4] $DRC3_{comp}$ 0x3E [7:4] DRC4 0x42 [7:4]	

Value	A_TIME	Value	A_TIME
0x0	0ms	0x8	6ms
0x1	0.5ms	0x9	7ms
0x2	1ms	0xA	8ms
0x3	1.5ms	0xB	9ms
0x4	2ms	0xC	10ms
0x5	3ms	0xD	20ms
0x6	4ms	0xE	30ms
0x7	5ms	0xF	40ms

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R_TIME setting of DRC1, DRC2, DRC3, and DRC4

DRC1, DRC2, DRC3 and DRC4 are individually setting.

Default = 0x3 *Blue square means initial value.

Select Address	Explanation of operation
$DRC1_{slope}$ 0x2B [2:0] $DRC2_{slope}$ 0x33 [2:0] $DRC3_{slope}$ 0x3B [2:0] $DRC1_{comp}$ 0x2F [2:0] $DRC2_{comp}$ 0x37 [2:0] $DRC3_{comp}$ 0x3E [2:0] DRC4 0x42 [2:0]	

Value	R_TIME	Value	R_TIME
0x0	5ms	0x4	100ms
0x1	10ms	0x5	200ms
0x2	25ms	0x6	300ms
0x3	50ms	0x7	400ms

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1-7. Post-Scaler

Post-Scaler adjusts gain of output audio data. The adjustable-range can be set from +48 dB to -79 dB with the 0.5-dB step. (Lch/Rch use same value)
Pre-Scaler doesn't have a soft transfer feature.

Default = 0x60 *Blue square means initial value.

Select Address	Explanation of operation
0x13 [7:0]	

Value	Gain
0x00	+48dB
0x01	+47.5dB
⋮	⋮
0x60	0dB
0x61	-0.5dB
0x62	-1dB
⋮	⋮
0xFE	-79dB
0xFF	-∞

1-8. Fine Post-Scaler

An adjustable range can be set up at a 0.1dB step from +0.7dB to –0.8dB. Fine Post-Scaler does not have a smooth transition function.
(Lch and Rch can be set different value.)

Default= 0x8 *Blue square means initial value.

Select Address	Explanation of operation
Lch 0x14 [7:4] Rch 0x14 [3:0]	

Command	Gain	Command	Gain
0x0	-0.8dB	0x8	0dB
0x1	-0.7dB	0x9	+0.1dB
0x2	-0.6dB	0xA	+0.2dB
0x3	-0.5dB	0xB	+0.3dB
0x4	-0.4dB	0xC	+0.4dB
0x5	-0.3dB	0xD	+0.5dB
0x6	-0.2dB	0xE	+0.6dB
0x7	-0.1dB	0xF	+0.7dB

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1-9. Hard Clipper

Measuring output of the television, output power is measured in 10% THD+N condition. It can be made to clip with any output amplitude by using a clipper function. For example, the output of 10W or 5W can be gained using the amplifier of 15W output.

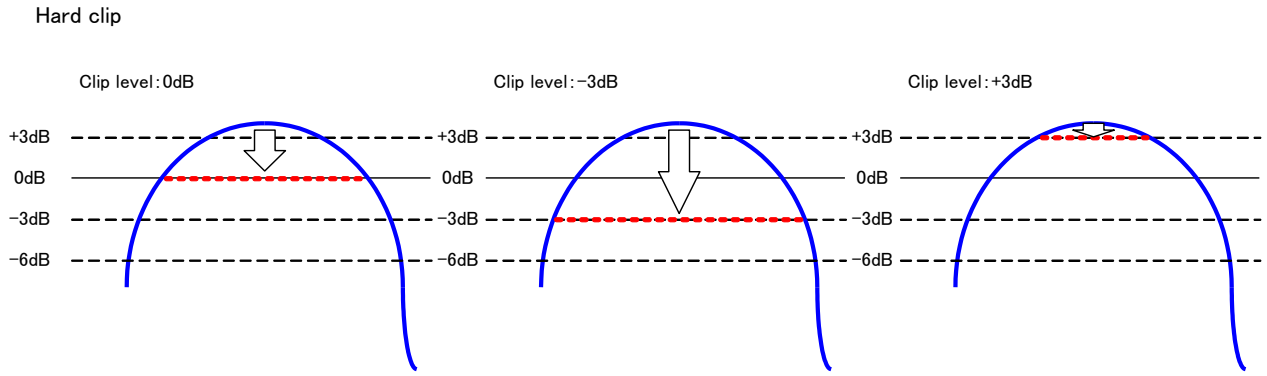


Figure 61.

Clipper setting

Default = 0x1 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x1A [0]	0x0	Clipper function is not used.
	0x1	Hard clipper function is used.

Clip level selection

Default = 0xE1 *Blue square means initial value.

Select Address	Explanation of operation
0x1B [7:0]	

Value	Gain
0x00	-22.5dB
0x01	-22.4dB
⋮	⋮
0xE0	-0.1dB
0xE1	0dB
0xE2	+0.1dB
⋮	⋮
0xFE	+2.9dB
0xFF	+3dB

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1-10. DC Cut HPF

DC offset element of the digital signal outputted from audio DSP is cut by this HPF.
The cutoff frequency fc of HPF uses the 1Hz filter, and the degree uses the first-order filter.

Default = 0x1 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x18 [0]	0x0	Not use
	0x1	Use

1-11. RAM clear

The data RAM of DSP and coefficient RAM are cleared.
40μs or more is required until all the data is cleared.

Clear of the data RAM

Default = 0x1 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x01 [7]	0x0	Normal
	0x1	Clear

Clear of coefficient RAM

Default = 0x1 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x01 [6]	0x0	Normal
	0x1	Clear

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1-12. Audio Output Level Meter

It is possible to output the peak level of the PCM data inputted into a PWM processor.
A peak value can be read using the 2-wire command interface as 16 bit data of an absolute value.
The interval holding a peak value can be selected from six steps (50ms step) from 50ms to 300ms.
A peak hold result can be selected from L channel, R channel, and a monophonic channel {(Lch+Rch) /2}.

Audio Output Level Meter block diagram

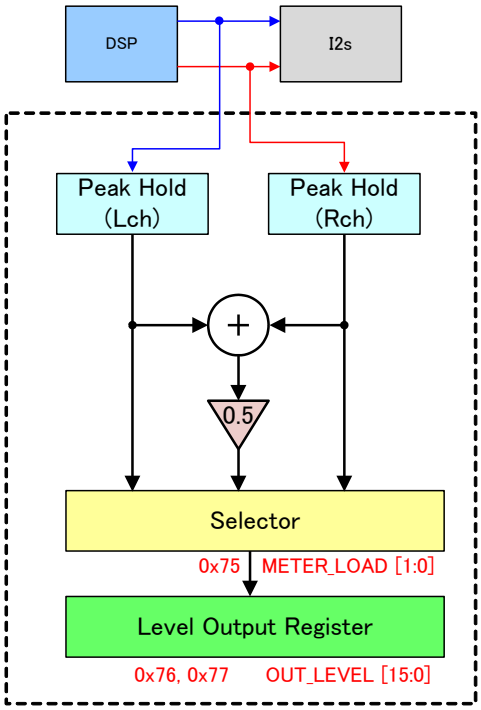


Figure 62.

Setting of the peak level hold time interval of Audio Output Level Meter

Default = 0x0 *Blue square means initial value.

Select Address	Explanation of operation
0x74 [2:0]	Value / Hold time 0x0 / 50ms 0x1 / 100ms 0x2 / 150ms 0x3 / 200ms 0x4 / 250ms 0x5 / 300ms

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The signal of Audio Level Meter read-back is selected.
A value will be taken into a read-only register if a setting value is written in.
In order to update this register value, it is necessary to write in a setting value again.

Write only

Select Address	Value	Explanation of operation
0x75 [1:0]	0x0	The peak level of L channel
	0x1	The peak level of R channel
	0x2	The peak level of monophonic channel {(Lch+Rch) /2}

Read-back of Audio Output Level
0x76 (upper 8 bits) and a 0x77 (lower 8 bits) commands are read for the maximum within the period appointed by the command 0x74 using the 2-wire interface.

(Example)
When 0xFFFF is read, mean 1.0 (0dBFs).
When 0x8000 is read, mean 0.5 (-6dBFs).

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2. Setting and reading method of BQ

It explains a detailed sequence of the setting method and the reading method of the parametric equalizer separately for usage.

2-1 BQ coefficient setting

The parametric equalizer consists of biquad filter as follows. Each coefficient of biquad filter can be written directly. It is S2.21 format, and setting range is -4≦x＜+4.
Moreover, the coefficient address is shown in Table 1.

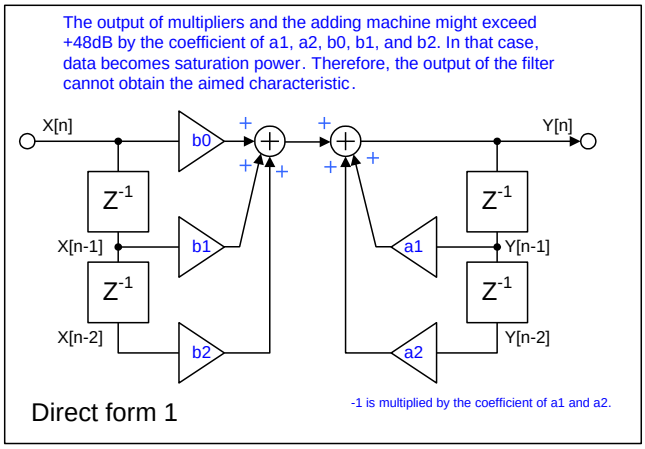


Figure 63.

2-1-1 Writing sequence (It sets up in number order)

1. Address setting (0x61) (*1)Table 1 is referred to.
2. 24bit coefficient upper [23:16] bit setting (0x62[7:0])
3. 24bit coefficient middle [15:8] bit setting (0x63[7:0])
4. 24bit coefficient lower [7:0] bit setting (0x64[7:0])
5. The writing of coefficients is performed. (0x65[0] = 0x1) *

* After completion of writing coefficients this register is cleared automatically. It is not necessary to transmit 0x65[0] = 0x0. Coefficient writing takes about 100μs.100μs should not change an address setup and several 24-bit setup after coefficient write-in execution.

(ex) When 0x3DEDE7 is written, same L/Rch, 12band BQ1 b0
1. 0x61 = 0x00 (12band BQ1 b0 is appointed)
2. 0x62 = 0x3D (Upper [23:16] is setting)
3. 0x63 = 0xED (Middle [15:8] is setting)
4. 0x64 = 0xE7 (Lower [7:0] is setting)
5. 0x65 = 0x01 (Coefficient transfer)*

*After completion of writing coefficients this register is cleared automatically.
6. 100μs or more wait

2-1-2 Read-back sequence (It sets up in number order)

1. Address setting (0x61) . Please refer to Table 1.
2. Setting of a read-back register address (0xD0)
3. Read-back of the 24bit coefficient upper[23:16]bit (0x66[7:0])
4. Read-back of the 24bit coefficient middle[15:8]bit (0x67[7:0])
5. Read-back of the 24bit coefficient lower[7:0]bit (0x68[7:0])

2-1-3 When the coefficient of PEQ is set up directly and a soft transition is performed
1. Set PEQ coefficient to soft transition address whose address is 0x50-0x54. Please refer to Table1.
   Since in the case of 0x60[4] = 0x1(Enable L/R independent setting) and 0x53 [5:4] = 0x0 a soft transition is carried out and it is set to LR simultaneously, please write a coefficient in both LR address.
   In the case of 0x53[5:4] = 0x1, coefficient is set to only Lch address.
   In the case of 0x53[5:4] = 0x2, coefficient is set to only Rch address.
2. Select PEQ Band that is performed soft transition by setting 0x51[4:0] address.(Refer to chapter 1-4)
3. 0x58[0] = 0x1 : Start soft transition (After the completion of soft transition this register is automatically cleared.)
4. Wait soft transition completion (It depend on soft transition time setting), or read command 0x59 [0], and stand by until it is cleared.

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Table1. Specified coefficient

0x61[6:0]	Destination	0x61[6:0]	Destination	0x61[6:0]	Destination
0x00	12BandBQ1 b0	0x23	12BandBQ8 b0	0x46	DRC2_1 b0
0x01	12BandBQ1 b1	0x24	12BandBQ8 b1	0x47	DRC2_1 b1
0x02	12BandBQ1 b2	0x25	12BandBQ8 b2	0x48	DRC2_1 b2
0x03	12BandBQ1 a1	0x26	12BandBQ8 a1	0x49	DRC2_1 a1
0x04	12BandBQ1 a2	0x27	12BandBQ8 a2	0x4A	DRC2_1 a2
0x05	12BandBQ2 b0	0x28	12BandBQ9 b0	0x4B	DRC2_2 b0
0x06	12BandBQ2 b1	0x29	12BandBQ9 b1	0x4C	DRC2_2 b1
0x07	12BandBQ2 b2	0x2A	12BandBQ9 b2	0x4D	DRC2_2 b2
0x08	12BandBQ2 a1	0x2B	12BandBQ9 a1	0x4E	DRC2_2 a1
0x09	12BandBQ2 a2	0x2C	12BandBQ9 a2	0x4F	DRC2_2 a2
0x0A	12BandBQ3 b0	0x2D	12BandBQ10 b0	0x50	Smooth BQ b0
0x0B	12BandBQ3 b1	0x2E	12BandBQ10 b1	0x51	Smooth BQ b1
0x0C	12BandBQ3 b2	0x2F	12BandBQ10 b2	0x52	Smooth BQ b2
0x0D	12BandBQ3 a1	0x30	12BandBQ10 a1	0x53	Smooth BQ a1
0x0E	12BandBQ3 a2	0x31	12BandBQ10 a2	0x54	Smooth BQ a2
0x0F	12BandBQ4 b0	0x32	12BandBQ11 b0	0x55	DRC3_1 b0
0x10	12BandBQ4 b1	0x33	12BandBQ11 b1	0x56	DRC3_1 b1
0x11	12BandBQ4 b2	0x34	12BandBQ11 b2	0x57	DRC3_1 b2
0x12	12BandBQ4 a1	0x35	12BandBQ11 a1	0x58	DRC3_1 a1
0x13	12BandBQ4 a2	0x36	12BandBQ11 a2	0x59	DRC3_1 a2
0x14	12BandBQ5 b0	0x37	12BandBQ12 b0	0x5A	DRC3_2 b0
0x15	12BandBQ5 b1	0x38	12BandBQ12 b1	0x5B	DRC3_2 b1
0x16	12BandBQ5 b2	0x39	12BandBQ12 b2	0x5C	DRC3_2 b2
0x17	12BandBQ5 a1	0x3A	12BandBQ12 a1	0x5D	DRC3_2 a1
0x18	12BandBQ5 a2	0x3B	12BandBQ12 a2	0x5E	DRC3_2 a2
0x19	12BandBQ6 b0	0x3C	DRC1_1 b0		
0x1A	12BandBQ6 b1	0x3D	DRC1_1 b1		
0x1B	12BandBQ6 b2	0x3E	DRC1_1 b2		
0x1C	12BandBQ6 a1	0x3F	DRC1_1 a1		
0x1D	12BandBQ6 a2	0x40	DRC1_1 a2		
0x1E	12BandBQ7 b0	0x41	DRC1_2 b0		
0x1F	12BandBQ7 b1	0x42	DRC1_2 b1		
0x20	12BandBQ7 b2	0x43	DRC1_2 b2		
0x21	12BandBQ7 a1	0x44	DRC1_2 a1		
0x22	12BandBQ7 a2	0x45	DRC1_2 a2		

When L/R independent, Lch:0x61[7]=0x0, Rch:0x61[7]=0x1.
When L/R is same, 0x61[7] is not effective.

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3. The mute function by a terminal

BM28720MUV has a mute function of audio DSP by a terminal.
It is possible to perform mute of the output from Audio DSP by setting a MUTEX terminal to low.

Transition time setting at the time of mute is as follows.

Smooth transition mute time setting
The transition time when changing to a mute state is selected.
The soft transition time at the time of mute release is 10.7ms fixed.

Default = 0x3 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x15 [1:0]	0x0	10.7ms
	0x1	21.4ms
	0x2	42.7ms
	0x3	85.4ms

0x15[1:0] Mute time setting
It is only operated by mute terminal.

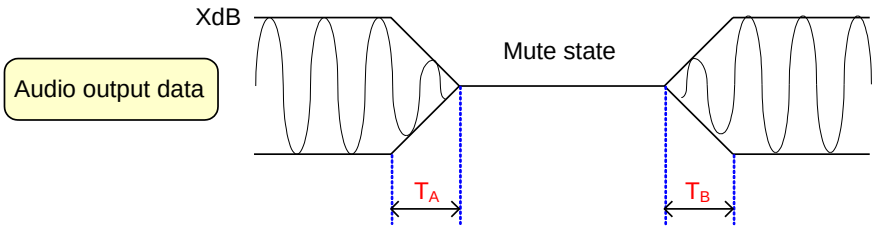


Figure 64.

0x15[1:0] setting

Command	T_A	T_B
0x0	10.7ms	10.7ms
0x1	21.4ms	10.7ms
0x2	42.7ms	10.7ms
0x3	85.4ms	10.7ms

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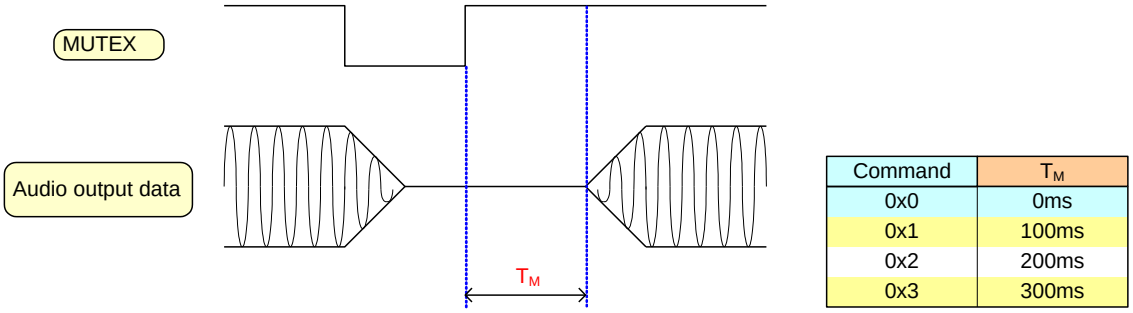
Smooth transition mute release time setting

Time after detecting mute release until it actually begins mute release operation is set up.

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x15 [5:4]	0x0	0ms
	0x1	100ms
	0x2	200ms
	0x3	300ms

Operation of mute delay 0x15[5:4]



Command	T_M
0x0	0ms
0x1	100ms
0x2	200ms
0x3	300ms

Figure 65.

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4. Small signal input detection function

There is a function which detects the audio data input of a non-signal or a small signal. This function is used in order to reduce the standby power consumption of an audio set. Setting of a detection level and detection time can be performed.
If the signal below a setting detection level continues in both low channel and R channel, a small signal detection flag will become "high". A detection result can be read from command 0x72 [0].
The point which acts as a monitor of the small signal becomes input data of audio DSP block.

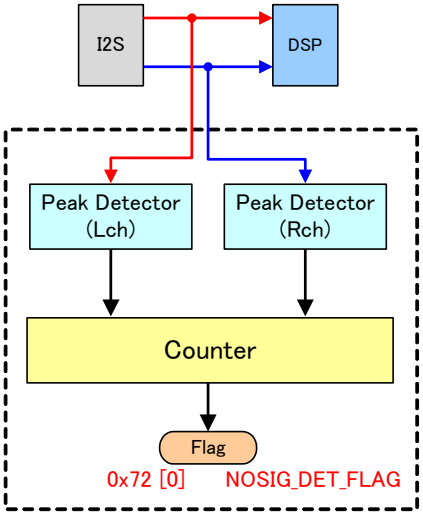


Figure 66.

Detection level setting

Default = 0x00 *Blue square means initial value.

Select Address	Explanation of operation
0x70 [4:0]	

Value	Level	Value	Level	Value	Level
0x00	-103dB	0x08	-77dB	0x10	-69dB
0x01	-93dB	0x09	-76dB	0x11	-68dB
0x02	-91dB	0x0A	-75dB	0x12	-67dB
0x03	-87dB	0x0B	-74dB	0x13	-66dB
0x04	-84dB	0x0C	-73dB	0x14	-65dB
0x05	-80dB	0x0D	-72dB	0x15	-64dB
0x06	-79dB	0x0E	-71dB	0x16	-62dB
0x07	-78dB	0x0F	-70dB	0x17	-60dB

Detection time setting

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x71 [1:0]	0x0	42.7ms
	0x1	85.4ms
	0x2	170.7ms
	0x3	341.4ms

* Sampling frequency is value of Fs = 48kHz. In the case of Fs = 44.1kHz, it will be about 1.09 times the setting value.

Detection flag read-back

Read Only

Select Address	Value	Explanation of operation
0x72 [0]	0x0	Undetected
	0x1	Detecting

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5. Clock stop detection and detection of BCLK frequency begin too low or too high or asynchronous state detection

5-1. Clock stops detection

BM28720MUV needs some clock source for generating proper clock to process Audio data.
By stopping these cock sources, these clocks to process Audio data also stop.
To prevent noise sounds, we need to detect BCLK or LRCLK stop condition.
As we detect stop flag that is to be valid, output is gone to mute state (mute instantly).

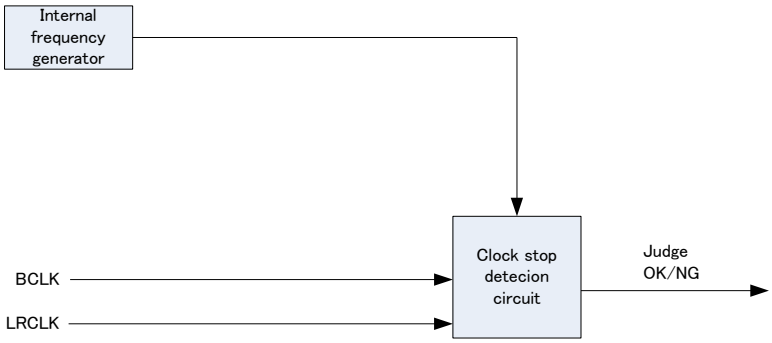


Figure 67.

Each detect condition is set by below command. We can check detected result by reading back flag register.
These flags are cleared only by sending specified commands.

LRCLK stop detection time

Default = 0x2 *Blue square means initial value.

Select Address	Value	Operation
LRCLK 0x07 [2:0]	0x0	10μs to 20μs
	0x1	20μs to 40μs
	0x2	50μs to 100μs
	0x3	100μs to 200μs
	0x4	200μs to 400μs
	0x5	300μs to 600μs
	0x6	400μs to 800μs
	0x7	500μs to 1000μs

※Detection time has the above-mentioned variation within the limits.

BCLK stop detection time

Default = 0x0 *Blue square means initial value.

Select Address	Value	Operation
BCLK 0x08 [6:4]	0x0	10μs to 20μs
	0x1	20μs to 40μs
	0x2	50μs to 100μs
	0x3	100μs to 200μs
	0x4	200μs to 400μs
	0x5	300μs to 600μs
	0x6	400μs to 800μs
	0x7	500μs to 1000μs

※Detection time has the above-mentioned variation within the limits.

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Stop detection flag read back register

Read Only

Select Address	Value	Operation
0x09 [5]	0x0	Normal
	0x1	Detection of LRCLK stop flag
0x09 [4]	0x0	Normal
	0x1	Detection of BCLK stop flag

Stop detection flag clear register

Write Only

Select Address	Operation
0x09 [1]	LRCLK stop detection flag is cleared by writing 1.
0x09 [0]	BCLK stop detection flag is cleared by writing 1.

※When using a clock error auto return function (P.59), this flag is cleared automatically.

LRCLK stop flag valid or invalid selection

Default = 0x1 *Blue square means initial value.

Select Address	Value	Operation
0x07 [3]	0x0	Valid
	0x1	Invalid

BCLK stop flag valid or invalid selection

Default = 0x0 *Blue square means initial value.

Select Address	Value	Operation
0x08 [7]	0x0	Valid
	0x1	Invalid

5-2. Synchronous blank detection

As for synchronous blank detecting function, it detects as synchronous blank error when it counts between the rising edges of LRCK with internal clock (49.152MHz), and it shifts more than the definite value, and whether PLL is normally locked is judged.

Input sampling frequency	32kHz,44.1kHz,48kHz
Count value (Start of counting from 0)	1023

As for the detection result, reading from the register is possible. Register value is not cleared until a clear command is transmitted even if the state of the clock returns normally. Moreover, the setting of the detection approval frequency is also possible, and if the error counts more than the predetermined number is detected, the flag (0x06[1]) becomes 1.

Synchronous blank flag reading register

Read Only

Select Address	Value	Explanation of operation
0x06 [1]	0x0	Normal
	0x1	Detect synchronous error

Synchronous blank flag clear register

Write Only

Select Address	Explanation of operation
0x06 [0]	When 1 is written, the synchronous blank flag is cleared.

* When using a clock error auto return function (P.59), this flag is cleared automatically.

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Synchronous blank count setting

Default = 0x2 *Blue square means initial value.

Select Address	Explanation of operation
0x06 [6:4]	Please set more than 1.

5-3. BCLK high or low speed detection

BCLK high or low speed detection function is to judge BCLK speed being too high or low by measuring by using internal clock (12MHz to 25MHz).
When using BCLK speed detection, speed failure detection can be more correctly performed by setting a command according to inputted sample rate.
When you use error detection function, please set up the sample rate by setting address 0x0C[1:0]. A high speed and the low-speed detection flag can be set up valid or invalid respectively, and if the error is detected, mute (mute instantly) will be carried out.

Valid or invalid frequency value setting up by 0x0C[1:0] command.

Default = 0x0 *Blue square means initial value.

Select Address	Value	Operation
0x0A [3]	0x0	Valid
	0x1	Invalid

Setting of sampling rate
Default = 0x0 *Blue square means initial value.

Select Address	Value	Operation
0x0C [1:0]	0x0	48kHz
	0x1	44.1kHz
	0x2	32kHz

The constraints of a high speed or a low-speed condition
Default = 0x0 *Blue square means initial value.

Select Address	Value	Operation
0x0A [2]	0x0	±10%

We can check detection result by reading back.
The result judged that is once unusual is not cleared until it transmits a clear command, even if the condition of a clock returns to normal. We can set up
We can set up the constraints of the count of formation, and it does not set a flag until it detects it by count continuation.

BCLK high speed flag

Read Only

Select Address	Value	Operation
0x0A [1]	0x0	Normal
	0x1	High speed detection flag

BCLK low speed flag

Read Only

Select Address	Value	Operation
0x0B [1]	0x0	Normal
	0x1	Low speed detection flag

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High speed detection clear register

Write Only

Select Address	Operation
0x0A [0]	If 1 is written in, a high speed detection flag will be cleared.

※When using a clock error auto return function (P.59), this flag is cleared automatically.

Low speed detection clear register

Write Only

Select Address	Operation
0x0B [0]	If 1 is written in, a high speed detection flag will be cleared.

※When using a clock error auto return function (P.59), this flag is cleared automatically.

A constraint of the count of judging with high speed flag detection

Default = 0x2 *Blue square means initial value.

Select Address	Operation
0x0A [6:4]	Please set more than 1.

A constraint of the count of judging with low speed flag detection

Default = 0x2 *Blue square means initial value.

Select Address	Operation
0x0B [6:4]	Please set more than 1.

High speed detection flag valid or invalid

Default = 0x0 *Blue square means initial value.0x0h

Select Address	Value	Operation
0x0A [7]	0x0	Valid
	0x1	Invalid

Low speed detection flag valid or invalid

Default = 0x0 *Blue square means initial value.

Select Address	Value	Operation
0x0B [7]	0x0	Valid
	0x1	Invalid

The frequency range of BCLK by which high speed detection or low speed detection is carried out becomes below.

Setting1	Settin2	Low detection lowest frequency (MHz)	High detection highest frequency (MHz)
64fs BCLK(0x03[5:4]=0x0)	48kHz(0x0C[1:0]=0x0)	1.28	7.13
	44.1kHz(0x0C[1:0]=0x1)	1.21	6.55
	32kHz(0x0C[1:0]=0x2)	0.88	4.76
48fs BCLK(0x03[5:4]=0x1)	48kHz(0x0C[1:0]=0x0)	0.96	5.35
	44.1kHz(0x0C[1:0]=0x1)	0.91	4.92
	32kHz(0x0C[1:0]=0x2)	0.66	3.57
32fs BCLK(0x03[5:4]=0x2)	48kHz(0x0C[1:0]=0x0)	0.64	3.56
	44.1kHz(0x0C[1:0]=0x1)	0.60	3.28
	32kHz(0x0C[1:0]=0x2)	0.44	2.38

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6. Auto recovery from clock error function

If clock error is detected, immediately output is muted.
In that case, if the clock error auto return function is enabled, when it returns to a normal input, a mute condition will be canceled automatically.
If the clock error auto return function is OFF, it is necessary to clear these error flag manually.
Since it is invalid at initial state, we recommend to send 0x0D[6] = 0x1 and to enable auto recovery function.

Valid or invalid auto recover from clock error

Default = 0x0 *Blue square means initial value.

Select Address	Value	Operation
0x0D [6]	0x0	Invalid
	0x1	Valid

Each error flag can be read from the following addresses. When 1 is read from a read address, the error flag stands. Error flag is not cleared automatically until this register is cleared manually.

Error flag read register

Select Address	Operation
0x0E [6]	Asynchronous flag
0x0E [4]	LRCLK stop flag
0x0E [3]	BCLK stop flag
0x0E [2]	BCLK high speed detection flag
0x0E [1]	BCLK low speed detection flag

7. The wake-up Procedure of power-up

It recommends starting power-up in the following Procedures.

1. Power up
   Wait over 10ms
2. Release reset(RSTX=H)
   Wait over 1ms
3. 0x0C[1:0]=0x* : Sampling rate(Please set up 0x0 in the case of 48kHz, set up 0x1 in the case of 44.1kHz and 0x02 in 32kHz.)
   Please input BCLK and LRCLK
4. 0xE9=0x10 : changing clock to normal state
   Wait over 100ms
5. 0x01=0x00 : Set RAM clear OFF
6. 0x0D=0x40 : Valid auto recover from clock error
7. 0x0E=0x00 : Clear error flag
8. 0x92=0x11 : PWM setting1
9. 0x93=0x1C : PWM setting2
10. 0x94=0x15 : PWM setting3
11. 0x95=0x04 : PWM setting4
12. Please set up DSP function such as volume, PEQ, DRC, and Scaler etc.
13. MUTEX=high : Release mute

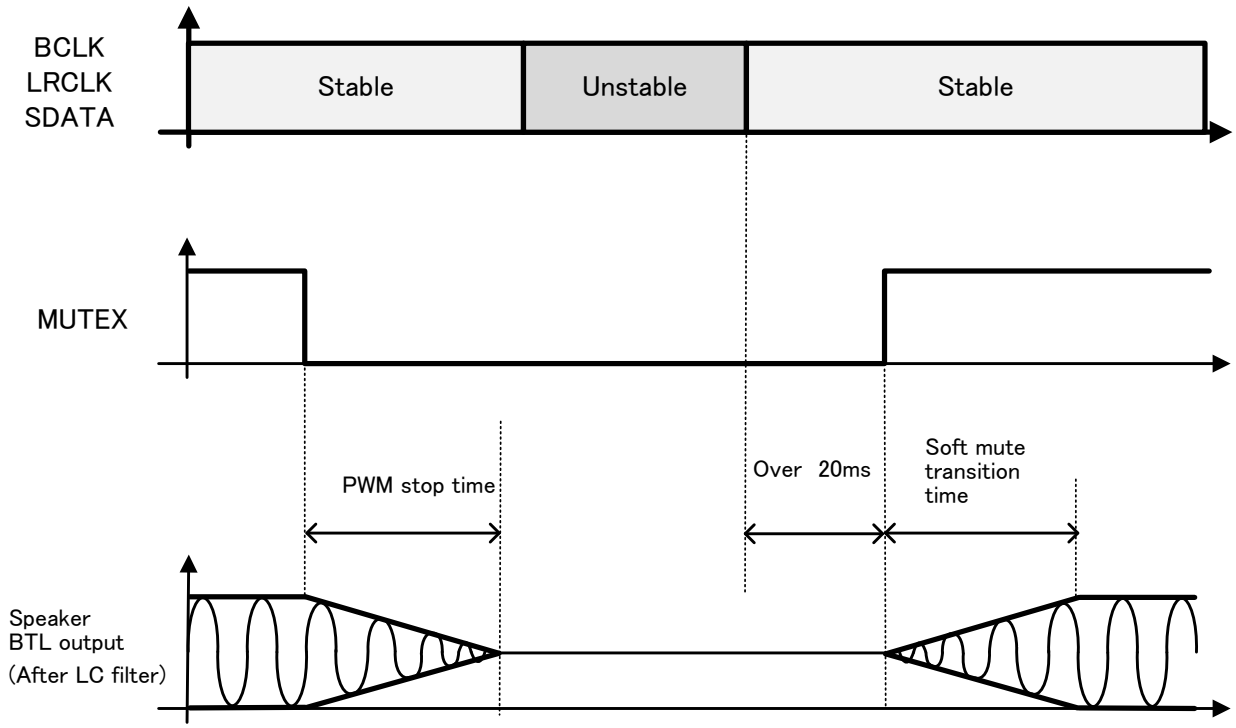
* The wait time, Twait, is necessary between 2 and 13.(Please refer to P15 for Twait)

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8. The operating procedure in a status with an unstable clock

In the period which I^2S input may become unstable, please set to MUTEX=low and carry out mute.

1. Set MUTEX=low
2. Please wait over 20ms after stabilizing I^2S input.
2. Set MUTEX=high



(Note 1)When clock stop was detected, mute release procedure world follow clock stop error release condition.

Figure 68.

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9. I²S Data output select

Output I²S data signal From SDATAO (pin12). That SDATAO synchronize to inputted LRCK and BCK signal.
And enable to select output SDATA signal as shown below.
Whatever output is selected, hard clip is processed.

SDATAO output select

Default = 0x0 *Blue square means initial value.

Select Address	Value	Explanation of operation
0x78 [6:4]	0x0	DSP output (point1)
	0x1	DSP input (pont2)
	0x2	Pre Scaler output (point3)
	0x3	Mixer output (point4)
	0x4	12 Band PEQ output (point5)
	0x5	Fine Master Volume output (point6)
	0x6	No use
	0x7	Fine Post Scaler output (point7)

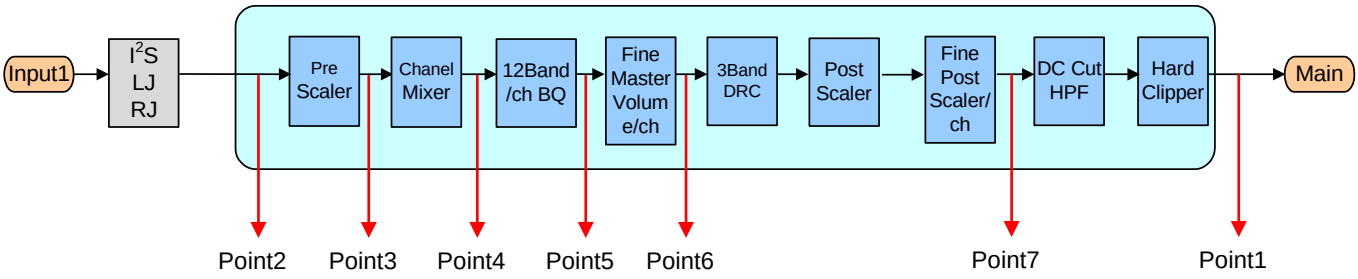


Figure 69.

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Application Circuit Example1 (Stereo BTL output, R_L=8Ω, Vcc=10V to 18V)

・When using at Vcc>18V, fc of the LC filter should be lowered to about 60kHz and decrease the influence of LCR resonance using application circuit. Please refer 5) Output LC Filter Circuit (Vcc>18V)

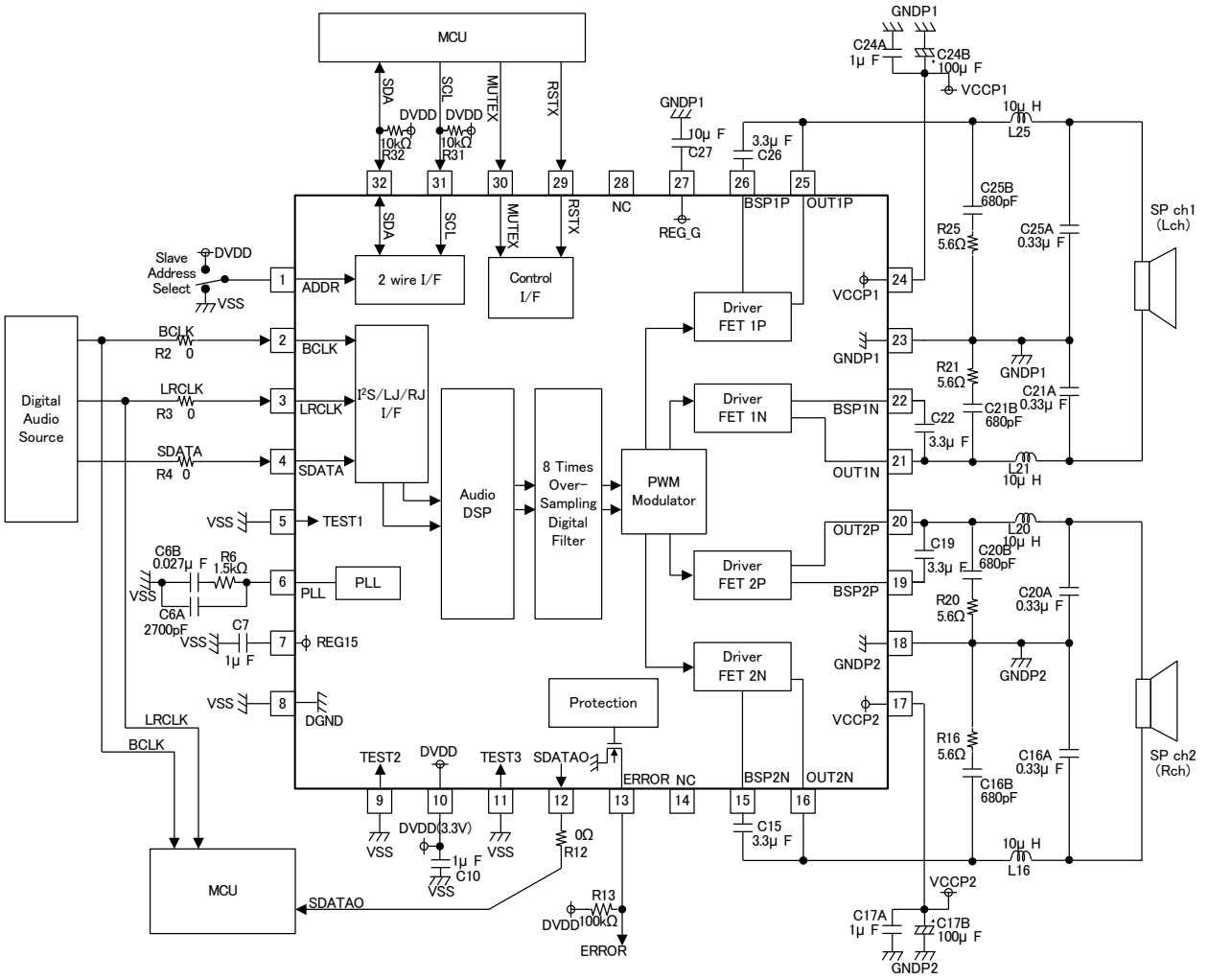


Figure 70.

BOM list1(Stereo BTL output, R_L=8Ω, Vcc=10V to 18V)

Parts	Qty	Parts No.	Description	Company	Product No.
Inductor	4	L16, L20, L21, L25	10μH / (±20%) / 7.6mm×7.6mm	TOKO	B1047AS-100M
Resistor	4	R16, R20 R21, R25	5.6Ω / 1/10W / J(±5%) / 1.6mm×0.8mm	ROHM	MCR03EZPJ5R6
	1	R6	1.5kΩ / 1/16W / F(±1%) / 1.0mm×0.5mm		MCR01MZPF1501
	2	R31, R32	10kΩ / 1/16W / J(±5%) / 1.0mm×0.5mm		MCR01MZPJ103
	4	R2, R3, R4, R12	0Ω / 1/10W / J(±5%) / 1.6mm×0.8mm		MCR03EZPJ000
	1	R13	100kΩ / 1/16W / J(±5%) / 1.0mm×0.5mm		MCR01MZPJ104
Capacitor	4	C16B, C20B C21B, C25B	680pF / 50V / B(±10%) / 1.6mm×0.8mm	MURATA	GRM188B11H681KA01
	1	C6A	2700pF / 6.3V / B(±10%) / 0.6mm×0.3mm		GRM033B10J272KA01
	1	C6B	0.027μF / 6.3V / B(±10%) / 0.6mm×0.3mm		GRM033B10J273KE01
	4	C16A, C20A, C21A, C25A,	0.33μF / 50V / B(±10%) / 2.0mm×1.25mm		GRM219B31H334KA87
	2	C17A, C24A (Note 1)	1μF / 50V / B(±10%) / 2.0mm×1.25mm		GRM21BB31H105KA12
	4	C15, C19, C22, C26	3.3μF / 16V / B(±10%) / 1.6mm×0.8mm		GRM188B31A335KE15
	2	C7, C10	1μF / 10V / B(±10%) / 1.6mm×0.8mm		GRM185B31A105KE25
	1	C27	10μF / 10V / B(±10%) / 1.6mm×0.8mm		GRM188B31A106KE69
	2	C17B, C24B	100μF / 35V / (±20%) / φ6.3mm×11.2mm	PANASONIC	ECA1VMH101

(Note 1) Please put the C17A and C24A near the VCCP1 and VCCP2 pins on the board.

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Application Circuit Example2 (Monaural BTL output, R_L=8Ω, Vcc=10V to 18V)

・When using at Vcc>18V, fc of the LC filter should be lowered to about 60kHz and decrease the influence of LCR resonance using application circuit. Please refer 5) Output LC Filter Circuit (Vcc>18V)

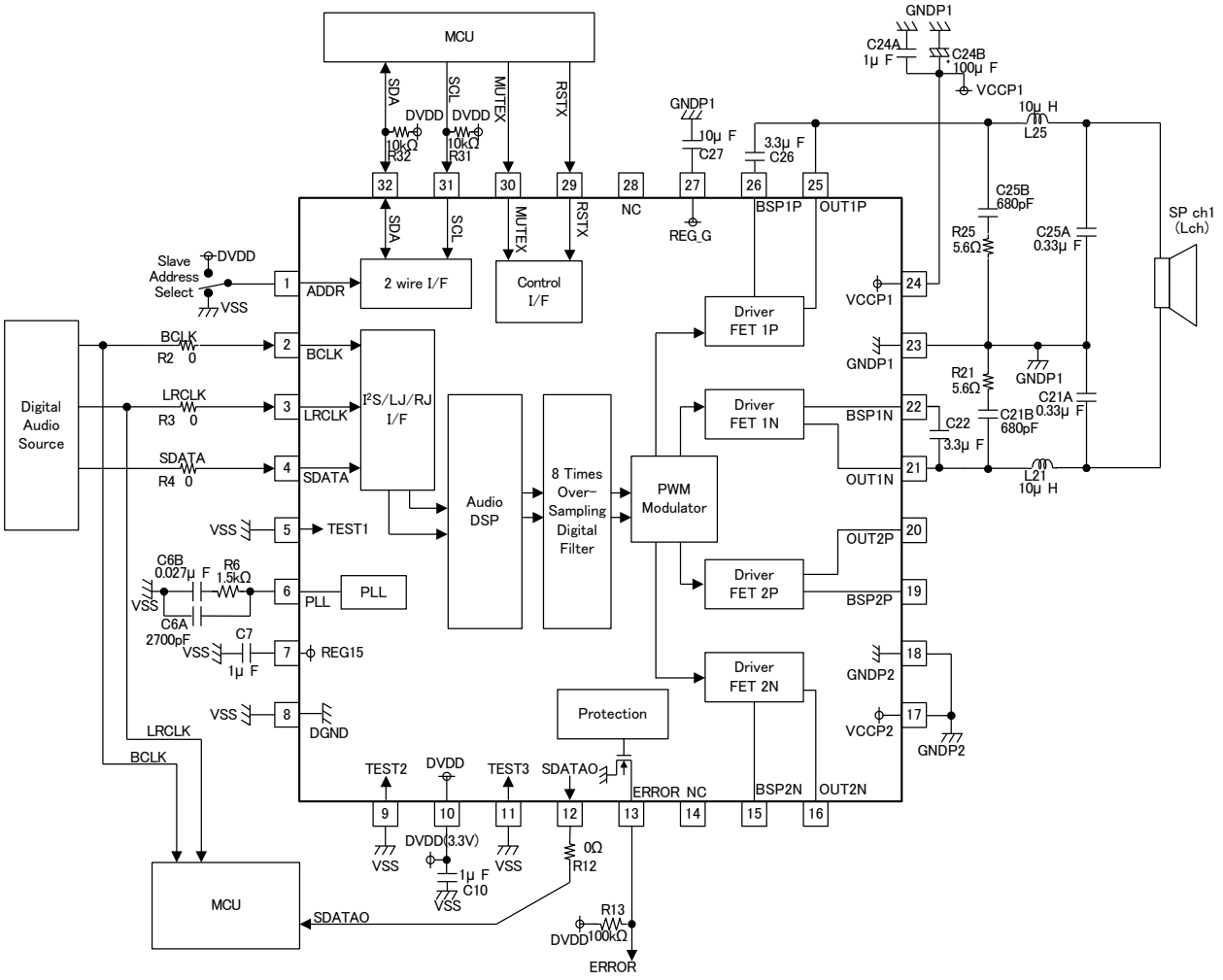


Figure 71.

BOM list2(Monaural BTL output, R_L=8Ω, Vcc=10V to 18V)

Parts	Qty	Parts No.	Description	Company	Product No.
Inductor	2	L21, L25	10μH / (±20%) / 7.6mm×7.6mm	TOKO	B1047AS-100M
Resister	2	R21, R25	5.6Ω / 1/10W / J(±5%) / 1.6mm×0.8mm	ROHM	MCR03EZPJ5R6
	1	R6	1.5kΩ / 1/16W / F(±1%) / 1.0mm×0.5mm		MCR01MZPF1501
	2	R31, R32	10kΩ / 1/16W / J(±5%) / 1.0mm×0.5mm		MCR01MZPJ103
	4	R2, R3, R4, R12	0Ω / 1/10W / J(±5%) / 1.6mm×0.8mm		MCR03EZPJ000
	1	R13	100kΩ / 1/16W / J(±5%) / 1.0mm×0.5mm		MCR01MZPJ104
Capacitor	2	C21B, C25B	680pF / 50V / B(±10%) / 1.6mm×0.8mm	MURATA	GRM188B11H681KA01
	1	C6A	2700pF / 6.3V / B(±10%) / 0.6mm×0.3mm		GRM033B10J272KA01
	1	C6B	0.027μF / 6.3V / B(±10%) / 0.6mm×0.3mm		GRM033B10J273KE01
	2	C21A, C25A	0.33μF / 50V / B(±10%) / 2.0mm×1.25mm		GRM219B31H334KA87
	1	C24A (Note 1)	1μF / 50V / B(±10%) / 2.0mm×1.25mm		GRM21BB31H105KA12
	2	C22, C26	3.3μF / 16V / B(±10%) / 1.6mm×0.8mm		GRM188B31A335KE15
	2	C7, C10	1μF / 10V / B(±10%) / 1.6mm×0.8mm		GRM185B31A105KE25
	1	C27	10μF / 10V / B(±10%) / 1.6mm×0.8mm		GRM188B31A106KE69
	1	C24B	100μF / 35V / ±20% / φ6.3mm×11.2mm	PANASONIC	ECA1VMH101

(Note 1) Please put the C24A near the VCCP1 pins on the board.

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Selection of Components Externally Connected (Vcc=10V to 18V)

1) Output LC Filter Circuit

An output filter is required to eliminate radio-frequency components exceeding the audio-frequency region supplied to a load (speaker). Because this IC uses sampling clock frequency 384kHz(fs=48kHz) in the output PWM signals, the high-frequency components must be appropriately removed.

This section takes an example of an LC type LPF shown below, in which coil L and capacitor C compose a differential filter with an attenuation property of -12dB/oct. A large part of switching currents flow to capacitor C, and only a small part of the currents flow to speaker R_{L1}. This filter reduces unwanted emission this way. In addition, coil L and capacitor Cg composes a filter against in-phase components, reducing unwanted emission further.

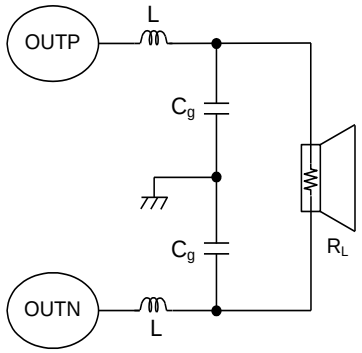


Figure 72.

Following presents output LC filter constants with typical load impedances.

R_L	L	C_g
4Ω	10μH	1μF
6Ω	10μH	0.47μF
8Ω	10μH	0.33μF

Use coils with a low direct-current resistance and with a sufficient margin of allowable currents. A high direct-current resistance causes power losses. In addition, select a closed magnetic circuit type product in normal cases to prevent unwanted emission.

Use capacitors with a low equivalent series resistance, and good impedance characteristics at high frequency ranges (100kHz or higher). Also, select an item with sufficient withstand voltage because flowing massive amount of high-frequency currents is expected.

2) The value of the LC filter circuit computed equation

The output LC filter circuit of BM28720MUV is as it is shown in Figure 73. The LC filter circuit of Figure 73 is thought to substitute it like Figure 74 on the occasion of the computation of the value of the LC filter circuit.

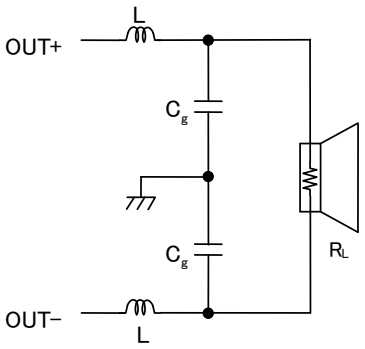


Figure 73. Output LC filter 1

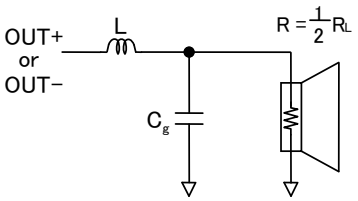


Figure 74. Output LC filter 2

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The transfer function H(s) of the LC filter circuit of Figure 74 becomes the following.

$$H(s) = \frac{\frac{1}{LC_g}}{s^2 + \frac{1}{C_g R}s + \frac{1}{LC_g}} = \frac{\omega^2}{s^2 + \frac{\omega}{\mathrm{Q}}s + \omega^2}$$

The ω and Q become the followings here.

$$\omega^2 = \frac{1}{LC_g} \qquad \omega = 2\pi f_C \qquad f_C = \frac{1}{2\pi\sqrt{LC_g}}$$

$$Q = R\sqrt{\frac{C_g}{L}} = \frac{1}{2}R_L\sqrt{\frac{C_g}{L}}$$

Therefore, L and C_g become the followings.

$$L = \frac{1}{\omega^2 C_g} = \frac{R_L}{4\pi f_C Q} \qquad C_g = \frac{Q}{\omega R} = \frac{Q}{\pi f_C R_L}$$

The R_L and L should be made known, and f_c is set up, and C_g is decided.

3) The settlement of the L value of the coil

For selection of the L value of a coil, please consider side effect as shown below.

①When L value was made small.
(1) Circuit electric currents increase without a signal. And, efficiency in the low output gets bad.
(2) Direct current resistance value is restrained small when the coil of other L value and size are made the same. Therefore, maximum output is easy to take out. And, it can be used in the low power supply voltage because DC electric current (allowable electric current) value can be taken greatly.

②When L value was made large.
(1) Circuit electric current is restrained low without a signal. Efficiency in the low output improves.
(2) Direct current resistance value grows big when the coil of other L value and size are made the same. Therefore, maximum output is hard to take out. And, because it becomes small, use becomes difficult 【 the DC electric current (allowable electric current) value 】 in the low power supply voltage, too.

4) The settlement of the f_c

As for the settlement of the fixed number of the LC filter circuit, it is taken into consideration about two points of the following, and set up.

①The PWM sampling frequency fPWM (=8f_S) of BM28720MUV is set up in 384kHz (@fS=48kHz).
It is set up with f_C < fPWM to restrain career frequency omission after the LC filter circuit.
②When fc is lowered too much, the voltage profit of the voice obi stage (especially, the neighborhood of 20kHz) declines in the speaker output frequency character of the difference movement mode.
And, the speaker output frequency character of the difference movement mode becomes the following.

R_L=8Ω				R_L=6Ω				R_L=4Ω			
L[μH]	C_g[μF]	f_c[kHz]	L[μH]	C_g[μF]	f_c[kHz]	L[μH]	C_g[μF]	f_c[kHz]	L[μH]	C_g[μF]	f_c[kHz]
10	0.1	75.32	0.40	10	0.1	51.01	0.30	10	0.1	32.19	0.20
	0.15	80.85	0.49		0.15	54.76	0.37		0.15	33.35	0.24
	0.22	86.79	0.59		0.22	56.73	0.44		0.22	34.55	0.30
	0.33	89.92	0.73		0.33	63.1	0.54		0.33	35.8	0.36
	0.47	86.79	0.87		0.47	66.68	0.65		0.47	38.37	0.43
	1.0	69.01	1.26		1.0	62.29	0.95		1.0	44.1	0.63
15	0.1	46.99	0.33	15	0.1	33.11	0.24	15	0.1	21.68	0.16
	0.15	49.66	0.40		0.15	34.36	0.30		0.15	22.08	0.20
	0.22	53.46	0.48		0.22	35.65	0.36		0.22	22.49	0.24
	0.33	57.54	0.59		0.33	38.37	0.44		0.33	22.91	0.30
	0.47	59.7	0.71		0.47	41.3	0.53		0.47	23.77	0.35
	1.0	52.75	1.03		1.0	44.67	0.77		1.0	27.47	0.52
22	0.1	30.76	0.27	22	0.1	22.49	0.20	22	0.1	14.72	0.13
	0.15	31.92	0.33		0.15	22.91	0.25		0.15	14.72	0.17
	0.22	33.73	0.40		0.22	23.77	0.30		0.22	15	0.20
	0.33	36.31	0.49		0.33	24.66	0.37		0.33	15.28	0.24
	0.47	39.08	0.58		0.47	26.06	0.44		0.47	15.56	0.29
	1.0	39.30	0.85		1.0	30.05	0.64		1.0	17.33	0.43

5) Output LC Filter Circuit (Vcc>18V)

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When using at Vcc>18V, fc of the LC filter should be lowered to about 60kHz or less and decrease the influence of LCR resonance using application circuit.

R_{L1}	L	C
4Ω	10μH	1μF
6Ω	15μH	0.47μF
8Ω	15μH	0.33μF
	22μH	0.47μF

Use coils with a low direct current resistance and with a sufficient margin of allowable currents. A high direct current resistance causes power losses. In addition, select a closed magnetic circuit type product in normal cases to prevent unwanted emission.
Use capacitors with a low equivalent series resistance and good impedance characteristics at high frequency ranges (100kHz or higher). Also, select an item with sufficient voltage rating because massive amount of high frequency currents flow is expected.

In addition, please do not place the C_{BTL} shown in Figure 75.
When considering only common mode signals, OUTP and OUTN are equal to each other and this circuit is equivalent to the circuit shown in Figure 76.
Therefore, LC resonance may occur depending on the constant of a LC filter.

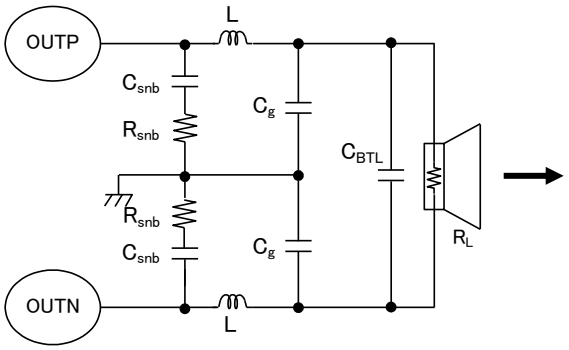


Figure 78.

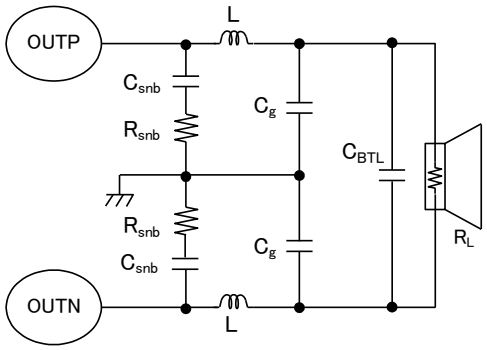


Figure 79.

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6) The settlement of the snubber

The snubber circuit must be optimized for application circuit to reduce the overshoot and undershoot of output PWM.

① Measure the ringing resonance frequency f1 of the PWM output wave shape (When it stands up.) by using FET probe in the OUT terminal. (Figure 77) The FET probe is to monitor very near pin and shorten ground lead at the time of that.
② Measure resonance frequency f2 of the ringing as a snubber circuit fixed number R=0Ω. (Only with connecting the capacitor C to GND) At this time, the value of the capacitor C is adjusted until it becomes half of the frequency (2f2=f1) of the resonance frequency f1 of ①. The value of C which it could get here is three times of the parasitic capacity C_p that a ringing is formed. ($C=3C_p$)
③ Parasitic inductance L_p is looked for at the next formula.

$$L_p = \frac{1}{(2\pi f_1)^2 C_p}$$

④ The character impedance Z of resonance is looked for from the parasitic capacity C_p and the parasitism inductance L_p at the next formula.

$$Z = \sqrt{\frac{L_p}{C_p}}$$

⑤ A snubber circuit fixed number R is set up in the value which is the same as the character impedance Z. A snubber circuit fixed number C is set up in the value of 4-10 times of the parasitic capacity C_p. ($C=4C_p$ to $10C_p$)
Decide it with trade-off with the character because switching electric currents increase when the value of C is enlarged too much.

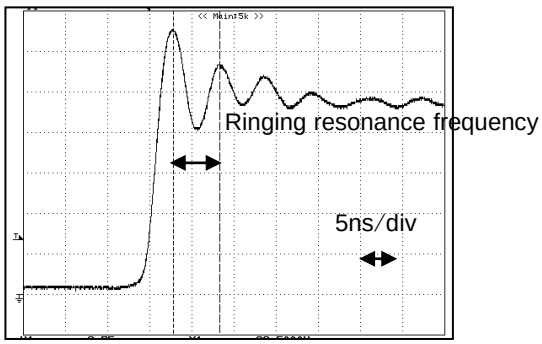


Figure 77. PWM Output waveform
(Measure of ringing resonance frequency

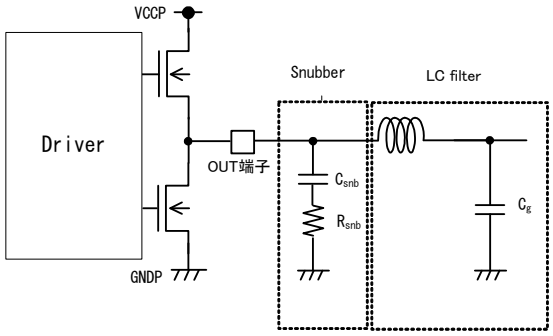


Figure 78. Snubber schematic

Following presents snubber filter constants with the recommendation value at ROHM 4 layer board.

R_L	C_{snb}	R_{snb}
4Ω	680pF ~ 1200pF, 50V B(±10%)	5.6Ω, 1/10W J(±5%)
6Ω	680pF ~ 1200pF, 50V B(±10%)	5.6Ω, 1/10W J(±5%)
8Ω	680pF ~ 1200pF, 50V B(±10%)	5.6Ω, 1/10W J(±5%)

7) Operating condition with the application component

Parameter	Parts No.	Limit			Unit Min	Conditions
		Min	Typ	Max		
Capacitor for BSP	C15, C19, C22, C26	2.0 (Note 1)	3.3	4.5 (Note 2)	μF	Recommend characteristics, 16V ceramic type capacitor
		2.0 (Note 1)	4.7	6.3 (Note 2)	μF	

(Note1) Capacitor value should not be less than a minimum in consideration of temperature characteristics and dc-bias characteristics.
(Note2) It is value in consideration of +/-10% of capacity unevenness, capacity rate of change 22%. Please use the capacitor within this limit.

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Level Diagram of Audio Signal

Level diagram of audio signal is shown the below figure. Speaker output level is depended on I^{2}S digital audio input level, DSP gain, PWM gain, BTL gain and Loss of power stage and low pass filter.
I2S input level is full-scale signal, the supply voltage of the block is DVDD, and therefore, 0dBFS is equal to DVDD voltage [Vpp]. DSP gain is set by 2 wire control variably, and -0.3dB is set at PWM Modulator block usually. At the Power stage, the PWM Modulator output is shifted PWM signal level from DVDD to VCC, and added loss of the output transistor resistance r_{DS} and DC resistance of coil r_{DC}.

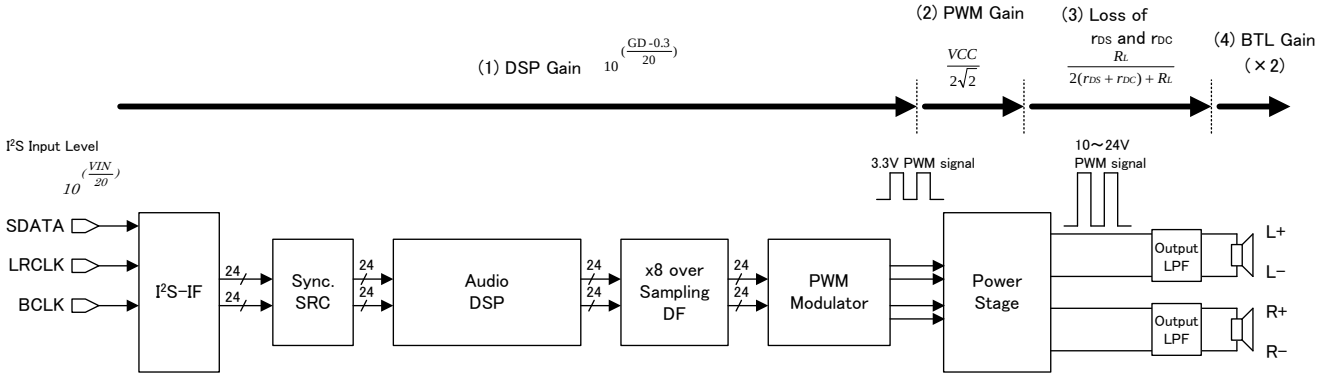


Figure 79. Level Diagram of Audio Signal

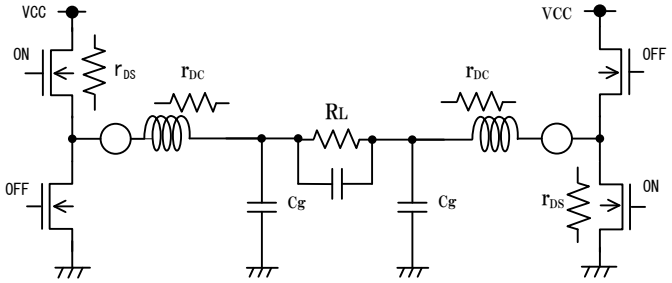


Figure 80. Output LPF circuit

In Bridge-Tied-Load (BTL) connection, the following formula gives an approximate value of output power *Po at non*-clipping output waveform:

$$P_O = \frac{(10^{VIN/20} \times 10^{(GD-0.3)/20} \times \frac{VCC}{2\sqrt{2}} \times 2 \times \frac{R_L}{2\times(r_{DS}+r_{DC})+R_L})^2}{R_L}$$

I2S Input Level / DSP Gain / PWM Gain / BTL Gain / Loss of r_{DS} and r_{DC}

VIN : I^{2}S Input level [dBFS]
GD : DSP gain [dB]
VCC : Power supply voltage of Power stage [V]
DVDD : Power supply voltage of DSP block [V]
RL : Load impedance [Ω]
r_{DS} : Turn-on resistance of output MOS Tr. [Ω]
(typ.=160m Ω)
r_{DC} : DC resistance of output LPF coil [Ω]

If the circuit is driven further until an output waveform is clipped, an output power higher than that without distortion is obtained. In general a clipped output is quantified where “THD+N = 1% and 10%,” and a maximum output power under that status is calculated by the following formula:

$$P_{O(1\%)} = \frac{(10^{(-0.3/20)} \times \frac{VCC}{\sqrt{2}} \times \frac{R_L}{2(r_{DS}+r_{DC})+R_L})^2}{R_L} [W]$$

$$P_{O(10\%)} = P_{O(1\%)} \times 1.25 [W]$$

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Power Dissipation

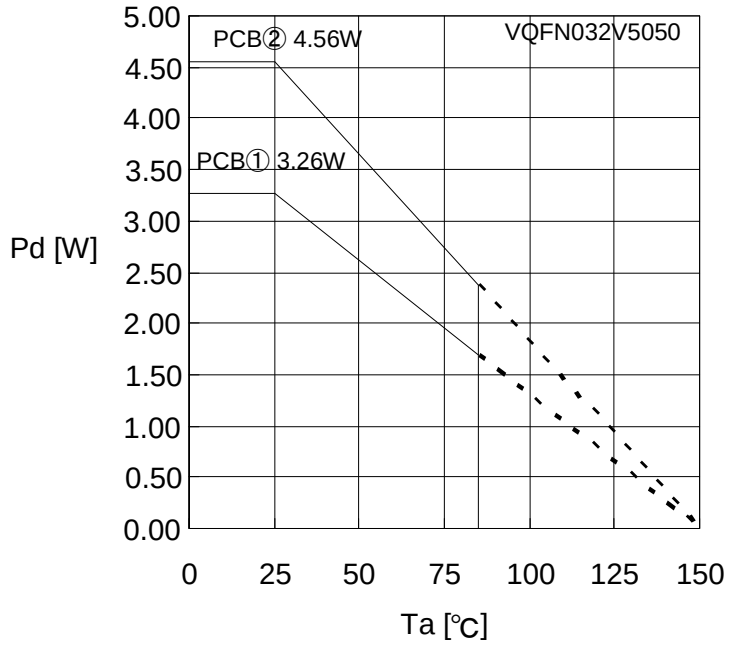


Figure 81. Allowable Power Dissipation

Measuring instrument：TH-156(Shibukawa Kuwano Electrical Instruments Co, Ltd.)
Measuring conditions：Installation on ROHM’s board
Board size：74.2mm×74.2mm×1.6mm(with thermal via on board)
Material：FR4
・The board on exposed heat sink on the back of package are connected by soldering.

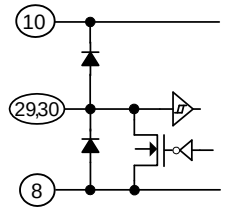
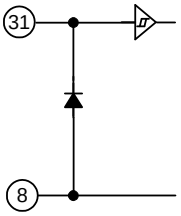
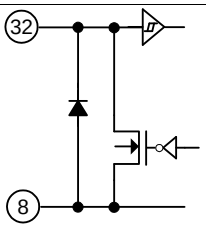
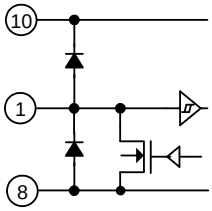
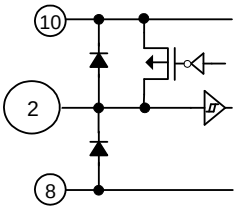
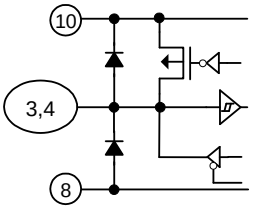
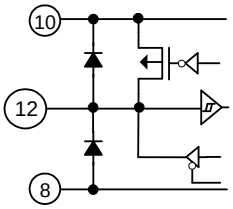
PCB1：4- layer board (Top and bottom layer back copper foil size: 20.2mm^2, 2nd and 3rd layer back copper foil size: 5505mm^2) , θja = 38.3°C/W
PCB2：4-layer board(back copper foil size: 5505mm^2), θja = 27.4°C/W

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions. This IC exposes its frame of the backside of package. Note that this part is assumed to use after providing heat dissipation treatment to improve heat dissipation efficiency. Try to occupy as wide as possible with heat dissipation pattern not only on the board surface but also the backside.
Class D speaker amplifier is high efficiency and low heat generation by comparison with conventional Analog power amplifier. However, In case it is operated continuously by maximum output power, Power dissipation (Pdiss) may exceed package dissipation. Please consider about heat design that Power dissipation (Pdiss) does not exceed Package dissipation (Pd) in average power (Poav). (Tjmax ：Maximum junction temperature=150°C, Ta ：Peripheral temperature[°C], θja ：Thermal resistance of package[°C/W], Poav：Average power[W], η：Efficiency)

Package dissipation： Pd(W)=(Tjmax - Ta)／θja
Power dissipation : Pdiss(W)= Poav ×(1／η- 1)

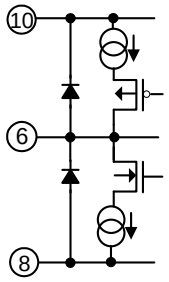
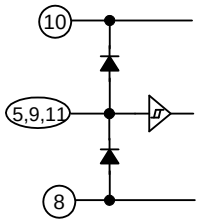
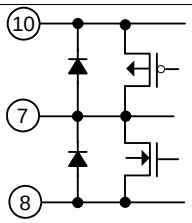
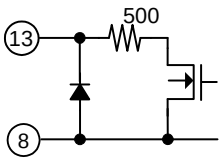
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I/O equivalence circuit (Provided pin voltages are typ. Values)

Pin No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
29 30	RSTX MUTEX	0V 0V	Reset pin for digital circuit High : Reset OFF Low : Reset ON Speaker output mute control pin High : Mute OFF Low : Mute ON	
8	DGND	0V	GND pin for Digital I/O	―
31	SCL	―	2 wire Bus control transmit clock input pin ・Please notice. Absolute Maximum Voltage is 4.5V.	
32	SDA	―	2 wire Bus control data input/output pin ・Please notice. Absolute Maximum Voltage is 4.5V.	
1	ADDR	0V	2 wire Bus control Slave address select pin Select LSB data of slave address for 2 wire Bus control.	
2	BCLK	3.3V	Digital sound bit clock input pin Input bit clock of digital audio signal.	
4 3	SDATA LRCLK	3.3V	Digital sound signal input pin Input LR clock of digital audio signal to LRCLK terminal. Input data of digital audio signal to SDATA terminal.	
12	SDATAO	3.3V	Digital sound signal output pin Output data of digital audio signal.	

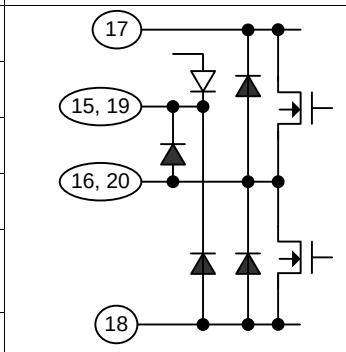
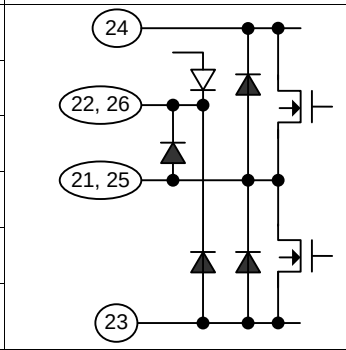
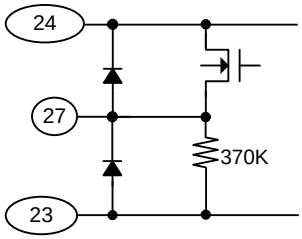
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I/O equivalence circuit (Provided pin voltages are typ. Values)

Pin No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
6	PLL	1V	PLL's filter pin Connect filter circuit for PLL.	
10	DVDD	3.3V	Power supply pin for Digital I/O.	—
5 9 11	TEST1 TEST2 TEST3	— — —	Test pin Connect VSS.	
7	REG15	1.5V	Internal power supply pin for Digital circuit Connect capacitor.	
13	ERROR	3.3V	Error flag pin H: Normal operation L: Error	
14 28	NC	—	No connection Pin	—

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I/O equivalence circuit (Provided pin voltages are typ. Values)

Pin No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
17	VCCP2	VCC	Power supply pin for ch2 PWM signal	
20	OUT2P	VCC to 0V	Output pin of ch2 positive PWM Connect output LPF.	
19	BSP2P	–	Boot-strap pin of ch2 positive Connect capacitor.	
18	GNDP2	0V	GND pin for ch2 PWM signal	
16	OUT2N	VCC to 0V	Output pin of ch2 negative PWM Please connect to Output LPF.	
15	BSP2N	–	Boot-strap pin of ch2 negative Connect capacitor.	
22	BSP1N	–	Boot-strap pin of ch1 negative Connect capacitor.	
21	OUT1N	VCC to 0V	Output pin of ch1 negative PWM Connect output LPF.	
23	GNDP1	0V	GND pin for ch1 PWM signal	
26	BSP1P	–	Boot-strap pin of ch1 positive Connect capacitor.	
25	OUT1P	VCC to 0V	Output pin of ch1 positive PWM Connect output LPF.	
24	VCCP1	VCC	Power supply pin for ch1 PWM signal	
27	REG_G	5.7V	Internal power supply pin for gate driver Connect capacitor.	

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Operational Notes

1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) Power supply lines
As return of current regenerated by back EMF of output coil happens, take steps such as putting capacitor between power supply and GND as an electric pathway for the regenerated current. Be sure that there is no problem with each property such as emptied capacity at lower temperature regarding electrolytic capacitor to decide capacity value. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.

3) GND potential (Pin 8, 18, 23)
Any state must become the lowest voltage about DGND, GNDP1 and GNDP2 terminal.

4) Input terminal
The parasitic elements are formed in the IC because of the voltage relation. The parasitic element operating causes the wrong operation and destruction. Therefore, please be careful so as not to operate the parasitic elements by impressing to input terminals lower voltage than DGND and VSS. Please do not apply the voltage to the input terminal when the power-supply voltage is not impressed.

5) Actions in strong magnetic field
Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Thermal shutdown circuit
This product is provided with a built-in thermal shutdown circuit. When the thermal shutdown circuit operates, the output transistors are placed under open status. The thermal shutdown circuit is primarily intended to shut down the IC avoiding thermal runaway under abnormal conditions with a chip temperature exceeding Tjmax = 150℃.

7) Shorts between pins and miss-installation
When mounting the IC on a board, pay adequate attention to orientation and placement discrepancies of the IC. If it is miss-installed and the power is turned on, the IC may be damaged. It also may be damaged if it is shorted by a foreign substance coming between pins of the IC or between a pin and a power supply or a pin and a GND.

8) Power supply on/off (Pin 10, 17, 24)
In case power supply is started up, RSTX(Pin 29) and MUTEX(Pin 30) always should be set Low. And in case power supply is shut down, it should be set Low likewise. Then it is possible to eliminate pop noise when power supply is turned on/off. And also, all power supply terminals should start up and shut down together.

9) ERROR terminal (Pin 13)
An error flag is outputted when Output short protection or DC voltage protection. This flag is the function which the condition of this product is shown in.

10) N.C. terminal (Pin 14, 28)
N.C. terminal (Non Connection Pin) does not connect to the inside circuit. Therefore, possible to use open.

11) TEST terminal (Pin 5, 9, 11)
TEST terminal connects with ground to prevent the malfunction by external noise.

12) Precautions for Speaker-setting
If the impedance characteristics of the speakers at high-frequency range while increase rapidly, the IC might not have stable-operation in the resonance frequency range of the LC-filter. Therefore, consider adding damping-circuit, etc., depending on the impedance of the speaker.

13) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

14) About the rush current
For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of wiring.

Status of this document

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority

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Ordering Information

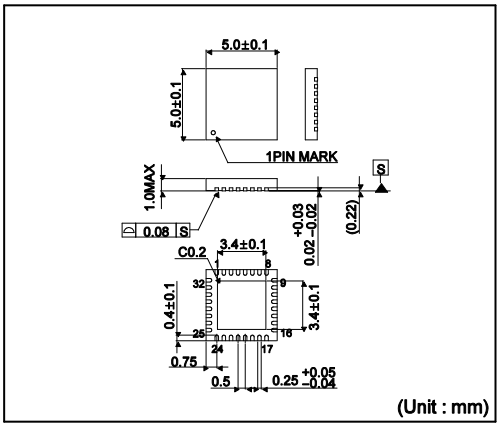
B	M	2	8	7	2	0	M	U	V	-	E2

Package
MUV:
VQFN032V5050

Packaging and forming specification
E2: Embossed tape and reel

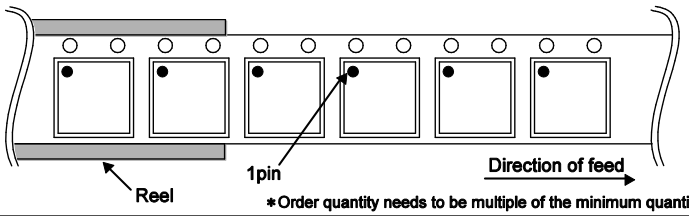
Physical Dimensions Tape and Reel Information

VQFN032V5050



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Marking Diagram

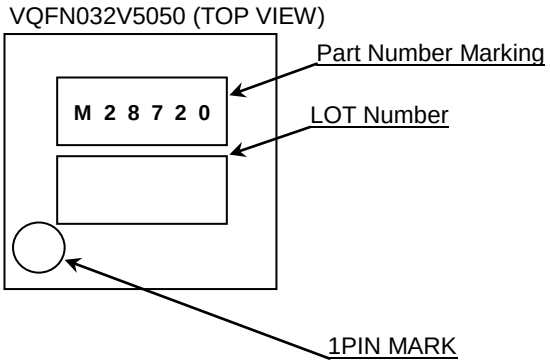


Figure 82.

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Revision History

Date	Revision	Changes
21.Oct.2013	001	First version
10.Dec.2013	002	Corrected (P.2) Corrected performance curves (P.5-7) Modified recommend constant (P.63-64, 67, 68) Deleted application circuit (P.63-64)
10.Jun.2016	003	Modify electric characteristics, condition, explanation of command Correction of errors Modify power up sequence(P.22) Modify procedure for power up(P.59)

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Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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BM28720MUV - Web Page

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Distribution Inventory

Part Number	BM28720MUV
Package	VQFN032V5050
Unit Quantity	2500
Minimum Package Quantity	2500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes