M66281FP

5120 × 8-Bit × 2 Line Memory

REJ03F0254-0200
Rev.2.00
Sep 14, 2007

Description

The M66281FP is high speed line memory that uses high performance silicon gate CMOS process technology and adopts the FIFO (First In First Out) structure consisting of 5120 words × 8 bits × 2.

Since memory is available to simultaneously output 1 line delay and 2 line delay data, the M66281FP is optimal for the compensation of data of multiple lines.

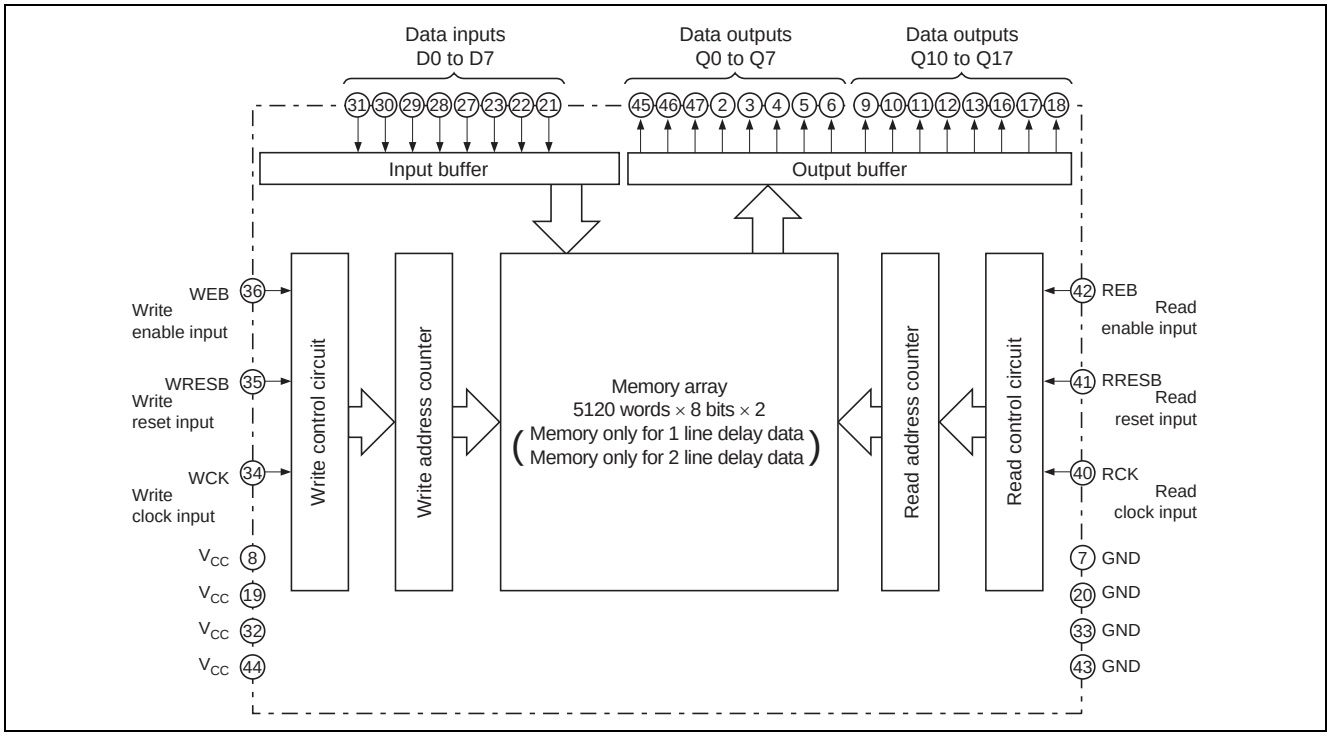
Features

- Memory configuration: 5120 words × 8 bits × 2 (dynamic memory)
- High speed cycle: 25 ns (Min)
- High speed access: 18 ns (Max)
- Output hold: 3 ns (Min)
- Reading and writing operations can be completely carried out independently and asynchronously
- Variable length delay bit
- Input/output: TTL direct connection allowable
- Output: 3 states
- Q00 to Q07: 1 line delay
- Q10 to Q17: 2 line delay

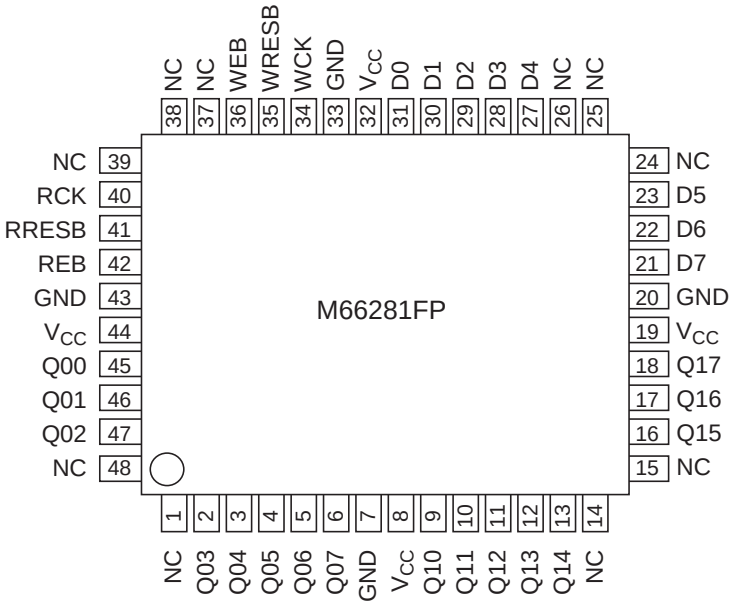
Application

Digital copying machine, laser beam printer, high speed facsimile, etc.

Block Diagram



Pin Arrangement



(Top view)

NC: No connection

Outline: PRQP0048JA-A (48P6S-A)

Absolute Maximum Ratings

(Ta = 0 to 70°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	–0.3 to +4.6	V	Value based on the GND pin
Input voltage	V_I	–0.3 to V_{CC} + 0.3	V	
Output voltage	V_O	–0.3 to V_{CC} + 0.3	V	
Power dissipation	Pd	540	mW	*
Storage temperature	Tstg	–55 to 150	°C	

Note: * Ta = 0 to 63°C. Ta > 63°C are derated at –9 mW / °C

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.15	3.6	V
Supply voltage	GND	—	0	—	V
Operating temperature	Topr	0	—	70	°C

Electrical Characteristics

(Ta = 0 to 70°C, V_{CC} = 2.7 to 3.6 V, GND = 0 V, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
High-level input voltage	V_{IH}	2.0	—	—	V		
Low-level input voltage	V_{IL}	—	—	0.8	V		
High-level output voltage	V_{OH}	V_{CC} – 0.4	—	—	V	I_{OH} = –4 mA	
Low-level output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4 mA	
High-level input current	I_{IH}	—	—	1.0	µA	$V_I = V_{CC}$	WEB, WRESB, WCK, REB, RRESB, RCK, D0 to D7
Low-level input current	I_{IL}	—	—	–1.0	µA	V_I = GND	WEB, WRESB, WCK, REB, RRESB, RCK, D0 to D7
Off-state high-level output current	I_{OZH}	—	—	5.0	µA	$V_O = V_{CC}$	
Off-state low-level output current	I_{OZL}	—	—	–5.0	µA	V_O = GND	
Average supply current during operation	I_{CC}	—	—	150	mA	$V_I = V_{CC}$, GND, Output open t_{WCK}, t_{RCK} = 25 ns	
Input capacitance	C_I	—	—	10	pF	f = 1 MHz	
Off-time output capacitance	C_O	—	—	15	pF	f = 1 MHz	

Function

When write enable input WEB is set to "L", the contents of data inputs D0 to D7 are written into memory only for 1 line delay data in synchronization with a rising edge of write clock input WCK to perform writing operation. When this is the case, the write address counter of memory only for 1 line delay data is incremented simultaneously.

When WEB is set to "H", the writing operation is inhibited and the write address counter of memory only for 1 line delay data stops.

When write reset input WRESB is set to "L", the write address counter of memory only for 1 line delay data is initialized.

When read enable input REB is set to "L", the contents of memory only for 1 line delay data are output to data outputs Q00 to Q07 and the contents of memory only for 2 line delay data are output to Q10 to Q17 in synchronization with a rising edge of read clock input RCK to perform reading operation.

When this is the case, the read address counters of memory only for 1 line delay data and memory only for 2 line delay data are incremented simultaneously.

In addition, data of Q00 to Q07 is written into memory only for 2 line delay data in synchronization with a rising edge of RCK. When this is the case, the write address counter of memory only for 2 line delay data is then incremented.

When REB is set to "H", operation for reading data from memory only for 1 line delay and from memory only for 2 line delay data is inhibited and the read address counter of each memory stops.

Outputs Q00 to Q07 and Q10 to Q17 are placed in a high impedance state. In addition, the write address counter of memory only for 2 line delay data then stops.

When read reset input RRESB is set to "L", the read address counters of memory only for 1 line delay data as well as the write address counter and read address counter of memory only for 2 line delay data are then initialized.

Switching Characteristics

(Ta = 0 to 70°C, V_{CC} = 2.7 to 3.6 V, GND = 0 V, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit
Access time	t_{AC}	—	—	18	ns
Output hold time	t_{OH}	3	—	—	ns
Output enable time	t_{OEN}	3	—	18	ns
Output disable time	t_{ODIS}	3	—	18	ns

Timing Requirements

(Ta = 0 to 70°C, V_{CC} = 2.7 to 3.6 V, GND = 0 V, unless otherwise noted)

Item	Symbol	Min	Typ	Max	Unit
Write clock (WCK) cycle	t_{WCK}	25	—	—	ns
Write clock (WCK) "H" pulse width	t_{WCKH}	11	—	—	ns
Write clock (WCK) "L" pulse width	t_{WCKL}	11	—	—	ns
Read clock (RCK) cycle	t_{RCK}	25	—	—	ns
Read clock (RCK) "H" pulse width	t_{RCKH}	11	—	—	ns
Read clock (RCK) "L" pulse width	t_{RCKL}	11	—	—	ns
Input data setup time for WCK	t_{DS}	7	—	—	ns
Input data hold time for WCK	t_{DH}	3	—	—	ns
Reset setup time for WCK/RCK	t_{RESS}	7	—	—	ns
Reset hold time for WCK/RCK	t_{RESH}	3	—	—	ns
Reset non-selection setup time for WCK/RCK	t_{NRESS}	7	—	—	ns
Reset non-selection hold time for WCK/RCK	t_{NRESH}	3	—	—	ns
WEB setup time for WCK	t_{WES}	7	—	—	ns
WEB hold time for WCK	t_{WEH}	3	—	—	ns
WEB non-selection setup time for WCK	t_{NWES}	7	—	—	ns
WEB non-selection hold time for WCK	t_{NWEH}	3	—	—	ns
REB setup time for RCK	t_{RES}	7	—	—	ns
REB hold time for RCK	t_{REH}	3	—	—	ns
REB non-selection setup time for RCK	t_{NRES}	7	—	—	ns
REB non-selection hold time for RCK	t_{NREH}	3	—	—	ns
Input pulse up/down time	tr, tf	—	—	20	ns
Data hold time*	t_H	—	—	20	ms

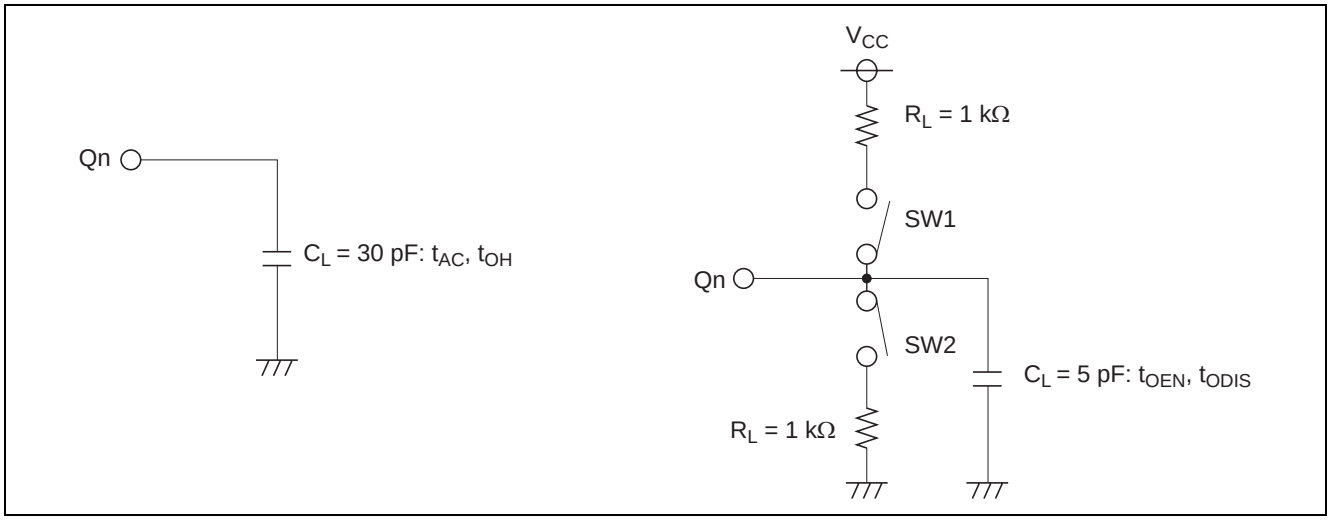
Notes: Perform reset operation after turning on power supply.

* For 1 line access, the following conditions must be satisfied:

WEB high-level period ≤ 20 ms – 5120 • t_{WCK} – WRESB low-level period

REB high-level period ≤ 20 ms – 5120 • t_{RCK} – RRESB low-level period

Switching Characteristics Measurement Circuit



Input pulse level: 0 to 3 V

Input pulse up/down time: 3 ns

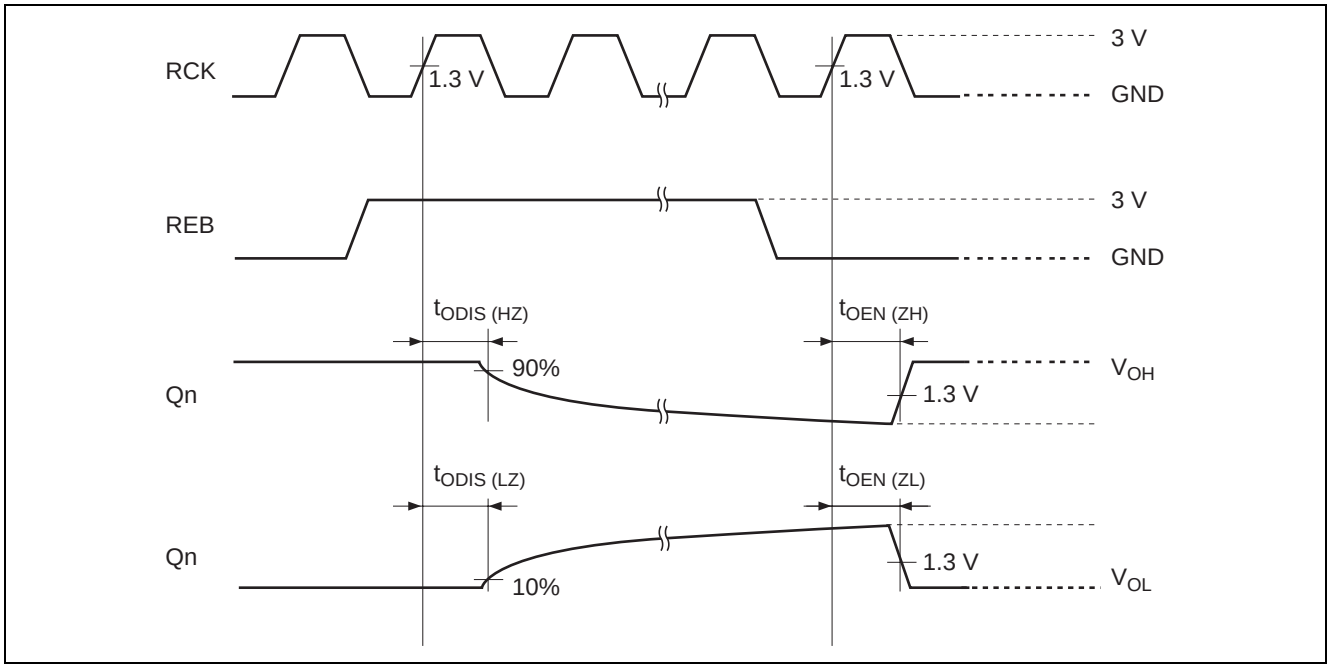
Judging voltage Input: 1.3 V

Output: 1.3 V (However, $t_{ODIS\ (LZ)}$ is judged with 10% of the output amplitude, while $t_{ODIS\ (HZ)}$ is judged with 90% of the output amplitude)

Load capacitance C_L includes the floating capacity of connected lines and input capacitance of probe.

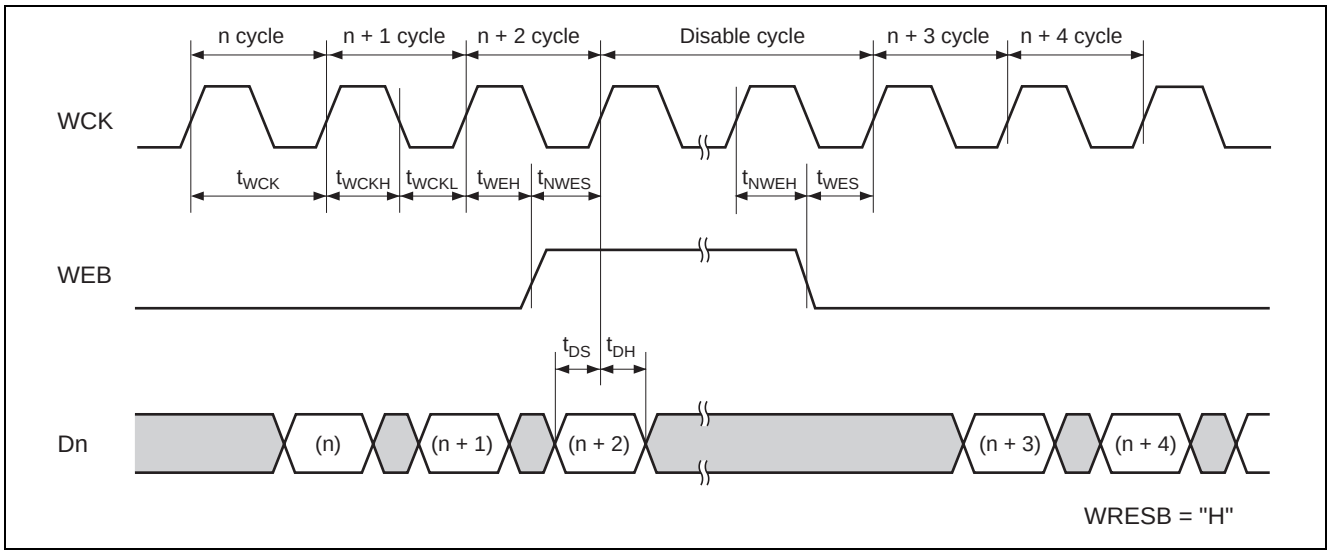
Item	SW1	SW2
$t_{ODIS\ (LZ)}$	Close	Open
$t_{ODIS\ (HZ)}$	Open	Close
$t_{OEN\ (ZL)}$	Close	Open
$t_{OEN\ (ZH)}$	Open	Close

t_{ODIS} and t_{OEN} Measurement Condition

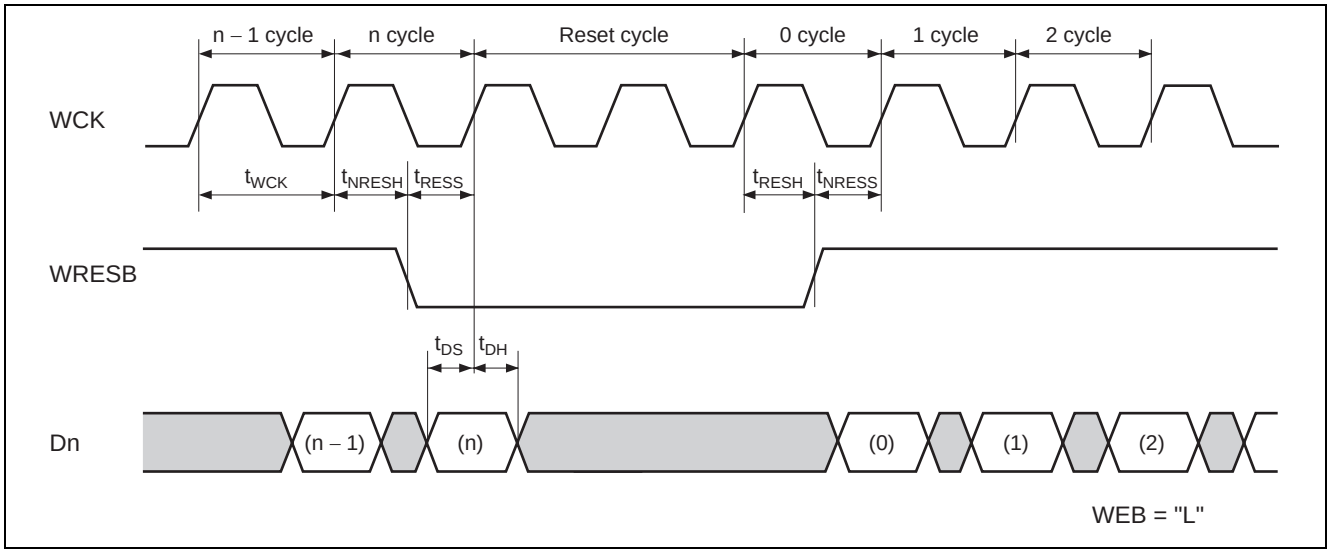


Operation Timing

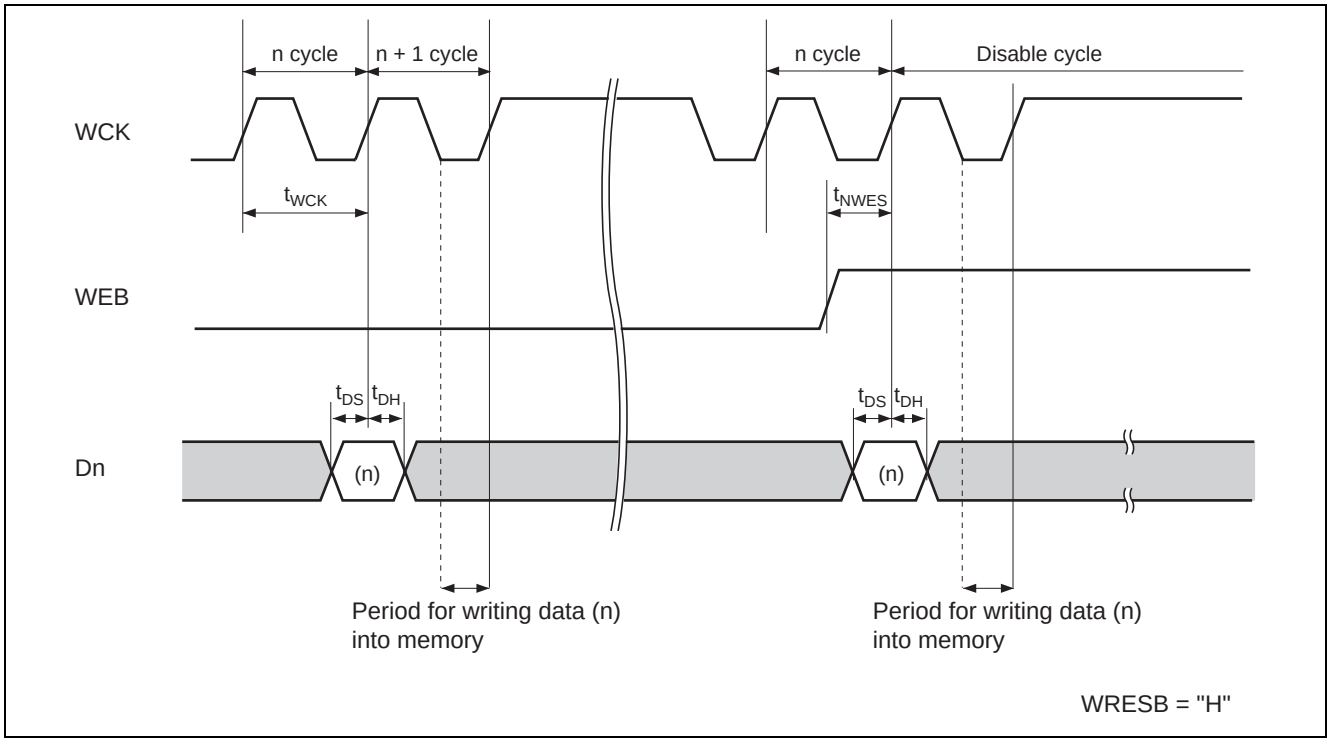
Write Cycle



Write Reset Cycle



Matters that Needs Attention when WCK Stops

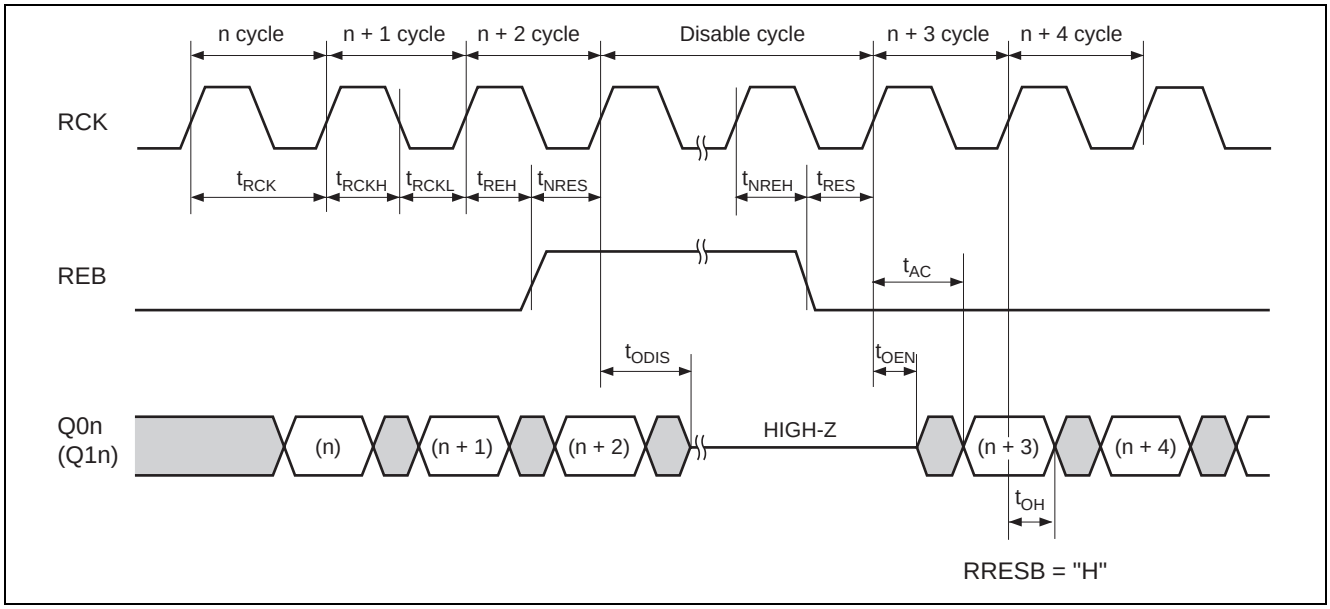


Input data of n cycle is read at the rising edge after WCK of n cycle and writing operation starts in the WCK low-level period of n + 1 cycle. The writing operation is complete at the falling edge after n + 1 cycle.

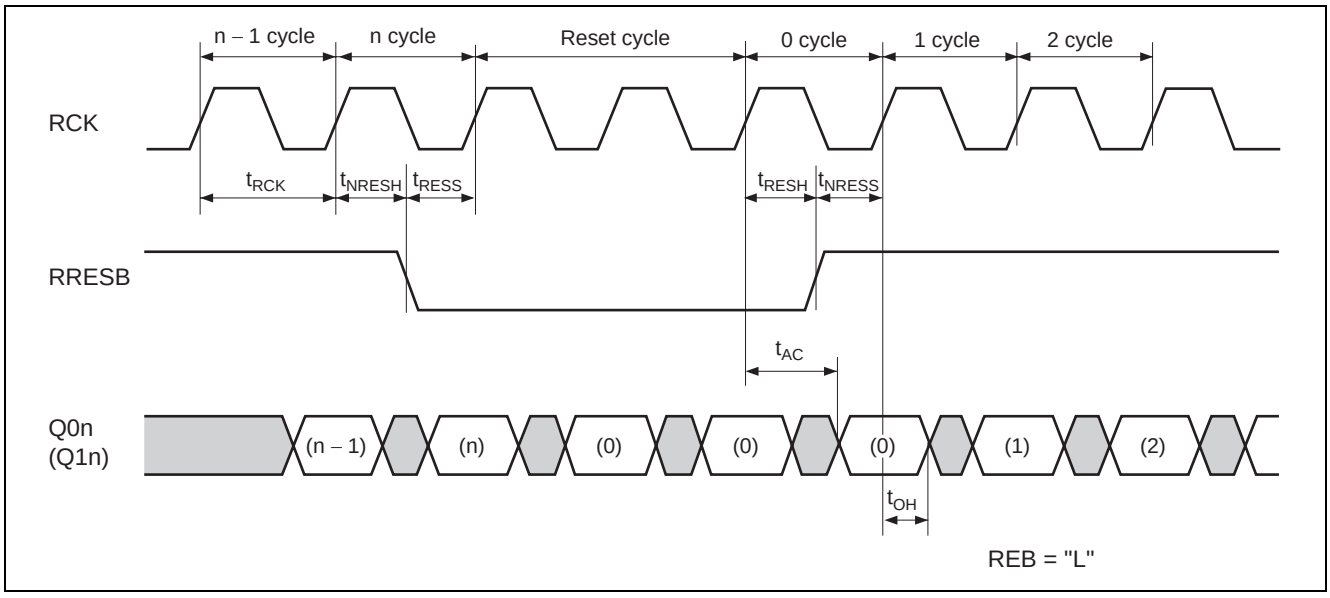
To stop reading write data at n cycle, enter WCK before the rising edge after n + 1 cycle.

When the cycle next to n cycle is a disable cycle, WCK for a cycle requires to be entered after the disable cycle as well.

Read Cycle

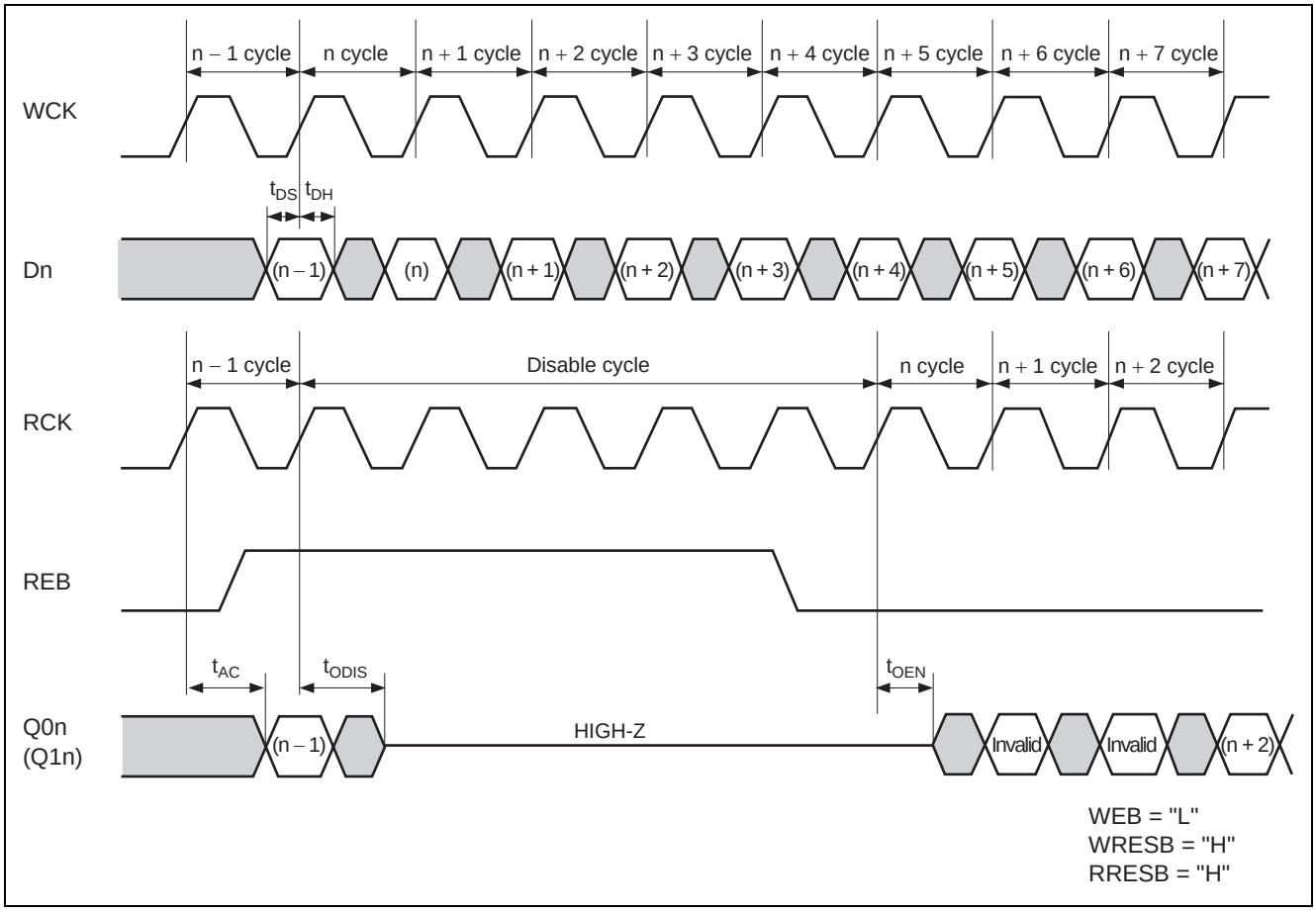


Read Reset Cycle



Notes on Reading of Written Data in Read Disable

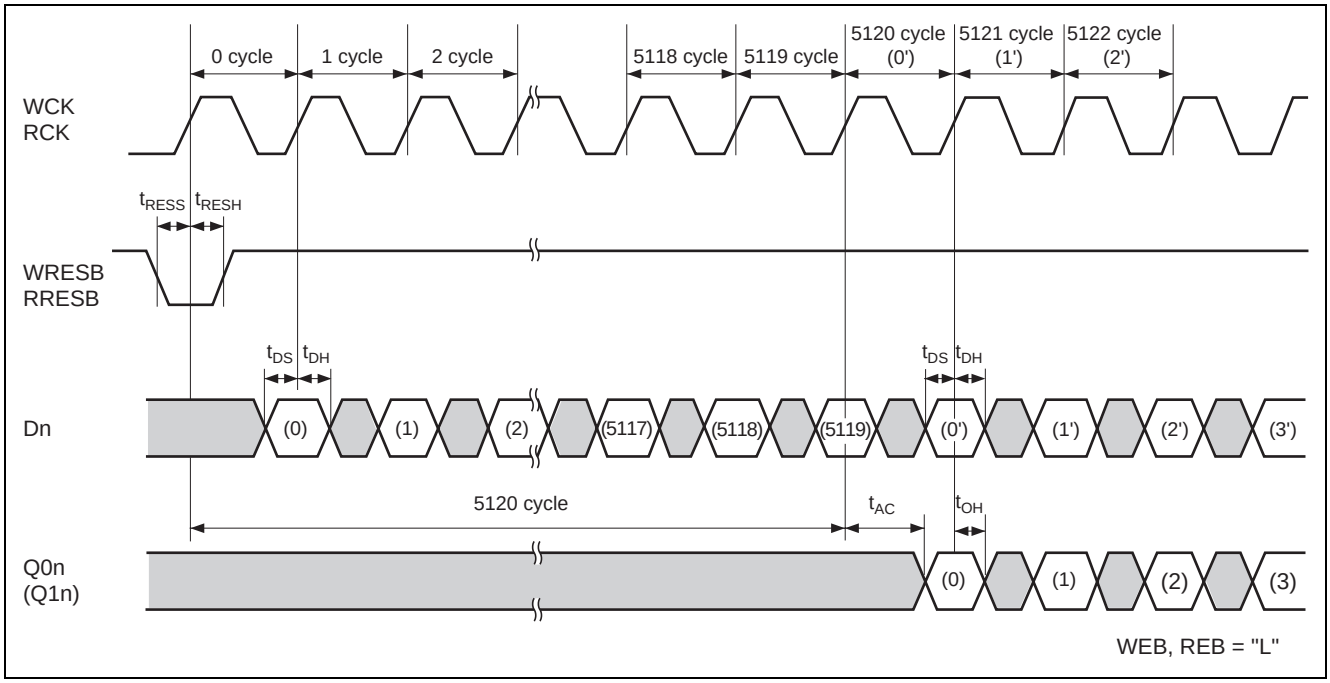
When writing operation is performed at n cycle and n + 1 cycle on the writing side in the read disable period after n – 1 cycle on the reading side, output at n cycle and n + 1 cycle after read enable is invalid. For output at n + 2 cycle and after, however, data written in the read disable period is to be output.



Variable Length Delay Bit

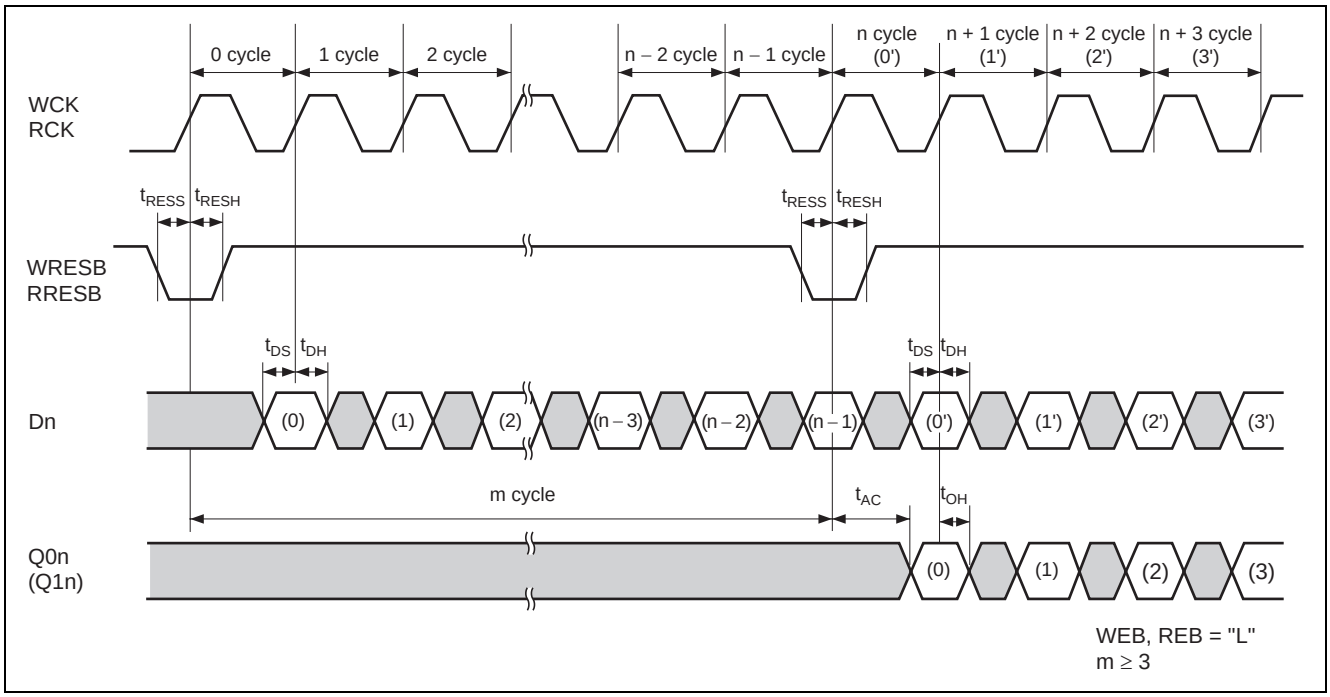
1 Line (5120 Bits) Delay

Input data can be written at the rising edge of WCK after write cycle and output data is read at the rising edge of RCK before read cycle to easily make 1 line delay.



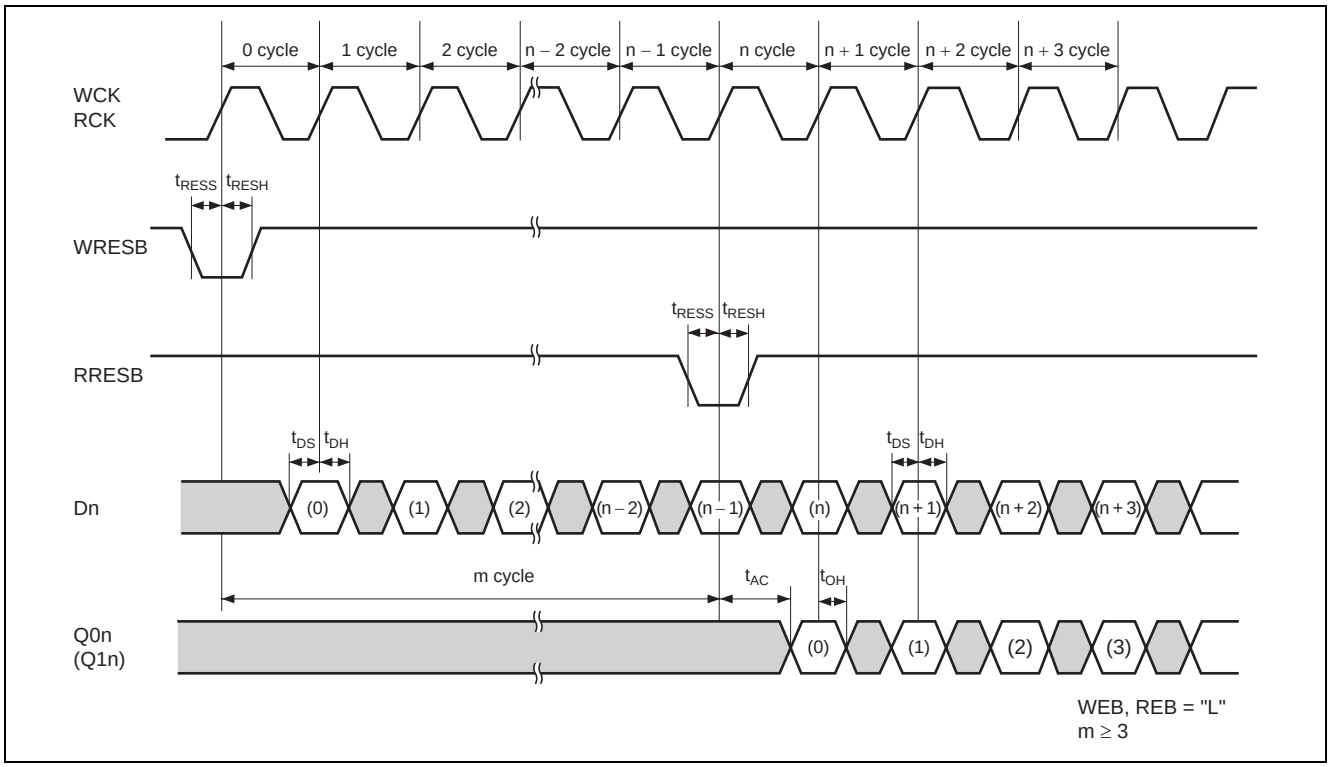
n-bit Delay Bit

(Reset at cycles according to the delay length)



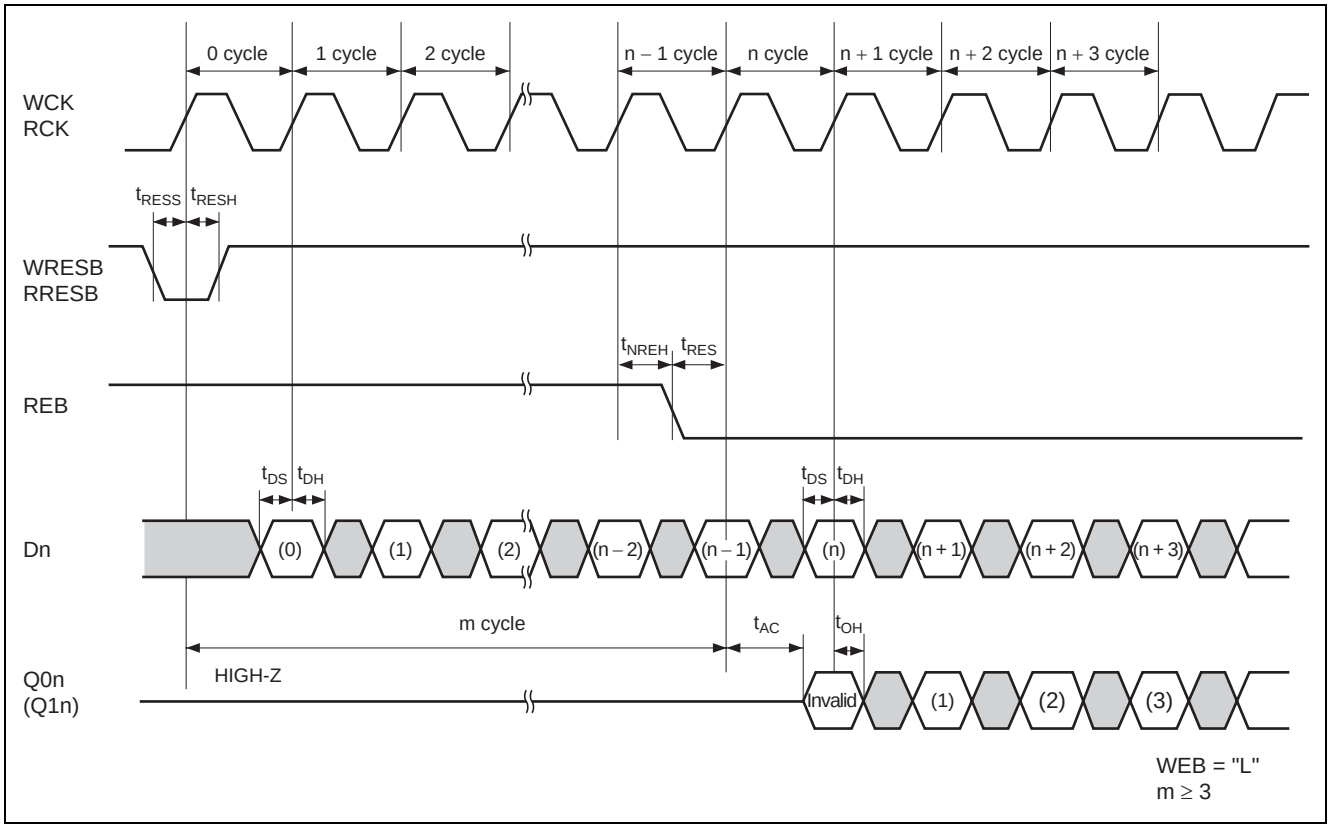
n-bit Delay 2

(Slides input timings of WRESB and RRESB at cycles according to the delay length)



n-bit Delay 3

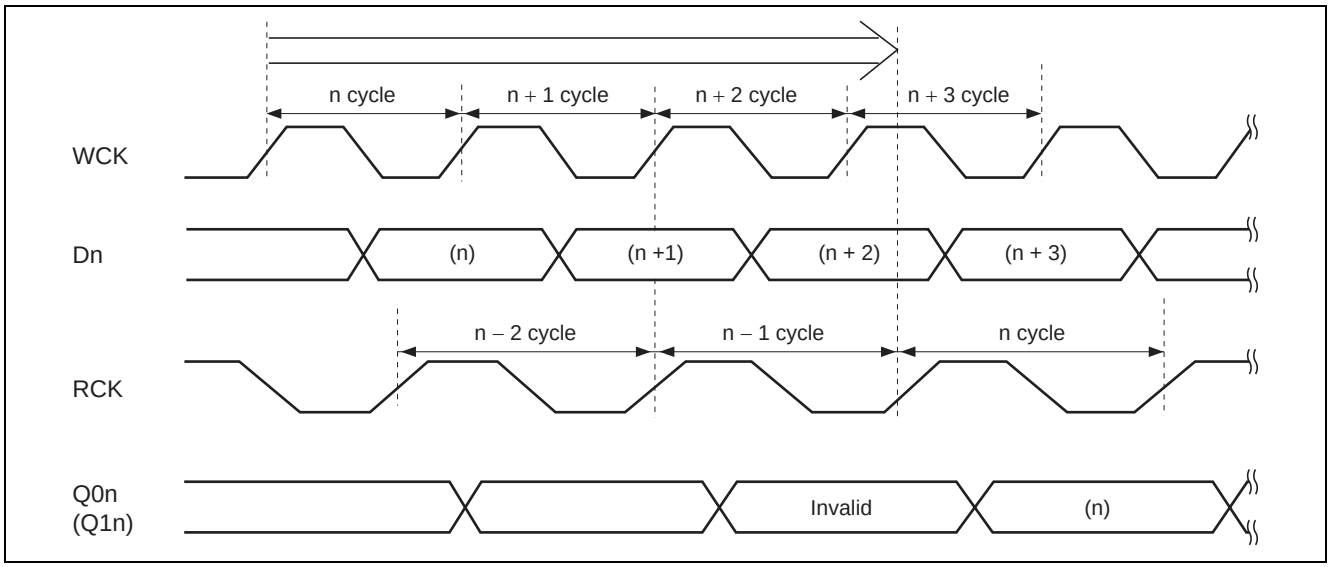
(Slides address by disabling REB in the period according to the delay length)



Reading Shortest n-cycle Write Data "n"

(Reading side n – 2 cycle ends after the end of writing side n + 1 cycle)

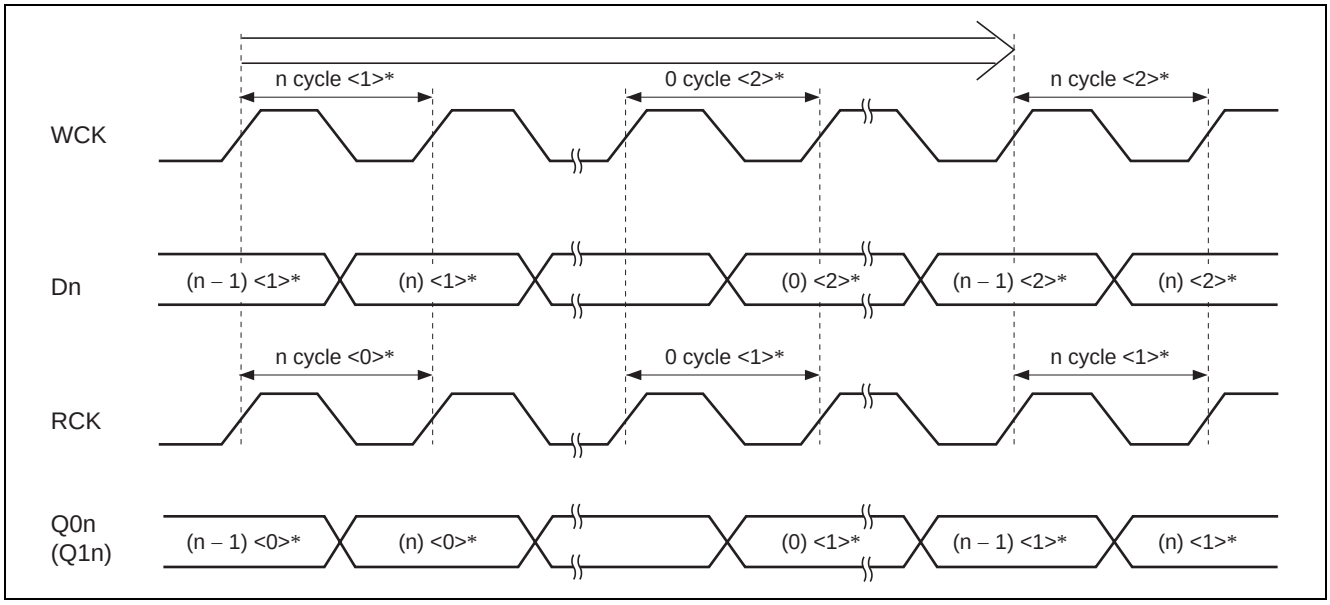
When the reading side n – 2 cycle ends before the end of the writing side n + 1 cycle, output Qn of n cycle is made invalid. In the following diagram, end of reading side n – 2 cycle and end of writing side n + 1 cycle overlap each other. This example can read n cycle data in the shortest time. When this is the case, reading operation at n – 1 cycle is invalid.



Reading Longest n-cycle Write Data "n": 1 Line Delay

(When writing side n-cycle <2> starts, reading side n cycle <1> then starts)

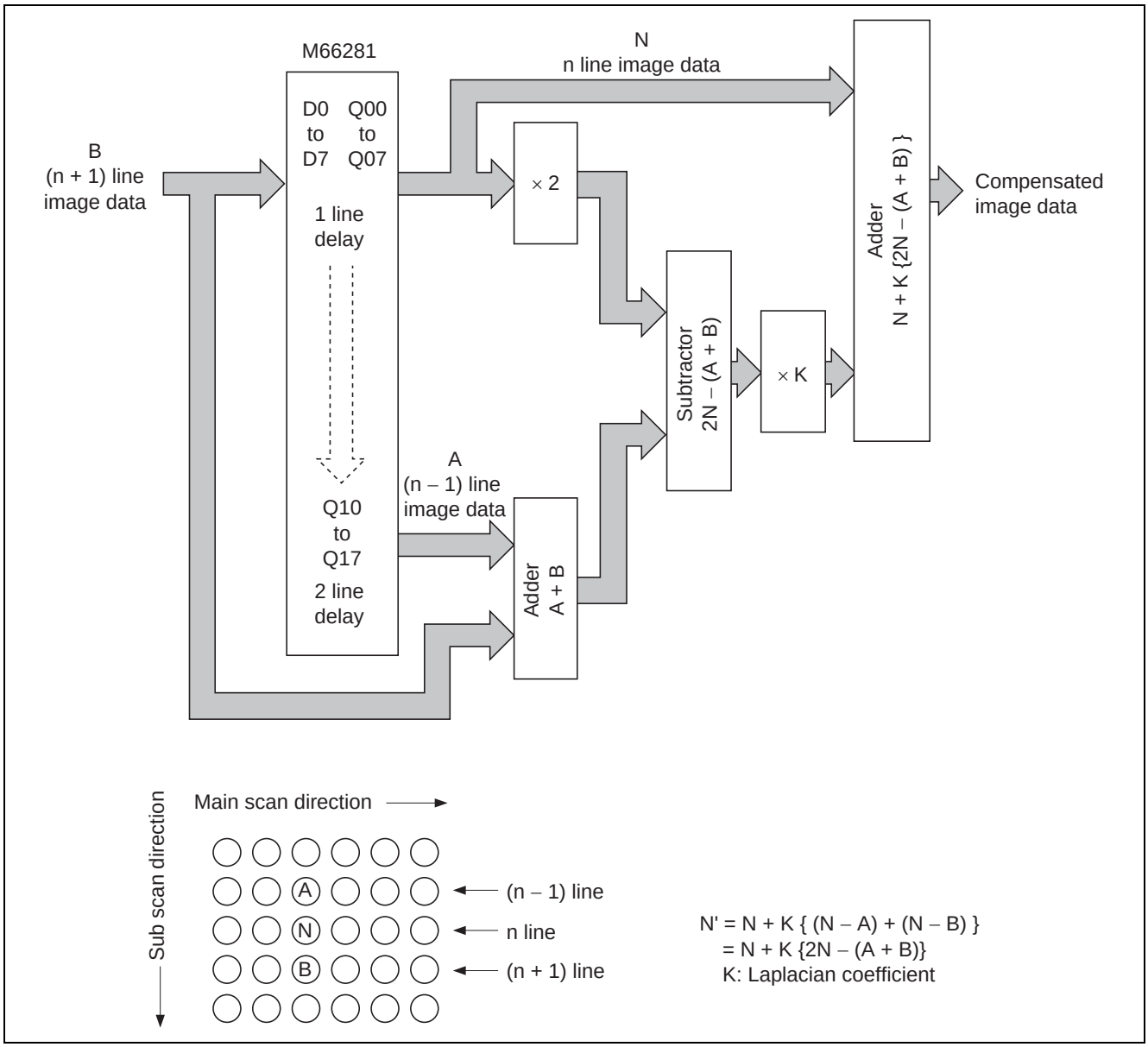
Output Qn of n cycle <1>* can be read until the start of reading side n cycle <1> and the start of writing side n cycle <2>* overlap each other.



Note: <0>*, <1>* and <2>* indicate value of lines.

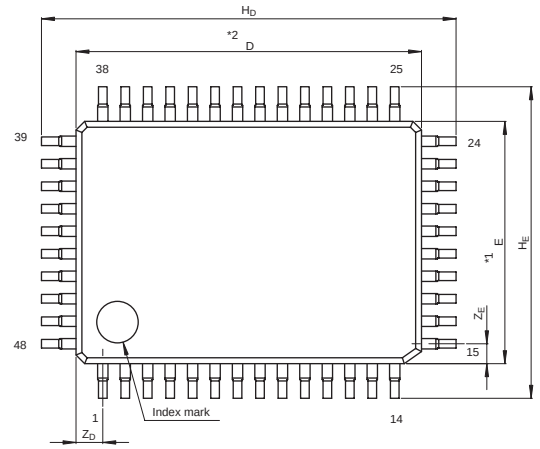
Application Example

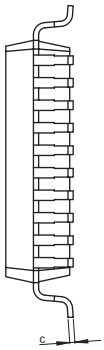
Sub Scan Resolution Compensation Circuit with Laplacian Filter

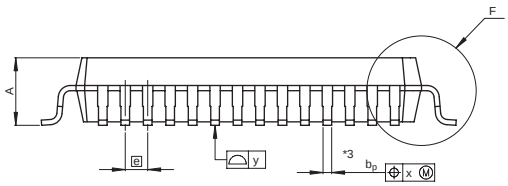


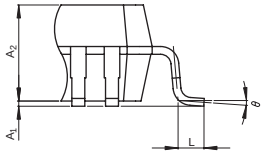
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP48-7x10-0.65	PRQP0048JA-A	48P6S-A	0.3g









Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.8	10.0	10.2
E	6.8	7.0	7.2
A_2	—	1.85	—
H_D	11.7	12.0	12.3
H_E	8.7	9.0	9.3
A	—	—	2.15
A_1	0	0.1	0.2
b_p	0.2	0.25	0.35
c	0.13	0.15	0.2
θ	0°	—	10°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.775	—
Z_E	—	0.575	—
L	0.3	0.5	0.7

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

Colophon .7.0