# 256K x 32, 256K x 36 and 512K x 18 FLOW-THROUGH 'NO WAIT' STATE BUS SRAM

**PRELIMINARY INFORMATION**
**APRIL 2001**

## FEATURES

- 100 percent bus utilization
- No wait cycles between Read and Write
- Internal self-timed write cycle
- Individual Byte Write Control
- Single R/W (Read/Write) control pin
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining for TQFP
- Power Down mode
- Common data inputs and data outputs
- $\overline{CKE}$ pin to enable clock and suspend operation
- JEDEC 100-pin TQFP, 119 PBGA package
- Single +3.3V power supply (± 5%)
- NF Version: 3.3V I/O Supply Voltage
- NLF Version: 2.5V I/O Supply Voltage
- Industrial temperature available

## DESCRIPTION

The 8 Meg 'NF' product family feature high-speed, low-power synchronous static RAMs designed to provide a burstable, high-performance, 'no wait' state, device for network and communications customers. They are organized as 262,144 words by 32 bits, 262,144 words by 36 bits and 524,288 words by 18 bits, fabricated with *ISSI*'s advanced CMOS technology.

Incorporating a 'no wait' state feature, wait cycles are eliminated when the bus switches from read to write, or write to read. This device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit.

All synchronous inputs pass through registers are controlled by a positive-edge-triggered single clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable, $\overline{CKE}$ is HIGH. In this state the internal device will hold their previous values.

All Read, Write and Deselect cycles are initiated by the ADV input. When the ADV is HIGH the internal burst counter is incremented. New external addresses can be loaded when ADV is LOW.

Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs and when $\overline{WE}$ is LOW. Separate byte enables allow individual bytes to be written.

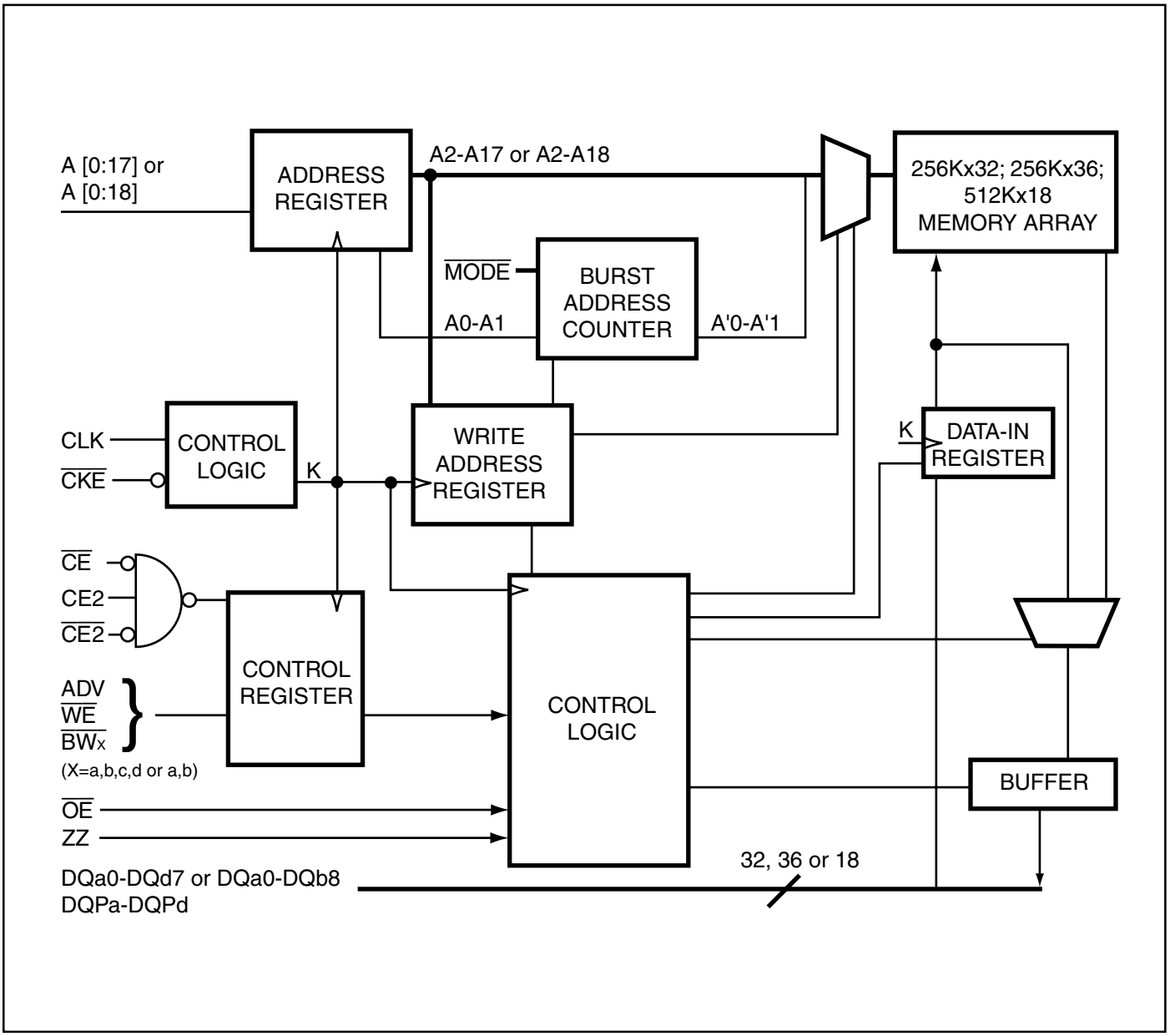
A burst mode pin (MODE) defines the order of the burst sequence. When tied HIGH, the interleaved burst sequence is selected. When tied LOW, the linear burst sequence is selected.

## FAST ACCESS TIME

| Symbol | Parameter | -10 | Units |
|---|---|---|---|
| $t_{KQ}$ | Clock Access Time | 10 | ns |
| $t_{KC}$ | Cycle Time | 12 | ns |
| | Frequency | 83 | MHz |

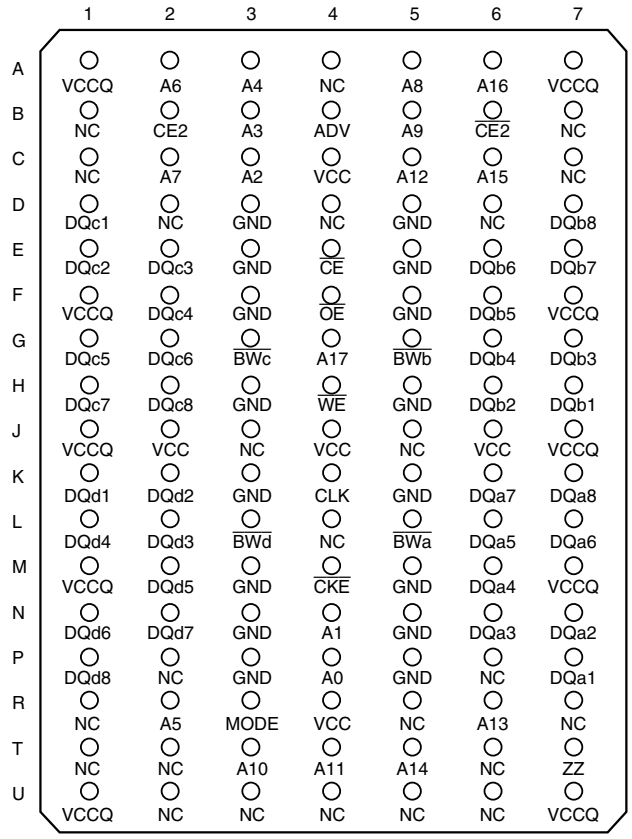
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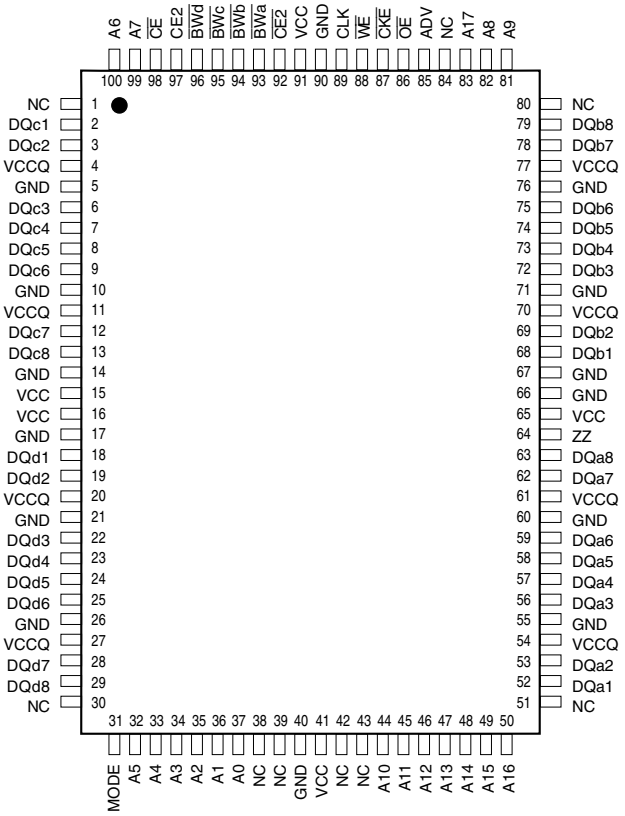
## BLOCK DIAGRAM



## PIN CONFIGURATION

### 119-pin PBGA (Top View) and 100-Pin TQFP




**256K x 32**

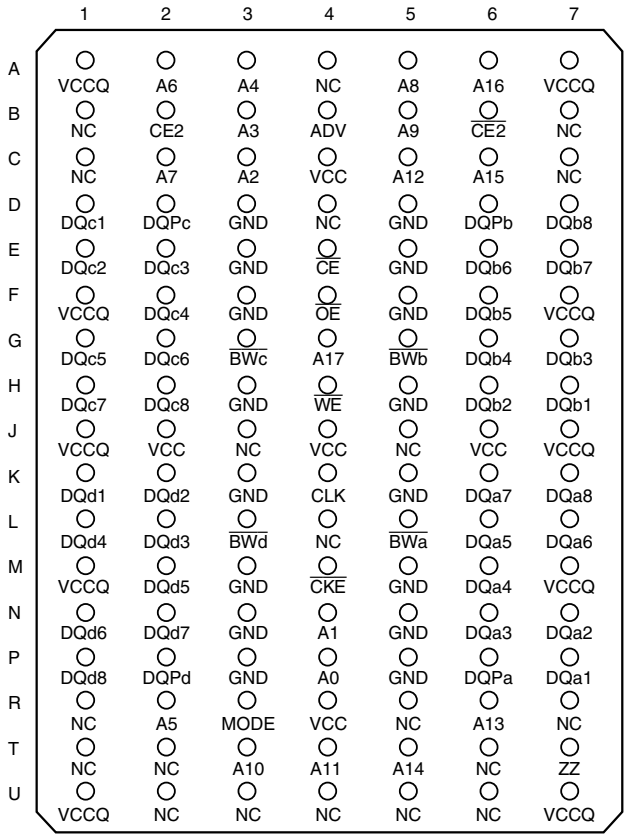
## PIN DESCRIPTIONS

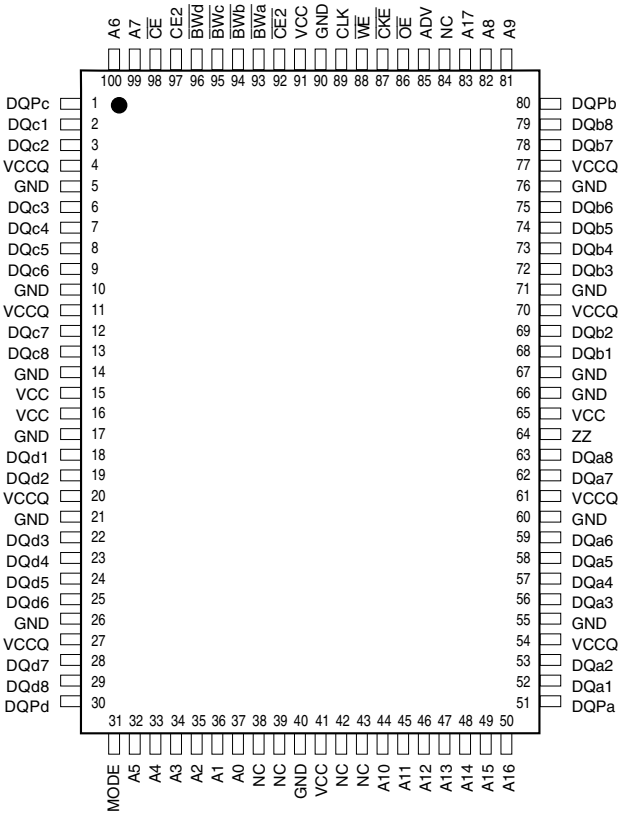
| | |
|---|---|
| A0, A1 | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. |
| A2-A17 | Synchronous Address Inputs |
| CLK | Synchronous Clock |
| ADV | Synchronous Burst Address Advance |
| $\overline{BWa}$-$\overline{BWd}$ | Synchronous Byte Write Enable |
| $\overline{WE}$ | Write Enable |
| $\overline{CKE}$ | Clock Enable |

| | |
|---|---|
| $\overline{CE}$, $\overline{CE2}$, CE2 | Synchronous Chip Enable |
| $\overline{OE}$ | Output Enable |
| DQa-DQd | Synchronous Data Input/Output |
| MODE | Burst Sequence Mode Selection |
| $V_{CC}$ | +3.3V Power Supply |
| GND | Ground |
| $V_{CCQ}$ | Isolated Output Buffer Supply: +3.3V/2.5V |
| ZZ | Snooze Enable |

## PIN CONFIGURATION

### 119-pin PBGA (Top View) and 100-Pin TQFP




**256K x 36**

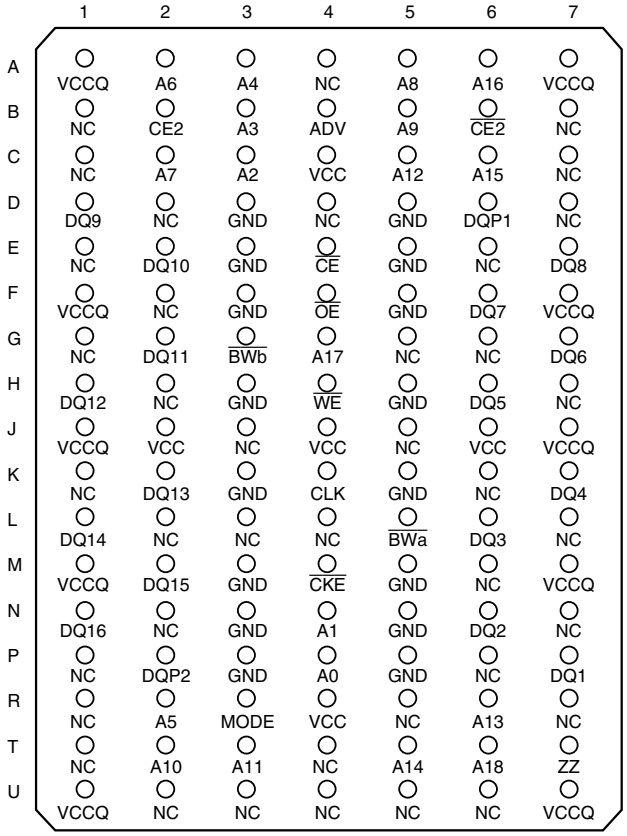
## PIN DESCRIPTIONS

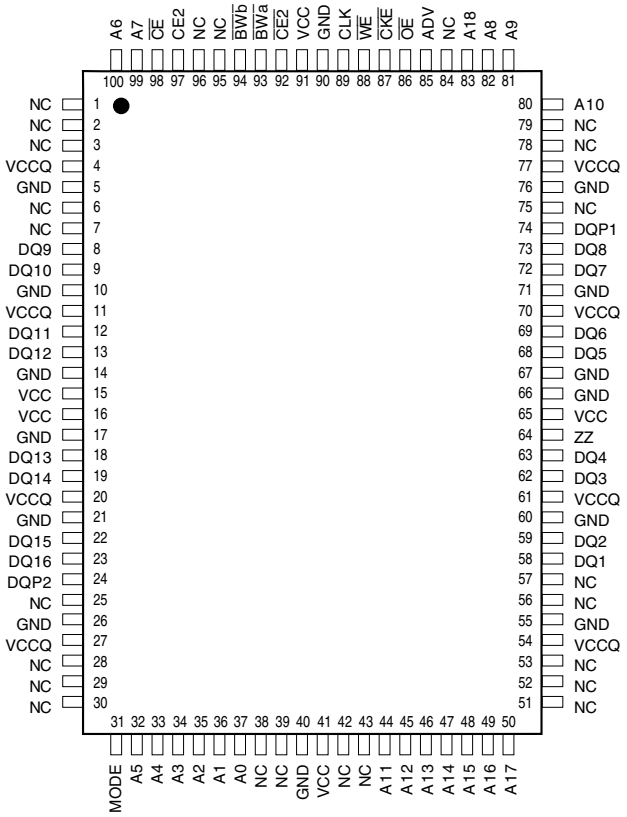
| | |
|---|---|
| A0, A1 | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. |
| A2-A17 | Synchronous Address Inputs |
| CLK | Synchronous Clock |
| ADV | Synchronous Burst Address Advance |
| $\overline{BWa}$-$\overline{BWd}$ | Synchronous Byte Write Enable |
| $\overline{WE}$ | Write Enable |

| | |
|---|---|
| $\overline{CKE}$ | Clock Enable |
| $\overline{CE}$, $\overline{CE2}$, CE2 | Synchronous Chip Enable |
| $\overline{OE}$ | Output Enable |
| DQa-DQd | Synchronous Data Input/Output |
| MODE | Burst Sequence Mode Selection |
| $V_{CC}$ | +3.3V Power Supply |
| GND | Ground |
| $V_{CCQ}$ | solated Output Buffer Supply: +3.3V/2.5V |
| ZZ | Snooze Enable |
| DQPa-DQPd | Parity Data I/O |

## PIN CONFIGURATION

### 119-pin PBGA (Top View) and 100-Pin TQFP



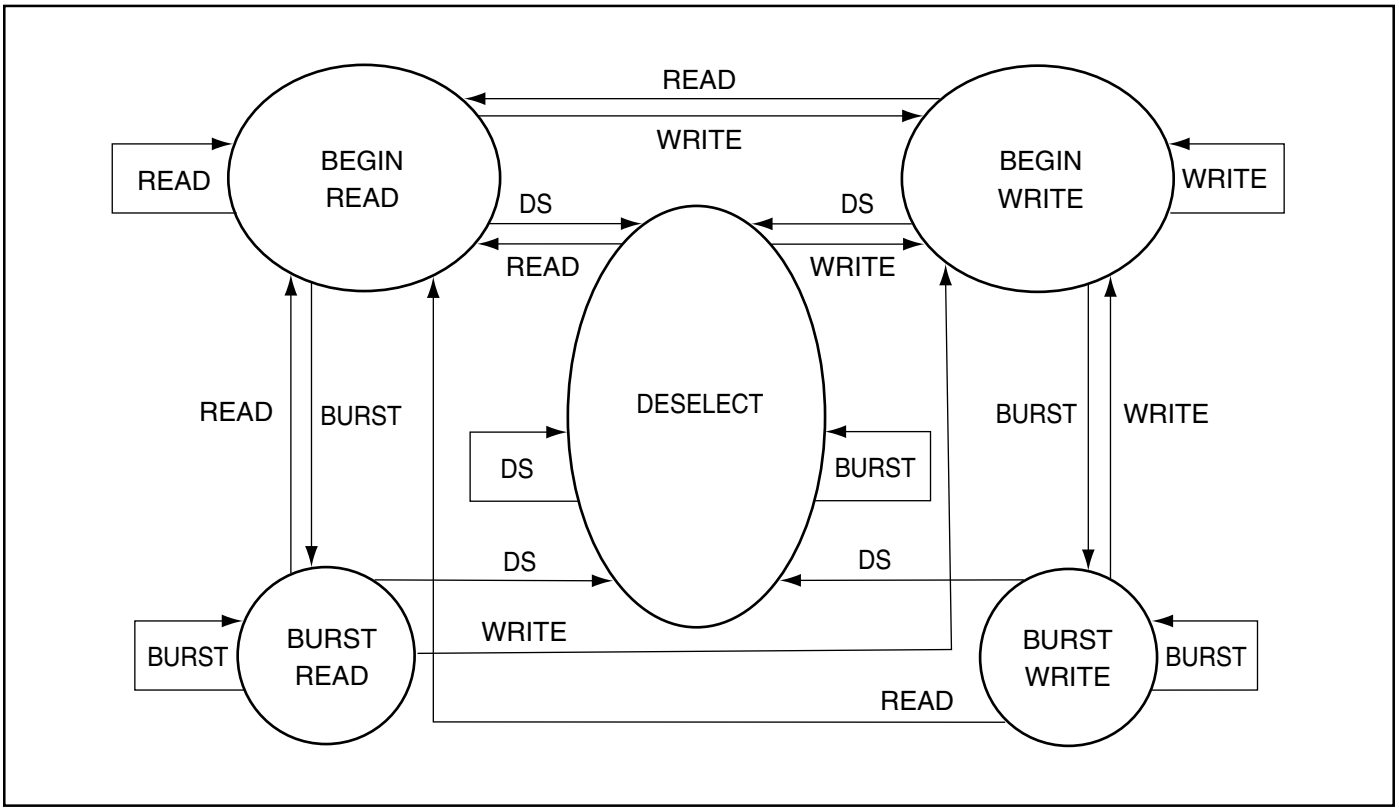

**512K x 18**

## PIN DESCRIPTIONS

| | |
|---|---|
| A0, A1 | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. |
| A2-A18 | Synchronous Address Inputs |
| CLK | Synchronous Clock |
| ADV | Synchronous Burst Address Advance |
| $\overline{BWa}$-$\overline{BWb}$ | Synchronous Byte Write Enable |
| $\overline{WE}$ | Write Enable |
| $\overline{CKE}$ | Clock Enable |

| | |
|---|---|
| $\overline{CE}$, CE2, $\overline{CE2}$ | Synchronous Chip Enable |
| $\overline{OE}$ | Output Enable |
| DQ1-DQ16 | Synchronous Data Input/Output |
| MODE | Burst Sequence Mode Selection |
| $V_{CC}$ | +3.3V Power Supply |
| GND | Ground |
| $V_{CCQ}$ | Isolated Output Buffer Supply: +3.3V/2.5V |
| ZZ | Snooze Enable |
| DQP1-DQP2 | Parity Data I/O DQP1 is parity for DQ1-8; DQP2 is parity for DQ9-16 |

## STATE DIAGRAM




## SYNCHRONOUS TRUTH TABLE(1)

| Operation | Address Used | $\overline{CS}1$ | CS2 | $\overline{CS}2$ | ADV | $\overline{WE}$ | $\overline{BW}x$ | $\overline{OE}$ | $\overline{CKE}$ | CLK |
|---|---|---|---|---|---|---|---|---|---|---|
| Not Selected Continue | N/A | X | X | X | H | X | X | X | L | ↑ |
| Begin Burst Read | External Address | L | H | L | L | H | X | L | L | ↑ |
| Continue Burst Read | Next Address | X | X | X | H | X | X | L | L | ↑ |
| NOP/Dummy Read | External Address | L | H | L | L | H | X | H | L | ↑ |
| Dummy Read | Next Address | X | X | X | H | X | X | H | L | ↑ |
| Begin Burst Write | External Address | L | H | L | L | L | L | X | L | ↑ |
| Continue Burst Write | Next Address | X | X | X | H | X | L | X | L | ↑ |
| NOP/Write Abort | N/A | L | H | L | L | L | H | X | L | ↑ |
| Write Abort | Next Address | X | X | X | H | X | H | X | L | ↑ |
| Ignore Clock | Current Address | X | X | X | X | X | X | X | H | ↑ |

**Notes:**
1. "X" means don't care.
2. The rising edge of clock is symbolized by ↑
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. $\overline{WE}$ = L means Write operation in Write Truth Table.
   $\overline{WE}$ = H means Read operation in Write Truth Table.
5. Operation finally depends on status of asynchronous pins (ZZ and $\overline{OE}$).

## ASYNCHRONOUS TRUTH TABLE(1)

| Operation | ZZ | $\overline{OE}$ | I/O STATUS |
|---|---|---|---|
| Sleep Mode | H | X | High-Z |
| Read | L<br>L | L<br>H | DQ<br>High-Z |
| Write | L | X | Din, High-Z |
| Deselected | L | X | High-Z |

**Notes:**

1. X means "Don't Care".
2. For write cycles following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
3. Sleep Mode means power Sleep Mode where stand-by current does not depend on cycle time.
4. Deselected means power Sleep Mode where stand-by current depends on cycle time.

## WRITE TRUTH TABLE (x18)

| Operation | $\overline{WE}$ | $\overline{BW}$a | $\overline{BW}$b |
|---|---|---|---|
| READ | H | X | X |
| WRITE BYTE a | L | L | H |
| WRITE BYTE b | L | H | L |
| WRITE ALL BYTEs | L | L | L |
| WRITE ABORT/NOP | L | H | H |

**Notes:**

1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

## WRITE TRUTH TABLE (x32/x36)

| Operation | $\overline{WE}$ | $\overline{BW}$a | $\overline{BW}$b | $\overline{BW}$c | $\overline{BW}$d |
|---|---|---|---|---|---|
| READ | H | X | X | X | X |
| WRITE BYTE a | L | L | H | H | H |
| WRITE BYTE b | L | H | L | H | H |
| WRITE BYTE c | L | H | H | L | H |
| WRITE BYTE d | L | H | H | H | L |
| WRITE ALL BYTEs | L | L | L | L | L |
| WRITE ABORT/NOP | L | H | H | H | H |

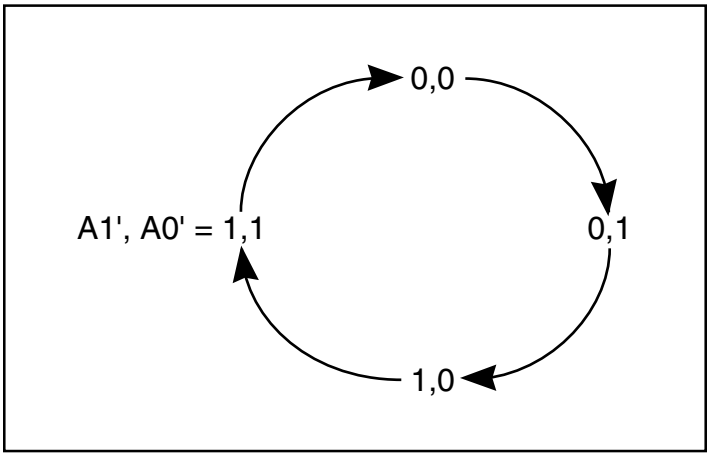
**Notes:**

1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

## INTERLEAVED BURST ADDRESS TABLE (MODE = $V_{CC}$)

| External Address A1 A0 | 1st Burst Address A1 A0 | 2nd Burst Address A1 A0 | 3rd Burst Address A1 A0 |
|---|---|---|---|
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

## LINEAR BURST ADDRESS TABLE (MODE = GND)




## ABSOLUTE MAXIMUM RATINGS[1]

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_{BIAS}$ | Temperature Under Bias | –10 to +85 | °C |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $P_D$ | Power Dissipation | 1.6 | W |
| $I_{OUT}$ | Output Current (per I/O) | 100 | mA |
| $V_{IN}$, $V_{OUT}$ | Voltage Relative to GND for I/O Pins | –0.5 to $V_{CCQ}$ + 0.3 | V |
| $V_{IN}$ | Voltage Relative to GND for for Address and Control Inputs | –0.3 to 4.6 | V |

**Notes:**
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

## OPERATING RANGE

| Range | Ambient Temperature | Vcc | VccQ |
|---|---|---|---|
| Commercial | 0°C to +70°C | 3.3V ± 5%<br>3.3V ± 5% | 3.3V ± 5%<br>2.5V ± 5% |
| Industrial | -40°C to +85°C | 3.3V ± 5% | 3.3V ± 5% |

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| | | | 2.5V | | 3.3V | | |
|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Test Conditions | Min. | Max. | Min. | Max. | Unit |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –4.0 mA (3.3V)<br>$I_{OH}$ = 1.0 mA (2.5V) | 2.0 | — | 2.4 | — | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 8.0 mA (3.3V)<br>$I_{OL}$ = 1.0 mA (2.5V) | — | 0.4 | — | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | 1.7 | $V_{CC}$ + 0.3 | 2.0 | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | –0.3 | 0.7 | –0.3 | 0.8 | V |
| $I_{LI}$ | Input Leakage Current | GND ≤ $V_{IN}$ ≤ $V_{CC}$[1] | –5 | 5 | –5 | 5 | µA |
| $I_{LO}$ | Output Leakage Current | GND ≤ $V_{OUT}$ ≤ $V_{CCQ}$, $\overline{OE}$ = $V_I$ | –5 | 5 | –5 | 5 | µA |

## POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

| | | | -10 MAX | | |
|---|---|---|---|---|---|
| Symbol | Parameter | Test Conditions | x18 | x32/36 | Unit |
| $I_{CC}$ | AC Operating Supply Current | Device Selected, $\overline{OE}$ = $V_{IH}$, ZZ ≤ $V_{IL}$, All Inputs ≤ 0.2V or ≥ $V_{CC}$ – 0.2V, Cycle Time ≥ $t_{KC}$ min.<br>Com.<br>Ind. | 300<br>350 | 300<br>350 | mA |
| $I_{SB}$ | Standby Current TTL Input | Device Deselected, $V_{CC}$ = Max., All Inputs ≤ 0.2V or ≥ $V_{CC}$ – 0.2V, ZZ ≤ $V_{IL}$, f = Max.<br>Com.<br>Ind. | 80<br>90 | 80<br>90 | mA |
| $I_{SBI}$ | Standby Current CMOS Input | Device Deselected, $V_{CC}$ = Max., $V_{IN}$ ≤ GND + 0.2V or ≥ $V_{CC}$ – 0.2V f = 0<br>Com.<br>Ind. | 20<br>25 | 20<br>25 | mA |

**Note:**
1. MODE pin has an internal pullup and should be tied to Vcc or GND. It exhibits ±30 µA maximum leakage current when tied to ≤ GND + 0.2V or ≥ Vcc – 0.2V.

## CAPACITANCE[1,2]

| Symbol | Parameter | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | pF |
| $C_{OUT}$ | Input/Output Capacitance | $V_{OUT}$ = 0V | 8 | pF |

**Notes:**
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: $T_A$ = 25°C, f = 1 MHz, Vcc = 3.3V.

## 3.3V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|---|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

## 3.3V I/O OUTPUT LOAD EQUIVALENT

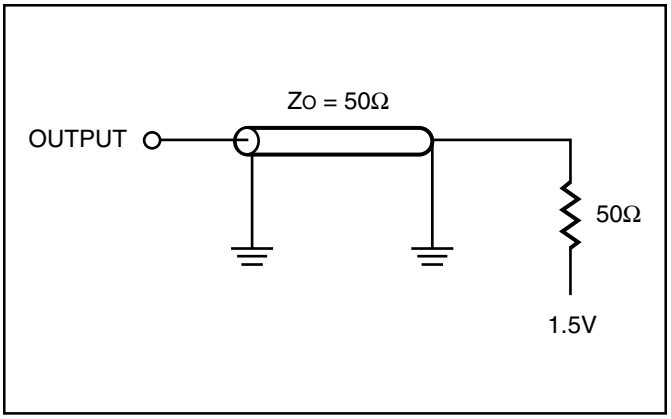



**Figure 1**

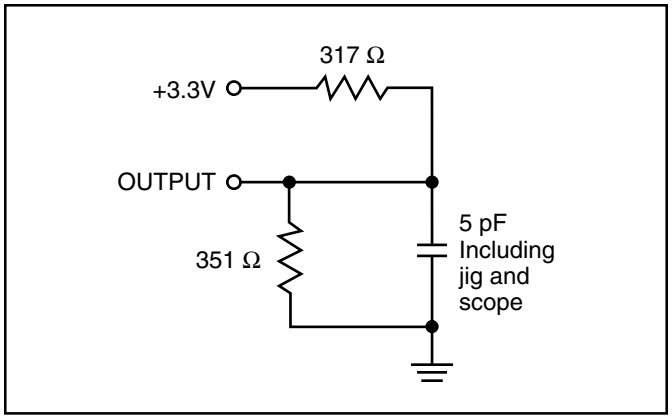



**Figure 2**

## 2.5V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|---|
| Input Pulse Level | 0V to 2.5V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 1.25V |
| Output Load | See Figures 3 and 4 |

## 2.5V I/O OUTPUT LOAD EQUIVALENT

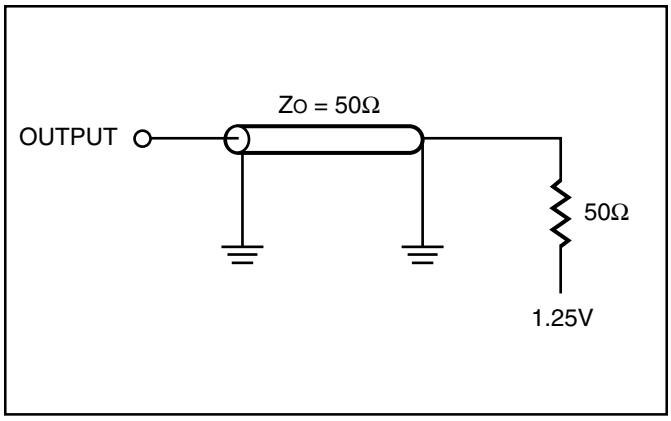



**Figure 3**

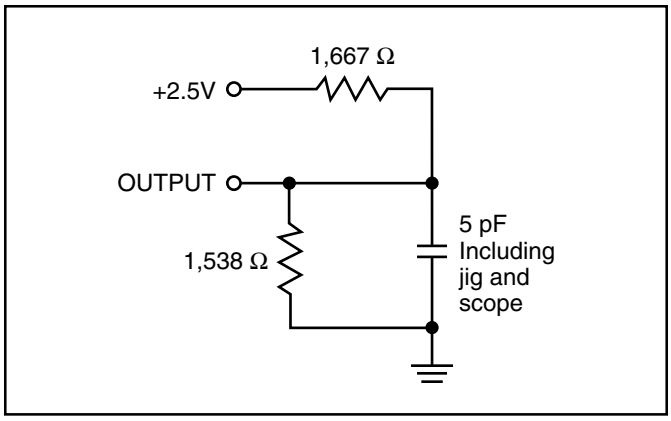



**Figure 4**

## READ/WRITE CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

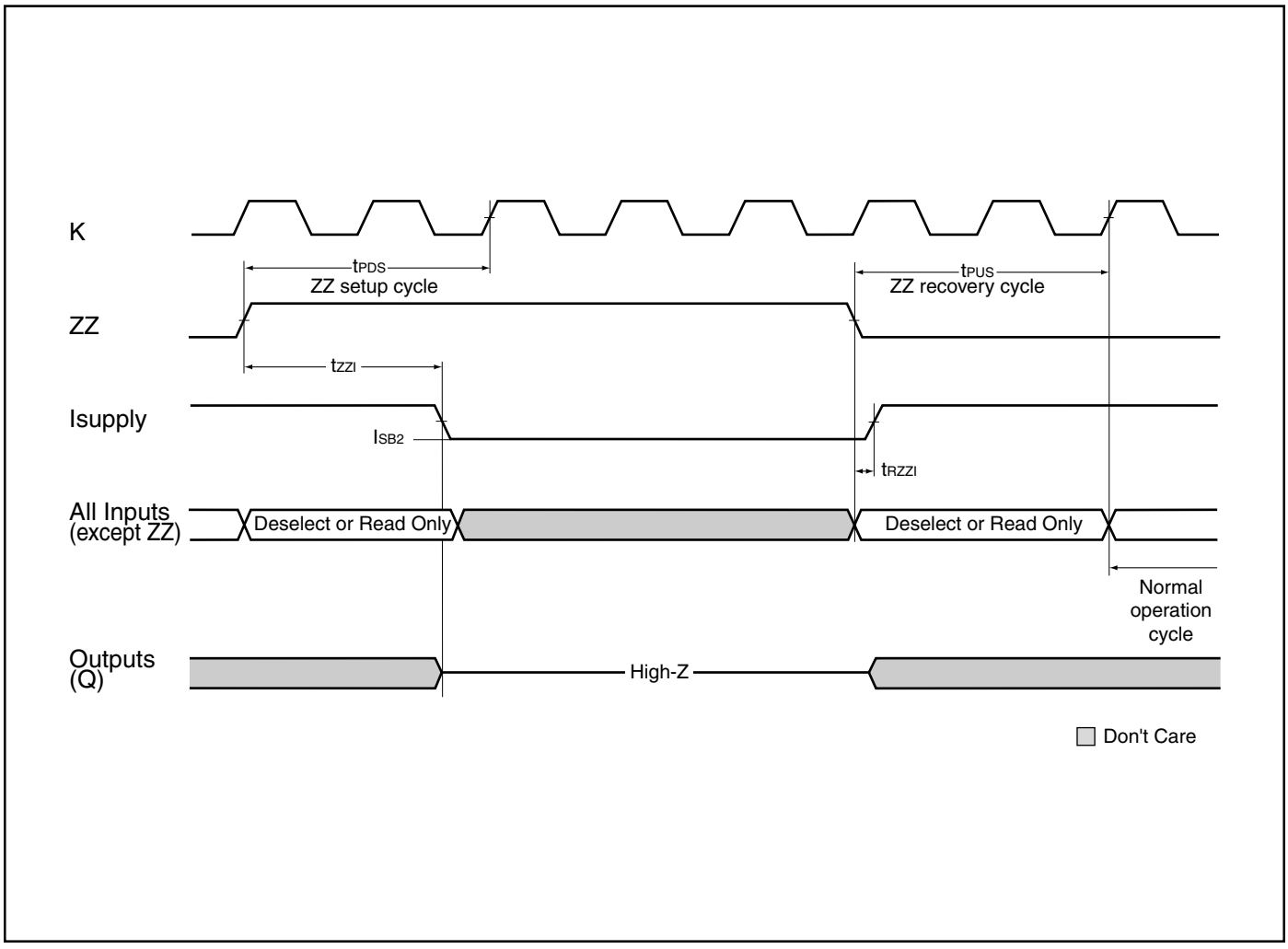
| Symbol | Parameter | -10 Min. | -10 Max. | Unit |
|---|---|---|---|---|
| fmax | Clock Frequency | — | 83 | MHz |
| $t_{KC}$ | Cycle Time | 12 | — | ns |
| $t_{KH}$ | Clock High Time | 3 | — | ns |
| $t_{KL}$ | Clock Low Time | 3 | — | ns |
| $t_{KQ}$ | Clock Access Time | — | 10 | ns |
| $t_{KQX}$[2] | Clock High to Output Invalid | 3 | — | ns |
| $t_{KQLZ}$[2,3] | Clock High to Output Low-Z | 2.5 | — | ns |
| $t_{KQHZ}$[2,3] | Clock High to Output High-Z | — | 6 | ns |
| $t_{OEQ}$ | Output Enable to Output Valid | — | 3.5 | ns |
| $t_{OELZ}$[2,3] | Output Enable to Output Low-Z | 0 | — | ns |
| $t_{OEHZ}$[2,3] | Output Disable to Output High-Z | — | 4 | ns |
| $t_{AS}$ | Address Setup Time | 2 | — | ns |
| $t_{WS}$ | Read/Write Setup Time | 2 | — | ns |
| $t_{CES}$ | Chip Enable Setup Time | 2 | — | ns |
| $t_{SE}$ | Clock Enable Setup Time | 2 | — | ns |
| $t_{AVS}$ | Address Advance Setup Time | 2 | — | ns |
| $t_{DS}$ | Data Setup Time | 2 | — | ns |
| $t_{AH}$ | Address Hold Time | 0.5 | — | ns |
| $t_{HE}$ | Clock EnableHold Time | 0.5 | — | ns |
| $t_{WH}$ | Write Hold Time | 0.5 | — | ns |
| $t_{CEH}$ | Chip Enable Hold Time | 0.5 | — | ns |
| $t_{ADVH}$ | Address Advance Hold Time | 0.5 | — | ns |
| $t_{DH}$ | Data Hold Time | 0.5 | — | ns |

**Notes:**
1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

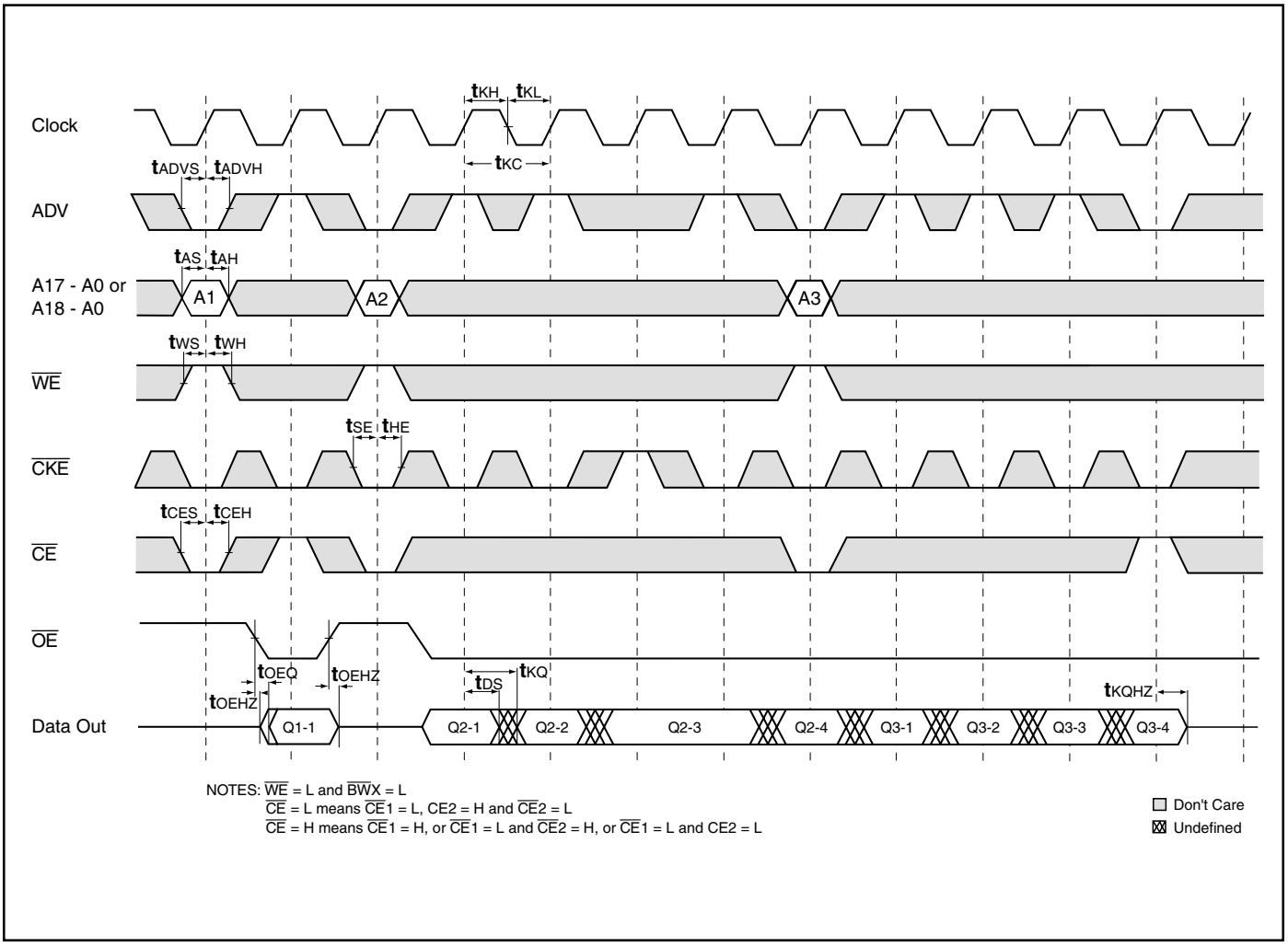
## SLEEP MODE ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{SB2}$ | Current during SLEEP MODE | ZZ ≥ Vih | — | 10 | mA |
| $t_{PDS}$ | ZZ active to input ignored | | 2 | — | cycle |
| $t_{PUS}$ | ZZ inactive to input sampled | | 2 | — | cycle |
| $t_{ZZI}$ | ZZ active to SLEEP current | | 2 | — | cycle |
| $t_{RZZI}$ | ZZ inactive to exit SLEEP current | | 0 | — | ns |

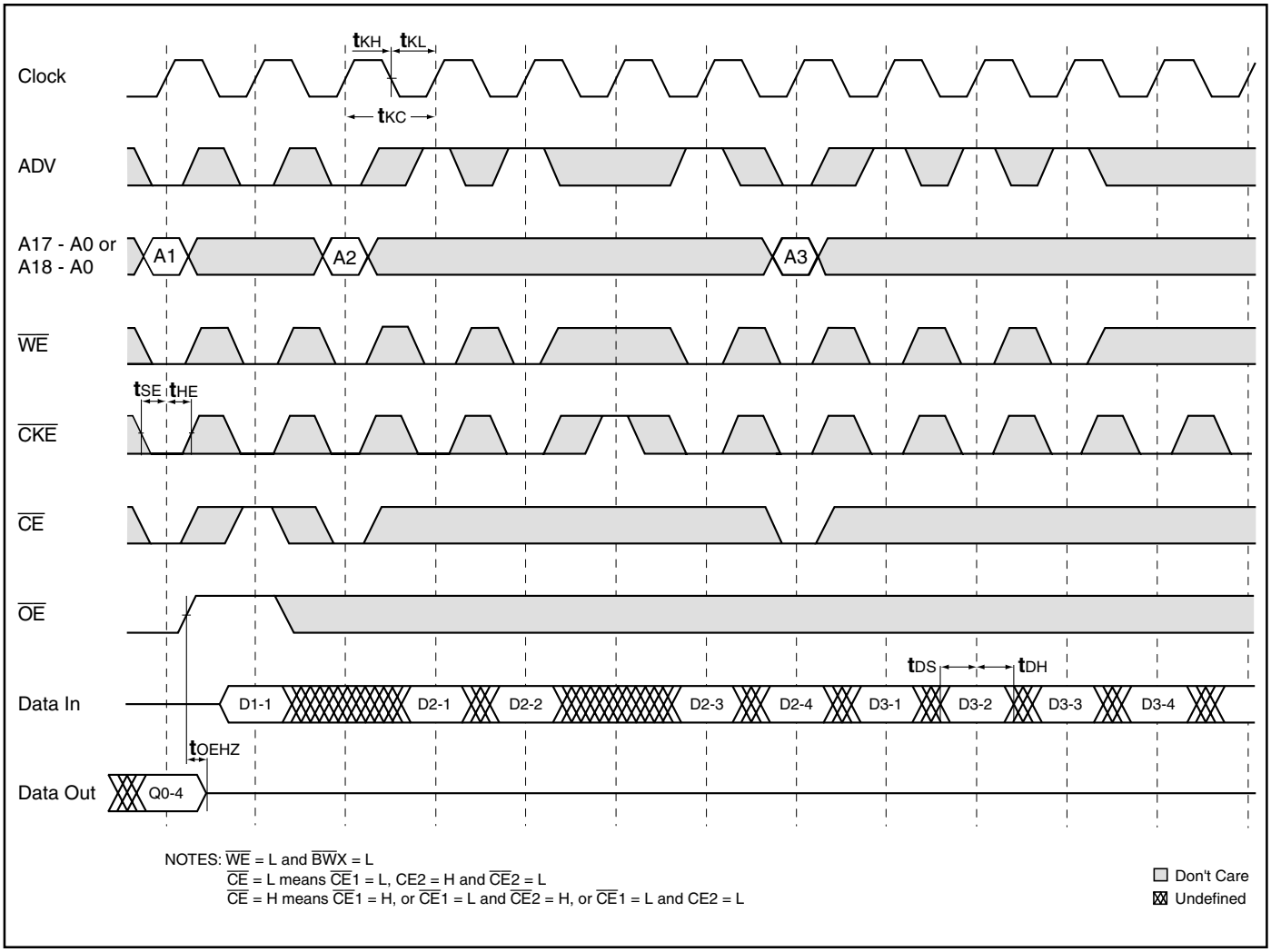
## SLEEP MODE TIMING



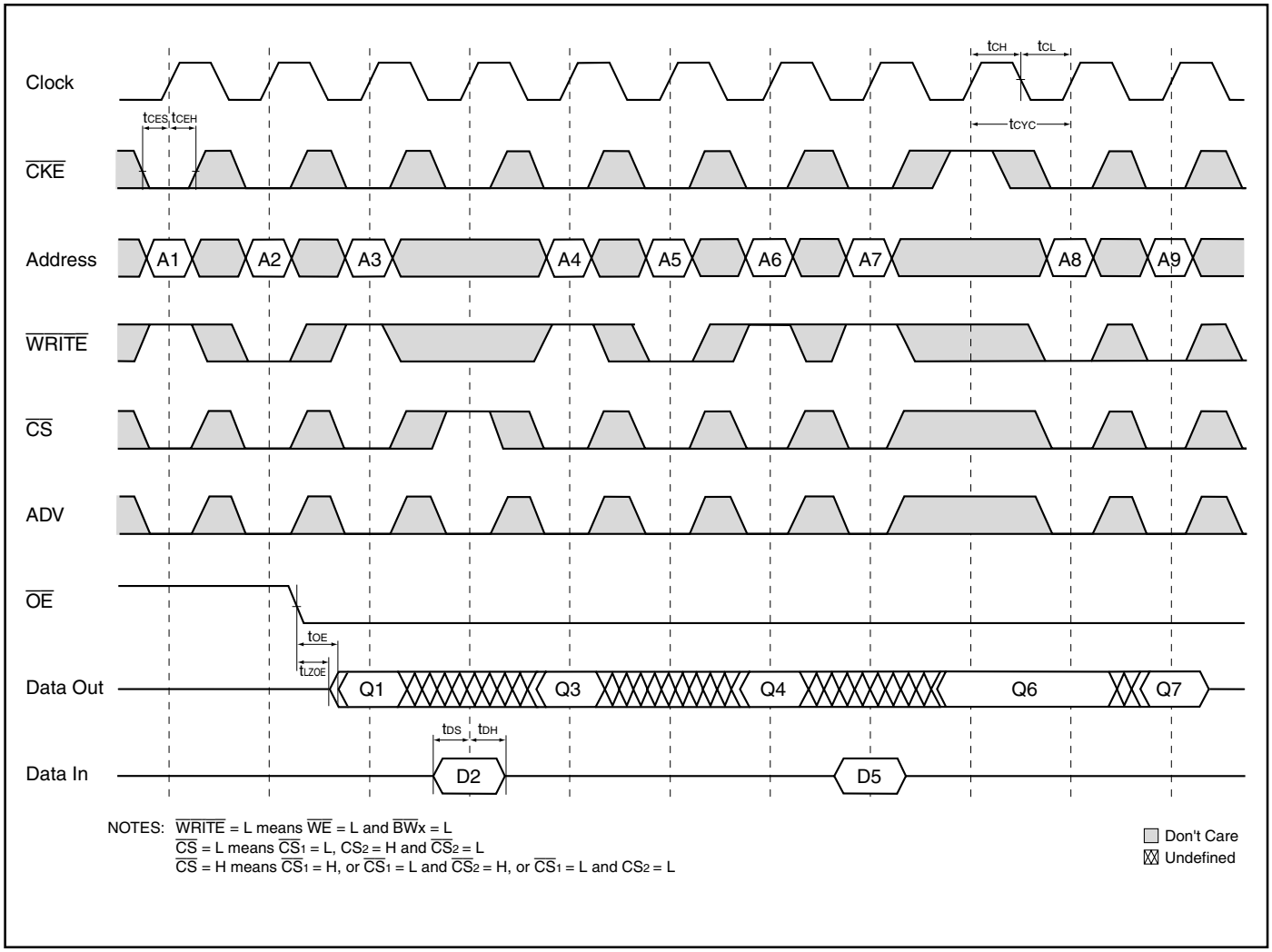
## READ CYCLE TIMING



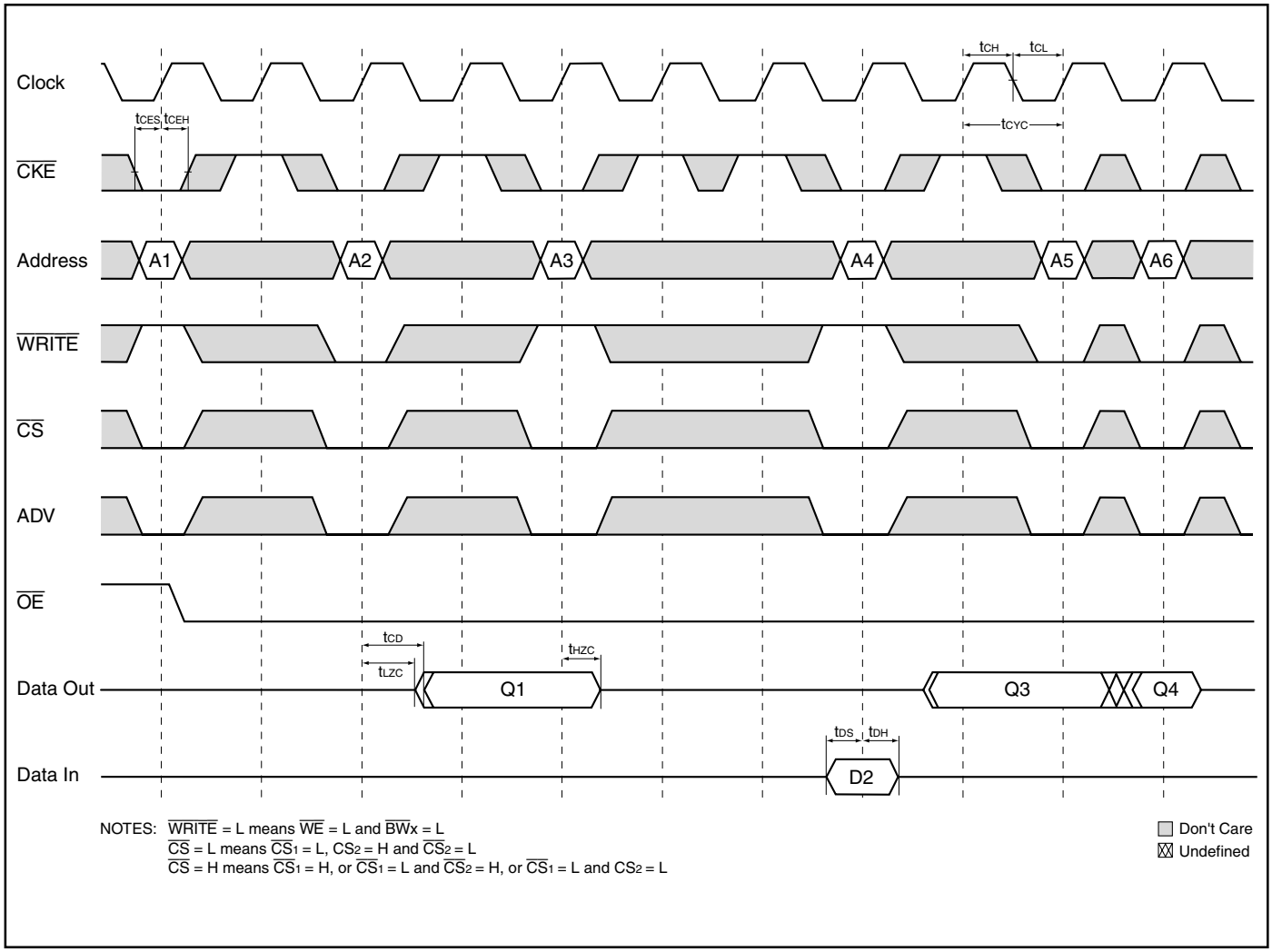
## WRITE CYCLE TIMING



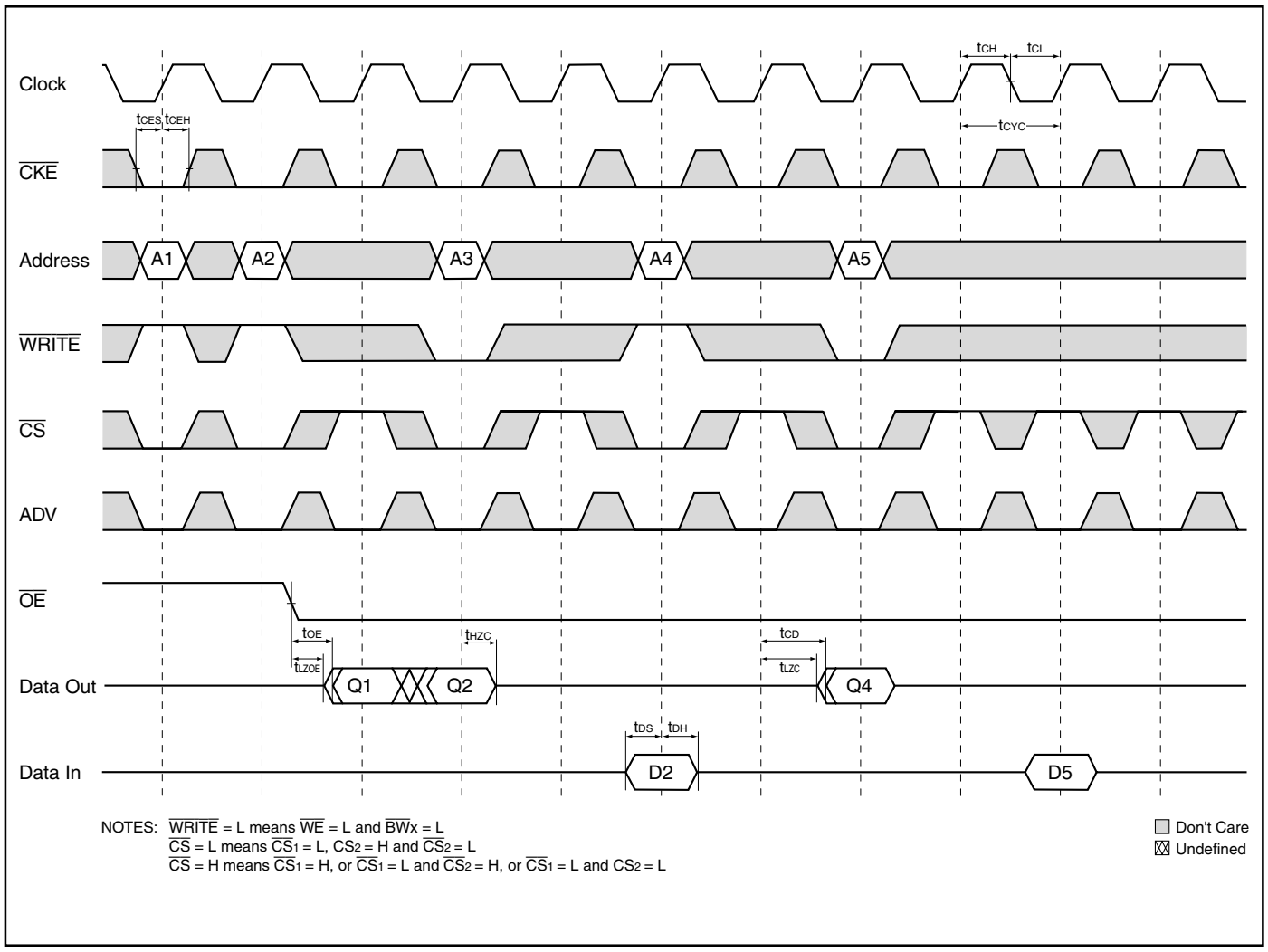
## SINGLE READ/WRITE CYCLE TIMING



## $\overline{CKE}$ OPERATION TIMING



## $\overline{CS}$ OPERATION TIMING



## ORDERING INFORMATION

### Commercial Range: 0°C to +70°C

| Frequency | Order Part Number | Package |
|---|---|---|
| **256Kx32** | | |
| 10 | IS61NF25632-10TQ | TQFP |
| | IS61NF25632-10B | PBGA |
| **256Kx36** | | |
| 10 | IS61NF25636-10TQ | TQFP |
| | IS61NF25636-10B | PBGA |
| **512Kx18** | | |
| 10 | IS61NF51218-10TQ | TQFP |
| | IS61NF51218-10B | PBGA |

### Industrial Range: -40°C to +85°C

| Frequency | Order Part Number | Package |
|---|---|---|
| **256Kx32** | | |
| 10 | IS61NF25632-10TQI | TQFP |
| | IS61NF25632-10BI | PBGA |
| **256Kx36** | | |
| 10 | IS61NF25636-10TQI | TQFP |
| | IS61NF25636-10BI | PBGA |
| **512Kx18** | | |
| 10 | IS61NF51218-10TQI | TQFP |
| | IS61NF51218-10BI | PBGA |

## ORDERING INLFORMATION

### Commercial Range: 0°C to +70°C

| Frequency | Order Part Number | Package |
|---|---|---|
| **256Kx32** | | |
| 10 | IS61NLF25632-10TQ | TQFP |
| | IS61NLF25632-10B | PBGA |
| **256Kx36** | | |
| 10 | IS61NLF25636-10TQ | TQFP |
| | IS61NLF25636-10B | PBGA |
| **512Kx18** | | |
| 10 | IS61NLF51218-10TQ | TQFP |
| | IS61NLF51218-10B | PBGA |

### Industrial Range: -40°C to +85°C

| Frequency | Order Part Number | Package |
|---|---|---|
| **256Kx32** | | |
| 10 | IS61NLF25632-10TQI | TQFP |
| 10 | IS61NLF25632-10BI | PBGA |
| **256Kx36** | | |
| 10 | IS61NLF25636-10TQI | TQFP |
| 10 | IS61NLF25636-10BI | PBGA |
| **512Kx18** | | |
| 10 | IS61NLF51218-10TQI | TQFP |
| 10 | IS61NLF51218-10BI | PBGA |

***Integrated Silicon Solution, Inc.***
2231 Lawson Lane
Santa Clara, CA 95054
Tel: 1-800-379-4774
Fax: (408) 588-0806
E-mail: sales@issi.com
**www.issi.com**