PRODUCT BRIEF*

AHA4541

311 MBITS/SEC TURBO PRODUCT CODE ENCODER/DECODER

The AHA4541 device is a single-chip Turbo Product Code (TPC) Forward Error Correction (FEC) Encoder/Decoder capable of 311 Mbit/sec data rates (up to 360 Mbit/sec channel rates). This device integrates both a TPC encoder and decoder, and can be operated in a full duplex mode. In addition to TPC coding, support is included for helical interleaving, synchronization mark insertion and detection, CRC computation, scrambling, and higher order modulation symbol mapping. Figure 1 shows the functional block diagram.

The channel interface supports direct connection to various modulators and demodulators. Support for an arbitrary constellation mapping is included with external logic.

The encode path accepts byte-wide data, computes and inserts a CRC, and scrambles the data before TPC encoding. After the error correction code (ECC) bits are inserted by the encoder, the data is helically interleaved, and block synchronization marks are inserted to assist the decoder. Finally, the data is mapped according to the constellation and output from the device.

The decoder accepts input symbols via the demodulated in-phase (I) and quadrature (Q) components or alternately as soft metric inputs from an external demodulator. An internal block synchronizer searches for synchronization marks, rotating the input symbol phase as necessary. After synchronization is achieved, the data is helically deinterleaved and decoded by the TPC decoder. The output of the decoder is descrambled, and the CRC is computed to verify data integrity. Decoded data is output in a parallel, byte-wide fashion.

Internal circuitry enables the transfer rate across all ports, generating a constant, non-burst data flow. In addition, control of an external VCO can be used to generate data clocks, greatly simplifying system clocking issues.

FEATURES

PERFORMANCE:

- Maximum 360 Mbit/sec channel rate
- Payload data rates of at least 311 Mbit/sec for code rates >0.86
- Symbol rates up to 90 MSym/sec
- Encode Latency of less than 10 clocks
- Integrated encoder/decoder; scrambler/descrambler; and interleaver/deinterleaver for full duplex operation
- Supports enhanced Turbo Product Codes (eTPCs)
- Corrections count and averaging for channel SNR estimation

FLEXIBILITY:

- Code Rates from .25 to 0.98
- Variable iterations up to 256 per block
- Block Sizes from 256 bits to 16 Kbits
- Programmable code shortening supports exact block sizes
- 32 bit CRC Insertion and Checking with programmable packet length

CHANNEL INTERFACE:

- Accepts in-phase and quadrature (I & Q) inputs, up to 8 bits each
- Supports soft metric inputs at up to 4 soft metrics of 4 bits each
- Soft metric computation for BPSK, QPSK, 8-PSK, 16-QAM, 64-QAM, and 256-QAM
- Supports additional modulation formats with external logic
- Encoder and decoder pass through modes
- Programmable packet and block level synchronization
- Automatic phase ambiguity resolution
- Supports insertion and detection of sync marks up to 32 bits in length
- 8-bit Parallel Data Input/Output
- Support for external VCO to generate data clocks

OTHERS:

- Intel or Motorola microprocessor interface
- 3.3V I/O, 1.8V core operation
- Commercial or Industrial temperature rating

This product is covered under multiple patents held or licensed by Comtech AHA Corp. This product is covered by a Turbo Code Patent License from France Telecom - TDF - Groupe des ecoles des telecommunications.

**Request the AHA4541 Product Specification for complete details.*

CODE TYPES

Table 1 shows a partial list of the codes supported by this product. Note that this is not a complete list of base codes. In addition, each of the codes listed can be shortened to achieve smaller block size with only minor changes to code rate.

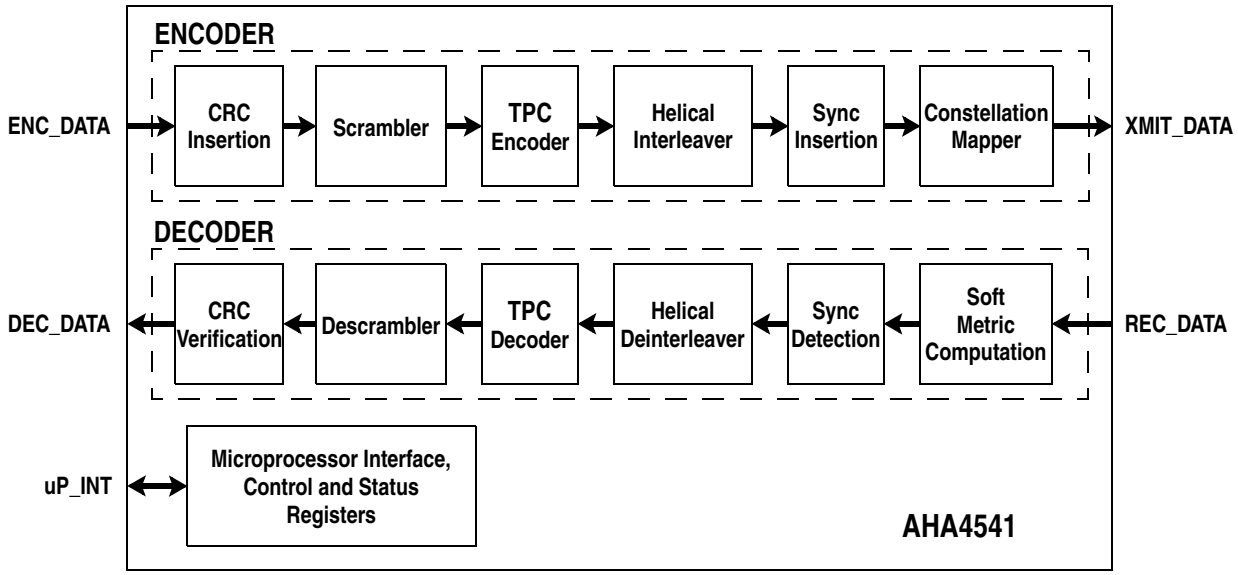
Table 1: Partial Code List

CODE (X)x(Y)x(Z)	*BLOCK SIZE (bits)*	*DATA SIZE (bits)*	*RATE*	*CODING GAIN (dB)*
(128,127)x(128,126)+	16384	16002	0.977	4.3*
(128,120)x(128,126)+	16384	15120	0.923	5.5*
(128,120)x(128,120)	16384	14400	0.879	6.6*
(64,57)x(16,15)x(16,15)	16384	12825	0.783	7.2
(128,127)x(64,62)+	8192	7874	0.961	4.4*
(128,120)x(64,62)+	8192	7440	0.908	5.5*
(128,120)x(64,57)	8192	6840	0.84	6.8
(32,26)x(16,15)x(16,15)	8192	5850	0.714	7.2
(64,63)x(64,62)+	4096	3906	0.954	4.5*
(64,57)x(64,57)	4096	3249	0.793	7.1
(64,63)x(32,30)+	2048	1890	0.923	4.5*
(64,57)x(32,26)	2048	1482	0.724	6.9
(32,26)x(32,26)	1024	676	0.660	6.3

* *Estimated Coding Gain is measured on a Binary Input Additive White Gaussian Noise (AWGN) channel at 10^{-6} Bit Error Rate (BER) with maximum decoder iterations that support a data rate of 311 Mbps. Only TPC codes with code rates above 0.86 meet the 311 Mbps data rate.*

\+ *enhanced TPC (includes hyper diagonal axis).*

Figure 1: Turbo Product Code Encoder/Decoder



FUNCTIONAL OVERVIEW

The channel encoder is designed to input data in a byte-wide fashion. This data is CRC encoded and randomized before coding by the TPC encoder. Synchronization marks are then inserted into the data before it is mapped to a user programmable constellation. The blocks may be bypassed if not needed.

Each symbol for modulation is output synchronous to the transmit clock, with one symbol transferred for each rising edge of the clock. The format for output data depends on the modulation format chosen.

The channel decode data path begins with received symbols input to the device synchronous to the receive clock, with one symbol transferred per rising edge.

When using internal soft metric computation, the input data is an I and Q sample value for the given symbol. The soft metric computation engine converts each I and Q sample to the soft metrics required by the TPC decoder.

When soft metric computation is disabled, the input data is a soft metric value for each bit in the TPC block with up to 4 bits transferred on each clock edge. Each bit would consist of up to 4 confidence bits per data bit. If enabled, all synchronization is controlled by the device including phase ambiguity resolution. Output is in a byte wide fashion with packet start, end and error signals.

CODE PERFORMANCE

Figure 2: Bit Error Rate (BER) Performance (simulated) on a QPSK Channel

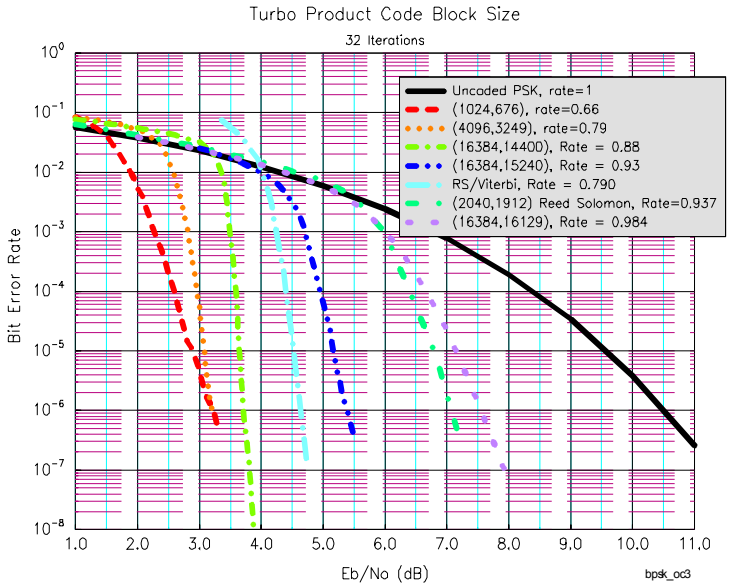
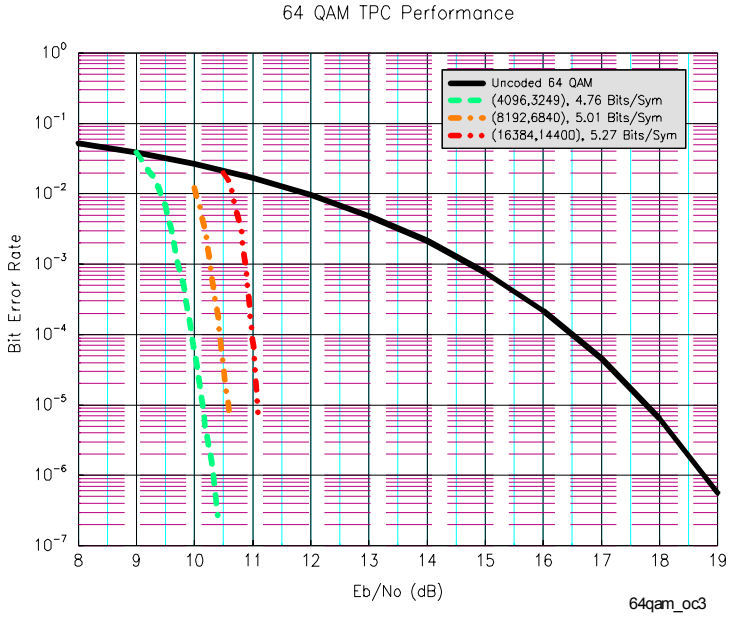


Figure 3: Performance (simulated) of Several Codes on a 64 QAM System



ORDERING INFORMATION

PART NUMBER	*DESCRIPTION*
AHA4541A-PQC	311 Mbit/sec Turbo Product Code Encoder/Decoder - Commercial Temp
AHA4541A-PQI	311 Mbit/sec Turbo Product Code Encoder/Decoder - Industrial Temp

ABOUT AHA

Comtech AHA Corporation (AHA) develops and markets superior integrated circuits, boards, and intellectual property core technology for communications systems architects worldwide. AHA has been setting the standard in Forward Error Correction and Lossless Data Compression technology for many years and provides flexible, cost-effective solutions for today's growing bandwidth and reliability challenges. Comtech AHA Corporation is a wholly owned subsidiary of Comtech Telecommuncations Corp. (NASDAQ: CMTL). For more information, visit www.aha.com.

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