Digital combo multi-mode PFC and time-shift LLC resonant controller



Product status link
STNRG011A

Product summary		
Order code	STNRG011A	STNRG011ATR
Package	SO20	
Packing	Tube	Tape & Reel

Product label
SUSTAINABLE TECHNOLOGY

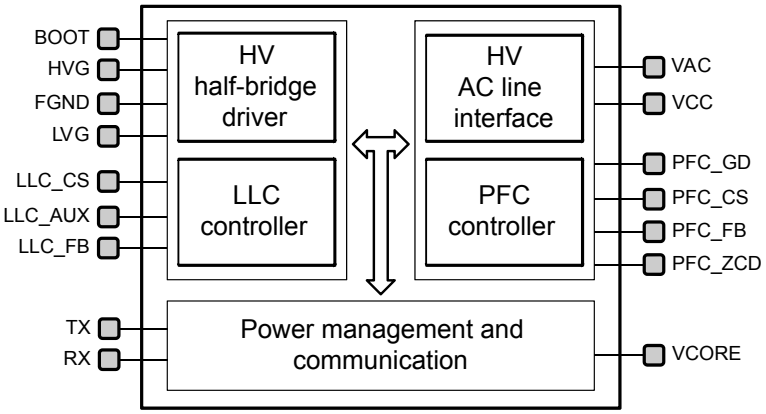
Features

- Digital combo multi-mode PFC + time-shift LLC resonant half-bridge controller
- Onboard 800 V startup circuit, line sense and X-cap discharge compliant with IEC 62368-1, for reduced standby power
- Enhanced fixed on time multi-mode TM PFC controller with input voltage feed-forward, THD optimizer and frequency limitation
- Complete set of PFC protections
- Time-shift control of resonant half-bridge
- Enhanced burst-mode at light load with fast transient response and line adaptive half- bridge brown-out protection
- Complete set of half-bridge protections
- Available in SO20 package

Applications

- Open frame SMPS
- Flat screen TV SMPS
- ATX power supply
- AC-DC adapter

Figure 1. Block diagram



1 Description

The STNRG011A embodies a multi-mode (transition-mode and DCM) PFC controller, a high- voltage double-ended controller for the LLC resonant half-bridge, an 800 V-rated startup generator and a sophisticated digital engine, that manage optimal operation of three blocks.

The STNRG011A manages only input line AC.

The device comes in a 20-pin SO package and offers an advanced solution for power- factor-corrected high-efficiency converters supposed to comply with the most stringent energy saving regulations.

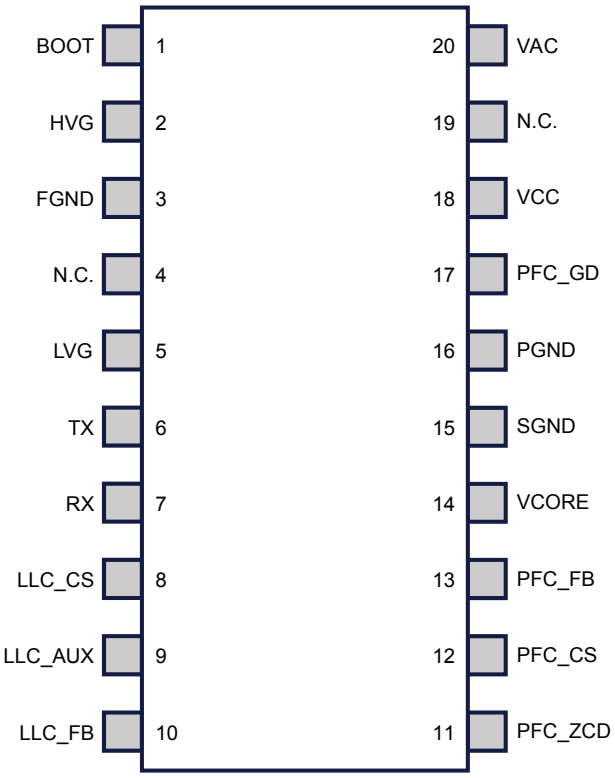
The power system and the control algorithms are managed by an 8-bit core with dedicated fast peripherals (SMED). Optimized digital algorithms together with HW analog IPs are implemented to guarantee a very high performance, BOM optimization and robustness.

The digital algorithms are stored into an internal ROM memory and all key application parameters can be stored into a device's NVM (non-volatile memory) memory during the production phase allowing wide configurability and calibration.

The device can also externally communicate through a 2-pin UART, allowing the monitoring function, the black box storing into an external E2PROM and the software patch upload from the external E2PROM.

2 Pin connection

Figure 2. **Pin connection (top view)**



3 Absolute maximum ratings and thermal data

Table 1. Absolute maximum ratings

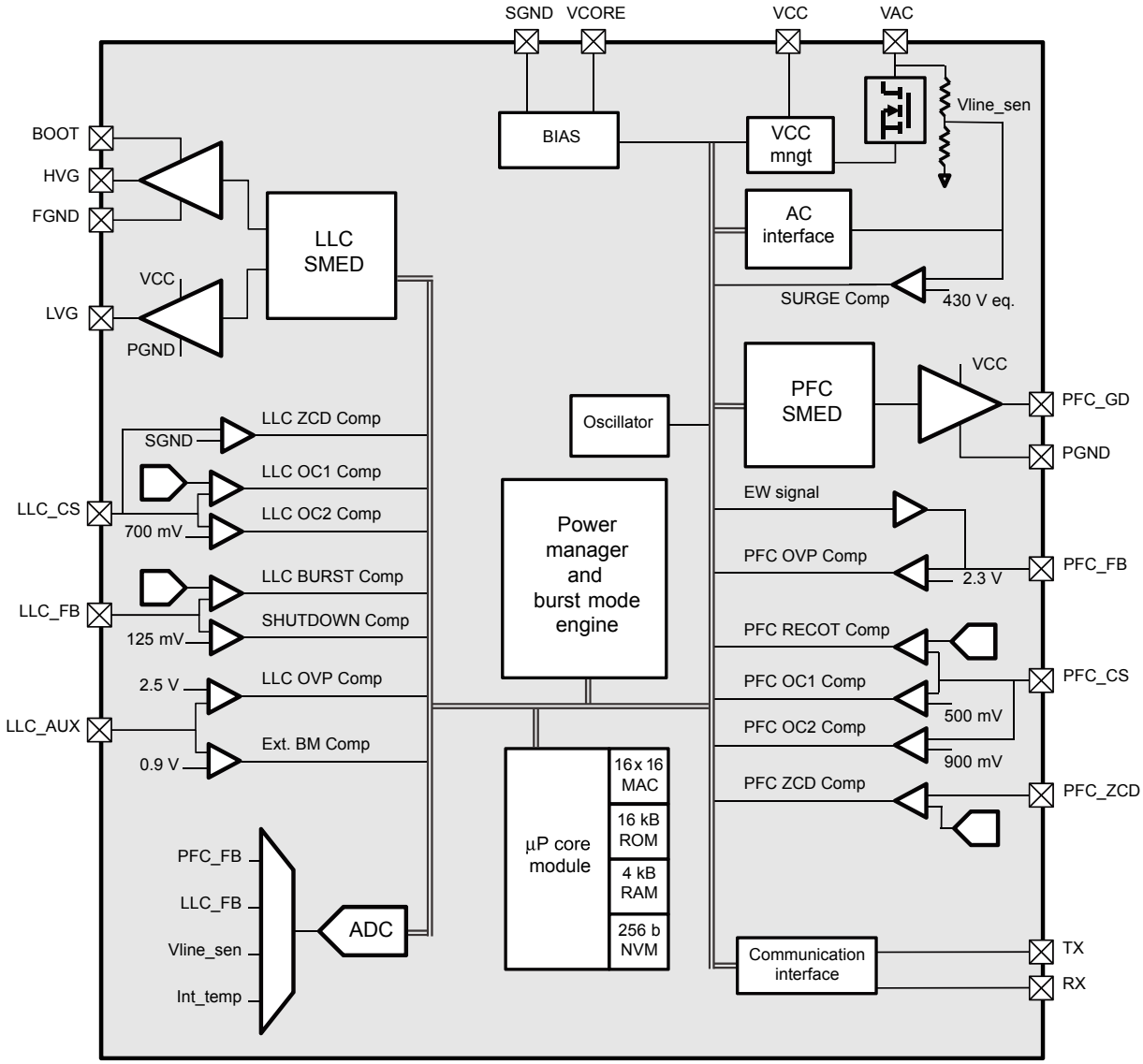
Symbol	Pin	Parameter	Value	Unit
V_{VAC}	VAC	Voltage range	-1 to 800	V
V_{BOOT}	BOOT	Floating supply voltage, referred to GND	-0.3 to 600 + VCC	V
V_{FGND}	FGND	Floating ground voltage, connected to the half-bridge node	-3 up to a value included in the range BOOT - VCC and BOOT +0.3	V
dV_{FGND} /dt	FGND	Floating ground max. slew rate	50	V/ns
V_{HVG}	HVG	HVG voltage	FGND -0.3 to BOOT +0.3	V
V_{VCC}	VCC	IC supply voltage	-0.3 to 19	V
V_{LVG} V_{PFC_GD}	LVG, PFC_GD	Voltage range	-0.3 to VCC	V
V_{VCORE}	VCORE	Voltage range	-0.3 to 5.5	V
I_{PFC_CS}, I_{LLC_CS}, I_{PFC_ZCD},	PFC_CS, LLC_CS, PFC_ZCD	Clamped source current (pin voltage: < 0 V, self-limited)	2	mA
V_{PFC_CS}, V_{LLC_CS}, V_{PFC_ZCD}	PFC_CS, LLC_CS, PFC_ZCD	Positive voltage range	VCORE +0.3	V
V_{PFC_FB}, V_{LLC_FB}	PFC_FB. LLC_FB	Voltage range	-0.3 to VCORE +0.3	V
V_{RX}	RX	Voltage range	-0.3 to VCORE +0.3	V
V_{TX}	TX	Voltage range	-0.3 to VCORE+ 0.3	V

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Max. thermal resistance, junction to ambient	120	°C/W
T_j	Junction temperature operating range	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

4 Detailed block diagram

Figure 3. **Detailed block diagram**



5 Pin function

Table 3. Pin function detailed description

No.	Name	Function
1	BOOT	High-side gate-drive floating supply voltage. The bootstrap capacitor is connected between this pin and FGND. A fast diode has to be connected from this pin and VCC to guarantee recharge of the bootstrap capacitor.
2	HVG	High-side gate-drive output. The driver is capable of 0.5 A source and 0.75 A sink peak current (minimum values) to drive the upper MOSFET of the half-bridge leg. A resistor internally connected to FGND ensures that the pin is never floating.
3	FGND	High-side gate-drive floating ground. It is the return path for the high-side gate-drive current. Layout carefully the connection of this pin to avoid too large spikes below ground.
4	N.C.	High-voltage spacer. The pin is not internally connected to isolate the high-voltage section and ease compliance with safety regulations (creepage distance) on the PCB.
5	LVG	Low-side gate-drive output. The driver is capable of 0.5 A source and 0.75 A sink peak current (minimum values) to drive the lower MOSFET of the half-bridge leg. The pin is actively pulled to GND during UVLO.
6	TX	TX pin for UART/SDA pin for I_2C interface
7	RX	RX pin for UART/SCL pin for I_2C interface
8	LLC_CS	LLC tank current sensing input. A voltage proportional to the tank current (usually obtained with a capacitive divider) has to be applied to this pin. The information is used for zero-crossing detection (required by time-shift algorithm), the first and second level OCP.
9	LLC_AUX	LLC_AUX is connected to a divider sensing the auxiliary voltage from the LLC transformer. The LLC OVP detection is active on this pin.
10	LLC_FB	The voltage from this pin is used as the LLC feedback voltage. It has to be connected to the feedback phototransistor collector and a pull-up resistor to VCORE.
11	PFC_ZCD	PFC ZCD input, connected to the PFC AUX winding through a resistor divider detecting the PFC inductor demagnetization.
12	PFC_CS	Current sense input for PFC. The current flowing in the MOSFET is sensed through a resistor, and the resulting voltage is applied to this pin. After GD turns on, a first voltage threshold cross allows enhanced COT control implementation. A second level can be detected for overcurrent protection.
13	PFC_FB	Input for PFC output voltage. It is used for closing the PFC loop and OVP protection. It has to be connected with a voltage divider to the bulk capacitor. If the early warning feature is enabled this pin is brought to 5 V when the EW pulse is released.
14	VCORE	Internal VCORE bypass capacitor connection.
15	SGND	Signal ground. Reference ground for analog signals.
16	PGND	Power ground. Current return for the PFC gate-driver and the low-side gate-driver of the half- bridge. Keep the PCB trace that goes from this pin to the sources of the PFC and the low-side MOSFETs separate from the trace that collects the grounding of the bias components.
17	PFC_GD	PFC gate-driver output. The output stage is able to drive power MOSFETs, it is capable of 0.7 A source current and 0.8 A sink current (minimum values).

No.	Name	Function
18	VCC	Supply voltage of both the signal part of the IC and the gate-drivers. A bypass capacitor to GND is necessary to sustain the IC during startup and low power modes. The voltage on the pin is internally clamped to protect the internal circuits from temporary excessive supply voltages.
19	N.C.	The pin is not internally connected to isolate the high-voltage section and ease compliance with safety regulations (creepage distance) on the PCB.
20	VAC	High-voltage startup generator input. The pin has to be connected directly to the mains voltage through two dedicated diodes. If the voltage on the pin is higher than 50 V, an internal current source charges the capacitor connected between the pin VCC and GND until the voltage on the VCC pin reaches the startup threshold. Normally, the generator is re-enabled when the voltage on the VCC pin falls below the UVLO threshold. The pin is also used as the line voltage sensing input. This pin is internally connected to a 20 MΩ resistor divider. It is used for all line sense related functions: the AC brown-out, surge detection, line disconnection, input voltage feed-forward, line synchronization. When a line disconnection is detected, the internal current source is activated to discharge the X-capacitor.

6 Electrical characteristics

Tj = 0 to +125 °C, V_{CC} = V_{BOOT} = 15 V, C_{HVG} = C_{LVG} = C_{PFC_GD} = 1 nF; unless otherwise specified.

Note: Adjust Vcc above Vcc_{On} before setting at 15 V.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage						
Vccz	Vcc clamp voltage	-	19	-	-	V
Vcc	Operating range	After turn-on	9.5	-	19	V
Vcc_{On}	Processing turn-on threshold	Voltage rising(1)	16	17	18	V
Vcc_{Off}	Processing turn-off threshold	Voltage falling(1)	8	8.7	9.4	V
Hys	Hysteresis	-	-	8.3	-	V
Vcc_{CoreOn}	VCC threshold for VCore turn-on	Voltage rising(1)	-	8	-	V
$Vcc_{CoreOff}$	VCC threshold for VCore turn-off	Voltage falling(1)	-	7	-	V
VCore	Operating range	I_{source} 0 to 1 mA	4.75	-	5.25	V
Supply current						
I_{Vccs}	Quiescent current during sleep (BM)	T 25 °C	-	0.5	-	mA
I_{Vccop}	Operating supply current at f_{sw} = 50 kHz, C = 1 nF, VCC = 12 V	PFC and LLC off	-	18	-	mA
		PFC driver only (during PFC SS)	-	20	-	
		All drivers	-	22	-	
High-voltage startup generator						
V_{VAC_BR}	Breakdown voltage	I_{HV} < 50 µA V_{CC} > Vcc_{On}	800	-	-	V
I_{VAC_on}	ON-state VAC input current	V_{VAC} > 40 V V_{CC} < 0.8 V	-	1	-	mA
		V_{VAC} > 40 V 0.8 V < V_{CC} < Vcc_{CoreOn}	-	6	-	
		V_{VAC} > 100 V Vcc_{CoreOn} < V_{CC} < 14 V	-	6	-	
		V_{VAC} > 100 V 14 V < V_{CC} < Vcc_{On}	-	4	-	
		40 V < V_{VAC} < 100 V Vcc_{CoreOn} < V_{CC} < 14 V	-	20	-	
		40 V < V_{VAC} < 100 V 14 V < V_{CC} < Vcc_{On}	-	10	-	
I_{Vcc_charge}	ON-state VCC charge current	V_{VAC} > 40 V V_{CC} < 0.8 V	-0.5	-0.75	-1.3	mA
		V_{VAC} > 40 V 0.8 V < V_{CC} < Vcc_{CoreOn}	-3.5	-5	-8	

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{Vcc_charge}	ON-state VCC charge current	V_{VAC} > 100 V Vcc_{CoreOn} < V_{CC} < 14 V	-	-5	-	mA
		V_{VAC} > 100 V 14 V < V_{CC} < Vcc_{On}	-	-3.5	-	
		40 V < V_{VAC} < 100 V Vcc_{CoreOn} < V_{CC} < 14 V	-	-18	-	
		40 V < V_{VAC} < 100 V 14 V < V_{CC} < Vcc_{On}	-	-8	-	
I_{VAC_off}	OFF-state VAC input current	V_{VAC} = 400 V, V_{CC} > Vcc_{On}	-	20	40	µA
$I_{VAC_HV_SINK}$	VAC reading improvement current	V_{VAC} = 100 V	-	100	-	µA
PFC - gate-driver						
V_{OL}	Output low voltage	I_{sink} = 100 mA	-	-	0.7	V
V_{OH}	Output high voltage	I_{source} = -10 mA V_{CC} = 10 V, V_{CC} = 18 V	 9.85 17.9	 9.95 17.95	 - -	V
I_{srcpk}	Peak source current	Cgate = 4.7 nF(2)	-0.7	-1.1	-	A
I_{snkpk}	Peak sink current	Cgate = 4.7 nF(2)	0.8	1.3	-	A
t_f	Voltage fall time	-	-	25	-	ns
t_r	Voltage rise time	-	-	30	-	ns
PFC_GD_uvlo	UVLO saturation	V_{CC} = 0 to Vcc_{On}, I_{sink} = 1 mA	-	0.9	1.15	V
Low-side gate-driver (voltages referred to GND)						
V_{OL}	Output low voltage	I_{sink} = 100 mA	-	-	0.7	V
V_{OH}	Output high voltage	I_{source} = -10 mA V_{CC} = 10 V V_{CC} = 18 V	 9.85 17.85	 9.9 17.9	 - -	V
I_{srcpk}	Peak source current	Cgate = 4.7 nF(2)	-0.5	-0.8	-	A
I_{snkpk}	Peak sink current	Cgate = 4.7 nF(2)	0.75	1.2	-	A
t_f	Voltage fall time	-	-	25	-	ns
t_r	Voltage rise time	-	-	40	-	ns
LVG_uvlo	UVLO saturation	V_{CC} = 0 to Vcc_{On}, I_{sink} = 1 mA	-	0.9	1.1	V
High-side gate-driver (voltages referred to FGND)						
V_{OL}	Output low voltage	I_{sink} = 100 mA	-	-	0.7	V
V_{OH}	Output high voltage	I_{source} = -10 mA V_{BOOT}= 10 V, V_{BOOT} = 18 V	9.85 17.85	9.9 17.9	- -	V
I_{srcpk}	Peak source current	Cgate = 4.7 nF(2)	-0.5	-0.8	-	A
I_{snkpk}	Peak sink current	Cgate = 4.7 nF(2)	0.75	1.2	-	A
t_f	Voltage fall time	-	-	25	-	ns
t_r	Voltage rise time	-	-	40	-	ns

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
HVG_pdw	HVG-FGND pull-down resistor	-	-	25	-	kΩ
I_{FGND}	Current from V_{BOOT} to FGND	V_{BOOT} = 200 V	-	1.5	-	µA
X-CAP discharge						
XCD_inact_time	Inactivity detection time	-	-	50	-	ms
I_{XCD}	Discharge current	-	4	-	-	mA
Brown-in/out						
BI	TH	Vline rising	112	114	116	V
BO		Vline falling	-	108	-	V
BIBO_H	HYST	-	5.25	6	6.75	V
BO_mask	Brown-out time	-	-	45	-	ms
Overtemperature (by design)						
OTP	TH	T rising	130	140	150	°C
	HYST	T falling	-	-30	-	°C
CK						
Fck	System clock in run mode	-	57	60	63.7	MHz
ADC						
ADC_res	Resolution	Vin ADC > 50 mV	-	10	-	bit
FSR_L	Conversion range	CS	0	-	1.5	V
FSR_H		Other	0	-	2.5	V
DNL	Differential non linearity	Vin ADC > 50 mV	-	±1.5	-	lsb
Fck_ADC	Clock frequency	Vin ADC > 50 mV	-	15	-	MHz
Ts	Sampling time	Vin ADC > 50 mV	-	7	-	ADC Ck cycles
Tc	Total conversion time (sampling included)	Vin ADC > 50 mV	-	18	-	ADC Ck cycles
Comparators						
PFC_CS RECOT[3]	TH RISING (DAC 6 bits)	Input pin PFC_CS	FSR = 125 STEP = 1.95			mV
	HYST		5			
PFC_CS OC1	TH RISING	Input pin PFC_CS	-	500	-	mV
	TH FALLING		-	450	-	
PFC_CS OC2	TH RISING	Input pin PFC_CS	-	900	-	mV
	TH FALLING		-	850	-	
PFC_ZCD ZCD[3]	TH FALLING (TH_F)	Input pin PFC_ZCD	0/50/100/200			mV
	TH RISING (TH_R)		210/110[4]/310/ TH_F +10			
PFC_FB OVP	TH RISING	Input pin PFC_FB	-	2.33	-	V
	HYST		-	75	-	mV
LLC_FB[3] BURST	TH RISING	Input pin LLC_FB	0.75/1/1.25			V
	HYST		5/10			mV
LLC_FB SHUTDOWN	TH RISING	Input pin LLC_FB	-	145	-	mV

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
LLC_FB SHUTDOWN	TH FALLING	Input pin LLC_FB	-	125	-	mV
LLC_AUX OVP	TH RISING	Input pin LLC_AUX	-	2.5	-	V
	TH FALLING		-	2.4	-	
LLC_AUX Ext. BM	TH RISING	Input pin LLC_AUX	-	0.9	-	V
	TH FALLING		-	0.8	-	
LINE SURGE	TH RISING	Input pin VAC	-	430	-	V
	TH FALLING		-	410	-	
LLC_CS OC1[3]	TH RISING	Input pin LLC_CS	FSR = 500 STEP = 15.6			mV
	HYST		20			
LLC_CS OC2	TH RISING	Input pin LLC_CS	-	700	-	mV
	TH FALLING		-	650	-	

1. *Parameters tracking each other.*
2. *Guaranteed by design, not production tested.*
3. *Thresholds and hysteresis are programmed by the software in use.*
4. *The selection for TH_R = 110 mV is not allowed if TH_F = 200 mV.*

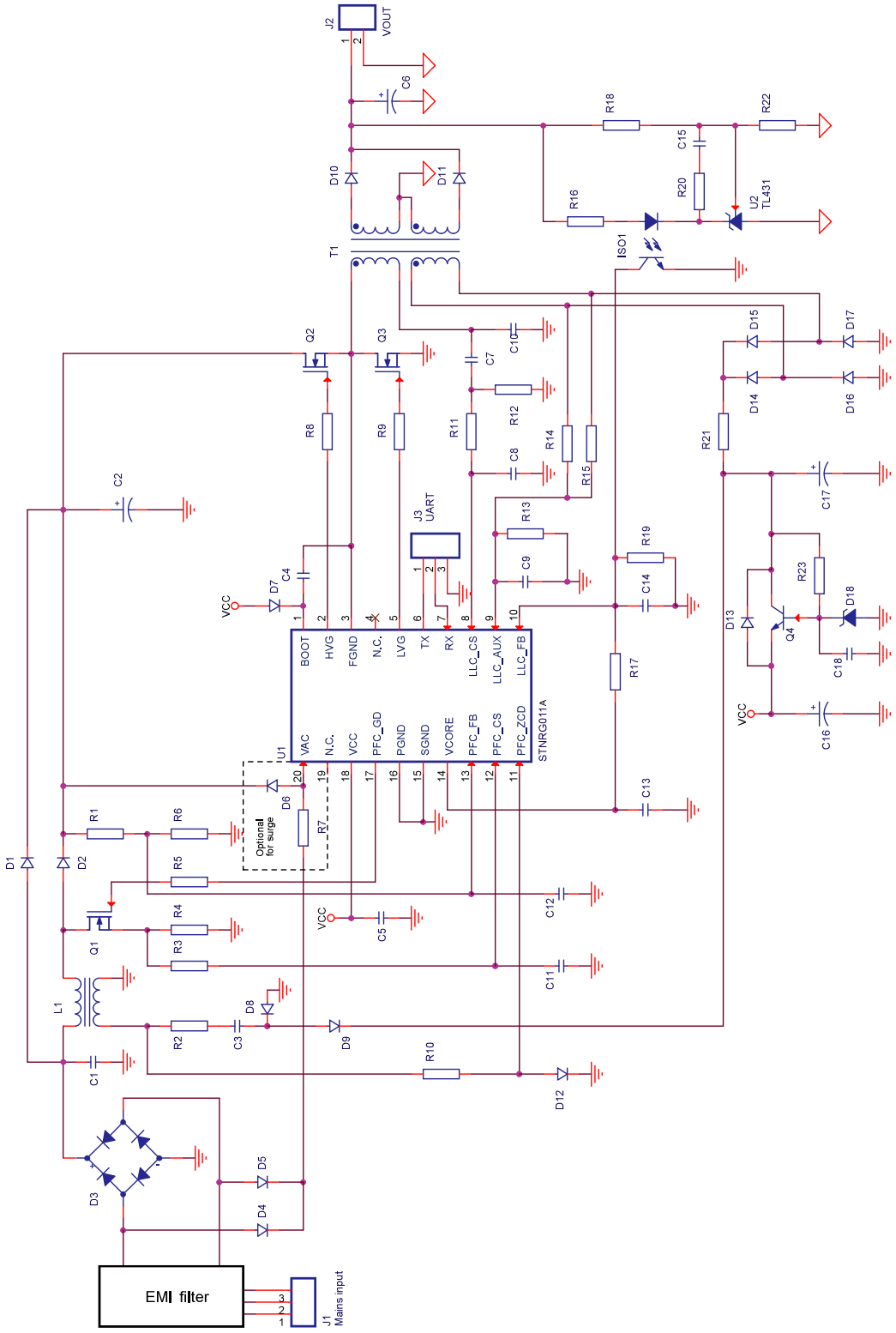
7 Safety data

Table 5. **X-Cap discharge safety data according to IEC 62368**

Parameter	Value
Maximum line voltage	240 Vrms + 10%
Overvoltage category	II
External capacitor value	0.1 µF - 2.2 µF
Series resistor value	20 Ω - 100 Ω

8 Application schematics

Figure 4. **Typical application schematic**



9 Architecture

The PFC and LLC external MOSFETs gates are managed by the “State Machine Event Driven” (SMEDs): 2 for PFC (PFC SMEDs) and 2 for LLC (LLC SMEDs).

The SMEDs are programmable state machine driven by events:

- External events
  - Analog comparators outputs
  - Power manager generated events (protections)
- Internal events
  - Timer events

PFC **SMEDs**

- Input events: PFC RECOT, PFC OC1, PFC ZCD
- Outputs: PFC_GD

LLC SMEDs

- Input events: LLC ZCD
- Outputs: LVG, HVG

The **µP subsystem** dynamically manages the control loop.

- Analog comparators thresholds setting
- SMED configuration
- SMED timers
- ADC scheduler
- Interrupt management

The multichannel **ADC** is controlled by a programmable event driven scheduler: sampling sequence can be configured and every sample can be triggered by a specific SMED state occurrence and an internal timer value. Different priorities can be programmed to allow fast sampling for real time control and slow sampling for state control (i.e., temperature).

The scheduler can be programmed to generate interrupts after completion of selectable conversions.

A dedicated **AC line monitor** easily follows the AC line providing system triggers.

The µP reads data from the ADC and performs the loop calculation with the support of a dedicated 16-b x 16-b multiplier and a 32-b accumulator unit.

A **Power management and burst-mode machine** manages the system power state in order to have very low idle consumption and fast activity restart during the burst-mode operation.

Hard protections are managed with a very low propagation delay; the protection enable and the latched/not latched response are programmable.

The power manager controls also the brown-in/out, VCC charge/discharge, AC monitor and X-cap discharge.

A **Watchdog** resets the system in case of missed µP signal for a long time.

A **communication peripheral** allows serial communication at startup and during the normal operation for:

- External memory communication for
  - Black box external recording
  - Patch SW upload
- Monitoring
- Internal memory R/W and OTP management
- Test mode

10 Functional description

The main functions are:

- HV startup and VCC management
- Line monitor and protection
- Drivers
- PFC control and fault management
- Resonant LLC HB control and fault management
- Power management
- Communication and configuration

10.1 HV startup and VCC management

The VAC pin voltage is a rectified sine wave at 100 Hz/120 Hz, connected to the mains AC line (Vline) through two dedicated diodes. The VAC pin is the device supply at the startup.

The VAC pin voltage is different from the PFC power path (Vin) where big caps are connected: the VAC pin partially follows the Vline also at no load condition while the Vin could be very close to a DC; this assumption allows to detect the AC line disconnection to implement the X-cap discharge function.

At the VAC pin a HV DMOS is internally connected to charge the capacitor connected to the VCC pin.

From the VCC pin an internal LDO provides the 5 V VCore for analog and digital circuitry; the digital section is supplied by the internal LDO from the VCORE pin.

At startup, from the HV DMOS the capacitor connected to the VCC pin is charged to provide the power supply to the whole device; then the HV DMOS is turned off.

The VCC pin starts sourcing current to the connected capacitor after a minimum 15 V VAC pin voltage.

The VCC capacitor charge current is limited to 0.75 mA during the first charge phase to limit the temperature increase in case the VCC pin is short-circuited at startup. After the VCC pin voltage is above 0.8 V, the charging current rises to 5 mA.

VCORE pin voltage rises when the VCC pin crosses 8 V (Vcc_{CoreOn}). There is a VCORE overload protection that limits the VCC charging current below 1 mA in case the VCORE pin is short-circuited at startup. Then the VCC capacitor charge continues with an average current higher than 6 mA: the current is increased during the time the VAC pin voltage is below 100 V.

Once the VCC pin crosses the 17 V Vcc_{On} rising threshold the HV DMOS turns off and the whole device starts working: the µP boots.

If the VCC pin goes below the 9 V Vcc_{Off} falling threshold (UVLO threshold) the µP stops working and the HV DMOS turns on again.

If the VCC pin falls below 7 V ($Vcc_{CoreOff}$) the device stops working and the capacitor connected to the VCORE pin discharges. The VCC pin can rise again only after the voltage on the VCORE pin falls below 1 V.

The worst-case average charging current from the 0.8 V to the Vcc_{On} threshold is estimated in 4.63 mA and 4.11 mA, in case the mains voltage is 115 Vac - 60 Hz and 230 Vac - 50 Hz respectively.

10.2 AC line monitor and protection

A HV voltage divider is internally connected to the VAC pin to generate Vline_sense for the AC line monitoring and protection:

- Brown-in/out
- Line synchronization
- Line disconnection and X-cap discharge
- Surge detection and stop
- Line monitor for PFC control

10.2.1 Brown-in/out

Brown-in and -out functions are implemented based on the Vline_sense information. The peak VAC voltage is monitored to enable and disable the PFC.

The PFC is enabled when the AC line crosses the brown-in threshold. The PFC is disabled after 45 ms the AC line is below the brown-out threshold.

In order to improve AC line reading and avoid false brown-in, the HV DMOS is turned on sinking IXCD current for 100 ms in case of brown-out or line disconnection events. This function can be enabled / disabled through the dedicated NVM bit.

10.2.2 Line synchronization

A dedicated digital peripheral manages the PFC synchronization with the AC line sine wave.

In order to improve AC line reading and synchronization, the HV DMOS is turned on sinking IVAC_HV_SINK current at startup. This function can be enabled / disabled through the dedicated NVM bit.

10.2.3 Line disconnection and X-cap discharge

The Vline_sense is monitored to detect the AC line disconnection in order to discharge the X-cap through the internal HV DMOS.

The detection is based on AC activity absence on the VAC pin (the X-cap discharge function is triggered if there is no line activity for more than 50 ms). To discharge the X-cap, the HV DMOS turns on sinking a current of 4 mA minimum.

In order to improve AC line reading and avoid false brown-in, the HV DMOS is turned on sinking IXCD current for 100 ms in case of brown-out or line disconnection events. This function can be enabled / disabled through the dedicated NVM bit.

The discharge current stays on until the VAC pin is discharged or the AC line activity is detected again.

10.2.4 Vline surge stop

A surge can be detected on the VAC pin (430 V).

During the surge the PFC activity is stopped for one half-cycle.

If a line surge is detected during the PFC soft-start, the system shuts down with a not latched fault.

10.2.5 Line monitor for PFC control

A 20 MΩ voltage divider for the AC line monitor is internally connected from the VAC pin to GND.

10.2.6 Early warning signal

If a brown-out or another stopping event (early warning managed faults) is detected, the STNRG011A:

- Stops the PFC
- LLC continues switching for about 5 ms, trying to keep the LLC output voltage regulated
- PFC_FB pin is pulled up to VCore voltage for about 5 ms (early warning signal)

The early warning managed faults are:

- Brown-out
- X-cap
- PFC UVP
- LLC OLP (only in case of OLP time based management)

If any other faults / events occur, the STNRG011A stops both PFC and LLC and generates an early warning signal for about 250 µs.

The early warning signal generation is active as soon as the device starts driving the PFC MOSFET.

This function can be enabled / disabled through the dedicated NVM bit.

10.3 Gate-drivers

The HVG and LVG are matched drivers. Deadtimes are programmable by the user.

During the burst-mode sleep phase, the HS BOOT capacitor discharges. The burst packets always start with a LVG pulse to recharge the bootstrap capacitor. A fast external bootstrap diode is necessary.

10.4 PFC control and fault management

10.4.1 PFC resources

Table 6. **Related pins**

Pin name	Description	Level	Function
PFC_CS	PFC MOSFET current sense	0 - 125 mV	6-bit ramp enhanced COT feature
		500 mV	OCP1
		900 mV	OCP2 fault
PFC_ZCD	PFC auxiliary connection for ZCD detection	-	-
PFC_FB	Reading for PFC Vout estimation	ADC, 10 bits	-
VAC	Mains line voltage reading	ADC, 10 bits	-
PFC_GD	PFC MOSFET gate-driver	-	-

10.4.2 Vin reading

Input line voltage peak (Vin) reading on the VAC pin by the ADC at the AC line peak.

10.4.3 PFC output voltage feedback reading

PFC output voltage reading on the PFC_FB pin by the ADC.

10.4.4 PFC OVP comparator

The PFC OVP comparator sets the limit for the PFC output voltage. It monitors the PFC_FB pin with respect to a fixed 2.3 V threshold.

10.4.5 PFC RECOT comparator

The PFC RECOT comparator implements the TON adjustment for the ramp enhanced constant on-time (RECOT) control.

It monitors the PFC_CS pin with respect to a programmable threshold. Its output communicates to the PFC SMED.

10.4.6 PFC OC1 comparator

The PFC OC1 comparator sets the limit for the operational maximum allowed peak current into the PFC MOSFET. If the OC1 threshold is hit the PFC_GD is turned off. This protection works cycle by cycle.

It monitors the PFC_CS pin with respect to a fixed 500 mV threshold. Its output communicates to the PFC SMED.

10.4.7 PFC OC2 comparator

The PFC OC2 comparator sets an HW limit for the current flowing into the PFC MOSFET: it triggers the OCP fault.

It monitors the PFC_CS pin with respect to a fixed 900 mV threshold.

10.4.8 PFC ZCD

The PFC ZCD comparator performs the zero cross detection to implement the soft switching of the PFC MOSFET.

It monitors the PFC_ZCD pin with respect to two programmable rising and falling thresholds.

Its output communicates to the PFC SMED.

10.4.9 PFC state machine event driven (SMED)

The PFC high frequency operations are managed by a programmable 8-state ”State Machine Event Driven” (2 coupled 4-state SMEDs).

The SMED controls the PFC MOSFET based on the PFC comparators output and internally controlled counters.

It generates also the comparators' enable signals. It works at 60 MHz.

10.5 PFC algorithm

The PFC operates based on a multi-mode scheme.

A constant on-time (COT) control is implemented; T_{ON} is calculated from the PFC feedback and the measured Vin peak.

T_{ON} is calculated and updated at the line cycle valley.

Based on the working PFC's operating state variables the working mode is changed to optimize the overall efficiency.

10.5.1 Ramp enhanced COT improved (patented)

The PFC control is based on the constant on-time scheme, with a proprietary improved algorithm: the calculated TON is applied only after the PFC RECOT comparator is triggered to balance the recovery diode energy and the EMI capacitor current.

The PFC RECOT comparator threshold is adjusted by the core with a 6-bit DAC and allows to apply the programmed base and ramp (defined by user into NVM).

This feature allows improving the total harmonic distortion (THD) and the power factor (PF) of the application.

10.5.2 Operating modes

The PFC manager changes the operating modes by dynamically reconfiguring the SMEDs, obtaining optimal performances in term of both efficiency and THD/PF.

- Transition mode (TM mode)
- Valley skipping
- Discontinuous mode (DCM)

10.6 PFC protections

10.6.1 PFC OVP

In case the bulk voltage triggers the PFC OVP comparator, the system enters the fault state; the overvoltage protection can be programmed as latched or not latched.

The device implements also software overvoltage protection (SW OVP) that allows turning off the PFC until the next line valley in case the SW OVP threshold is reached. The SW OVP threshold is a NVM parameter.

10.6.2 PFC OCP2

If the PFC OC2 comparator is triggered, the PFC gate is truncated and remains off until the beginning of a new line half cycle. In case the PFC OC2 comparator is triggered for more than a programmable number of consecutive half line cycles the device enters the OCP2 fault and it is turned off.

The OCP2 fault can be programmed as latched or not latched.

10.6.3 Surge

When the surge comparator signal is high the PFC MOSFET is turned off and an interrupt is generated. The device will turn on the PFC MOSFET at the new line half cycle if the surge comparator output is low.

10.6.4 PFC soft-start timeout

If the PFC soft-start is not finished after 1 s the system enters the PFC soft-start timeout fault state and it is turned off. The fault is not latched.

10.6.5 PFC UVP

If the PFC_FB pin is below a threshold set by the user the device enters the PFC UVP fault and it is shut down. The system provides two different times of intervention configurable by NVM: adaptive and slow.

The slow intervention allows to shut off the system in case the UVP threshold is confirmed for at least 100 ms. The adaptive one allows to shut off the device immediately in case also the mains AC line is sensed below the brownout threshold for at least 1 half line cycle. On the contrary, the shut off will be delayed as if the intervention is set to slow, until the UVP and the mains conditions remain.

10.6.6 PFC_FB disconnection

If the PFC_FB is stuck low the system enters the PFC_FB disconnection fault state (latched) and it is turned off if the disconnection faults detection is enabled in NVM.

10.6.7 PFC_CS disconnection

If the PFC_CS pin is stuck low (or high) during the the PFC soft-start the system enters the PFC_CS disconnection fault state (latched) and it is shut down if the disconnection faults detection is enabled in NVM.
In case the PFC_CS is stuck high during the operative mode the system enters the PFC_CS disconnection fault state and it is turned off if the disconnection faults detection is enabled in NVM.

10.6.8 PFC_ZCD disconnection

If the PFC_ZCD pin is stuck low or high during the PFC soft-start, the system enters the PFC_ZCD disconnection fault (latched) and it is turned off if the disconnection faults detection is enabled in NVM.

10.7 LLC control and fault management

10.7.1 LLC related resources

Table 7. Pin descriptions

Pin name	Description	Level	Function
LLC_CS	Low-side current sense	0 - 500 mV	5-bit OLP
		700 mV	OCP2 fault
LLC_AUX	LLC auxiliary winding voltage sense	0.9 V	External burst-mode
		2.5 V	LLC output OVP
LLC_FB	LLC OPTO feedback sense, burst comparator and SHUTDOWN comparator	ADC, 10 bits	Feedback sense
		Programmable	Burst comparator
		125 mV	Shutdown comparator
HVG	High-side gate driving	-	-
LVG	Low-side gate driving	-	-

10.7.2 LLC OC1 comparator

The LLC OC1 comparator implements the overload protection (OLP). It monitors the LLC_CS pin with respect to a programmable threshold.

If the LLC_CS pin goes every cycle over the OC1 threshold for a programmable time or a programmable number of occurrences, the IC shuts down and enters the OLP fault.

Type of OLP management, threshold, duration and max number of occurrences are programmable through NVM parameters.

10.7.3 LLC OC2 comparator

The LLC OC2 comparator sets an HW limit for the current flowing into the LLC resonant tank: it triggers the OCP2 fault.

It monitors the LLC_CS pin with respect to a fixed 700 mV threshold. If this threshold is triggered for a programmable consecutive number of cycles, the OCP2 fault is triggered and the system shuts down.

10.7.4 LLC ZCD comparator

The LLC ZCD comparator detects the LLC current zero-crossing during the normal operation to implement the time-shift control and the anti capacitive protection.

Its output communicates to the LLC SMED.

10.7.5 LLC_FB voltage reading: OPTO feedback loop error

The LLC_FB pin is connected to the optocoupler and its voltage is the error signal of the LLC loop.

The LLC_FB voltage is sampled by the ADC to calculate the time-shift.

10.7.6 Shutdown feature

If the LLC_FB pin is forced below 125 mV, the device shuts down. If the voltage returns over such threshold the system restarts performing the soft-start.

This feature can be enabled / disabled using a NVM bit.

10.7.7 Algorithm

The LLC operation is based on “Symmetric Time-Shift Control” (STSC), an improved version of time-shift control that guarantees 50% of the HB duty cycle. The time-shift value is calculated from the LLC_FB pin.

10.8 LLC protections

10.8.1 Anti-capacitive protection

Anti-capacitive control is applied at the SMEDs level using ZCD time events.

The IC monitors the phase relationship between the LLC tank current sensed on the LLC_CS pin and the voltage at the HVG and LVG, checking the time between the gate rising edge and the tank current zero cross detection.

If this time is below a programmable threshold, which is indicative of impending the capacitive-mode operation, the monitoring circuit activates the “Soft” ACP procedure: the time-shift is reduced (and therefore the switching frequency is increased) in order to keep the converter away from that dangerous condition.

If the time reaches “zero” the device is stopped immediately. This is called “Hard” ACP. Both hard and soft ACP can be enabled and disabled through NVM.

10.8.2 LLC OLP

If the LLC OC1 comparator is triggered the system could enter the overload protection (OLP). STNRG011A is able to manage two OLP behaviours: time based and frequency based. If the frequency based management is selected, in case LLC OC1 comparator is triggered the device increases the frequency of the LLC, and if the maximum OLP occurrence (programmable value) is reached the device is shut down enetering the OLP fault state that can be programmed as latched or not latched. If the time based management is selected, once the OC1 threshold is triggered the system checks for a programmable time if the OCP1 event is still present, in this case the device is shut down entering the OLP fault state that can be programmed as latched or not latched.

10.8.3 LLC OCP2

If the LLC OC2 comparator is triggered for a number of times greater than a threshold set by the user the device sets the OCP2 fault and it is shut down. The OCP2 fault can be programmed as latched or not latched.

10.8.4 LLC soft-start timeout

If the LLC output voltage cannot reach the regulation value within 100 ms, the device enters the LLC soft-start timeout fault and it is shut down. The fault can be programmed as latched or not latched.

10.8.5 LLC OVP

If the LLC_AUX pin voltage is higher than the LLC OVP comparator threshold (2.5 V), the system enters the LLC OVP fault state and it is turned off. The fault can be programmed as latched or not latched and can be disabled.

10.8.6 LLC_CS disconnection

If the LLC_CS pin is stuck at 0 V or 5 V during the soft-start the system enters the LLC_CS disconnection fault (latched) and it is shut down if the disconnection faults detection is enabled in NVM.

10.8.7 LLC_AUX disconnection

If the pure external burst-mode is enabled and the LLC_AUX pin is stuck at 0 V during the burst and the LLC_FB pin is higher than the burst comparator threshold, after 32 burst packets, the system enters LLC_AUX disconnection protection (latched) and it is shut down if the disconnection faults detection is enabled in NVM.

10.9 ADC

The system ADC is an 8-channel 15-MHz SAR 10-bit A/D converter.

It needs 7 cycles (470 ns) for sampling and 11 cycles (740 ns) to convert the data.

It is controlled by a SW programmable scheduler allowing flexible system signals reading:

- Fixed time sequence conversion
- Event driven sequence conversion

Table 8. ADC input signals

Signal	Pin	Notes	FSR
Input line voltage	VAC	Internal voltage divider	484.5 V
PFC feedback voltage	PFC_FB	Direct reading	2.5 V
LLC feedback voltage	LLC_FB	Direct reading	2.5 V

10.10 Burst-mode

10.10.1 Specific resources

Burst comparator on LLC_FB pin

The LLC BURST comparator at the LLC_FB pin is used to wake-up the system, in order to perform a burst sequence.

The comparator is alive also during sleep and the wake-up threshold is programmable (0.75 V, 1 V, 1.25 V).

External burst-mode comparator on LLC_AUX pin

The external burst-mode comparator with the 0.9 V threshold on the LLC_AUX pin is used to enter / exit the burst-mode using an external digital signal. The external burst-mode operation can be enabled / disabled using a NVM bit.

30-kHz system oscillator

A 30-kHz oscillator (always on) keeps the system alive.

10.10.2 Algorithm

The system can manage the deep sleep state with very low VCC current consumption (500 µA).

The system in deep sleep

- Monitors the AC line for X-cap discharge and brown-out condition
- Monitors the burst comparator to detect wake condition
- Monitors the VCC for data integrity
- All RAM data are maintained

The device implements two different burst-mode algorithms: the LLC_FB burst or external burst. The first one is based on just the LLC_FB pin voltage, the second one is based on the external BM comparator on the LLC_AUX pin that can be driven sensing the output current.

The burst-mode can be programmed to depends either on the LLC_FB pin only, or LLC_AUX pin only, or both. This third possibility is called hybrid external burst.

In case of the LLC_FB burst-mode, the device enters the sleep mode if the LLC_FB pin voltage goes below a programmable threshold. The burst switching activity is enabled after the burst comparator is triggered.

The normal switching activity is restored if the time between two bursts is lower than

a programmable threshold. This time defines a precise power level at which the controller exits the burst-mode. In order to have a faster response to the big load transient the system exits the burst-mode also if the LLC_FB pin voltage is still above the burst comparator threshold after one burst packet.

In case of the LLC_AUX pin driven burst mode, two types of external burst mode could be defined:

- Pure external burst mode: only the external BM comparator manages the burst mode entering / exiting;
- Hybrid external burst mode: if the external BM comparator is high, the system stays out of burst mode while if the external BM comparator is low, burst mode entering / exiting is managed by the LLC_FB pin settings.

In both external burst mode cases, the burst switching activity is anyway managed by the LLC_FB pin and the burst comparator.

The PFC and LLC switching activities during the burst-mode are synchronized.

The LLC can perform a burst without the PFC, depending on the system conditions.

10.11 Communication and configuration

The device communicates with an external digital device through a serial interface.

The serial interface uses two dedicated pins with a standard UART protocol. It implements also an I2C protocol for external E2PROM writing and reading.

The serial interface allows the user to:

- write the NVM to configure the device in a specific application: 20 bytes are available.
- write into the RAM for test and SW patch purpose
- read the NVM content
- read the RAM content
- read register content
- configure the device for specific tests

Based on a specific code into the NVM the serial interface functionality can be reduced for security reasons.

10.11.1 Monitor

Some internal data can be provided to an external digital device trough the UART interface for monitoring purposes.

10.11.2 Black box

Black box data are written into the external E2PROM during the normal operation.

10.11.3 Patches

SW patches (if necessary) are uploaded by the device from the external E2PROM at the startup.

Maximum patch size is 2.5 kB.

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

11.1 SO20 package information

Figure 5. SO20 package outline

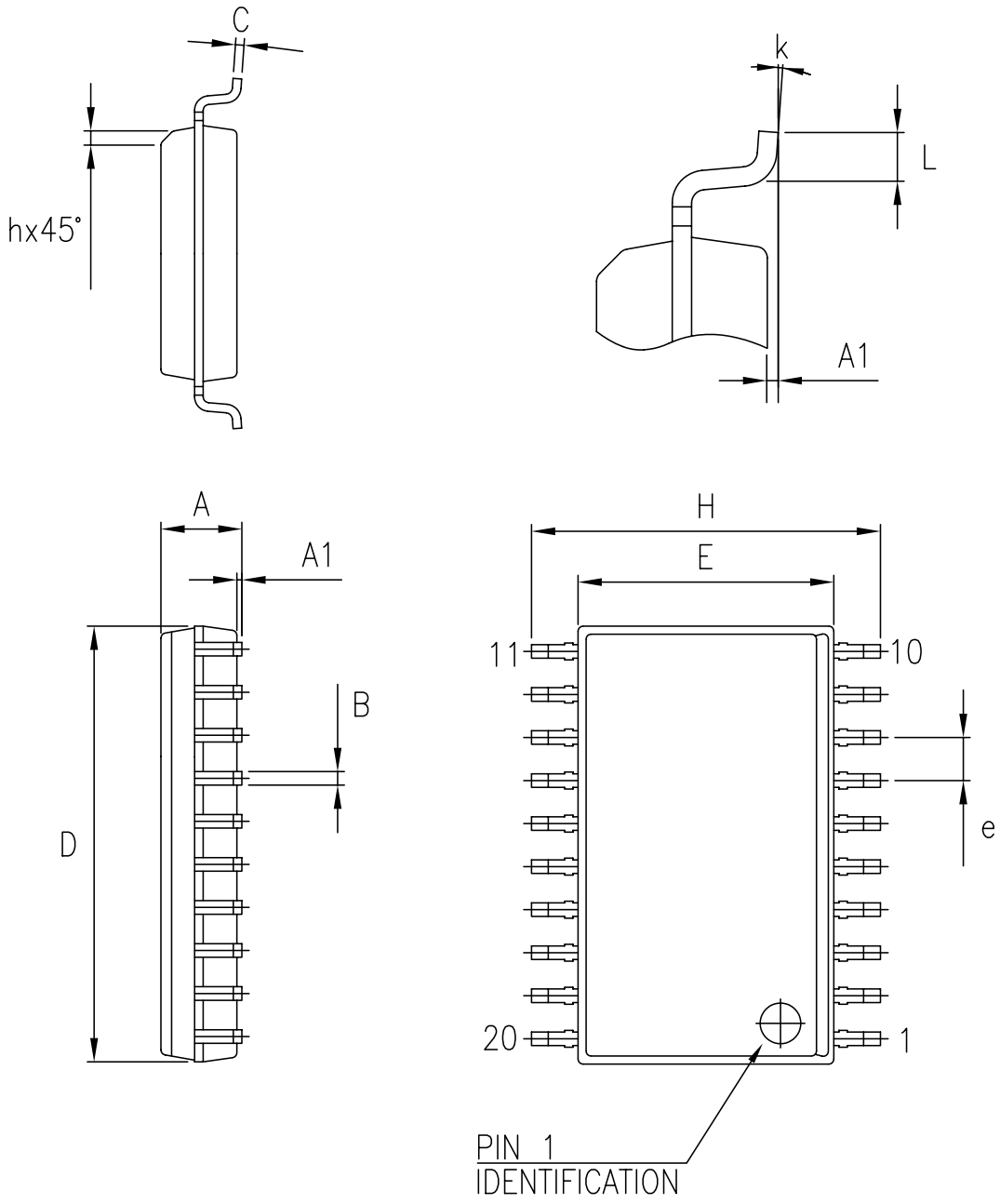


Table 9. **SO20 package mechanical data**

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.35	-	2.65	0.093	-	0.104
A1	0.10	-	0.30	0.004	-	0.012
B	0.33	-	0.51	0.013	-	0.020
C	0.23	-	0.32	0.009	-	0.013
D	12.60	-	13.00	0.496	-	0.512
E	7.40	-	7.60	0.291	-	0.299
e	-	1.27	-	-	0.050	-
H	10.00	-	10.65	0.394	-	0.419
h	0.25	-	0.75	0.010	-	0.030
L	0.40	-	1.27	0.016	-	0.050
K	0° (min.), 8° (max.)					

12 Ordering information

Table 10. **Order codes**

Part number	Package	Packing
STNRG011A	SO20	Tube
STNRG011ATR	SO20	Tape and reel

Revision history

Table 11. **Document revision history**

Date	Version	Changes
11-Apr-2022	1	Initial release.
15-Jul-2022	2	Safety data insertion.

Contents

1 Description 2
2 Pin connection 3
3 Absolute maximum ratings and thermal data 4
4 Detailed block diagram 5
5 Pin function 6
6 Electrical characteristics 8
7 Safety data 12
8 Application schematics 13
9 Architecture 14
10 Functional description 15
10.1 HV startup and VCC management 15
10.2 AC line monitor and protection 15
10.2.1 Brown-in/out 15
10.2.2 Line synchronization 16
10.2.3 Line disconnection and X-cap discharge 16
10.2.4 Vline surge stop 16
10.2.5 Line monitor for PFC control 16
10.2.6 Early warning signal 16
10.3 Gate-drivers 16
10.4 PFC control and fault management 17
10.4.1 PFC resources 17
10.4.2 Vin reading 17
10.4.3 PFC output voltage feedback reading 17
10.4.4 PFC OVP comparator 17
10.4.5 PFC RECOT comparator 17
10.4.6 PFC OC1 comparator 17
10.4.7 PFC OC2 comparator 17
10.4.8 PFC ZCD 17
10.4.9 PFC state machine event driven (SMED) 17
10.5 PFC algorithm 18
10.5.1 Ramp enhanced COT improved (patented) 18
10.5.2 Operating modes 18
10.6 PFC protections 18
10.6.1 PFC OVP 18
10.6.2 PFC OCP2 18

10.6.3 Surge . . . 18
10.6.4 PFC soft-start timeout . . . 18
10.6.5 PFC UVP . . . 18
10.6.6 PFC_FB disconnection . . . 19
10.6.7 PFC_CS disconnection . . . 19
10.6.8 PFC_ZCD disconnection . . . 19
10.7 LLC control and fault management . . . 19
10.7.1 LLC related resources . . . 19
10.7.2 LLC OC1 comparator . . . 19
10.7.3 LLC OC2 comparator . . . 19
10.7.4 LLC ZCD comparator . . . 20
10.7.5 LLC_FB voltage reading: OPTO feedback loop error . . . 20
10.7.6 Shutdown feature . . . 20
10.7.7 Algorithm . . . 20
10.8 LLC protections . . . 20
10.8.1 Anti-capacitive protection . . . 20
10.8.2 LLC OLP . . . 20
10.8.3 LLC OCP2 . . . 20
10.8.4 LLC soft-start timeout . . . 20
10.8.5 LLC OVP . . . 20
10.8.6 LLC_CS disconnection . . . 20
10.8.7 LLC_AUX disconnection . . . 21
10.9 ADC . . . 21
10.10 Burst-mode . . . 21
10.10.1 Specific resources . . . 21
10.10.2 Algorithm . . . 21
10.11 Communication and configuration . . . 22
10.11.1 Monitor . . . 22
10.11.2 Black box . . . 22
10.11.3 Patches . . . 22
11 Package information . . . 23
11.1 SO20 package information . . . 23
12 Ordering information . . . 25
Revision history . . . 26
List of tables . . . 29
List of figures . . . 30

List of tables

Table 1. Absolute maximum ratings . . . 4
Table 2. Thermal data . . . 4
Table 3. Pin function detailed description . . . 6
Table 4. Electrical characteristics . . . 8
Table 5. X-Cap discharge safety data according to IEC 62368 . . . 12
Table 6. Related pins . . . 17
Table 7. Pin descriptions . . . 19
Table 8. ADC input signals . . . 21
Table 9. SO20 package mechanical data . . . 24
Table 10. Order codes . . . 25
Table 11. Document revision history . . . 26

List of figures

Figure 1. Block diagram . . . 1
Figure 2. Pin connection (top view) . . . 3
Figure 3. Detailed block diagram . . . 5
Figure 4. Typical application schematic . . . 13
Figure 5. SO20 package outline . . . 23

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