



128K × 8 CMOS STATIC RAM

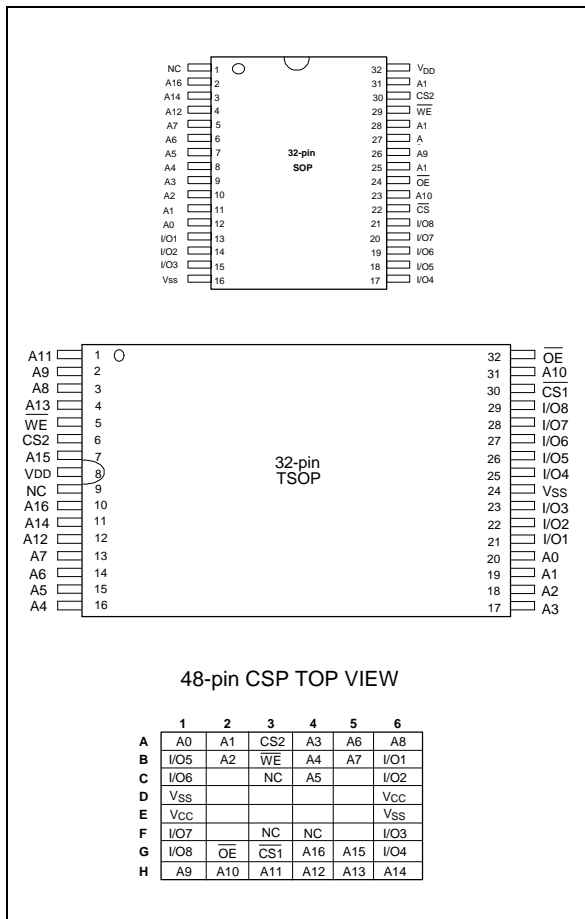
GENERAL DESCRIPTION

The W24L01 is a normal-speed, very low-power CMOS static RAM organized as 131072 × 8 bits that operates on a wide voltage range from 2.7V to 3.6V power supply. The W24L01 family, W24L01-LE and W24L01-LI, can meet the requirement of various operating temperature. This device is manufactured using Winbond's high performance CMOS technology.

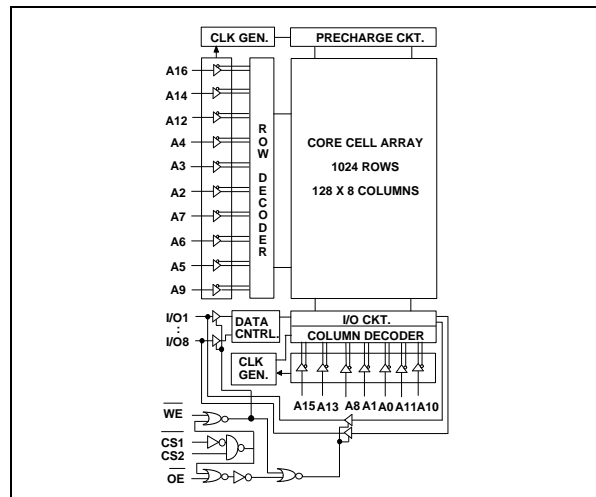
FEATURES

- Low power consumption
- Access time: 55 nS /70 nS
- 2.7V to 3.6V supply voltage
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 1.5V (min.)
- Packaged in 32-pin 450 mil SOP, standard type one TSOP (8 mm × 20 mm), small type one TSOP (8 mm × 13.4 mm) and 48-pin CSP

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|-------------|---------------------|
| A0 – A16 | Address Inputs |
| I/O1 – I/O8 | Data Inputs/Outputs |
| CS, CS2 | Chip Select Input |
| WE | Write Enable Input |
| OE | Output Enable Input |
| VDD | Power Supply |
| VSS | Ground |
| NC | No Connection |

TRUTH TABLE

| $\overline{CS1}$ | CS2 | \overline{OE} | \overline{WE} | MODE | I/O1- I/O8 | V _{DD} CURRENT |
|------------------|-----|-----------------|-----------------|----------------|------------|-------------------------|
| H | X | X | X | Not Selected | High Z | ISB, ISB1 |
| X | L | X | X | Not Selected | High Z | ISB, ISB1 |
| L | H | H | H | Output Disable | High Z | IDD |
| L | H | L | H | Read | Data Out | IDD |
| L | H | X | L | Write | Data In | IDD |

DC CHARACTERISTICS

Absolute Maximum Ratings

| PARAMETER | | RATING | UNIT |
|---|----|------------------------------|------|
| Supply Voltage to V _{SS} Potential | | -0.5 to +4.6 | V |
| Input/Output to V _{SS} Potential | | -0.5 to V _{DD} +0.5 | V |
| Allowable Power Dissipation | | 1.0 | W |
| Storage Temperature | | -65 to +150 | °C |
| Operating Temperature | LL | 0 to 70 | °C |
| | LE | -20 to 85 | |
| | LI | -40 to 85 | |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{SS} = 0V; T_A (°C) = 0 to 70 for LL, -20 to 85 for LE, -40 to 85 for LI)

| PARAMETER | SYM. | TEST CONDITIONS | W24L01 | | | UNIT |
|------------------------|-----------------|---|--------|-------|----------------------|------|
| | | | MIN. | TYP.* | MAX. | |
| Input Low Voltage | V _{IL} | - | -0.2 | - | +0.4 | V |
| Input High Voltage | V _{IH} | - | +2.2 | - | V _{DD} +0.3 | V |
| Input Leakage Current | I _{LI} | V _{IN} = V _{SS} to V _{DD} | -1 | - | +1 | μA |
| Output Leakage Current | I _{LO} | V _{I/O} = V _{SS} to V _{DD} , $\overline{CS1}$ = V _{IH} (min.) or CS2 = V _{IL} (max.) or \overline{OE} = V _{IH} (min.) or \overline{WE} = V _{IL} (max.) | -1 | - | +1 | μA |
| Output Low Voltage | V _{OL} | I _{OL} = +2.1 mA | - | - | 0.4 | V |
| Output High Voltage | V _{OH} | I _{OH} = -1.0 mA | 2.2 | - | - | V |

Operating Characteristics, continued

| PARAMETER | SYM. | TEST CONDITIONS | W24L01 | | | UNIT |
|--------------------------------|-----------------|---|-------------|----------------------|--------------------------|---------|
| | | | MIN. | TYP.* | MAX. | |
| Operating Power Supply Current | I _{DD} | $\overline{CS1} = V_{IL} \text{ (max.)}$ and $CS2 = V_{IH} \text{ (min.)}$, I/O = 0 mA, Cycle = min. Duty = 100% | - | 25 (3V) 30 (3.3V) | 40 (70 nS) 55 (55 nS) | mA |
| Standby Power Supply Current | ISB | $\overline{CS1} = V_{IH} \text{ (min.)}$ or $CS2 = V_{IL} \text{ (max.)}$, Cycle = min. Duty = 100% | - | - | 0.3 | mA |
| | ISB1 | $\overline{CS1} \geq V_{DD} - 0.2V$ or $CS2 \leq 0.2V$ | LL LE/LI | 2 | 5 7 | μA |

Note: Typical parameter is measured under ambient temperature $T_A = 25^\circ C$

CAPACITANCE

($T_A = 25^\circ C$, $f = 1 \text{ MHz}$)

| PARAMETER | SYM. | CONDITIONS | MAX. | UNIT |
|--------------------------|------------------|-----------------------|------|------|
| Input Capacitance | C _{IN} | V _{IN} = 0V | 8 | pF |
| Input/Output Capacitance | C _{I/O} | V _{OUT} = 0V | 10 | pF |

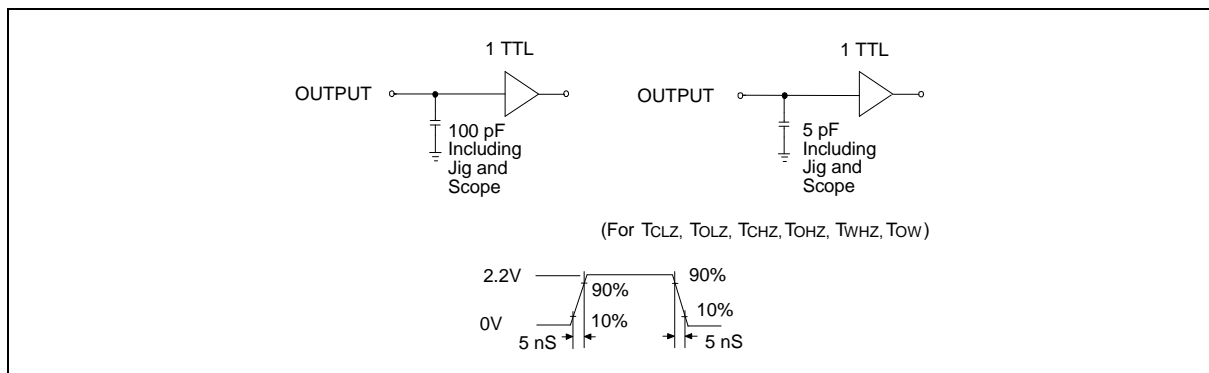
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

| PARAMETER | CONDITIONS |
|---|------------------------------|
| Input Pulse Levels | 0V to 2.2V |
| Input Rise and Fall Times | 5 nS |
| Input and Output Timing Reference Level | 1.5V, V _{DD} = 3.0V |
| Output Load | See the drawing below |

AC Test Loads and Waveform





AC Characteristics, continued

(V_{SS} = 0V; T_A (°C) = 0 to 70 for LL, -20 to 85 for LE, -40 to 85 for LI)**Read Cycle**

| PARAMETER | SYM. | MIN. | MAX. | MIN. | MAX. | UNIT |
|--------------------------------------|-------|------|------|------|------|------|
| Read Cycle Time | TRC | 55 | - | 70 | - | nS |
| Address Access Time | TAA | - | 55 | - | 70 | nS |
| Chip Select Access Time | TACS | - | 55 | - | 70 | nS |
| Output Enable to Output Valid | TAOE | - | 30 | - | 35 | nS |
| Chip Selection to Output in Low Z | TCLZ* | 10 | - | 10 | - | nS |
| Output Enable to Output in Low Z | TOLZ* | 5 | - | 5 | - | nS |
| Chip Deselection to Output in High Z | TCHZ* | - | 25 | - | 30 | nS |
| Output Disable to Output in High Z | TOHZ* | - | 25 | - | 30 | nS |
| Output Hold from Address Change | TOH | 5 | - | 10 | - | nS |

* These parameters are sampled but not 100% tested

Write Cycle

| PARAMETER | SYM. | MIN. | MAX. | MIN. | MAX. | UNIT | |
|------------------------------------|--|------|------|------|------|------|----|
| Write Cycle Time | TWC | 55 | - | 70 | - | nS | |
| Chip Selection to End of Write | TCW | 50 | - | 60 | - | nS | |
| Address Valid to End of Write | TAW | 50 | - | 60 | - | nS | |
| Address Setup Time | TAS | 0 | - | 0 | - | nS | |
| Write Pulse Width | TWP | 40 | - | 55 | - | nS | |
| Write Recovery Time | $\overline{CS1}$, $CS2$, \overline{WE} | TWR | 0 | - | 0 | - | nS |
| Data Valid to End of Write | TDW | 30 | - | 30 | - | nS | |
| Data Hold from End of Write | TDH | 0 | - | 0 | - | nS | |
| Write to Output in High Z | TWHZ* | - | 20 | - | 25 | nS | |
| Output Disable to Output in High Z | TOHZ* | - | 20 | - | 25 | nS | |
| Output Active from End of Write | TOW | 5 | - | 5 | - | nS | |

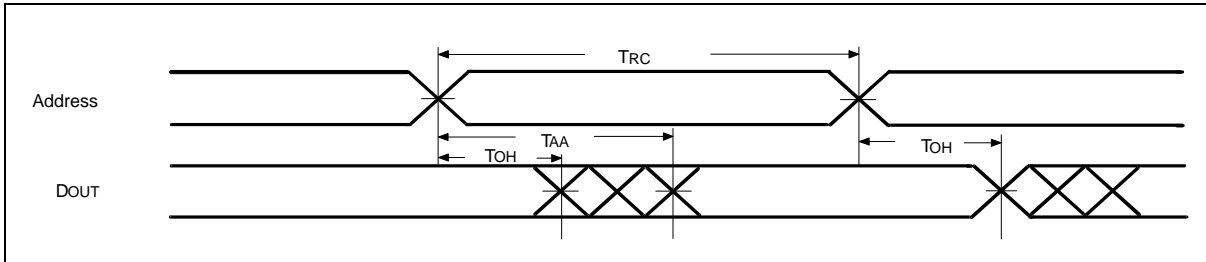
* These parameters are sampled but not 100% tested



TIMING WAVEFORMS

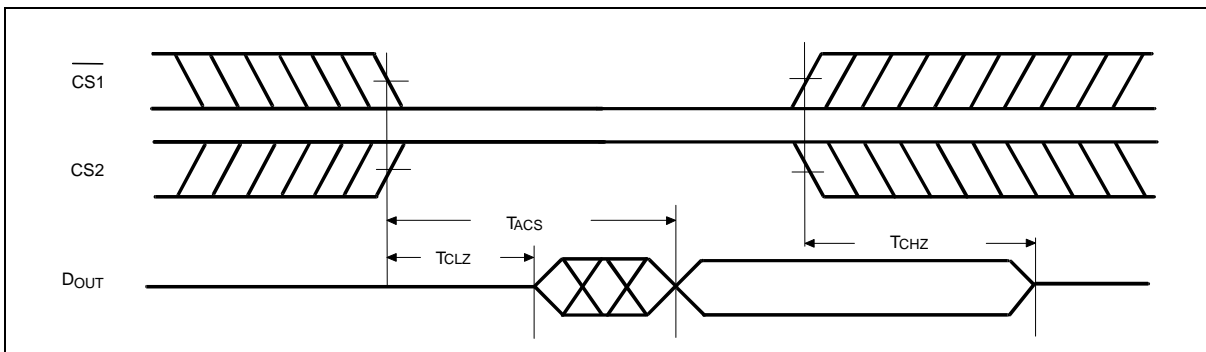
Read Cycle 1

(Address Controlled)



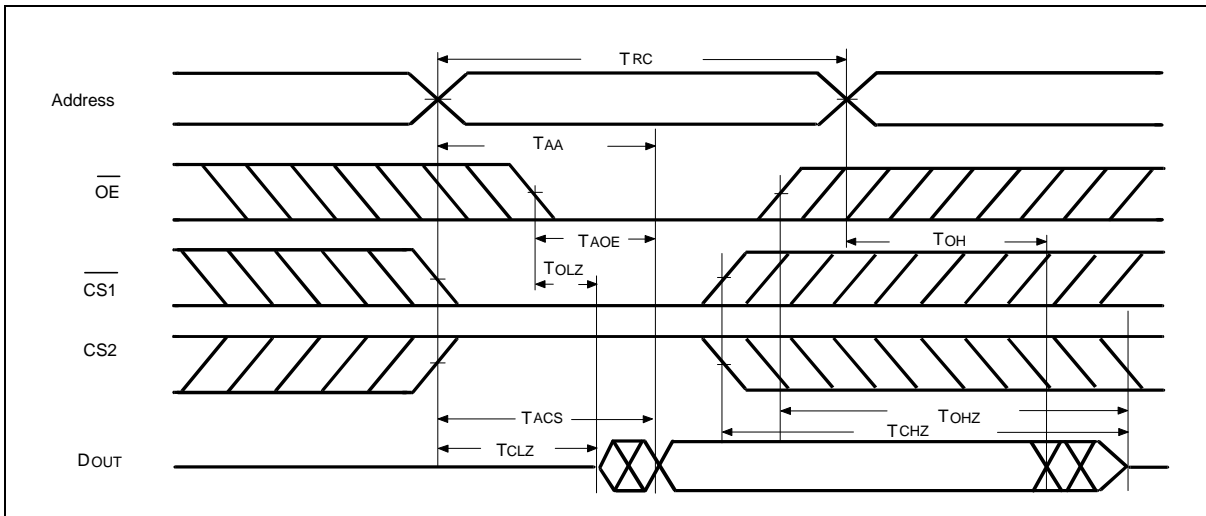
Read Cycle 2

(Chip Select Controlled)



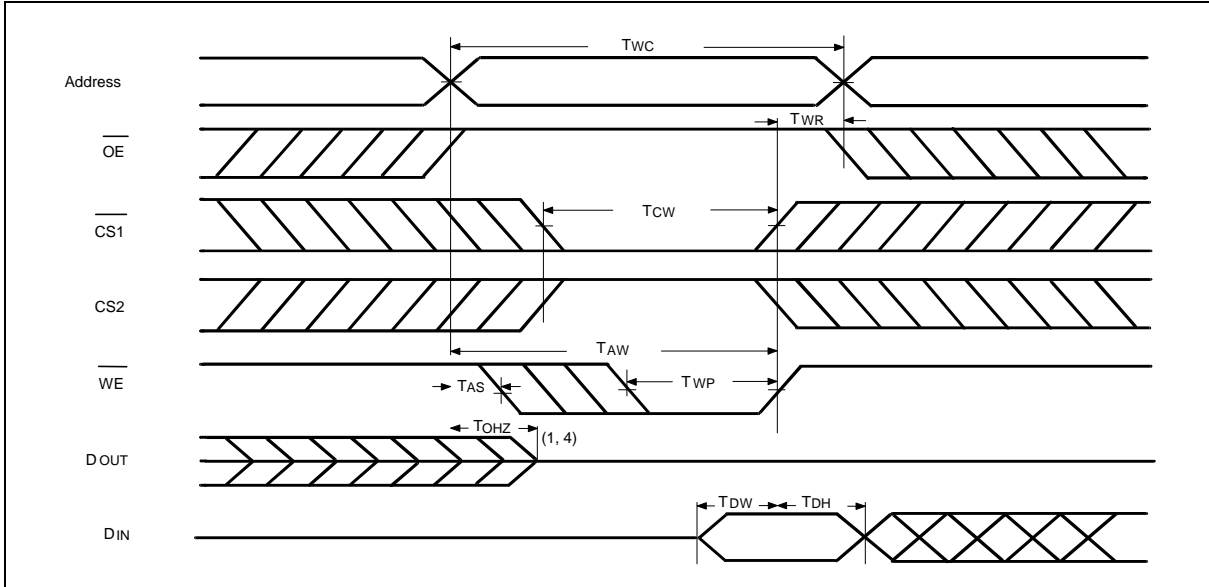
Read Cycle 3

(Output Enable Controlled)



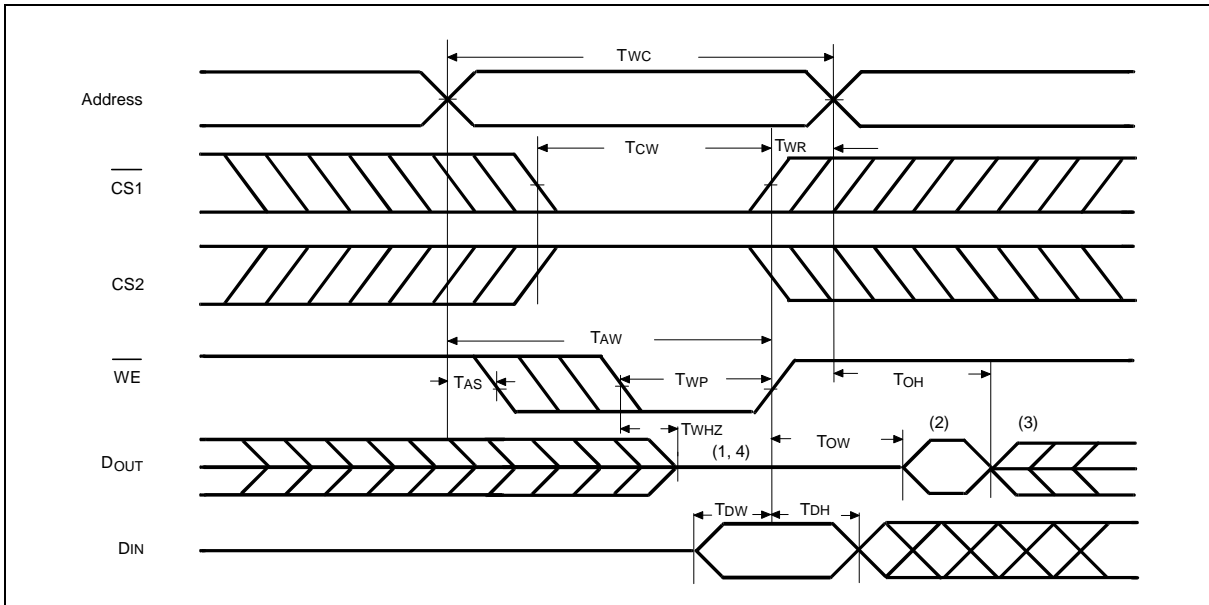
Timing Waveforms, continued

Write Cycle 1



Write Cycle 2

($\overline{OE} = V_{IL}$ Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.



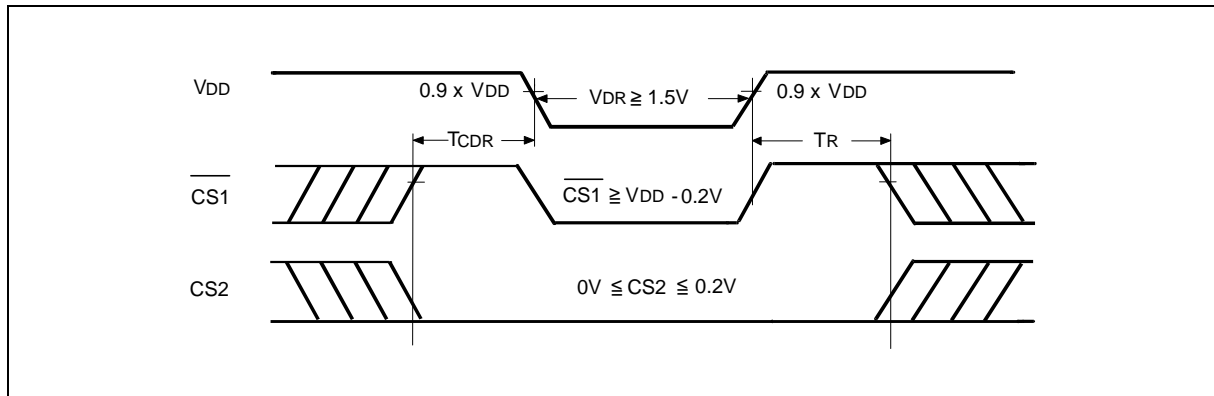
DATA RETENTION CHARACTERISTICS

(TA (°C) = 0 to 70 for LL, -20 to 85 for LE; -40 to 85 for LI)

| PARAMETER | SYM. | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------------------------------------|-------------------|--|-------------------|------|------|------|
| VDD for Data Retention | VDR | $\overline{CS1} \geq V_{DD} - 0.2V$ or $CS2 \leq 0.2V$ | 1.5 | - | - | V |
| Data Retention Current | I _{DDDR} | $\overline{CS1} \geq V_{DD} - 0.2V$ or $CS2 \leq 0.2V, V_{DD} = 3V$ | - | - | 5 | μA |
| Chip Deselect to Data Retention Time | T _{CDR} | See data retention waveform | 0 | - | - | nS |
| Operation Recovery Time | T _R | | T _{RC} * | - | - | nS |

* Read Cycle Time

DATA RETENTION WAVEFORM



ORDERING INFORMATION

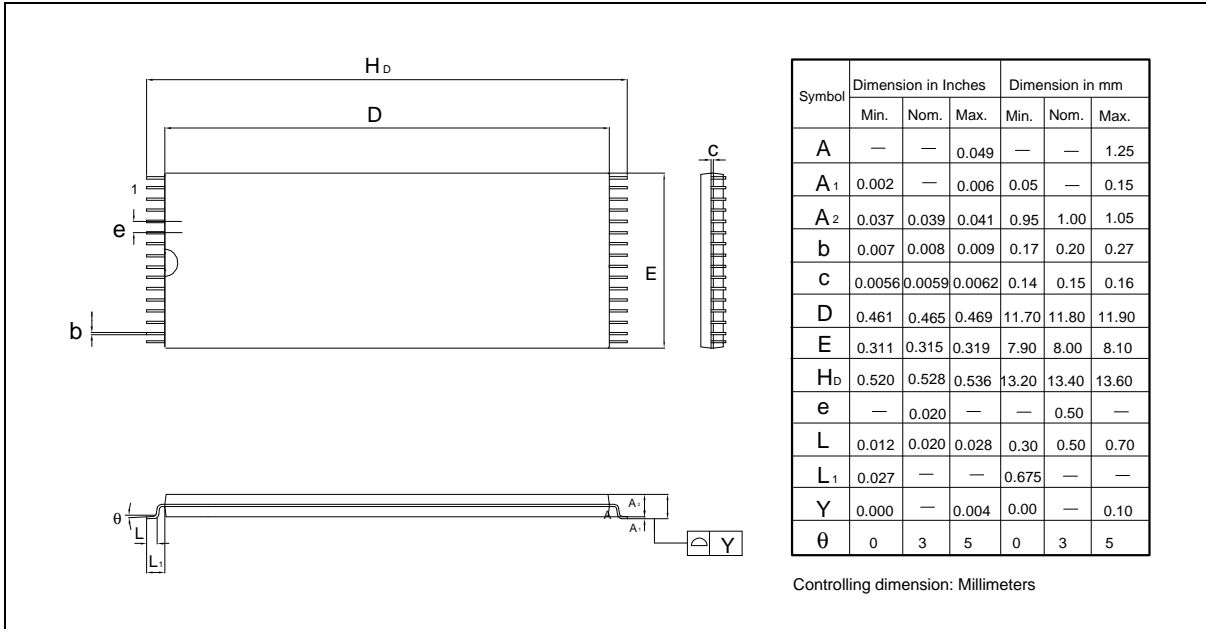
| PART NO. | ACCESS TIME (nS) | OPERATING VOLTAGE (V) | OPERATING TEMPERATURE (°C) | PACKAGE |
|--------------|------------------|-----------------------|----------------------------|------------------------|
| W24L01B-55LL | 55 | 2.7V – 3.6V | 0 to 70 | CSP |
| W24L01Q-55LL | 55 | 2.7V – 3.6V | 0 to 70 | Small type one TSOP |
| W24L01S-55LL | 55 | 2.7V – 3.6V | 0 to 70 | 450 mil SOP |
| W24L01T-55LL | 55 | 2.7V – 3.6V | 0 to 70 | Standard type one TSOP |
| W24L01B-55LE | 55 | 2.7V – 3.6V | -20 to 85 | CSP |
| W24L01Q-55LE | 55 | 2.7V – 3.6V | -20 to 85 | Small type one TSOP |
| W24L01S-55LE | 55 | 2.7V – 3.6V | -20 to 85 | 450 mil SOP |
| W24L01T-55LE | 55 | 2.7V – 3.6V | -20 to 85 | Standard type one TSOP |
| W24L01B-55LI | 55 | 2.7V – 3.6V | -40 to 85 | CSP |
| W24L01Q-55LI | 55 | 2.7V – 3.6V | -40 to 85 | Small type one TSOP |
| W24L01S-55LI | 55 | 2.7V – 3.6V | -40 to 85 | 450 mil SOP |
| W24L01T-55LI | 55 | 2.7V – 3.6V | -40 to 85 | Standard type one TSOP |
| W24L01B-70LL | 70 | 2.7V – 3.6V | 0 to 70 | CSP |
| W24L01Q-70LL | 70 | 2.7V – 3.6V | 0 to 70 | Small type one TSOP |
| W24L01S-70LL | 70 | 2.7V – 3.6V | 0 to 70 | 450 mil SOP |
| W24L01T-70LL | 70 | 2.7V – 3.6V | 0 to 70 | Standard type one TSOP |
| W24L01B-70LE | 70 | 2.7V – 3.6V | -20 to 85 | CSP |
| W24L01Q-70LE | 70 | 2.7V – 3.6V | -20 to 85 | Small type one TSOP |
| W24L01S-70LE | 70 | 2.7V – 3.6V | -20 to 85 | 450 mil SOP |
| W24L01T-70LE | 70 | 2.7V – 3.6V | -20 to 85 | Standard type one TSOP |
| W24L01B-70LI | 70 | 2.7V – 3.6V | -40 to 85 | CSP |
| W24L01Q-70LI | 70 | 2.7V – 3.6V | -40 to 85 | Small type one TSOP |
| W24L01S-70LI | 70 | 2.7V – 3.6V | -40 to 85 | 450 mil SOP |
| W24L01T-70LI | 70 | 2.7V – 3.6V | -40 to 85 | Standard type one TSOP |

Notes:

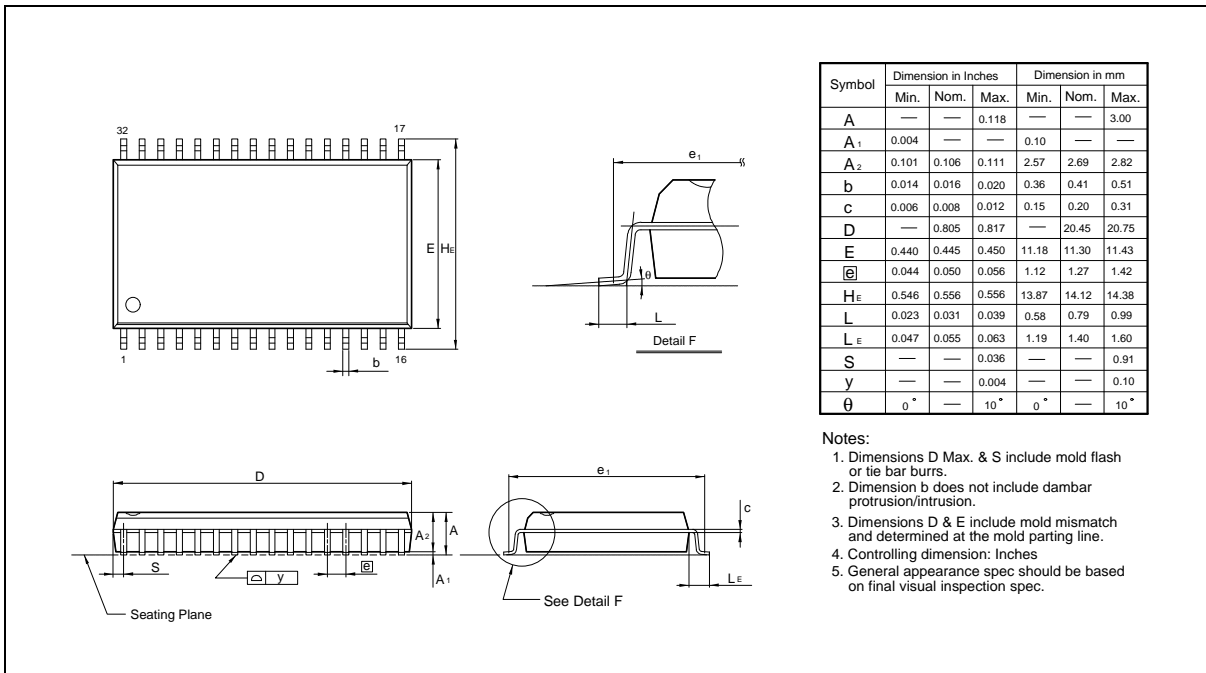
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

32-pin Small Type One TSOP

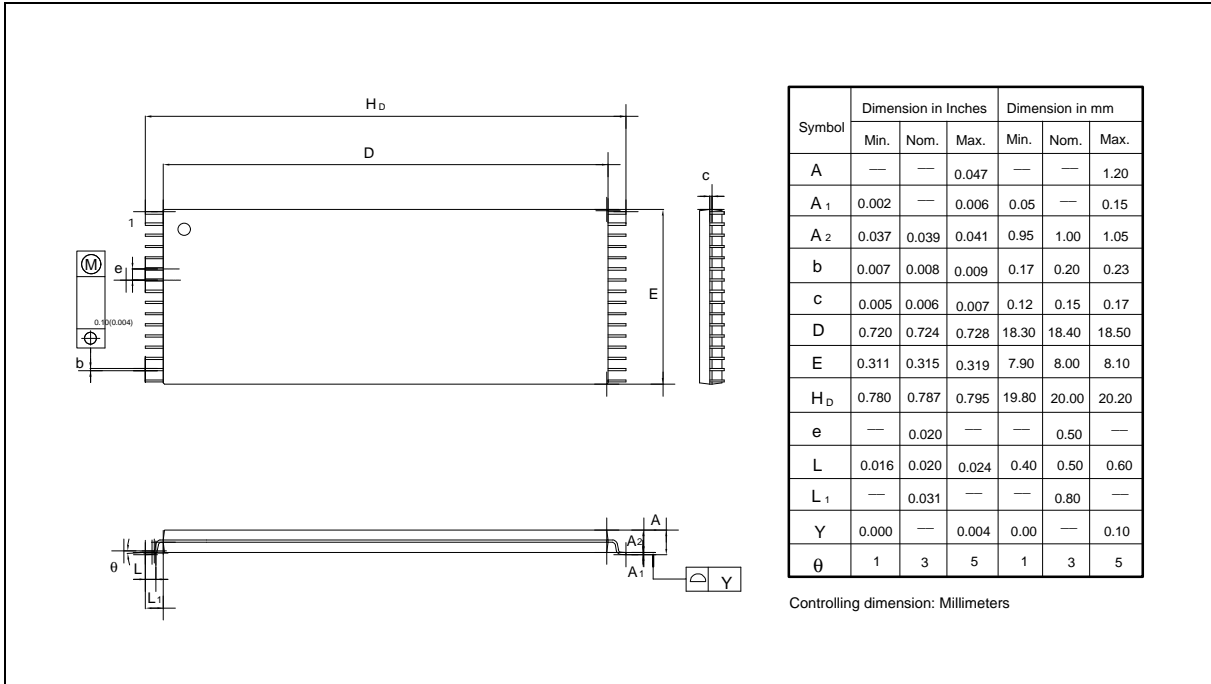


32-pin SOP Wide Body



Package Dimensions, continued

32-pin Standard Type One TSOP





VERSION HISTORY

| VERSION | DATE | DESCRIPTION |
|---------|--------------|--|
| A1 | Feb. 1998 | Initial Issued |
| A2 | Apr. 1998 | Add standby power supply current (ISB1) typical parameter when operation temperature $T_A = 25^\circ \text{C}$ |
| A3 | June 1998 | Change supply voltage range from (2.7V to 3.6V) to (2.3V to 3.3V) |
| A4 | Oct. 1998 | Add SOP package type |
| A5 | Jan. 1999 | Add SOP package pin configuration |
| A6 | Jan. 2, 2002 | Change supply voltage range from (2.3V – 3.3V) to (2.7V – 3.6V). Add 55 nS spec. Add LL grade. |



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