AT1175

Preliminary Product Information

8-Bit 20MSPS CMOS VIDEO A/D CONVERTER

Features

- Resolution: 8-Bit ± 0.5 LSB(DNL)
- Maximum Conversion Rate: 20 MSPS
- Built-in Sample and Hold Function
- Built-in Reference Voltage Self Bias Circuit
- Single +5.0 V Power Supply
- Three-State TTL Compatible Output
- Direct Replacement for the Sony CXD1175

Applications

- Video Digitizing
- Personal Computer Video
- Multimedia
- Digital Television

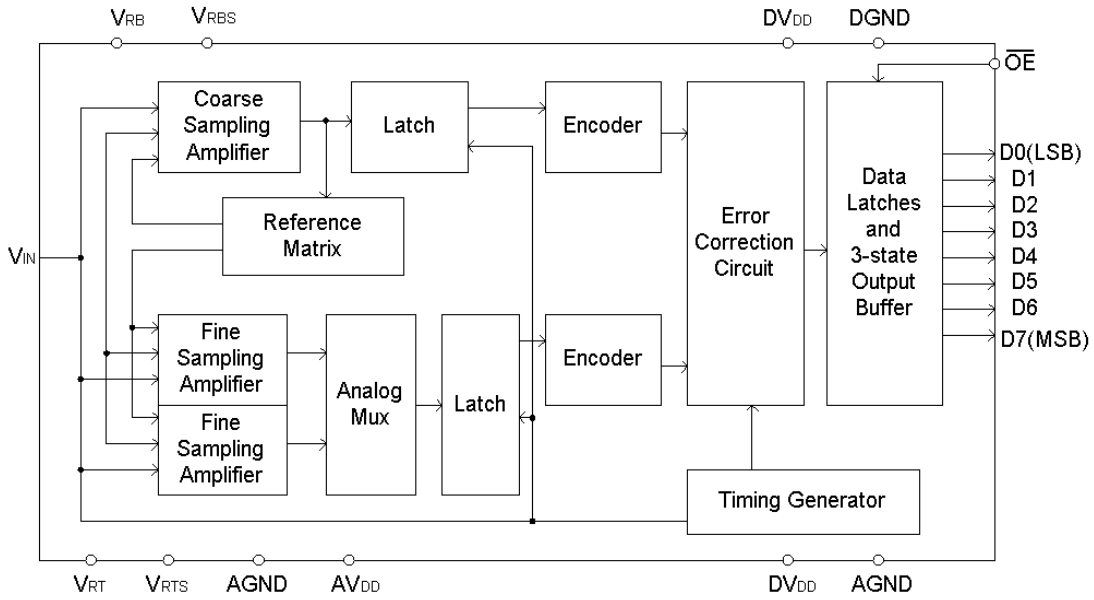
General Description

The AT1175 is a CMOS two-step A/D converter capable of digitizing full-scale analog input signals into 8-bit digital words at sample rate of 20 MSPS.

For most application, no external sample-and-hold or video driving amplifiers are needed thanks to the device's narrow aperture time, wide bandwidth, and low input capacitance.

The AT1175 operates from a single +5.0V power supply and has an internal voltage reference, which eliminates the need for external reference circuitry. All digital inputs are CMOS compatible and the tri-state outputs are TTL-compatible. The AT1175 is ideal for most video and image processing applications that require low power dissipation and low cost.

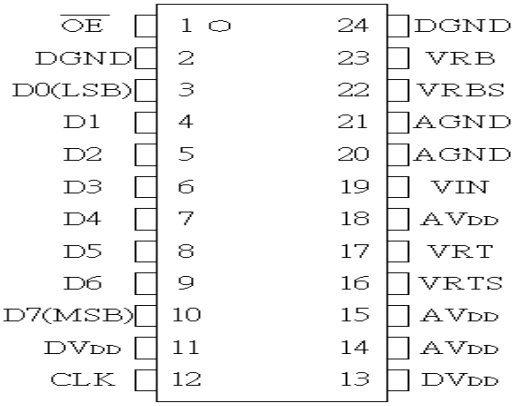
Block Diagram



Aimtron reserves the right without notice to change this circuitry and specifications.

2F, No.10, Prosperity RD. II, Science-Based Industrial Park, Hsinchu 300,Taiwan, R.O.C.
Tel: 886-3-563-0878 WWW: http://www.aimtron.com.tw
Fax: 886-3-563-0879 Email: service@aimtron.com.tw

Pin Configuration



Ordering Information

Part number.	Package	Marking
AT1175S	SOP24(300 mil)	AT1175S
AT1175S_GRE	SOP24(300 mil),Green	AT1175S, date code with one bottom line

Pin Description

PIN	NAME	FUNCTION	PIN	NAME	FUNCTION
1	$\overline{OE}$	Output Enable Control D0~D7 Enabled When $\overline{OE}$ = Low D0~D7 at Tri-state When $\overline{OE}$ = High	14 15 18	AVDD	Analog +5V Supply
2,24	DGND	Digital GND	23	VRB	Reference Voltage (Bottom)
3~10	D0~D7	Digital Output Data D0 (LSB), D7(MSB)	17	VRT	Reference Voltage (Top)
11,13	DVDD	Digital +5V Supply	19	VIN	Analog Input
12	CLK	Clock Input	20 21	AGND	Analog GND
16	VRTS	Shorted with VRT to Generate +2.6V Reference	22	VRBS	Shorted with VRB to Generate +0.6V Reference

Absolute Maximum Ratings (Beyond which damage may occur) 25^{0}C

Supply Voltages

V_{DD} ……...-0.5 to +7.0 V

Input Voltages

Analog Input ……...AGND to V_{DD}

Reference Input Voltage ……..…AGND to V_{DD}

ESD Susceptibility ……±1,500V

Temperature

Operating Temperature ……..……-20 to +70^{0}C

Junction Temperature ……175^{0}C

Lead Temperature, (Soldering 10 seconds) ……..300^{0}C

Storage Temperature ……...….-55 to +125^{0}C

Electrical Specifications

T_a=+25^{0}C, AV_{DD}=DV_{DD}= V_{DD} =+5.0V, AGND=DGND=0.0V, V_{RB}=1V and V_{RT}=3V, fs=20 MSPS ,unless otherwise specified.

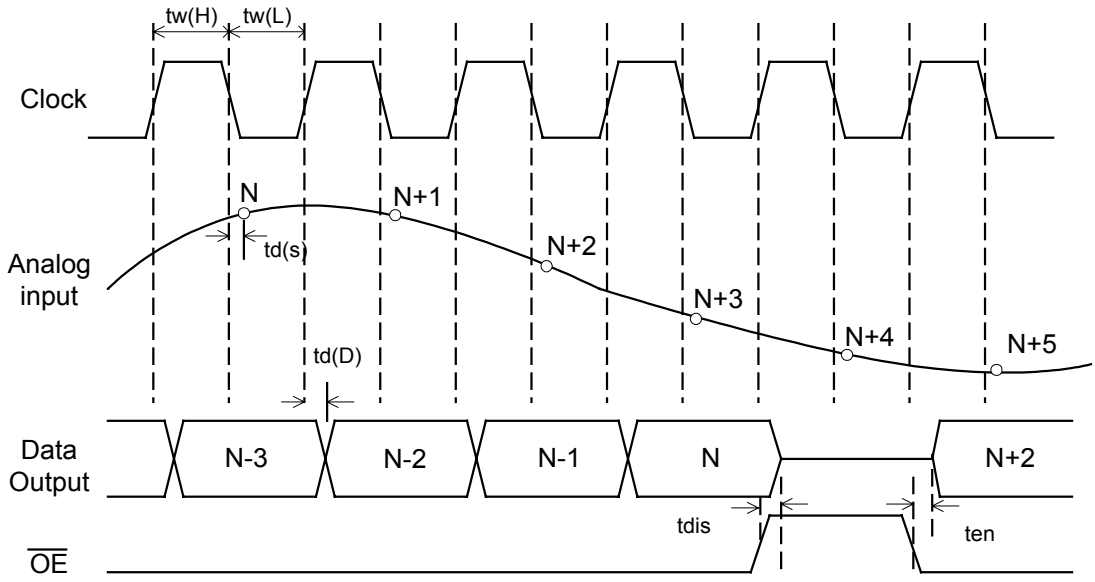
PARAMETERS	TEST CONDICTION	MIN	TYP	MAX	UNITS
Resolution		8			Bits
DC Accuracy (+25^{0}C)					
Integral Nonlinearity	fs=20 MSPS,		±0.8		LSB
Differential Nonlinearity	V_{IN} =1.0V to 3.0V		±0.5		LSB
Zero Scale Error	EZS	-10	-35	-60	mV
Full Scale Error	EFS	0	45	60	mV
No Missing Codes			Guaranteed		
Analog Input					
Input Voltage Range	V_{IN}	V_{RB}		V_{RT}	V
Input Bias Current				±5.0	μA
Input Resistance		100	200		kΩ
Input Capacitance			15		pF
Reference Input					
Reference Ladder Resistance	V_{RT} to V_{RB}	200	270	340	Ω
Reference Current	V_{RT} - V_{RB} =2.0V	5.2	7.5	10.5	mA
Reference Input Voltage	V_{RB}	0.0	0.6	3.0	V
	V_{RT}	2.0	2.6	V_{DD}	V
Reference Differential	V_{RT} - V_{RB}	1.0	-	5.0	V
Internal Bias1	V_{RB}	0.55	0.60	0.65	V
	V_{RT} –V_{RB}	1.9	2.0	2.1	V
	Short V_{RT} and V_{RTS}				
	Short V_{RB} and V_{RBS}				
Internal Bias2 (V_{RT})	Short V_{RT} and V_{RTS}	2.25	2.39	2.53	V
	Short V_{RB} and AGND				
Dynamic Performance					
Signal-To-Noise Ratio	fs=14.29 MSPS				
fin=1.667MHz		44	46		dB
fin=3.85MHz		43			dB
Spurious Free Dynamic Range	fs=14.29 MSPS				
fin=1.667MHz		43	48		dB
fin=3.85MHz		41	42		dB
Differential Phase	NTSC 40 IRE Mod Ramp		0.7		Degrees
Differential Gain	fs=14.3 MSPS		1.0		%
Digital Inputs					
Voltage, Logic High		4.0		V_{DD}	V

Voltage, Logic Low		0		1.0	V
Input Current, Logic High	V_{DD}=max, V_{IH}=V_{DD}			5.0	μA
Input Current, Logic Low	V_{DD}=max, V_{IL}=DGND			5.0	μA
Digital Outputs					
Output Current, Logic High	V_{DD}=min V_{OH}=4.25V	- 1.1			mA
Output Current, Logic Low	V_{DD}=min V_{OL}=0.4V	2.0			mA
Output Current, High 'Z'	V_{DD}=max /OE=V_{DD}			±1	μA
Voltage , Logic High	I_{OH} =-4mA	3.5			V
Voltage , Logic Low	I_{OL} =4mA			0.8	V
Power Supply Requirements					
AV_{DD} (Analog Supply Voltage)		+4.75	+5.0	+5.25	V
DV_{DD} (Digital Supply Voltage)		+4.75	+5.0	+5.25	V
Supply Voltage Difference	(AV_{DD}-DV_{DD})	-0.1	0.0	0.1	V
Supply Current	fs=20 MSPS(Does not include ref. current)		30		mA
Power Dissipation	NTSC ramp wave input		150		mW

Timing Specifications

T_a=+25^{0}C, AV_{DD}=DV_{DD}= V_{DD} =+5.0V, AGND=DGND=0.0V, V_{RB}=1V and V_{RT}=3V, fs=20 MSPS ,unless otherwise specified.

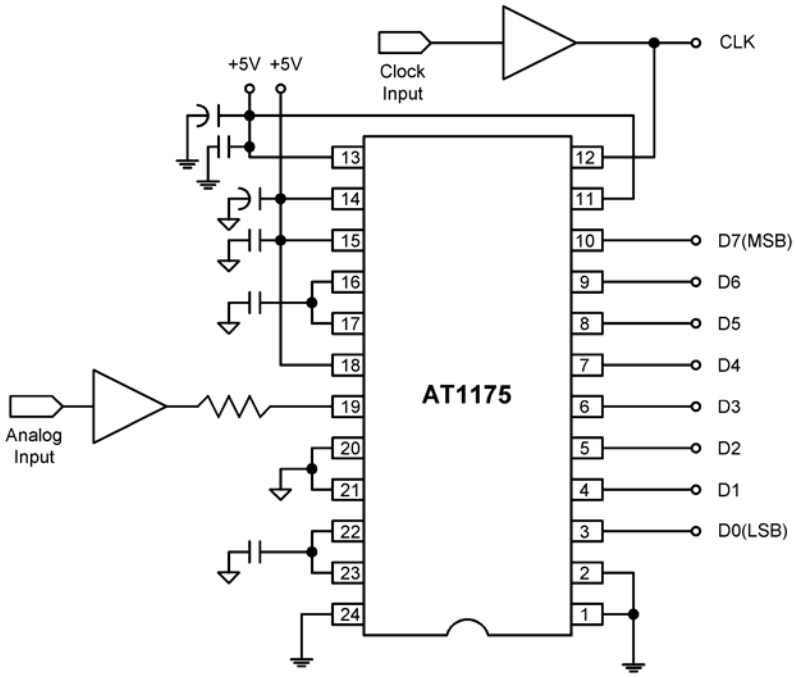
PARAMETERS	TEST CONDICTION	MIN	TYP	MAX	UNITS
f_S Maximum conversion rate	f_{in}=1kHz ramp	20			MSPS
$t_{W(H)}$ Pulse Width High		15			ns
$t_{W(L)}$ Pulse Width Low		15			ns
$t_{d(D)}$ Digital output delay time	C_L≦10pF		18	30	ns
t_{AJ} Aperture jitter time			30		ps
$t_{d(S)}$ Sampling delay time			4		ns
t_{en} Output Enable time	C_L=10pF		5		ns
t_{dis} Output Disable time	C_L=10pF		7		ns



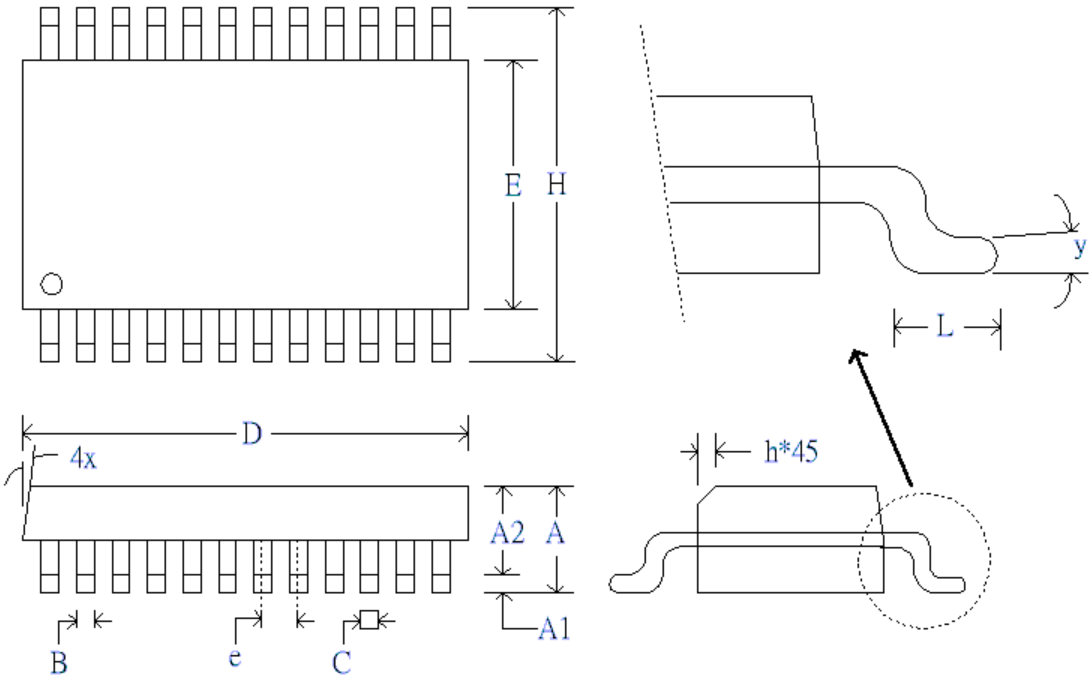
Digital Output Code

Input Signal Voltage	Step	Digital output code MSB							LSB
V_{RT}	0	1	1	1	1	1	1	1	1
	.	1	1	1	1	1	1	1	0
	.					.			
	.					.			
	127	1	0	0	0	0	0	0	0
	128	0	1	1	1	1	1	1	1
	.					.			
	.					.			
	254	0	0	0	0	0	0	0	1
V_{RB}	255	0	0	0	0	0	0	0	0

Typical Application Schematic



Package Outline (24-pin 300 mil Plastic SOP)



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	-	0.30	0.004	-	0.012
A2	-	2.34	-	-	0.092	-
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.23	0.25	0.33	0.009	0.010	0.012
D	15.19	15.39	15.49	0.598	0.606	0.610
E	7.39	7.49	7.59	0.291	0.295	0.299
e	-	1.27	-	-	0.050	-
H	10.01	10.31	10.64	0.394	0.406	0.419
L	0.38	0.81	1.27	0.015	0.032	0.050
y	0	-	8	0	-	8