SI2301

PUOLOP 迪浦

-20V P-Channel Enhancement Mode MOSFET

VDS= -20V

RDS(ON), Vgs@-4.5V, Ids@-2.3A ＜130mΩ

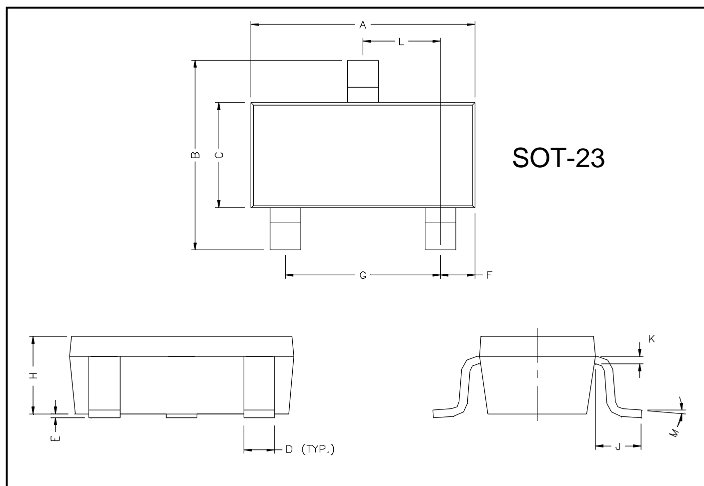
RDS(ON), Vgs@-2.5V, Ids@-2.0A ＜190mΩ

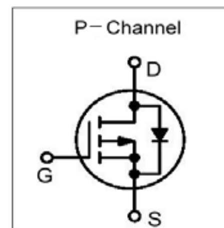
Features

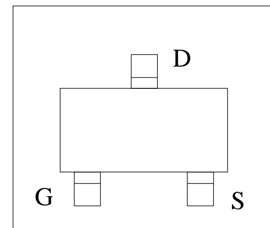
Advanced trench process technology

High Density Cell Design For Ultra Low On-Resistance

Package Dimensions







REF.	Millimeter		REF.	Millimete	
	Min.	Max.		Min.	Max.
A	2.80	3.00	G	1.80	2.00
B	2.30	2.50	H	0.90	1.1
C	1.20	1.40	K	0.10	0.20
D	0.30	0.50	J	0.35	0.70
E	0	0.10	L	0.92	0.98
F	0.45	0.55	M	0°	10°

Maximum Ratings and Thermal Characteristics (TA = 25oC unless otherwise noted)

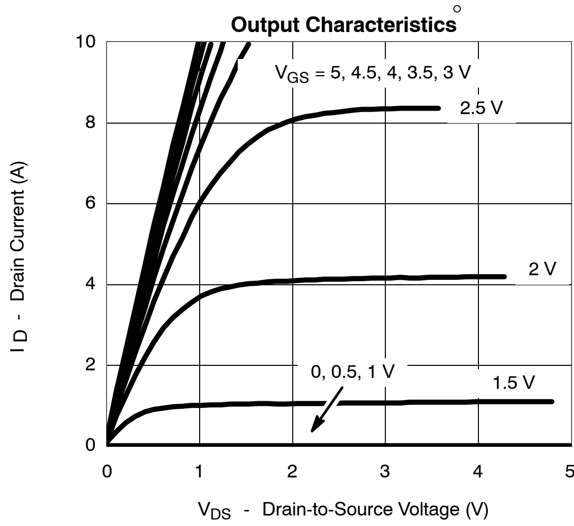
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current		I_D	-2.3	A
Pulsed Drain Current [1)]		I_{DM}	-8	
Maximum Power Dissipation [2)]	TA = 25°	P_D	1.25	W
	TA = 75°C		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Junction-to-Ambient Thermal Resistance (PCB mounted) [2)]		R_{thJA}	100	°C/W
Junction-to-Ambient Thermal Resistance (PCB mounted) [3)]			166	

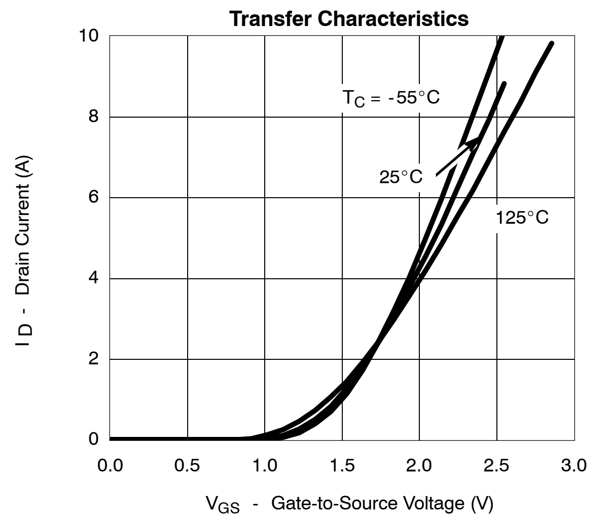
Notes
1) Pulse width limited by maximum junction temperature.
2) Surface Mounted on FR4 Board, t ≤ 5 sec.
3) Surface Mounted on FR4 Board.

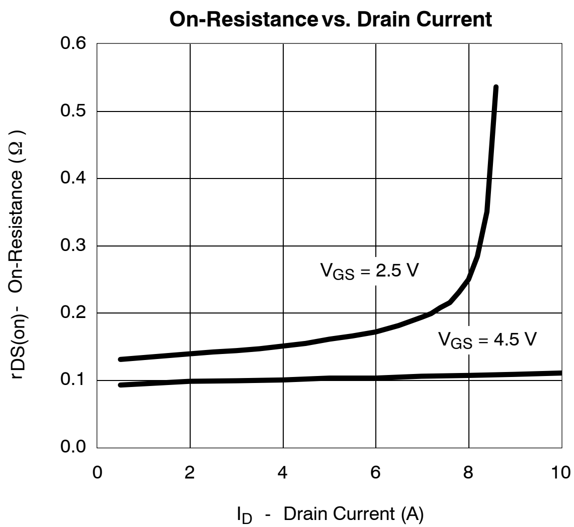
ELECTRICAL CHARACTERISTICS

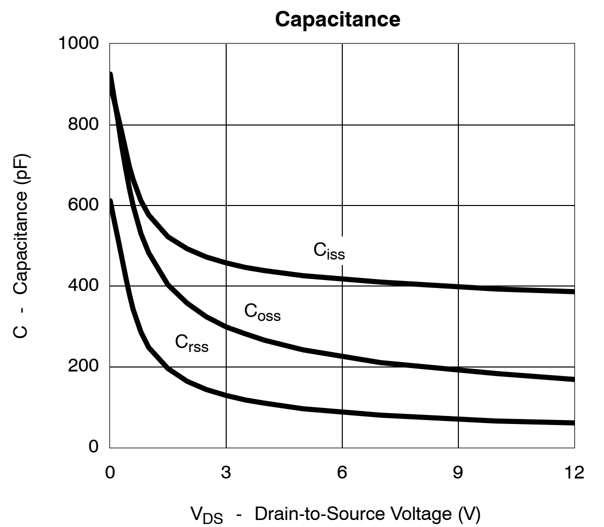
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250uA	-20			V
Drain-Source On-State Resistance[1)]	$R_{DS(on)}$	V_{GS} = -4.5V, I_D = -2.3A		105	130	mΩ
		V_{GS} = -2.5V, I_D = -2.0A		145	190	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D = -250uA	-0.45			V
Zero Gate Voltage Drain Current 0	I_{DSS}	V_{DS} = -16V, V_{GS} = 0V			-1	uA
		V_{DS} = -16V, V_{GS} = 0V TJ=55°C			-10	
Gate Body Leakage	I_{GSS}	V_{GS} = ± 8V, V_{DS} = 0V			±100	nA
Forward Transconductance[1)]	g_{fs}	V_{DS} = -5V, I_D = -2.3A		6.5	—	S
Dynamic						
Total Gate Charge	Q_g	V_{DS} = -6V, I_D ≅ -2.3A V_{GS} = -4.5V		5.8		nC
Gate-Source Charge	Q_{gs}			0.85		
Gate-Drain Charge	Q_{gd}			1.7		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -6V, RL=6Ω I_D ≅ -1.A, V_{GEN} = -4.5V R_G = 6Ω		13		ns
Turn-On Rise Time	t_r			36		
Turn-Off Delay Time	$t_{d(off)}$			42		
Turn-Off Fall Time	t_f			34		
Input Capacitance	C_{iss}	V_{DS} = -6V, V_{GS} = 0V f = 1.0 MHz		415		pF
Output Capacitance	C_{oss}			223		
Reverse Transfer Capacitance	C_{rss}			87		
Source-Drain Diode						
Max. Diode Forward Current	I_S				-1.6	A
Diode Forward Voltage	V_{SD}	I_S = -1.0A, V_{GS} = 0V		-0.8	-1.2	V

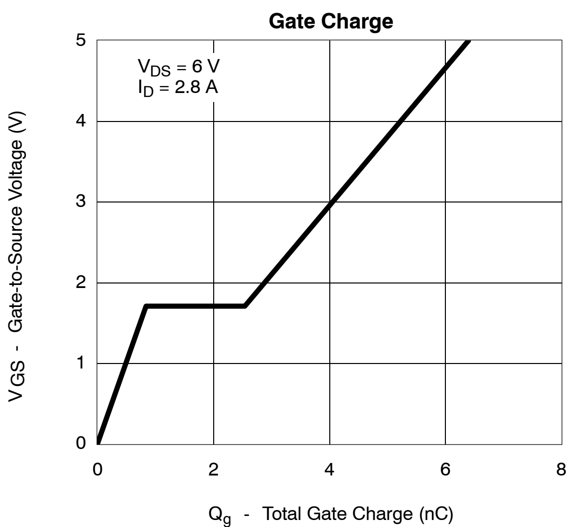
1) Pulse test: pulse width <= 300us, duty cycle<= 2%

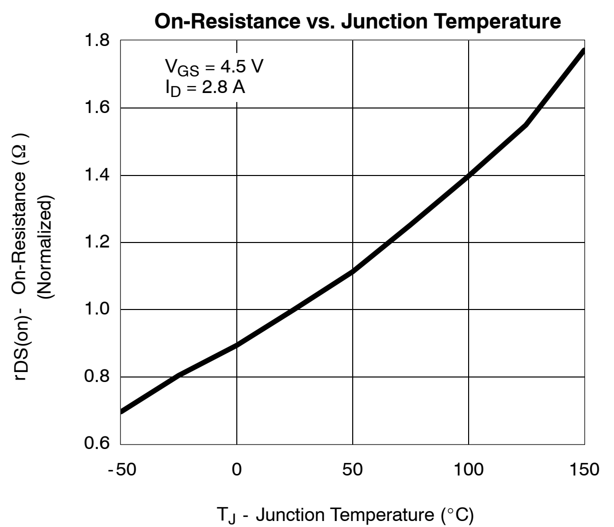

Output Characteristics
VGS = 5, 4.5, 4, 3.5, 3 V
2.5 V
2 V
1.5 V
0, 0.5, 1 V
I D - Drain Current (A)
VDS - Drain-to-Source Voltage (V)

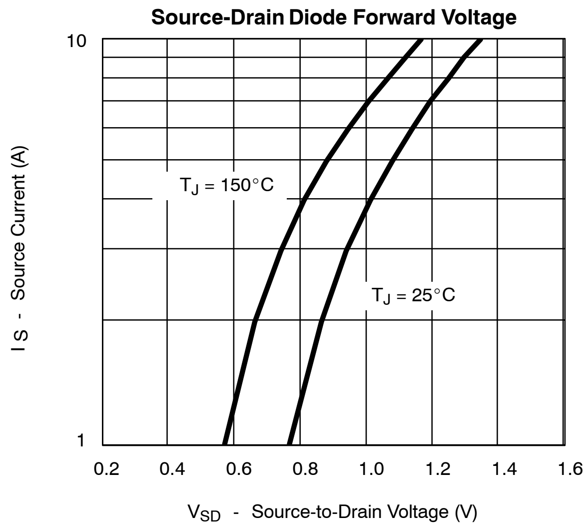

Transfer Characteristics
TC = -55°C
25°C
125°C
I D - Drain Current (A)
VGS - Gate-to-Source Voltage (V)

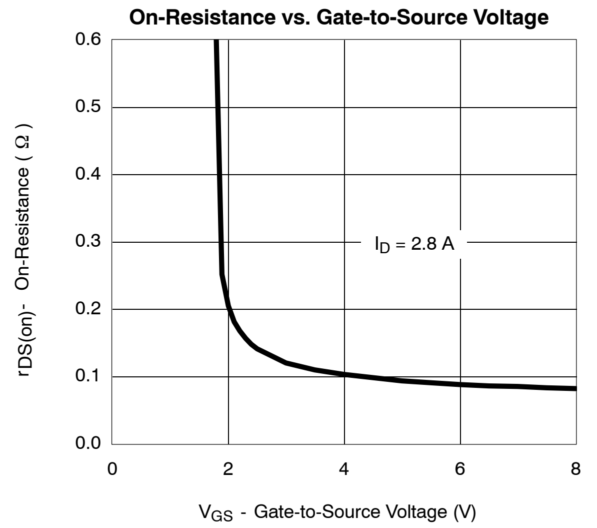

On-Resistance vs. Drain Current
VGS = 2.5 V
VGS = 4.5 V
rDS(on) - On-Resistance (Ω)
ID - Drain Current (A)

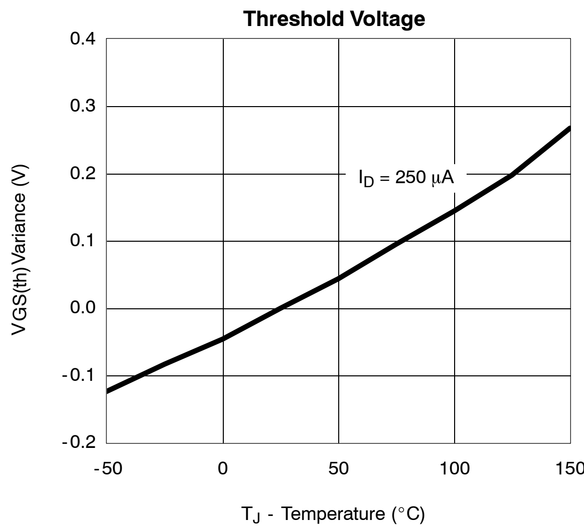

Capacitance
Ciss
Coss
Crss
C - Capacitance (pF)
VDS - Drain-to-Source Voltage (V)

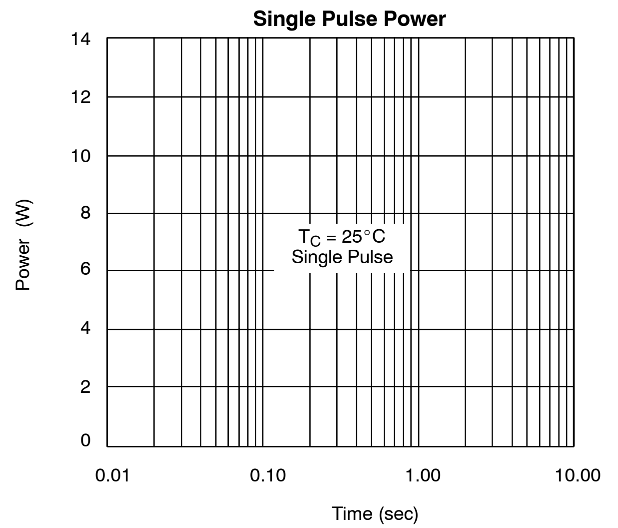

Gate Charge
VDS = 6 V
ID = 2.8 A
VGS - Gate-to-Source Voltage (V)
Qg - Total Gate Charge (nC)

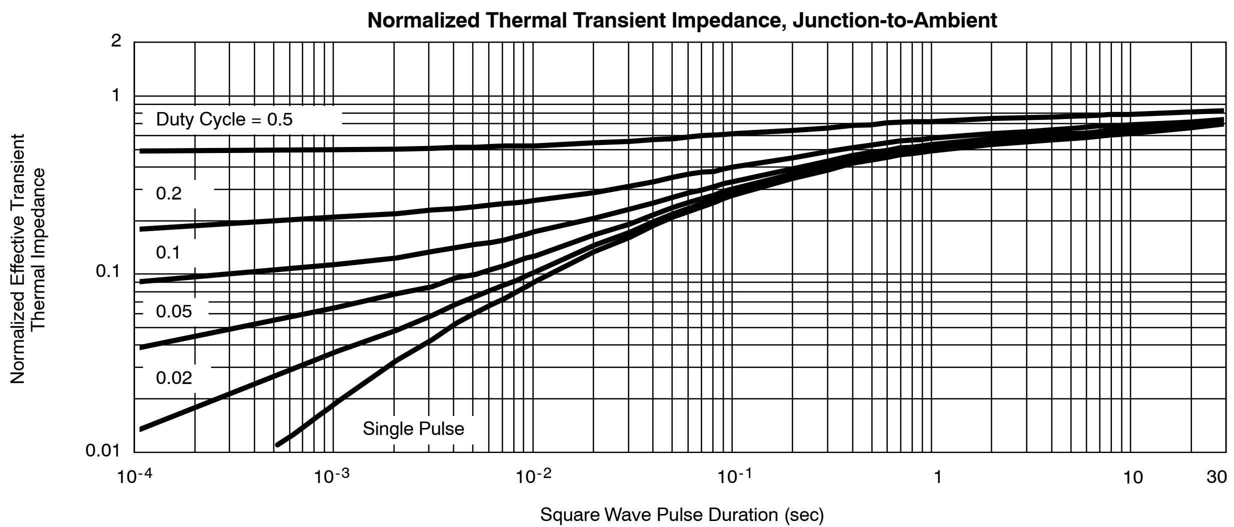

On-Resistance vs. Junction Temperature
VGS = 4.5 V
ID = 2.8 A
rDS(on) - On-Resistance (Ω)
(Normalized)
TJ - Junction Temperature (°C)


Source-Drain Diode Forward Voltage
10
1
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
TJ = 150°C
TJ = 25°C
I S - Source Current (A)
VSD - Source-to-Drain Voltage (V)


On-Resistance vs. Gate-to-Source Voltage
0.6
0.5
0.4
0.3
0.2
0.1
0.0
0
2
4
6
8
ID = 2.8 A
rDS(on)- On-Resistance (Ω)
VGS - Gate-to-Source Voltage (V)


Threshold Voltage
0.4
0.3
0.2
0.1
0.0
-0.1
-0.2
-50
0
50
100
150
ID = 250 µA
VGS(th) Variance (V)
TJ - Temperature (°C)


Single Pulse Power
14
12
10
8
6
4
2
0
0.01
0.10
1.00
10.00
TC = 25°C
Single Pulse
Power (W)
Time (sec)


Normalized Thermal Transient Impedance, Junction-to-Ambient
2
1
0.1
0.01
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
Single Pulse
10-4
10-3
10-2
10-1
1
10
30
Normalized Effective Transient Thermal Impedance
Square Wave Pulse Duration (sec)