19-3420; Rev 0; 9/04

EVALUATION KIT AVAILABLE

High-Current, Low-Voltage Linear Regulator with Power-Limited, External MOSFET

General Description

The MAX8704 high-current linear regulator uses an external n-channel MOSFET to generate low-voltage supplies for notebook computers. This linear regulator delivers an output voltage as low as 0.5V from an input voltage as low as 1.0V. Normally, this low input requirement would make the design of such a regulator very difficult. In this application, the 5V bias supply that is always available in the system powers the MAX8704 driver and control circuitry.

The MAX8704 includes a fixed current limit and an adjustable power limit to protect the external MOSFET from overheating. Additionally, the MAX8704 includes an internal thermal limit to prevent damage to the controller and provide remote thermal protection for the external MOSFET.

The MAX8704 features an adjustable soft-start function and generates a delayed power-good (PGOOD) signal that signals when the linear regulator is in regulation. The MAX8704 is available in a 10-pin µMAX® package.

Applications

V_{MCH} and V_{CCP} CPU Supplies

Notebook Computers

Desktop Computers

Servers

VID Power Supplies

Low-Voltage Bias Supplies

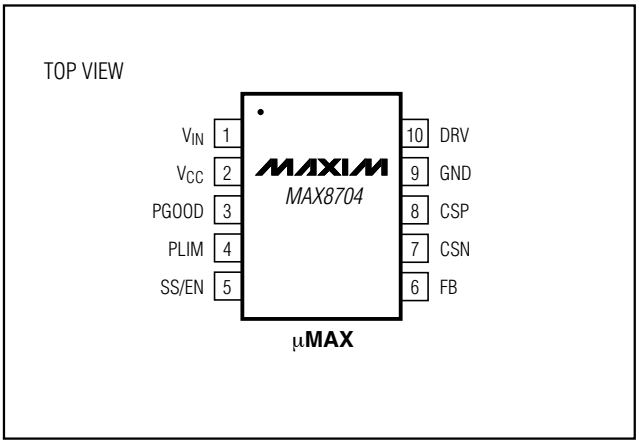
Features

- **Low-Cost, High-Current Linear Regulator**
- **External MOSFET Protection**
  - **MOSFET Power Limit**
  - **50mV (typ) Current Limit**
  - **Thermal Limit**
- **1.0V to 5.5V Input Supply Voltage**
- **1.2V or 1.5V Preset, or Adjustable Output Voltage**
- **Power-Good (PGOOD) Open-Drain Output with 3ms Startup Delay**
- **Programmable Soft-Start**
- **Shutdown with Output Discharge**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8704EUB	-40°C to +85°C	10 µMAX

Pin Configuration



µMAX is a registered trademark of Maxim Integrated Products, Inc.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

High-Current, Low-Voltage Linear Regulator with Power-Limited, External MOSFET

ABSOLUTE MAXIMUM RATINGS

V_{CC}, V_{IN} to GND .....-0.3V to +6V
CSP, CSN, DRV to GND .....-0.3V to +6V
FB, PLIM, SS/EN, PGOOD to GND.....-0.3V to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derated 5.6mW/°C above +70°C).....444mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V, V_{CC} = 5.0V, PLIM = FB = GND, CSP = CSN, SS/EN floating, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		1.0		5.5	V
	V_{CC}		4.5		5.5	
Preset Output Voltage (Fixed)	V_{OUT}	FB = V_{CC}	1.462	1.50	1.538	V
		FB = GND	1.170	1.20	1.230	
Feedback Voltage Accuracy (Adjustable)	V_{FB}	FB = CSN	490	500	510	mV
Load-Regulation Error		V_{CSP} - V_{CSN} = 45mV	-2.5	-2		%
Line-Regulation Error		V_{IN} = 1V to 5.5V		0.01		%
FB Input Bias Current	I_{FB}	V_{FB} = 0.6V	-1		+1	µA
CSN Input Bias Current	I_{CSN}	V_{CSN} = 1.6V		50	100	µA
DRV Output Voltage Swing	V_{DRV}	Output high	V_{CC} - 1.0	V_{CC} - 0.7		V
		Output low		0.7	1.0	
DRV Slew Rate		C_{DRV} = 40nF		0.2		V/µs
Quiescent Supply Current (V_{CC})	I_{CC}	FB forced above the regulation point, V_{CSN} = 1.6V		1.5	3	mA
Quiescent Supply Current (V_{IN})	I_{IN}	FB forced above the regulation point, V_{CSN} = 1.6V		5	10	µA
Shutdown Supply Current (V_{CC})		SS/EN = GND		35	70	µA
Shutdown Supply Current (V_{IN})		SS/EN = GND		5	10	µA
FAULT DETECTION						
Thermal-Shutdown Threshold	T_{SHDN}	Rising edge, 20°C hysteresis		+140		°C
V_{CC} Undervoltage-Lockout Threshold		Rising edge, 15mV hysteresis		4.2	4.45	V
Current-Limit Threshold	$V_{CSLIMIT}$	PLIM = GND	45	50	57	mV
Power-Limit Threshold	$V_{PWRLIMIT}$	Rising edge	0.96	1.0	1.04	V
Power-Limit Conversion Gain	K_{PLIM}	V_{CSP} - V_{CSN} = 30mV, V_{CSN} = 0.5V, V_{IN} = 3.5V	155	200	233	µA/V^2
Power-Limit Conversion Gain Variation		V_{CSP} - V_{CSN} = 25mV to 45mV, V_{CSN} = 0.5V, V_{IN} = 2V to 4.5V		±12		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 2.5V, V_{CC} = 5.0V, PLIM = FB = GND, CSP = CSN, SS/EN floating, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PLIM Output Current		V_{CSP} - V_{CSN} = 30mV, V_{IN} = 3.5V, V_{CSN} = 0.5V	14	18	21	µA
PLIM Output Current Offset		CSP = CSN, V_{IN} = 1.0V, V_{CSN} = 0.5V		0.5	2	µA
CSP Input Current		V_{CSN} = 1.50V, V_{CSP} = 1.55V	-1		+1	µA
SOFT-START AND SHUTDOWN						
Soft-Start Charge Current	I_{SS}	$V_{SS/EN}$ = 1.5V	4	5	6	µA
SS/EN Full Current Threshold				2		V
SS/EN Enable Threshold		Rising edge	0.4	0.5	0.6	V
SS/EN Discharge Current	$I_{SS/EN}$	$V_{SS/EN}$ = 1.5V, thermal fault, bias fault condition, or UVLO		10	20	µA
Discharge-Mode On-Resistance	R_{CSN}			10		Ω
INPUTS AND OUTPUTS						
PGOOD Trip Threshold		With respect to error-comparator threshold, 2% hysteresis	-10	-8	-6	%
PGOOD Startup Delay			1	3	5	ms
PGOOD Output Low Voltage		I_{SINK} = 4mA			0.3	V
PGOOD Leakage Current	I_{PGOOD}	V_{FB} = 1.0V (PGOOD high impedance), PGOOD forced to 5V	-1		+1	µA

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.5V, V_{CC} = 5.0V, PLIM = FB = GND, CSP = CSN, SS/EN floating, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Voltage Range	V_{IN}		1.0	5.5	V
	V_{CC}		4.5	5.5	
Preset Output Voltage (Fixed)	V_{OUT}	FB = V_{CC}	1.455	1.545	V
		FB = GND	1.158	1.242	
Feedback Voltage Accuracy (Adjustable)	V_{FB}	FB = CSN	485	515	mV
DRV Output Voltage Swing	V_{DRV}	Output high	V_{CC} - 1.1		V
		Output low		1.1	
Quiescent Supply Current (V_{CC})	I_{CC}	FB forced above the regulation point, V_{CSN} = 1.6V		3	mA
Quiescent Supply Current (V_{IN})	I_{IN}	FB forced above the regulation point, V_{CSN} = 1.6V		10	µA
Shutdown Supply Current (V_{CC})		SS/EN = GND		70	µA
Shutdown Supply Current (V_{IN})		SS/EN = GND		10	µA

High-Current, Low-Voltage Linear Regulator with Power-Limited, External MOSFET

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 2.5V, V_{CC} = 5.0V, PLIM = FB = GND, CSP = CSN, SS/EN floating, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

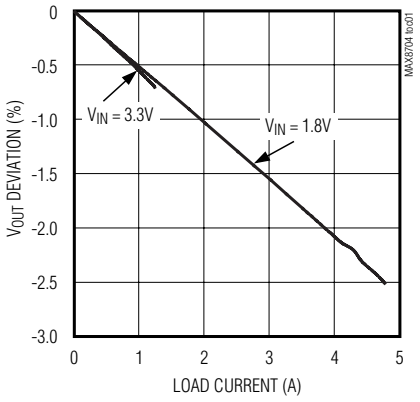
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
FAULT DETECTION					
V_{CC} Undervoltage-Lockout Threshold		Rising edge, 15mV hysteresis		4.45	V
Current-Limit Threshold	$V_{CSLIMIT}$	PLIM = GND	43	60	mV
Power-Limit Threshold	$V_{PWRLIMIT}$	Rising edge	0.90	1.10	V
PLIM Output Current		V_{CSP} - V_{CSN} = 30mV, V_{IN} = 3.5V, V_{CSN} = 0.5V	13	22	µA
SOFT-START AND SHUTDOWN					
Soft-Start Charge Current	I_{SS}	$V_{SS/EN}$ = 0	4	6	µA
SS/EN Enable Threshold		Rising edge	0.4	0.6	V
INPUTS AND OUTPUTS					
PGOOD Trip Threshold		With respect to error-comparator threshold, 2% hysteresis	-11	-5	%
PGOOD Startup Delay			0.5	5.5	ms
PGOOD Output Low Voltage		I_{SINK} = 4mA		0.3	V

Note 1: Specifications to -40°C are guaranteed by design, not production tested.

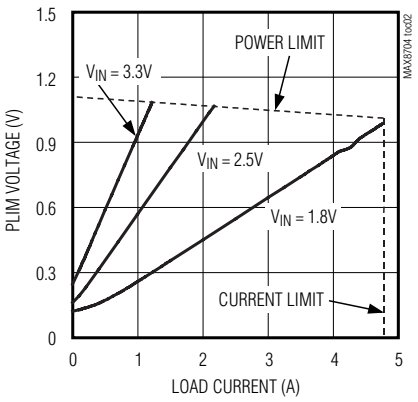
Typical Operating Characteristics

(Circuit of Figure 1, V_{OUT} = 1.5V, T_A = +25°C, unless otherwise noted.)

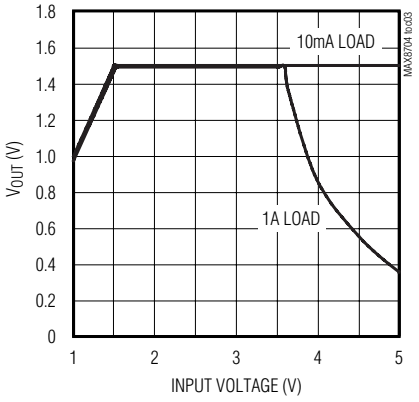
OUTPUT VOLTAGE DEVIATION vs. LOAD CURRENT



PLIM VOLTAGE vs. LOAD CURRENT



OUTPUT VOLTAGE vs. INPUT VOLTAGE

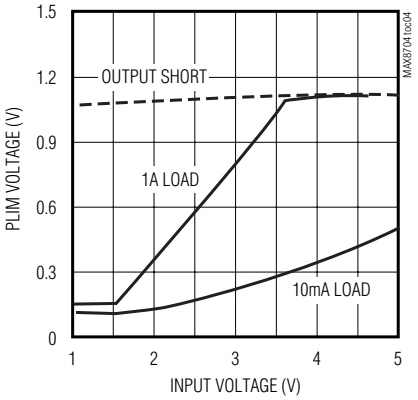


High-Current, Low-Voltage Linear Regulator with Power-Limited, External MOSFET

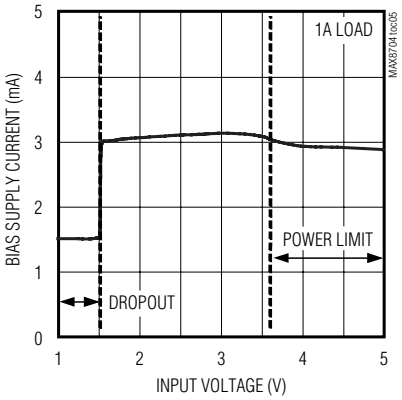
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{OUT} = 1.5V, T_A = +25°C, unless otherwise noted.)

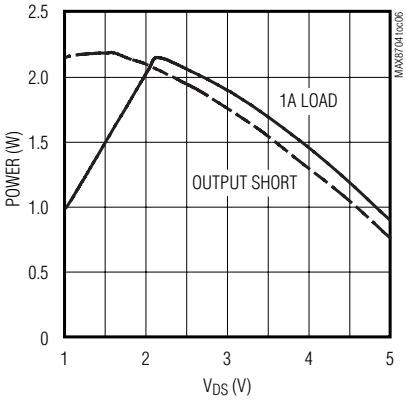
PLIM VOLTAGE vs. INPUT VOLTAGE



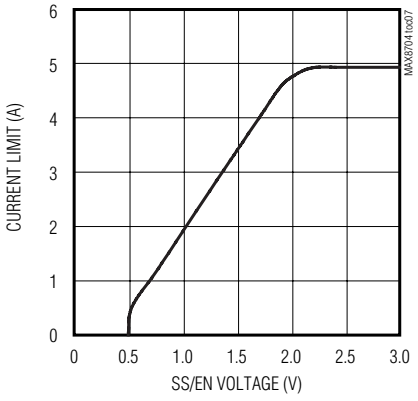
5V BIAS SUPPLY CURRENT vs. INPUT VOLTAGE



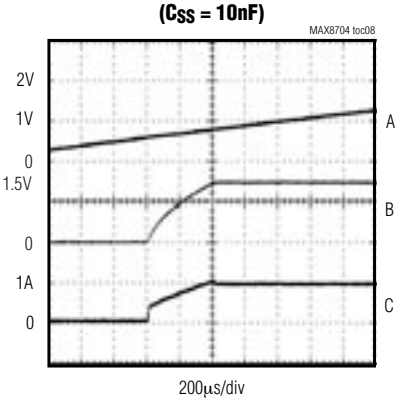
MOSFET POWER DISSIPATION vs. DRAIN-TO-SOURCE VOLTAGE



OUTPUT CURRENT LIMIT vs. SS/EN VOLTAGE

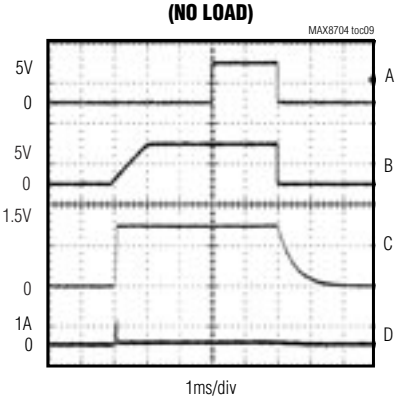


SOFT-START (C_{SS} = 10nF)



A. EN/SS, 1V/div
B. LDO OUTPUT, 1V/div
C. FET CURRENT, 1A/div
1.5Ω LOAD, V_{IN} = 1.8V

SHUTDOWN SEQUENCE (NO LOAD)



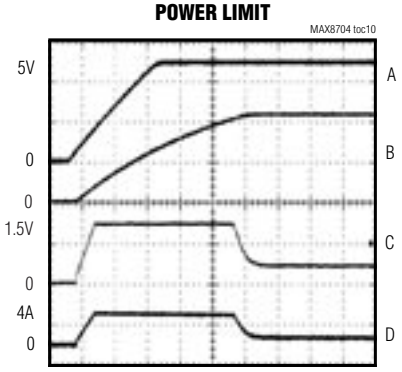
A. PGOOD, 5V/div
B. EN/SS, 5V/div
C. LDO OUTPUT, 1V/div
D. FET CURRENT, 2A/div
NO LOAD, C_{SS} = 1nF, V_{IN} = 1.8V

High-Current, Low-Voltage Linear Regulator with Power-Limited, External MOSFET

Typical Operating Characteristics (continued)

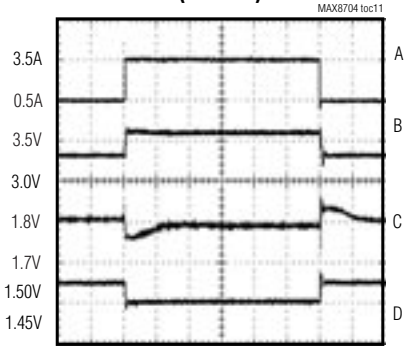
(Circuit of Figure 1, V_{OUT} = 1.5V, T_A = +25°C, unless otherwise noted.)

POWER LIMIT



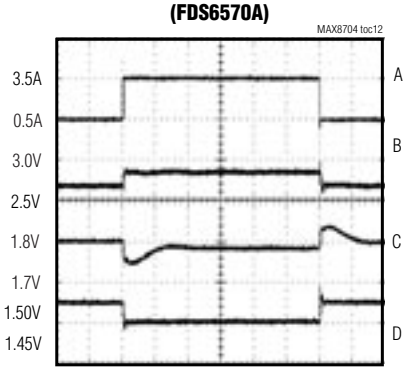
A. EN/SS, 2V/div
B. PLIM, 0.5V/div
C. LDO OUTPUT, 1V/div
D. FET CURRENT, 5A/div
0.4Ω LOAD, C_{SS} = 10nF, V_{IN} = 1.8V,
R_{PLIM} = 200kΩ, C_{PLIM} = 0.1µF

3A LOAD TRANSIENT (IRF7401)



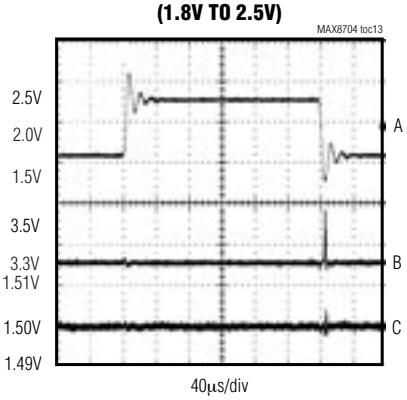
A. LOAD: 0.5A - 3.5A, 3A/div
B. DRV, 0.5V/div
C. INPUT, 100mV/div
D. OUTPUT, 50mV/div
V_{IN} = 1.8V

3A LOAD TRANSIENT (FDS6570A)



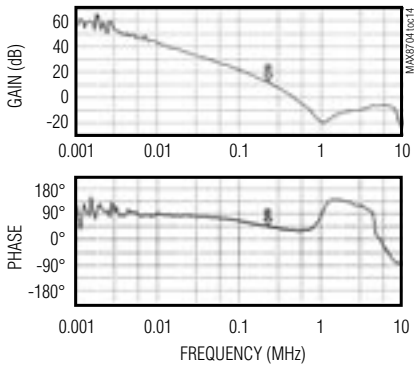
A. LOAD: 0.5A - 3.5A, 3A/div
B. DRV, 0.5V/div
C. INPUT, 100mV/div
D. OUTPUT, 50mV/div
V_{IN} = 1.8V

LINE TRANSIENT (1.8V TO 2.5V)



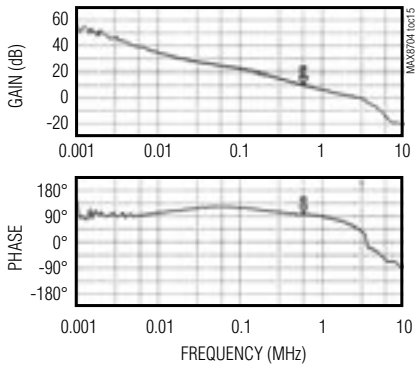
A. INPUT: 1.8V TO 2.5V, 0.5V/div
B. DRV, 200mV/div
C. OUTPUT, 10mV/div
R_{OUT} = 1.5Ω

GAIN AND PHASE vs. FREQUENCY



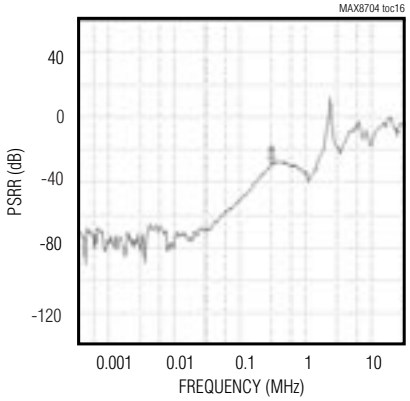
FB = CSN, V_{OUT} = 0.5V, V_{IN} = 1.0V
C_{OUT} = 2 x 22µF 1206 CERAMIC, I_{OUT} = 0.5A

GAIN AND PHASE vs. FREQUENCY



FB = CSN, V_{OUT} = 0.5V, V_{IN} = 1.0V
C_{OUT} = 100µF 70mΩ SANYO 4TPB100M, I_{OUT} = 0.5A

PSRR



FB = V_{CC}, V_{OUT} = 1.5V, V_{IN} = 2.5V
C_{OUT} = 2 x 22µF 1206 CERAMIC, I_{OUT} = 0.5A

Pin Description

PIN	NAME	FUNCTION
1	V_{IN}	Input Voltage Sense. The MAX8704 senses the voltage across the external MOSFET (V_{IN} - V_{CSN}) to determine the MOSFET's power dissipation.
2	V_{CC}	Analog and Driver Supply Input. Connect to the system supply voltage (+5.0V). Bypass V_{CC} to analog ground with a 1µF or greater ceramic capacitor.
3	PGOOD	Open-Drain Power-Good Output. PGOOD is low when the output voltage is more than 8% (typ) below the nominal regulation voltage. PGOOD is also pulled low during soft-start and in shutdown. Approximately 3ms (typ) after the LDO reaches the regulation voltage, PGOOD becomes high impedance as long as the output remains in regulation.
4	PLIM	Power-Limit Adjustment. The PLIM output sources a current directly proportional to the MOSFET's power dissipation. If the PLIM voltage exceeds the 1.0V power-limit threshold, the regulator reduces the power dissipation by folding back the current limit. An external resistor between PLIM and GND sets the maximum MOSFET's power dissipation. Additionally, an external capacitor filters the PLIM voltage, allowing short high-power transients to occur periodically.
5	SS/EN	Soft-Start and Enable Input. Connect SS/EN to an open-drain output. When SS/EN is pulled low, the linear regulator shuts down and pulls the output to ground. Connect a soft-start capacitor from SS/EN to GND to slowly ramp up the current limit during startup (see the *Soft-Start and Enable* section).
6	FB	Feedback Input. Connect FB to V_{CC} for a fixed 1.5V output, or connect FB to GND for a fixed 1.2V output. For an adjustable output, connect FB to a resistive divider from the output voltage. The FB regulation level is 0.5V.
7	CSN	Negative Current-Sense Input and Output Sense Input. Connect to the negative terminal of the current-sense element as shown in Figure 1. CSN serves as the feedback input in fixed-voltage mode (FB = GND or V_{CC}). When the MAX8704 is disabled, the output is discharged through a 10Ω resistor to GND.
8	CSP	Positive Current-Sense Input. Connect to the positive terminal of the current-sense element as shown in Figure 1. The MAX8704 driver reduces the gate voltage when the current-limit threshold is exceeded.
9	GND	Ground
10	DRV	Gate Drive for the External n-Channel MOSFET

Detailed Description

The MAX8704 is a low-dropout, external n-channel MOSFET linear regulator for low-voltage notebook power supplies. The regulator uses two separate supplies—the notebook's 5V bias supply (V_{CC}) for driving the external n-channel MOSFET, and the lowest system supply available for the power input (V_{IN}). By using separate bias and power inputs, the MAX8704 maximizes the gate drive while minimizing the power loss. The regulator provides an accurate (-2% typ load regulation) output that delivers up to 5A for powering the low-voltage (1.0V, 1.2V, 1.5V, and 1.8V) supplies required by notebook chipsets.

Figure 1 shows the standard application circuit, and Figure 2 shows the functional diagram. The MAX8704 standard application circuit delivers up to 5A and operates with input voltages up to 5.5V, but not simultaneously. Continuous high output currents can only be achieved when the input-to-output differential voltage is low (Figure 1).

5.0V Bias Supply (Vcc)

The V_{CC} input powers the control circuitry and provides the gate drive to the external n-channel MOSFET. This improves efficiency by allowing V_{IN} to be powered from a low-voltage system supply. Power V_{CC} from a well-regulated 5V supply. Current drawn from the V_{CC} supply remains relatively constant with variations in V_{IN} and

High-Current, Low-Voltage Linear Regulator with Power-Limited, External MOSFET

load current. Bypass V_{CC} with a 1µF or greater ceramic capacitor as close to the MAX8704 as possible.

Undervoltage Lockout (UVLO)

The V_{CC} input undervoltage-lockout (UVLO) circuitry ensures that the regulator starts up with a gate-drive voltage that can adequately bias the external n-channel MOSFET. The UVLO threshold is 4.2V (typ), and V_{CC} must remain above this level for proper operation.

Power-Supply Input (V_{IN})

The power input supply (V_{IN}) sources the current required by the linear regulator's output (V_{OUT}). V_{IN} connects to the drain of the external n-channel power MOSFET. V_{IN} may be as low as 1.0V, minimizing the power dissipation across the n-channel MOSFET. Bypass V_{IN} with a 10µF or greater capacitor as close to the external MOSFET as possible. To avoid input voltage sag during a load transient, the input supply should provide a low source impedance. If a high-impedance source is used, additional input bulk capacitance is required near the MAX8704.

Soft-Start and Enable (SS/EN)

As shown in Figure 2, a capacitor on SS/EN allows a gradual buildup of the MAX8704 current limit, reducing the initial inrush current peaks at startup. The input supply UVLO and thermal-overload fault trigger the internal SS/EN pulldown resistor ($R_{SS/EN}$ = 1kΩ), automatically forcing the MAX8704 into shutdown. When properly

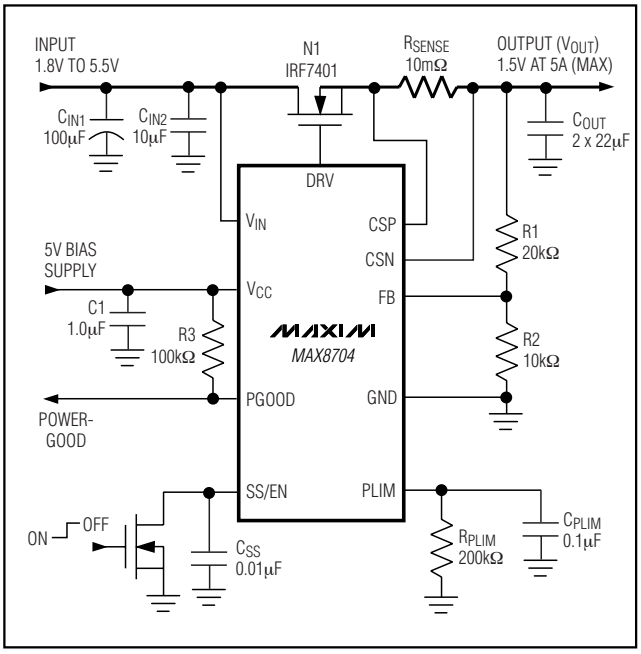


Figure 1. Standard Application Circuit

powered (V_{CC} above UVLO), the MAX8704 charges the soft-start capacitor with a constant 5µA current source (see the *Soft-Start Capacitor Selection* section). Once the SS/EN voltage rises above 0.5V, the linear regulator

Table 1. MOSFET Selection (>1.5V Output-Voltage Applications)

MOSFET	$R_{DS(ON)}$ (mΩ)		V_{DS} (V)	C_{ISS}* (nF)	PACKAGE	VENDOR
	2.5V	1.8V				
FDS6574A	7	9	20	8	SO-8 (2.5W)	Fairchild
Si4836DY	4	5	12	7	SO-8 (2.5W)	Siliconix (Vishay)

**C_{ISS} when V_{DS} = 1V*

Table 2. MOSFET Selection (0.5V to 1.5V Output-Voltage Applications)

MOSFET	$R_{DS(ON)}$ (mΩ)		V_{DS} (V)	C_{ISS}* (nF)	PACKAGE	VENDOR
	4.5V	2.5V				
IRF7401	22	30	20	2.7	SO-8 (2.5W)	International Rectifier
NDS8425	22	28	20	1.4	SO-8 (2.5W)	Fairchild
FDS6572A	6	8	20	6.2	SO-8 (2.5W)	Fairchild
FDS7064N	7.5	—	30	3.7	Bottomless SO-8 (3W)	Fairchild
Si9426DY	13.5	16	20	3.5	SO-8 (2.5W)	Siliconix (Vishay)
Si4866DY Si7882DP	5.5	8	12	3.2	SO-8 (2.5W) PowerPAK (5W)	Siliconix (Vishay)

**C_{ISS} when V_{DS} = 1V*

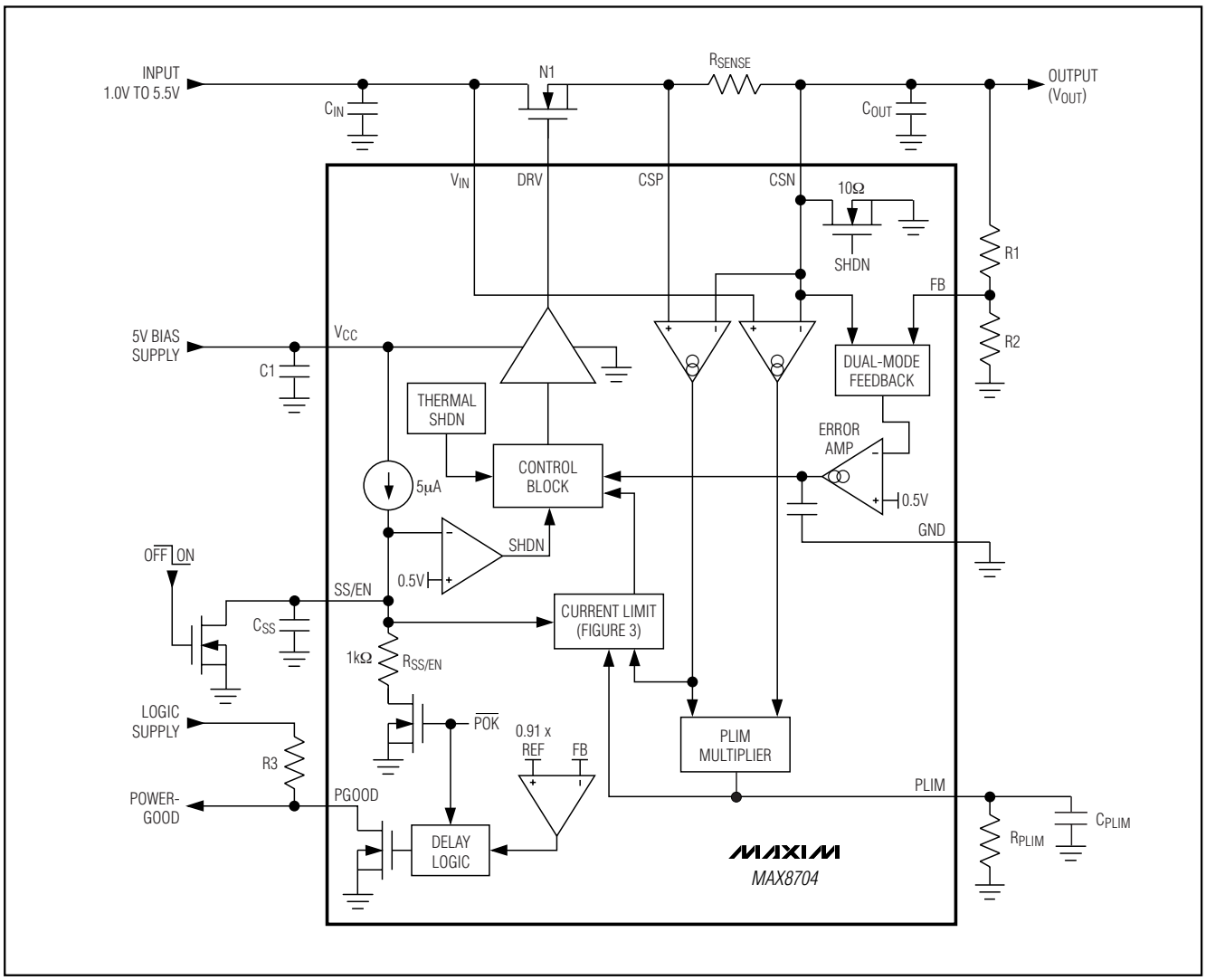


Figure 2. Functional Diagram

is enabled. As the voltage on SS/EN continues to increase, the current-limit threshold slowly ramps up, effectively limiting the input inrush current during power-up (Figure 3). The MAX8704 reaches the full current limit when the SS/EN voltage exceeds 2V.

When SS/EN is pulled low—either by an external open-drain output or by the internal power-OK (POK) lockout signal—the MAX8704 pulls the driver (DRV) low and discharges the output through a 10Ω discharge FET.

Drive SS/EN with a push/pull output to bypass soft-start.

Output Voltage and Dual Mode™ Feedback

The MAX8704's Dual-Mode operation allows the selection of two common preset voltages without requiring external components. Connect FB to V_{CC} for a fixed 1.5V output, or connect FB to GND for a fixed 1.2V output. Alternatively, the output voltage can be adjusted using a resistive voltage-divider (Figure 2). The adjusted output voltage is:

$$V_{OUT} = V_{FB}\left(1+\frac{R1}{R2}\right)$$

Dual Mode is a trademark of Maxim Integrated Products, Inc.

High-Current, Low-Voltage Linear Regulator with Power-Limited, External MOSFET

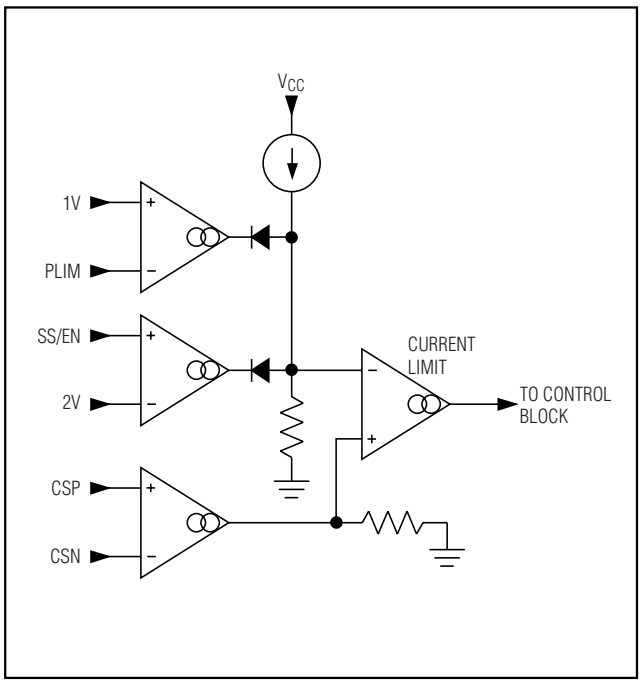


Figure 3. Current-Limit Functional Diagram

where the feedback threshold (V_{FB}) equals 0.5V, as specified in the *Electrical Characteristics* table. The minimum adjustable output voltage is 0.5V (FB = CSN). The maximum adjustable output voltage is limited by the gate driver's output-voltage swing range (see the *Electrical Characteristics* table) and the gate threshold of the selected n-channel MOSFET.

Fault Protection

Current Limit

The MAX8704 features a current limit (Figure 3) that monitors the voltage across the current-sense resistor, typically limiting the CSP to CSN voltage to 50mV. When the CSP to CSN voltage reaches the current-limit threshold, the MAX8704 regulates the output current rather than the output voltage. During startup, the soft-start circuit ramps the current limit to reduce the input surge current (see the *Soft-Start Capacitor Selection* section).

MOSFET Power-Limit Protection

The MAX8704 includes a proprietary power-limit circuit to protect the external n-channel MOSFET, especially under short-circuit conditions. The MAX8704 uses an internal multiplier circuit to generate an output current (I_{PLIM}) that is directly proportional to the MOSFET power dissipation. When the PLIM voltage exceeds 1.0V, the MAX8704 folds back the current limit to reduce the power dissipation across the external components (Figure 3). The power limit allows an output short for an indefinite period of time without damaging the MAX8704 or its external components.

Thermal-Overload Protection

Thermal-overload protection prevents the MAX8704 from overheating. When the junction temperature exceeds +140°C, the linear regulator automatically pulls PGOOD low and enters shutdown—the MAX8704 pulls SS/EN low with an internal 1kΩ pulldown resistor. This disables the driver and discharges the output, allowing the device to cool. Once the junction temperature cools by 20°C, the thermal protection circuit releases the SS/EN input, allowing the MAX8704 to automatically power up using the soft-start sequence. A continuous thermal-overload condition results in a pulsed output.

Power-Good

The MAX8704 provides an open-drain PGOOD output that goes high 3ms (typ) after the output initially reaches regulation. PGOOD transitions low immediately after the output voltage drops below 92% (typ) of the nominal regulation voltage, or when the MAX8704 enters shutdown. Connect a pullup resistor from PGOOD to V_{CC} for a logic-level output. Use a 100kΩ resistor to minimize current consumption.

Design Procedure

External MOSFET Selection

The external MOSFET selection depends on the gate threshold voltage, input-to-output voltage, and package power dissipation. The MAX8704 uses an external n-channel MOSFET controlled by a 5V driver, so the maximum gate-to-source voltage across the MOSFET ($V_{GS(MAX)}$) is equivalent to:

$$V_{GS(MAX)} = V_{DRV(MAX)} - V_{CSP}$$

where the maximum drive voltage is approximately V_{CC} - 1V. The selected MOSFET's on-resistance must be low enough to support the minimum input-to-output differential voltage (dropout voltage) and maximum load required by the application:

$$R_{DS(ON)(MIN)} = \frac{V_{IN(MIN)} - V_{CSLIMIT} - V_{OUT}}{I_{OUT(MAX)}}$$

For output voltages less than 1.5V, standard MOSFETs that provide on-resistance specifications with 2.5V gate-to-source voltages are sufficient. For output voltages greater than 1.5V, use low-threshold MOSFETs

that provide on-resistance specifications with a 1.8V gate-to-source voltage.

MOSFET Power Dissipation

The maximum power dissipation of the MAX8704 depends on the thermal resistance of the external n-channel MOSFET package, the board layout, the temperature difference between the die and ambient air, and the rate of airflow. The power dissipated in the MOSFET is:

$$P_{DIS} = I_{OUT} \times (V_{IN} - V_{CSP})$$

The maximum power dissipation allowed is determined by the following formula:

$$R_{DIS(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JC} + \theta_{CA}}$$

where $T_{J(MAX)}$ is the maximum junction temperature (+150°C), T_A is the ambient temperature, θ_{JC} is the thermal resistance from the die junction to the package case, and θ_{CA} is the thermal resistance from the case through the PC board, copper traces, and other materials to the surrounding air. Standard SO-8 MOSFETs are typically rated for 2W, while new power packages (PowerPAK, DirectFET, etc.) can achieve power dissipation ratings as high as 5W. For optimum power dissipation, use a large ground plane with good thermal contact to ground and use wide input and output traces. Extra copper on the PC board increases thermal mass and reduces the thermal resistance of the board.

Setting the Current Limit

The current-sense voltage threshold is preset to 50mV (typ), so the achievable peak source current (I_{PEAK}) is determined by the current-sense resistor. The current-sense resistor can be determined by:

$$R_{SENSE} = V_{CSLIMIT} / I_{PEAK}$$

For the best current-sense accuracy, use a 1% current-sense resistor between the source of the MOSFET and the output.

Setting the Power Limit

The MAX8704 includes a unique power-limit protection circuit that limits the maximum power dissipation in the external MOSFET. An external resistor (R_{PLIM}) adjusts the actual power limit as defined by the following equation:

$$R_{PLIM} = \frac{V_{PWRLIMIT}}{P_{LIMIT} \times K_{PLIM} \times R_{SENSE}}$$

where R_{SENSE} is the current-sense resistor, P_{LIMIT} is the maximum MOSFET power dissipation, the power-limit conversion gain (K_{PLIM}) equals 200µA/V^2, and the power-limit threshold ($V_{PWRLIMIT}$) equals 1.0V. An external capacitor (C_{PLIM}) adjusts the power-limit time constant ($\tau_{PLIM} = R_{PLIM} \times C_{PLIM}$), allowing short high-power transients while protecting against thermal stress.

Short PLIM to ground to disable the power-limit protection.

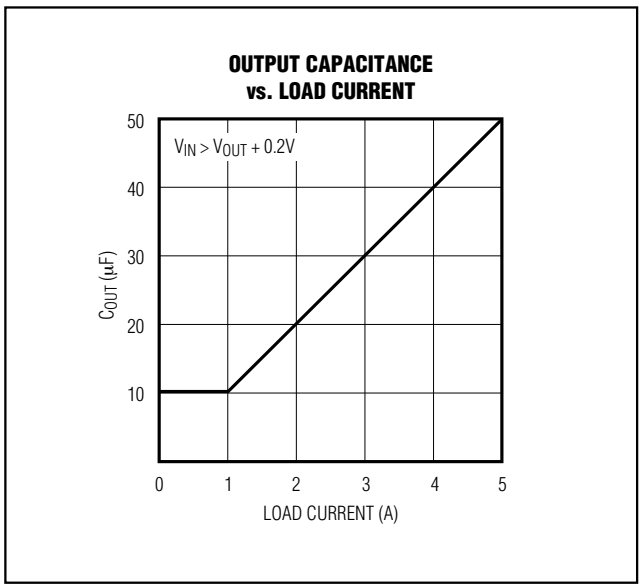


Figure 4. Output Capacitance vs. Load Current

Input Capacitor Selection (C_{IN})

Typically, the linear regulator is powered from the output of a step-down regulator, effectively providing a low-impedance source for the MAX8704. Under these conditions, a local 10µF or greater ceramic capacitor is sufficient for most applications. If the linear regulator is connected to a high-impedance input, low-ESR polymer capacitors are recommended on the input.

Output Capacitor Selection (C_{OUT})

The MAX8704 requires 10µF/A or greater ceramic capacitor for stable operation and optimized load-transient response. For higher capacitance values, the regulator remains stable with low-ESR, polymer output capacitors as shown in the Output Capacitance vs. Load Current graph (see Figure 4). When selecting the output capacitor to provide good transient response, the capacitor's ESR should be minimized:

$$\Delta V_{OUT} = \Delta I_{OUT} \times ESR$$

where ΔI_{OUT} is the maximum peak-to-peak load current step, and ΔV_{OUT} is the transient output-voltage tolerance.

High-Current, Low-Voltage Linear Regulator with Power-Limited, External MOSFET

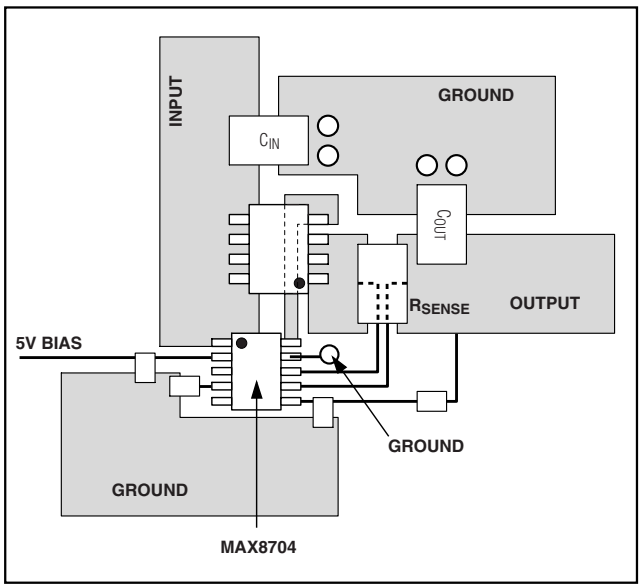


Figure 5. Recommended MAX8704 Layout

Using larger output capacitance can improve efficiency in applications where the load current changes rapidly. The output capacitor acts as a reservoir for the rapid transient currents, reducing the peak current supplied by the input supply and effectively lowering the I^2R power loss.

Soft-Start Capacitor Selection (C_{SS})

A capacitor (C_{SS}) connected from SS/EN to GND causes the MAX8704 output current to slowly rise during startup, reducing stress on the input supply. The rise time to full current limit (t_{SS}) is determined by:

$$t_{SS} = C_{SS} \times 1.5V / I_{SS}$$

where I_{SS} = 5µA is the soft-start current. Typical capacitor values between 1nF to 100nF are sufficient. Since the regulator ramps the current-limit threshold, the actual output-voltage slew rate depends on the load current and output capacitance.

Noise, PSRR, and Transient Response

The MAX8704 operates with low dropout voltage and low quiescent current in notebook computers while maintaining good noise, transient response, and AC rejection. See the *Typical Operating Characteristics* for a graph of PSRR vs. Frequency. Improved supply-noise rejection and transient response can be achieved by increasing the values of the input and output capacitors. Use passive filtering techniques when operating from noisy sources.

The MAX8704 load-transient response graphs (see the *Typical Operating Characteristics*) show two components of the output response: a DC load regulation and the transient response. A typical transient response for a step change in the load current from 0.5A to 3.5A is 25mV. Lowering the output impedance—increasing the output capacitor's value and/or decreasing the ESR—attenuates the output undershoot and overshoot.

PC Board Layout Guidelines

The MAX8704 requires proper layout to achieve the intended output power level and regulation characteristics. Proper layout involves the use of a ground plane, appropriate component placement, and correct routing of traces using appropriate trace widths (Figure 5).

- Minimize high-current ground loops: connect the ground of the MAX8704, the input capacitor, and the output capacitor together at one point.
- Minimize parasitic inductance: keep the input capacitor, external MOSFET, and output capacitor close together. Route the ground plane directly under the input and output power traces/planes.
- To optimize performance and power dissipation, a ground plane is essential. Dedicated ground plane layers reduce trace inductance, ground impedance, and noise coupling (ground shield) between layers, and improve thermal conductivity throughout the board.
- Connect the input filter capacitor less than 10mm from the MOSFET. The connecting copper trace carries large currents and must be at least 5mm wide. Use as much copper as necessary to decrease the thermal resistance of the MOSFET. In general, more copper provides better heatsinking capabilities.

Chip Information

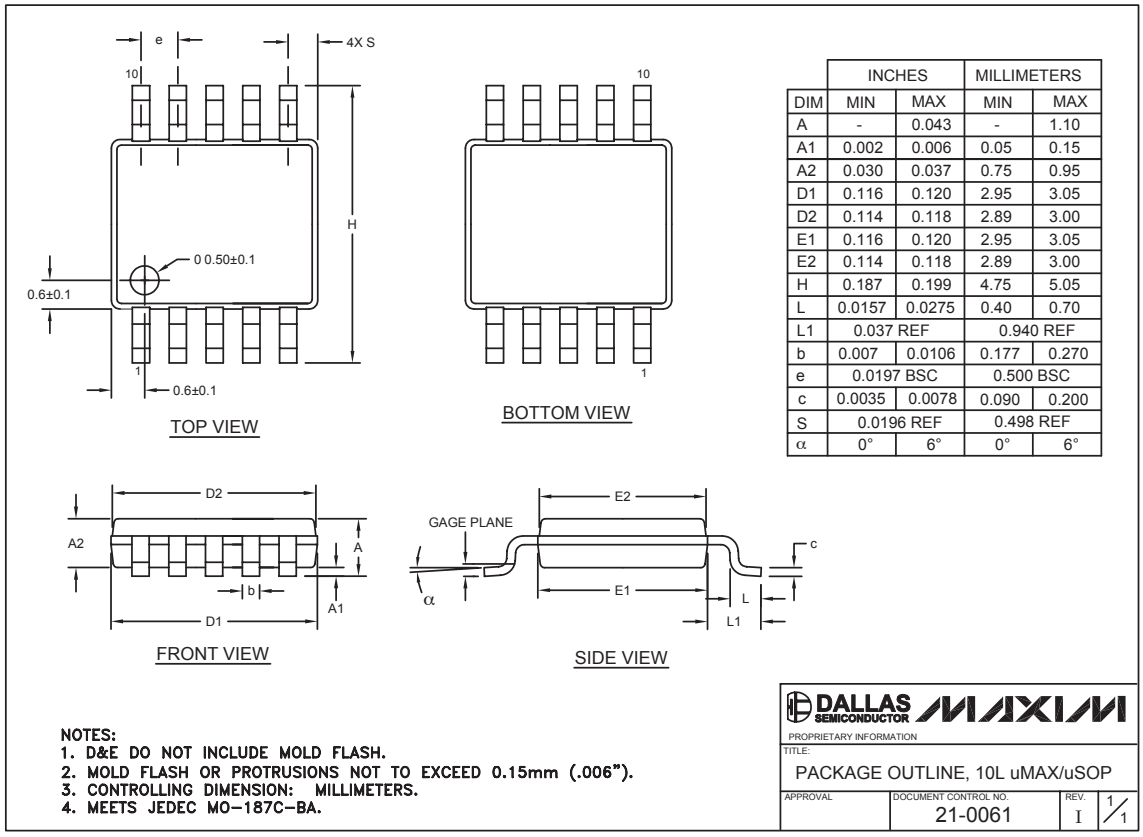
TRANSISTOR COUNT: 786

PROCESS: BiCMOS

High-Current, Low-Voltage Linear Regulator with Power-Limited, External MOSFET

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°

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