



SiPHY™ MULTI-RATE SONET/SDH CLOCK AND DATA RECOVERY IC

Features

Complete high speed, low power, CDR solution includes the following:

- Supports OC-48/12/3, STM-16/4/1, Gigabit Ethernet, and 2.7 Gbps FEC
- Low Power—270 mW (TYP OC-48)
- Small Footprint: 4 mm x 4 mm
- DSPLL™ Eliminates External Loop Filter Components
- 3.3 V Tolerant Control Inputs
- Exceeds All SONET/SDH Jitter Specifications
- Jitter Generation 3.0 mUI_{RMS} (TYP)
- Device Power Down
- Loss-of-Lock Indicator
- Single 2.5 V Supply

Applications

- SONET/SDH/ATM Routers
- Add/Drop Multiplexers
- Digital Cross Connects
- Gigabit Ethernet Interfaces
- SONET/SDH Test Equipment
- Optical Transceiver Modules
- SONET/SDH Regenerators
- Board Level Serial Links

Description

The Si5020 is a fully integrated low-power clock and data recovery (CDR) IC designed for high-speed serial communication systems. It extracts timing information and data from a serial input at OC-48/12/3, STM-16/4/1, or Gigabit Ethernet (GbE) rates. Support for 2.7 Gbps data streams is also provided for OC-48/STM-16 applications that employ forward error correction (FEC). DSPLL™ technology eliminates sensitive noise entry points thus making the PLL less susceptible to board-level interaction and helping to ensure optimal jitter performance.

The Si5020 represents a new standard in low jitter, low power, and small size for high speed CDRs. It operates from a single 2.5 V supply over the industrial temperature range (–40°C to 85°C).

Functional Block Diagram

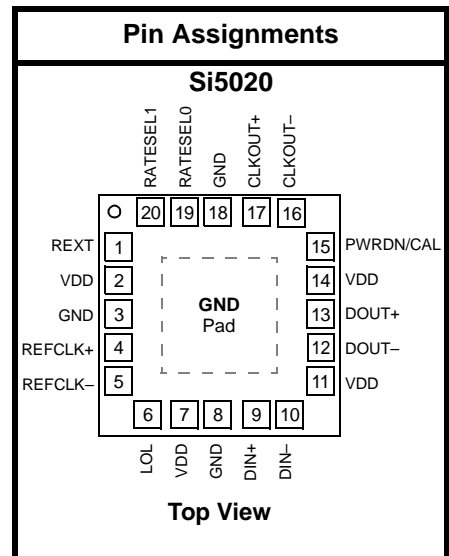
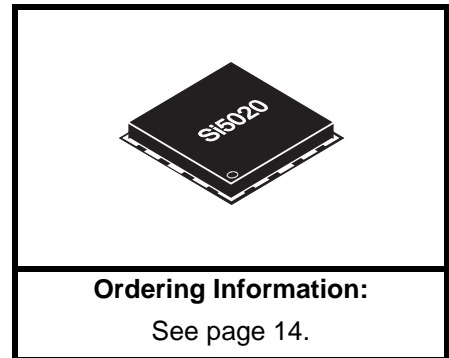
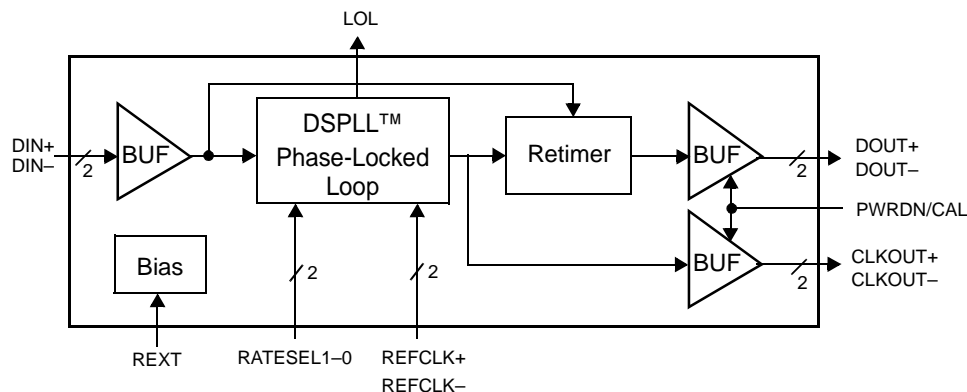


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Detailed Block Diagram

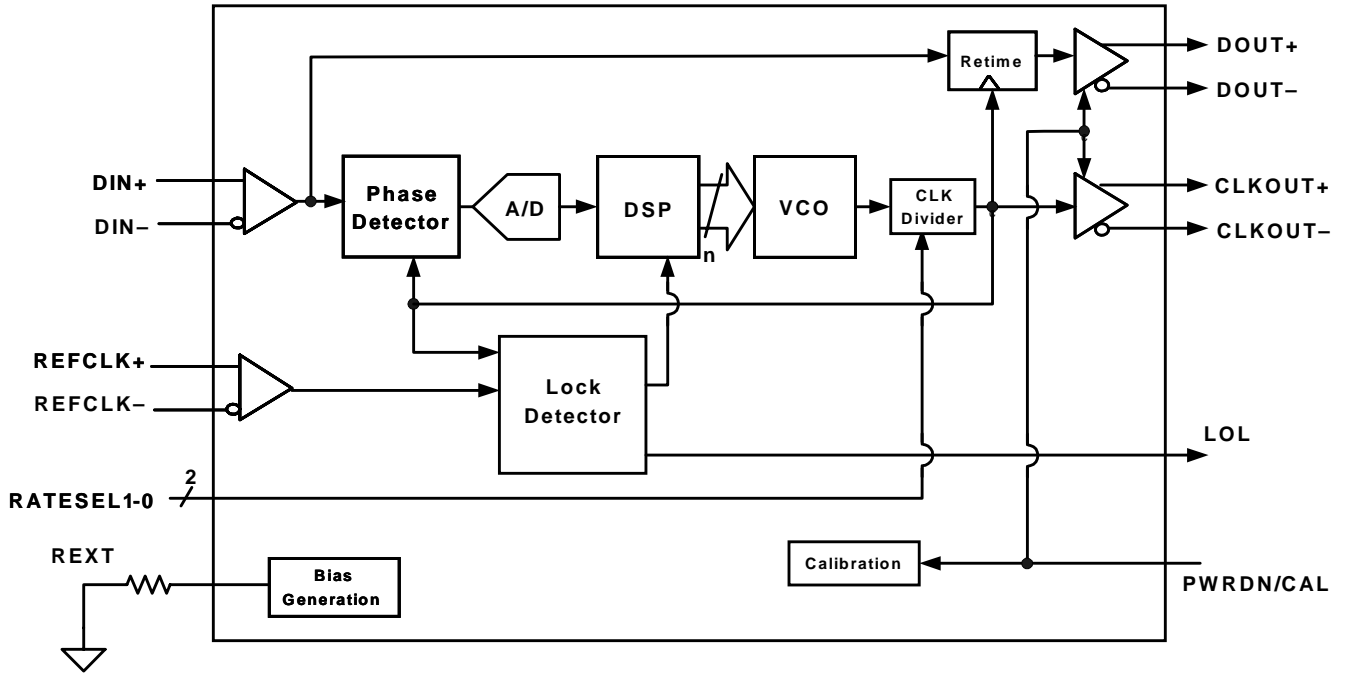


Figure 1. Detailed Block Diagram

Electrical Specifications

Table 1. Recommended Operating Conditions

| Parameter | Symbol | Test Condition | Min ¹ | Typ | Max ¹ | Unit |
|------------------------------------|----------|----------------|------------------|-----|------------------|------|
| Ambient Temperature | T_A | | -40 | 25 | 85 | °C |
| Si5020 Supply Voltage ² | V_{DD} | | 2.375 | 2.5 | 2.625 | V |

Notes:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25°C unless otherwise stated.
2. The Si5020 specifications are guaranteed when using the recommended application circuit (including component tolerance) of Figure 5 on page 9.

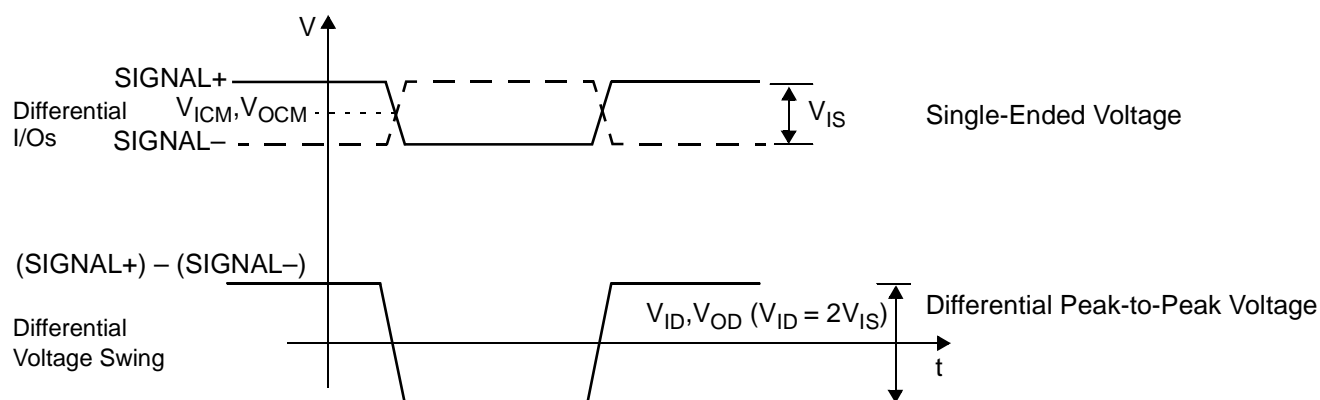


Figure 2. Differential Voltage Measurement (DIN, REFCLK, DOUT, CLKOUT)

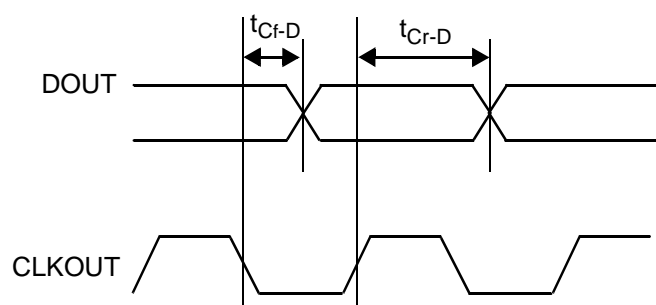


Figure 3. Clock to Data Timing

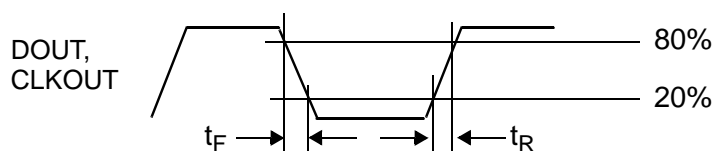


Figure 4. DOUT and CLKOUT Rise/Fall Times

Table 2. DC Characteristics

($V_{DD} = 2.5\text{ V} \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-------------|-----------------------------------|-----|--------------------------|--------------------------|---------------|
| Supply Current OC-48 and FEC (2.7 GHz) GigE OC-12 OC-3 | I_{DD} | | — | 108 113 117 124 | 118 123 127 134 | mA |
| Power Dissipation OC-48 and FEC (2.7 GHz) GigE OC-12 OC-3 | P_D | | — | 270 283 293 310 | 310 323 333 352 | mW |
| Common Mode Input Voltage (DIN, REFCLK) | V_{ICM} | varies with V_{DD} | — | $.80 \cdot V_{DD}$ | — | V |
| Single Ended Input Voltage (DIN, REFCLK) | V_{IS} | See Figure 2 | 100 | — | 750 | mV |
| Differential Input Voltage Swing (DIN, REFCLK) | V_{ID} | See Figure 2 | 200 | — | 1500 | mV (pk-pk) |
| Input Impedance (DIN, REFCLK) | R_{IN} | Line-to-Line | 84 | 100 | 116 | Ω |
| Differential Output Voltage Swing (DOUT) | V_{OD} | 100 Ω Load Line-to-Line | TBD | 940 | TBD | mV (pk-pk) |
| Differential Output Voltage Swing (CLKOUT) | V_{OD} | 100 Ω Load Line-to-Line | TBD | 900 | TBD | mV (pk-pk) |
| Output Common Mode Voltage (DOUT,CLKOUT) | V_{OCM} | 100 Ω Load Line-to-Line | — | $V_{DD} - 0.20$ | — | V |
| Output Impedance (DOUT,CLKOUT) | R_{OUT} | Single-ended | 84 | 100 | 116 | Ω |
| Output Short to GND (DOUT,CLKOUT) | $I_{SC(-)}$ | | — | 25 | TBD | mA |
| Output Short to V_{DD} (DOUT,CLKOUT) | $I_{SC(+)}$ | | TBD | -15 | — | mA |
| Input Voltage Low (LVTTL Inputs) | V_{IL} | | — | — | .8 | V |
| Input Voltage High (LVTTL Inputs) | V_{IH} | | 2.0 | — | — | V |
| Input Low Current (LVTTL Inputs) | I_{IL} | | — | — | 10 | μA |
| Input High Current (LVTTL Inputs) | I_{IH} | | — | — | 10 | μA |
| Output Voltage Low (LVTTL Outputs) | V_{OL} | $I_O = 2\text{ mA}$ | — | — | 0.4 | V |
| Output Voltage High (LVTTL Outputs) | V_{OH} | $I_O = 2\text{ mA}$ | 2.0 | — | — | V |
| Input Impedance (LVTTL Inputs) | R_{IN} | | 10 | — | — | k Ω |
| PWRDN/CAL Leakage Current | I_{PWRDN} | $V_{PWRDN} \geq 0.8\text{ V}$ | TBD | 25 | TBD | μA |

Table 3. AC Characteristics (Clock & Data) $(V_A = 2.5 \text{ V} \pm 5\%, T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-------------------|-------------------|---------------------------------|----------------------------------|---------------------------------|------|
| Output Clock Rate | f_{CLK} | | .15 | — | 2.7 | GHz |
| Output Rise Time | t_R | Figure 4 | — | 100 | TBD | ps |
| Output Fall Time | t_F | Figure 4 | — | 100 | TBD | ps |
| Clock to Data Delay FEC (2.7 GHz) OC-48 GigE OC-12 OC-3 | $t_{\text{Cr-D}}$ | Figure 3 | TBD TBD TBD TBD TBD | 250 255 500 890 4100 | TBD TBD TBD TBD TBD | ps |
| Clock to Data Delay FEC (2.7 GHz) OC-48 | $t_{\text{Cf-D}}$ | Figure 3 | TBD TBD | 51 50 | TBD TBD | ps |
| Input Return Loss | | 100 kHz – 2.5 GHz | 18.7 | — | — | dB |
| | | 2.5 GHz – 4.0 GHz | TBD | — | — | dB |



Table 4. AC Characteristics (PLL Characteristics)

(V_A 2.5 V \pm 5%, T_A = -40°C to 85°C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------|---------------------------------|-------|------|--------|---------------|
| Jitter Tolerance (OC-48)* | $J_{TOL(P-P)}$ | f = 600 Hz | 40 | TBD | — | UIp-p |
| | | f = 6000 Hz | 4 | TBD | — | UIp-p |
| | | f = 100 kHz | 4 | TBD | — | UIp-p |
| | | f = 1 MHz | 0.4 | TBD | — | UIp-p |
| Jitter Tolerance (OC-12 Mode)* | $J_{TOL(P-P)}$ | f = 30 Hz | 40 | TBD | — | UIp-p |
| | | f = 300 Hz | 4 | TBD | — | UIp-p |
| | | f = 25 kHz | 4 | TBD | — | UIp-p |
| | | f = 250 kHz | 0.4 | TBD | — | UIp-p |
| Jitter Tolerance (OC-3 Mode)* | $J_{TOL(P-P)}$ | f = 30 Hz | 60 | TBD | — | UIp-p |
| | | f = 300 Hz | 6 | TBD | — | UIp-p |
| | | f = 6.5 kHz | 6 | TBD | — | UIp-p |
| | | f = 65 kHz | 0.6 | TBD | — | UIp-p |
| Jitter Tolerance (Gigabit Ethernet) Receive Data Total Jitter Tolerance | $T_{JT(P-P)}$ | IEEE 802.3z Clause 38.68 | 600 | TBD | — | ps |
| Jitter Tolerance (Gigabit Ethernet) Receive Data Deterministic Jitter Tolerance | $D_{JT(P-P)}$ | IEEE 802.3z Clause 38.69 | 370 | TBD | — | ps |
| RMS Jitter Generation* | $J_{GEN(rms)}$ | with no jitter on serial data | — | 3.0 | 5.0 | mUI |
| Peak-to-Peak Jitter Generation* | $J_{GEN(rms)}$ | with no jitter on serial data | — | 25 | 55 | mUI |
| Jitter Transfer Bandwidth* | J_{BW} | OC-48 Mode | — | — | 2.0 | MHz |
| | | OC-12 Mode | — | — | 500 | kHz |
| | | OC-3 Mode | — | — | 130 | kHz |
| Jitter Transfer Peaking* | J_p | | — | 0.03 | 0.1 | dB |
| Acquisition Time | T_{AQ} | After falling edge of PWRDN/CAL | 1.45 | 1.5 | 1.7 | ms |
| | | From the return of valid data | 40 | 60 | 150 | μs |
| Input Reference Clock Duty Cycle | C_{DUTY} | | 40 | 50 | 60 | % |
| Reference Clock Range | | | 19.44 | — | 168.75 | MHz |
| Input Reference Clock Frequency Tolerance | C_{TOL} | | -100 | — | 100 | ppm |
| Frequency Difference at which Receive PLL goes out of Lock (REFCLK compared to the divided down VCO clock) | LOL | | TBD | 600 | TBD | ppm |
| Frequency Difference at which Receive PLL goes into Lock (REF-CLK compared to the divided down VCO clock) | LOCK | | TBD | 300 | TBD | ppm |

*Note: Bellcore specifications: GR-253-CORE, Issue 2, December 1995. Using PRBS 2²³ – 1 data pattern.

Table 5. Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|-----------|----------------------------|-------------|
| DC Supply Voltage | V_{DD} | -0.5 to 2.8 | V |
| LVTTL Input Voltage | V_{DIG} | -0.3 to 3.6 | V |
| Differential Input Voltages | V_{DIF} | -0.3 to ($V_{DD} + 0.3$) | V |
| Maximum Current any output PIN | | ± 50 | mA |
| Operating Junction Temperature | T_{JCT} | -55 to 150 | $^{\circ}C$ |
| Storage Temperature Range | T_{STG} | -55 to 150 | $^{\circ}C$ |
| Lead Temperature (soldering 10 seconds) | | 300 | $^{\circ}C$ |
| ESD HBM Tolerance (100 pf, 1.5 k Ω) | | 1 | kV |

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Thermal Characteristics

| Parameter | Symbol | Test Condition | Value | Unit |
|--|-------------|----------------|-------|---------------|
| Thermal Resistance Junction to Ambient | Φ_{JA} | Still Air | 38 | $^{\circ}C/W$ |

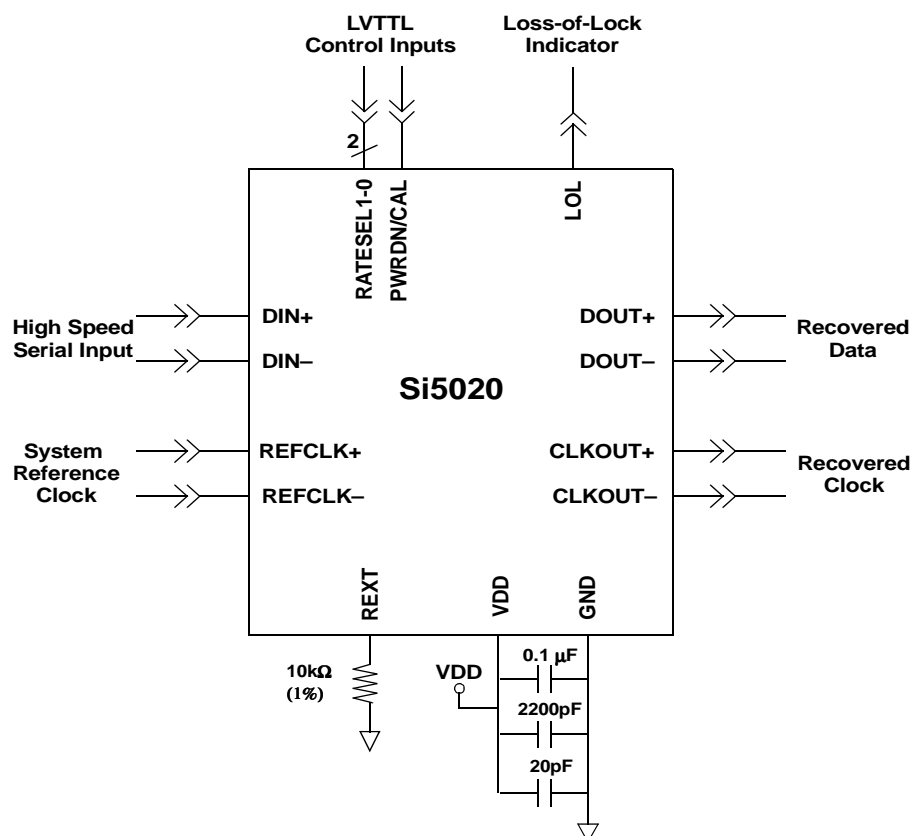


Figure 5. Si5020 Typical Application Circuit

Functional Description

The Si5020 utilizes a phase-locked loop (PLL) to recover a clock synchronous to the input data stream. This clock is used to retime the data, and both the recovered clock and data are output synchronously via current mode logic (CML) drivers. Optimal jitter performance is obtained by using Silicon Laboratories' DSPLL™ technology to eliminate the noise entry points caused by external PLL loop filter components.

DSPLL™

The phase-locked loop structure (shown in Figure 1 on page 4) utilizes Silicon Laboratories' DSPLL™ technology to eliminate the need for external loop filter components found in traditional PLL implementations. This is achieved by using a digital signal processing (DSP) algorithm to replace the loop filter commonly found in analog PLL designs. This algorithm processes the phase detector error term and generates a digital control value to adjust the frequency of the voltage controlled oscillator (VCO). Because external loop filter components are not required, sensitive noise entry points are eliminated thus making the DSPLL less susceptible to board-level noise sources that make SONET/SDH jitter compliance difficult to attain.

PLL Self-Calibration

The Si5020 achieves optimal jitter performance by using self-calibration circuitry to set the loop gain parameters within the DSPLL. For the self-calibration circuitry to operate correctly, the power supply voltage must exceed 2.25 V when calibration occurs. For best performance, the user should force a self-calibration once the supply has stabilized on power-up.

A self-calibration can be initiated by forcing a high-to-low transition on the power-down control input, PWRDN/CAL, while a valid reference clock is supplied to the REFCLK input. The PWRDN/CAL input should be held high at least 1 μs before transitioning low to guarantee a self-calibration. Several application circuits that could be used to initiate a power-on self-calibration are provided in Silicon Laboratories' "AN42: Controlling the Si5018/20 Self-Calibration."

Multi-Rate Operation

The Si5020 supports clock and data recovery for OC-48 and STM-16 data streams. In addition, the PLL was designed to operate at data rates up to 2.7 Gbps to support OC-48/STM-16 applications that employ forward error correction (FEC).

Multi-rate operation is achieved by configuring the device to divide down the output of the VCO to the desired data rate. The divide factor is configured by the

RATESEL0-1 pins. The RATESEL0-1 configuration and associated data rates are given in Table 7.

Table 7. Multi-Rate Configuration

| RATESEL [0:1] | SONET/SDH | Gigabit Ethernet | OC-48 with 15/14 FEC | CLK Divider |
|---------------|-------------|------------------|----------------------|-------------|
| 00 | 2.488 Gbps | — | 2.67 Gbps | 1 |
| 10 | 1.244 Gbps | 1.25 Gbps | — | 2 |
| 01 | 622.08 Mbps | — | — | 4 |
| 11 | 155.52 Mbps | — | — | 16 |

Reference Clock Detect

The Si5020 uses the reference clock to center the VCO output frequency so that clock and data can be recovered from the input data stream. The device will self configure for operation with one of three reference clock frequencies. This eliminates the need to externally configure the device to operate with a particular reference clock.

The reference clock centers the VCO for a nominal output of between 2.5 GHz and 2.7 GHz. The VCO frequency is centered at 16, 32, or 128 times the reference clock frequency. Detection circuitry continuously monitors the reference clock input to determine whether the device should be configured for a reference clock that is 1/16, 1/32, or 1/128 the nominal VCO output. Approximate reference clock frequencies for some target applications are given in Table 8.

Table 8. Typical REFCLK Frequencies

| SONET/SDH | Gigabit Ethernet | SONET/SDH with 15/14 FEC | Ratio of VCO to REFCLK |
|------------|------------------|--------------------------|------------------------|
| 19.44 MHz | 19.53 MHz | 20.83 MHz | 128 |
| 77.76 MHz | 78.125 MHz | 83.31 MHz | 32 |
| 155.52 MHz | 156.25 MHz | 166.63 MHz | 16 |

Forward Error Correction (FEC)

The Si5020 supports FEC in SONET OC-48 (SDH STM-16) applications for data rates up to 2.7 Gbps. In FEC applications, the appropriate reference clock frequency is determined by dividing the input data rate by 16, 32, or 128. For example, if an FEC code is used that produces a 2.70 Gbps data rate, the required reference clock would be 168.75 MHz, 84.375 MHz, or 21.09 MHz.

Lock Detect

The Si5020 provides lock-detect circuitry that indicates whether the PLL has achieved frequency lock with the incoming data. The circuit compares the frequency of a divided down version of the recovered clock with the frequency of the supplied reference clock (REFCLK). If the recovered clock frequency deviates from that of the reference clock by the amount specified in Table 4 on page 8, the PLL is declared out of lock, and the loss-of-lock (LOL) pin is asserted "high." In this state, the DSPLL will periodically try to reacquire lock with the incoming data stream. During reacquisition, the recovered clock, CLKOUT, will drift over a ± 600 ppm range relative to the supplied reference clock. The LOL output will remain asserted until the recovered clock frequency is within the REFCLK frequency by the amount specified in Table 4.

Note: LOL is not asserted during PWRDN/CAL.

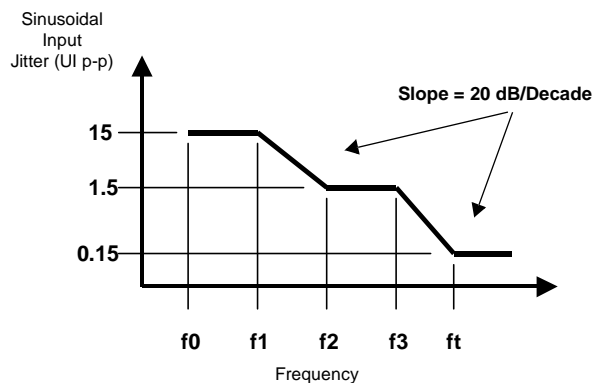
PLL Performance

The PLL implementation used in the Si5020 is fully compliant with the jitter specifications proposed for SONET/SDH equipment by Bellcore GR-253-CORE, Issue 2, December 1995 and ITU-T G.958.

Jitter Tolerance

The Si5020's tolerance to input jitter exceeds that of the Bellcore/ITU mask shown in Figure 6. This mask defines the level of peak-to-peak sinusoid jitter that must be tolerated when applied to the differential data input of the device.

Note: There are no entries in the mask table for the data rate corresponding to OC-24 as that rate is not specified by either GR-253 or G.958.



| SONET Data Rate | F0 (Hz) | F1 (Hz) | F2 (Hz) | F3 (kHz) | Ft (kHz) |
|-----------------|---------|---------|---------|----------|----------|
| OC-48 | 10 | 600 | 6000 | 100 | 1000 |
| OC-12 | 10 | 30 | 300 | 25 | 250 |
| OC-3 | 10 | 30 | 300 | 6.5 | 65 |

Figure 6. Jitter Tolerance Specification

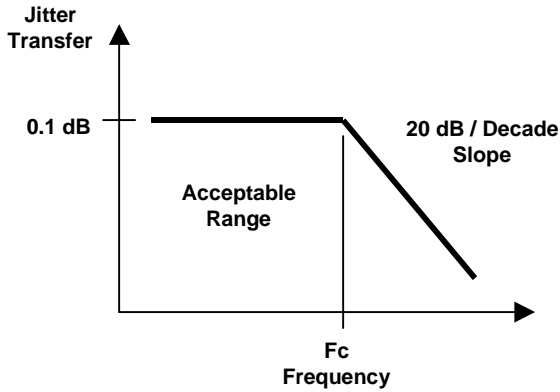
Jitter Transfer

The Si5020 is fully compliant with the relevant Bellcore/ITU specifications related to SONET/SDH jitter transfer. Jitter transfer is defined as the ratio of output signal jitter to input signal jitter as a function of jitter frequency (see Figure 7). These measurements are made with an input test signal that is degraded with sinusoidal jitter whose magnitude is defined by the mask in Figure 6.

Jitter Generation

The Si5020 exceeds all relevant specifications for jitter generation proposed for SONET/SDH equipment. The jitter generation specification defines the amount of jitter that may be present on the recovered clock and data outputs when a jitter free input signal is provided. The Si5020 typically generates less than 3.0 mUI rms of jitter when presented with jitter-free input data.





| SONET Data Rate | Fc (kHz) |
|-----------------|----------|
| OC-48 | 2000 |
| OC-12 | 500 |
| OC-3 | 130 |

Figure 7. Jitter Transfer Specification

Power Down

The Si5020 provides a power down pin, PWRDN/CAL, that disables the output drivers (DOUT, CLKOUT). When the PWRDN/CAL pin is driven “high”, the positive and negative terminals of CLKOUT and DOUT are each tied to VDD through 100 Ω on-chip resistors. This feature is useful in reducing power consumption in applications that employ redundant serial channels.

When PWRDN/CAL is released (set to “low”) the digital logic resets to a known initial condition, recalibrates the DSPLL, and will begin to lock to the data stream.

Device Grounding

The Si5020 uses the GND pad on the bottom of the 20-pin micro leaded package (MLP) for device ground. This pad should be connected directly to the analog supply ground. See Figures 10 and 11 for the ground (GND) pad location.

Bias Generation Circuitry

The Si5020 makes use of an external resistor to set internal bias currents. The external resistor allows precise generation of bias currents which significantly reduces power consumption versus traditional implementations that use an internal resistor. The bias generation circuitry requires a 10 kΩ (1%) resistor connected between REXT and GND.

Differential Input Circuitry

The Si5020 provides differential inputs for both the high speed data (DIN) and the reference clock (REFCLK) inputs. An example termination for these inputs is shown in Figure 8. In applications where direct DC coupling is possible, the 0.1 μF capacitors may be omitted. The DIN and REFCLK input amplifiers require an input signal with a minimum differential peak-to-peak voltage listed in Table 2 on page 6.

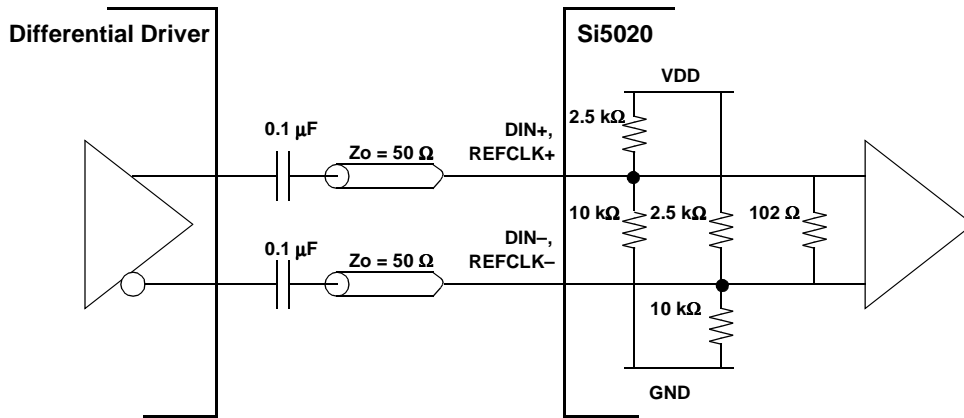


Figure 8. Input Termination for DIN and REFCLK (AC Coupled)

Differential Output Circuitry

The Si5020 utilizes a current mode logic (CML) architecture to output both the recovered clock (CLKOUT) and data (DOUT). An example of output termination with AC coupling is shown in Figure 9. In applications in which direct DC coupling is possible, the $0.1\ \mu\text{F}$ capacitors may be omitted. The differential peak-to-peak voltage swing of the CML architecture is listed in Table 2 on page 6.

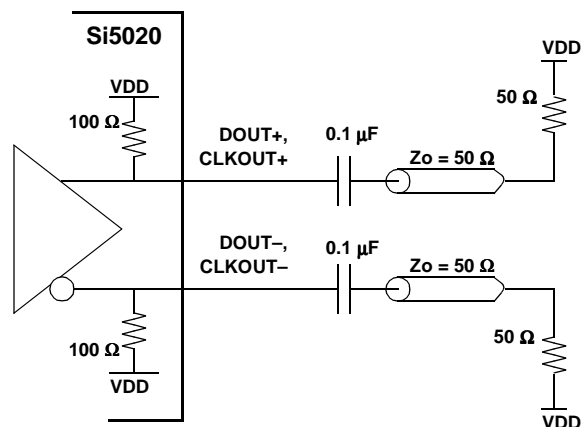
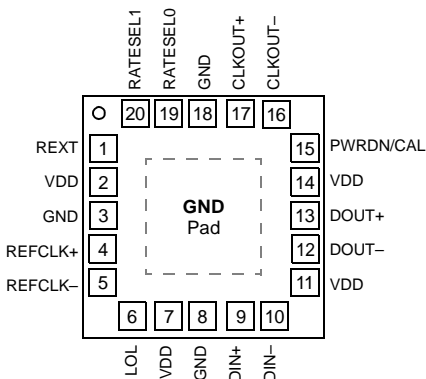


Figure 9. Output Termination for DOUT and CLKOUT (AC Coupled)

Pin Descriptions: Si5020



Top View

Figure 10. Si5020 Pin Configuration

Table 9. Si5020 Pin Descriptions

| Pin # | Pin Name | I/O | Signal Level | Description |
|--------|---------------------|-----|--------------|---|
| 1 | REXT | | | External Bias Resistor. This resistor is used by onboard circuitry to establish bias currents within the device. This pin must be connected to GND through a 10 kΩ (1%) resistor. |
| 4, 5 | REFCLK+, REFCLK- | I | See Table 2 | Differential Reference Clock. The reference clock sets the initial operating frequency used by the onboard PLL for clock and data recovery. Additionally, the reference clock is used to derive the clock output when no data is present. |
| 6 | LOL | O | LVTTL | Loss of Lock. This output is driven high when the recovered clock frequency deviates from the reference clock by the amount specified in Table 4 on page 8. |
| 9, 10 | DIN+, DIN- | I | See Table 2 | Differential Data Input. Clock and data are recovered from the differential signal present on these pins. |
| 12, 13 | DOUT-, DOUT+ | O | CML | Differential Data Output. The data output signal is a retimed version of the data recovered from the signal present on DIN. It is phase aligned with CLKOUT and is updated on the rising edge of CLKOUT. |

Table 9. Si5020 Pin Descriptions (Continued)

| Pin # | Pin Name | I/O | Signal Level | Description |
|--------------------------|-----------------------|-----|--------------|--|
| 15 | PWRDN/CAL | I | LVTTTL | <p>Power Down. To shut down the high-speed outputs and reduce power consumption, hold this pin high. For normal operation, hold this pin low.</p> <p>Calibration. To initiate an internal self-calibration, force a high-to-low transition on this pin. (See "PLL Self-Calibration," on page 10.)</p> <p>Note: This input has a weak internal pulldown.</p> |
| 16, 17 | CLKOUT–, CLKOUT+ | O | CML | <p>Differential Clock Output. The output clock is recovered from the data signal present on DIN. In the absence of data, the output clock is derived from REFCLK.</p> |
| 19, 20 | RATESEL1, RATESEL0 | I | LVTTTL | <p>Data Rate Select. These pins configure the onboard PLL for clock and data recovery at one of four user selectable data rates. See Table 7 for configuration settings.</p> <p>Note: These inputs have weak internal pulldowns.</p> |
| 2, 7, 11, 14 | VDD | | 2.5 V | <p>Supply Voltage. Nominally 2.5 V.</p> |
| 3, 8, 18, and GND Pad | GND | | GND | <p>Supply Ground. Nominally 0.0 V. The GND pad found on the bottom of the 20-pin micro leaded package (see Figure 11) must be connected directly to supply ground.</p> |



Ordering Guide

Table 10. Ordering Guide

| Part Number | Package | Temperature |
|--------------------|----------------|--------------------|
| Si5020-BM | 20-pin MLP | -40°C to 85°C |

Package Outline

Figure 11 illustrates the package details for the Si5020. Table 11 lists the values for the dimensions shown in the illustration.

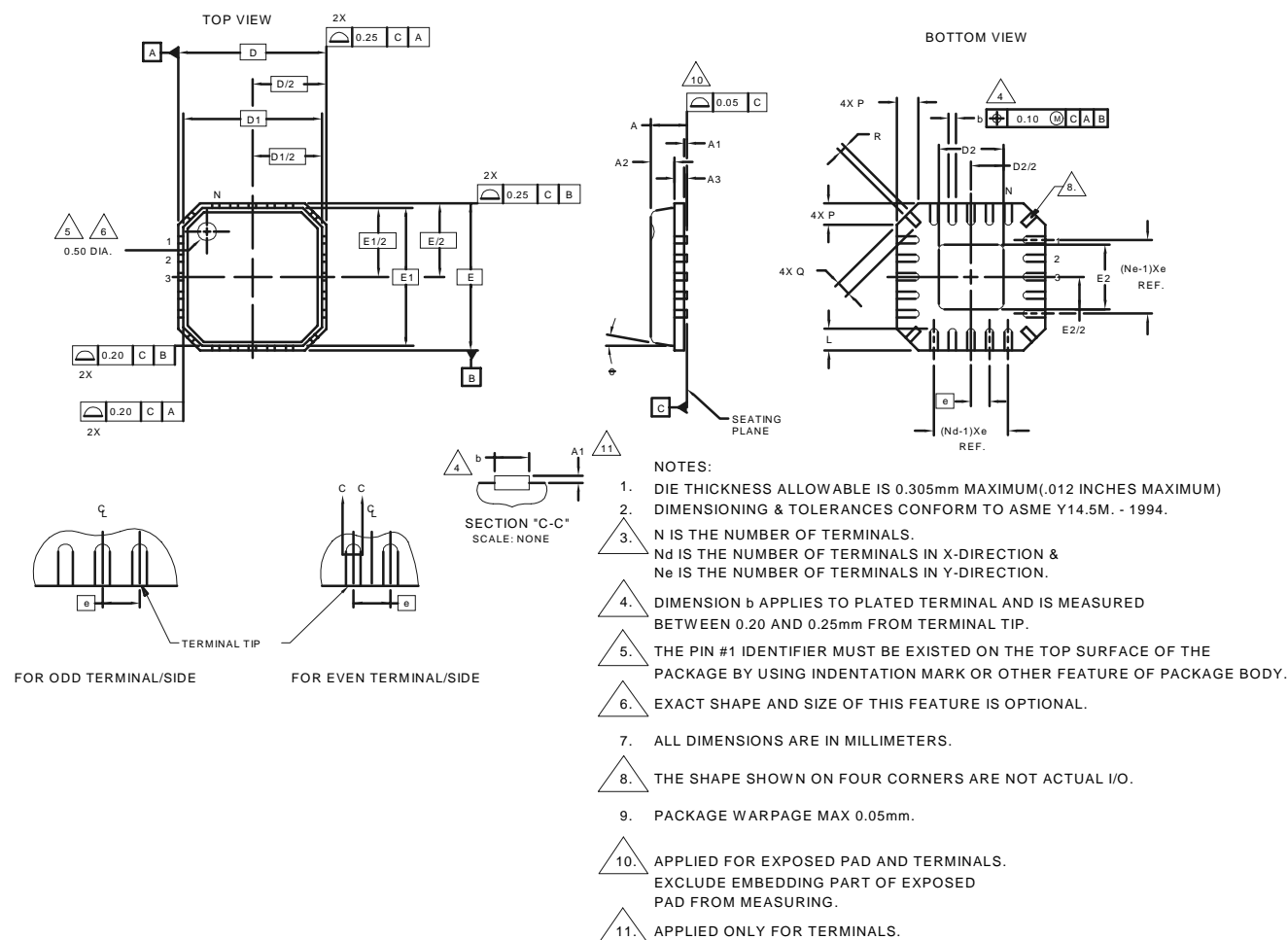


Figure 11. 20-pin Micro Leaded Package (MLP)

Table 11. Package Diagram Dimensions

| Symbol | Millimeters | | |
|--------|-------------|------|------|
| | Min | Nom | Max |
| A | — | 0.85 | 1.00 |
| A1 | 0.00 | 0.01 | 0.05 |
| A2 | — | 0.65 | 0.80 |
| A3 | 0.20 REF | | |
| b | 0.23 | 0.28 | 0.35 |
| D | 4.00 BSC | | |
| D1 | 3.75 BSC | | |
| D2 | 1.95 | 2.10 | 2.25 |
| e | 0.50 BSC | | |
| E | 4.00 BSC | | |

| Symbol | Millimeters | | |
|----------|-------------|------|------|
| | Min | Nom | Max |
| E1 | 3.75 BSC | | |
| E2 | 1.95 | 2.10 | 2.25 |
| N | 20 | | |
| Nd | 5 | | |
| Ne | 5 | | |
| L | 0.50 | 0.60 | 0.75 |
| P | 0.24 | 0.42 | 0.60 |
| Q | 0.30 | 0.40 | 0.65 |
| R | 0.13 | 0.17 | 0.23 |
| θ | — | — | 12° |

Contact Information

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