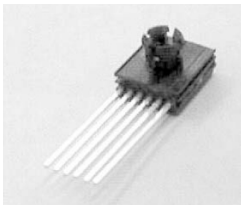
SPF BFT 003 03

Optical Bidirectional Transceiver for byteflight

Data Sheet



Short description of complete functional unit

The device consists of a LED mounted on a large area photodiode for bidirectional optical transmission in half duplex mode. LED and photodiode are driven by the multifunction IC E100.34C2 from ELMOS.

The transmitting and receiving functional units with ELMOS-IC E100.34C2 may be split into the following blocks:

Features

- Optical transmitter and receiver for maximum datarate 10 Mbaud (half duplex burst mode)
- Transmitter: LED with 650 nm for working in low attenuation range of PMMA fiber
- Receiver: Photodiode with preamp, digitizer with DC elimination circuit (tracked decision threshold), Sleep - and Wake-up-Function, output stage (electrical output driver)
- Built in transmitter and receiver gate for half duplex mode (mutual blocking of transmitter and receiver)
- Operation at 5V or 8V-11V power supply voltage
- Built in pulse width detection for indicating Sync, Alarm and continuous light on (integrated time basis to differentiate and evaluate Sync, Alarm and Continuous Light conditions Alarm output)
- Diagnose function for photocurrent
- Mechanical assembly: 6 Pin CAI package for easy coupling of POF (plastic optical fiber) with insert

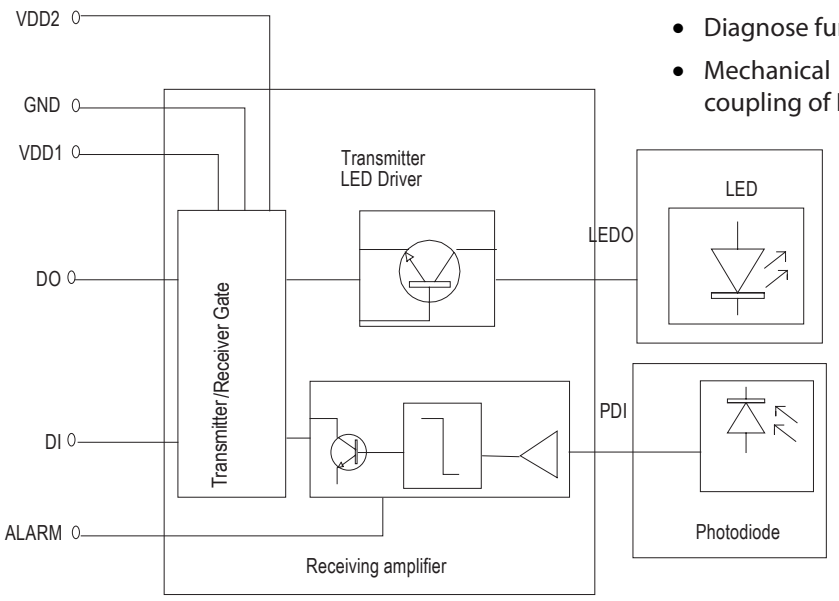


Figure 1. Basic functional units of SPF BFT3 03

Safety Hints

Applications of new chip technologies lead to increasing optical efficiency and growing and higher levels of optical performance. We therefore recommend that the current versions of the IEC 60825-1 and EN 60825-1 standards are taken into account right from the outset, i.e. at the equipment development stage, and that suitable protection facilities are provided.

Basic Specification

Absolute maximum ratings

Parameter	Symbol	min	max	Unit
Storage Temperature Range	T_{STG}	- 40	100	°C
Operating Temperature Range	T_A	- 40	85	°C
Soldering Temperature (≤ 10 seconds more than 4,5 mm apart from package; details see app. note)	T_S		235	°C
Maximum optical input power onto receiver	$P_{optmaxRec}$	-	5	mW

Parameter	Symbol	min	max	Unit
Voltages against GND:				
Supply Voltage	V_{DD1}	- 0,3	16	V
Signal Input DI	V_{inm}	- 0,3	6	V
Signal Output DO	V_{outm}	- 0,3	6	V
Output ALARM	V_{outm}	- 0,3	16	V
Output DO shortening time [1]	t_{sDO}	-	1	s
Current into Alarm-pin (active Alarm state)	I_{Alarm}	-	10	mA

Notes:
1. The electrical output DO may be shortened for a short period of time tsDO. During this time the voltage at DO has to be within 0V <= VDO <= 5V

Operating Conditions

All the data in this specification refer to the following operating conditions unless otherwise stated.

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{DD1}	4,75	5	5,5	V
Supply Voltage, optional	V_{DD1}	7,8	9	11,3	V
Datarate	DBR			10	Mbit/s
Duration of one bit	t_{bit}		100		ns
Duration of sync pulse	t_{sync}	2,9	3	3,1	µs
Duration of Alarm pulse	t_{alarm}	1,9	2	2,1	µs
Bright phase Wake-up Impulse	t_{plwu}	6	6,4	6,8	µs
Dark phase Wake-up Impulse	t_{pdwu}	6	6,4	6,8	µs

Caution: Usage of the device out of the maximum ranges given in this chapter may damage the transceiver!

Interface Description

Pinning

Pin	Pin-Name	Description
1	DI	Signal Input/Data In
2	ALARM	Alarm out (open drain)
3	VDD1	positive power supply
4	VDD2	internally regulated power supply
5	GND	Ground
6	DO	Signal Output/Data out (push-pull)

Optical Signals

Name	Description	Light on	Light off
LED0	optical Signal, emitted of Transceiver	1	0
PDI (=LEDI)	optical Signal, received of Transceiver	1	0

Note:
Transmitter and Receiver invert the signals, which means that
- in standard transmitting mode: low level (0V) at DI causes the illumination of the LED (LEDO „1" = light on) and vice versa,
- in standard receiving mode: no light onto the Photodiode (PDI „0" = light off) causes output of 5V at DO and vice versa.

Detailed Specification

Optical Function Transmitter

Electrical and Optical Characteristics of LED and Driver:

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Data Rate			[2]		10	Mbit/s
Optical Output Power (peak)	1mm Standard PMMA fiber 30cm optimum coupling, 0h, T_A=25°C	P_{opt25}	274(-5,6)	450(-3,5)	740(-1,3)	µW(dBm)
Optical Output Power (peak)	1mm Standard PMMA fiber 30cm optimum coupling, 0h, -40°C....+85°C	$P_{opt\text{-}40°\text{-}+85°}$	166(-7,8)		1000(0)	µW(dBm)
Optical Output Power (peak)	1mm Standard PMMA fiber 30cm optimum coupling, over lifetime, -40°C.....+85°C	$P_{opt\text{-}40°\text{-}+85°/life}$	132(-8,8)		1250(+1,0)	µW(dBm)
Optical Rise Time, Optical Fall Time	10% to 90%	t_r, t_f			35	ns
Pulse Width Distortion, Optical Signal		$P_{WDTrans}$	-5		+5	ns
Peak emission wavelength	+25°C	λ_{Peak}	640	650	660	nm
Peak emission wavelength	-40°C.....+85°C	λ_{Peak}	630	650	670	nm

Notes:
2. Limitation due to electrical power dissipation: Duty cycle for > 1s: 10 %, Duty cycle for < 1 s: 50 %

General remark: Not all mentioned parameters are subject to production test !

Optical Function Receiver

Electrical and optical characteristics of receiving photodiode with amplifier in high speed data receiving (active) mode:

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Data Rate					10	Mbit/s
Pulse Width Distortion [3]		PWD_{Rec}	- 25		+ 25	ns
Pulse Width Start pulse	Pmin	PW_{Start}	500	600	660	ns
Maximum receiveable power	Signal at DO according PWD_{Rec}	P_{max} [4]	800(-1,0)			µW(dBm)
Minimum receiveable power	Signal at DO according PWD_{Rec}	P_{min} [4]			20(-17)	µW(dBm)
Recovery time after last transmitted bit		t_{rec}			1,1	µs

Notes:

3. The Pulse Width Distortion is tested with a worst case pattern at a certain single high pulse P1 of the standard pattern some bits after starting the burst.
4. All Optical Power Data are peak values.

Static Characteristics

Parameter	Condition	Symbol	min	typ	max	Unit
Peak Supply Current in active mode [2]	LED on	I_{dda}			50	mA
Supply current in active mode	LED off	I_{dda}			10	mA
Supply current in stand-by mode	10ms after $t_{sleepmax}$	I_{Stby}		30	45	µA
Low Level Input Voltage DI		V_{IL}	0		0,8	V
High Level Input Voltage DI		V_{ICH}	2		6	V
Low Level Output Voltage DO	I = 1mA	V_{OLD}	0		0,4	V
High Level Output Voltage DO	I = -1mA	V_{OHD}	3,7		5	V
Low Level Output Voltage ALARM	I = 5mA	V_{OLA}	0		0,4	V
Input Capacitance at DI		C_{DI}			5	pF
Optical Power Threshold for photo current diagnosis [5]		P_{DIAG}	-	12(-19,2)	20(-17)	µW(dBm)
Internally regulated voltage	V_{dd1} = 8V - 11V	V_{DD2}	4,7		5,3	V
Leackage current at DO	V_{dd1} = 0V;VDO = 5V; +85°C	I_{LDO}	-3		+3	µA

Notes:

2. Limitation due to electrical power dissipation: Duty cycle for > 1s: 10 %, Duty cycle for < 1 s: 50 %
5. Measured only at +85°C

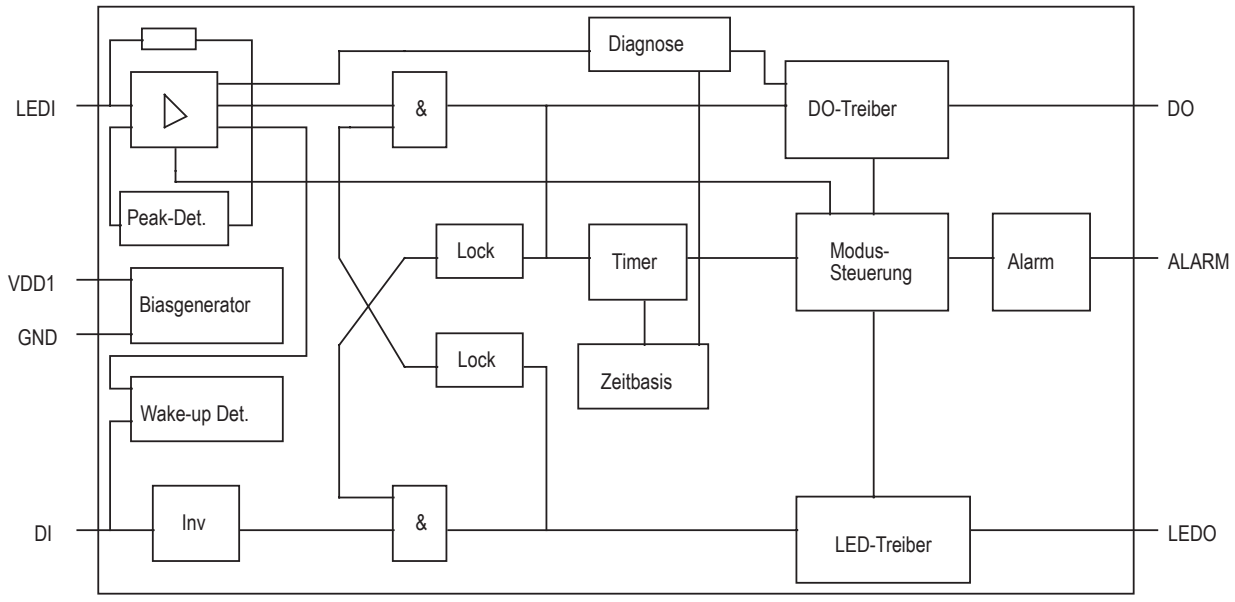
Dynamic Characteristics

Parameter	Condition	Symbol	min	typ	max	Unit
Signal delay (LEDI -> DO)		t_{del-Rx}			230	ns
Signal delay (DI - > LEDO)		t_{del-Tx}			230	ns
Rise and fall time on DO	CL= 30pF	t_r, t_f		30		ns
Wake-up time [6]		t_{wu}			10	ms
Sleep-in time [7]		t_{sl}	10		20	ms
Continuous light on time [8]		t_{cl}	10	11,4	15	µs
Locking time with el. signal [9]		t_{locke}	700		1100	ns
Locking time with opt. signal [10]		t_{locko}	300		700	ns
Duration of diagnosis impulse		t_{pdi}	80	100	120	ns
Pause before diagnosis impulse		t_{wdi}	1,17	1,3		µs
Delay diagnosis impulse		t_{ddi}	10		220	ns

Notes:
6. Time between the first optical wake-up pattern and switching into active mode
7. Time between transmitting last bit and switching into sleep mode
8. Duration for detection of continuous light
9. After recognizing High levels on the internal data path at the lock switch input (see block wiring diagram), the other relevant channel is blocked for this period. This time can not be measured at wafer level and therefore also not at the Byteflight module.
10. After recognizing High levels on the internal data path at the lock switch input (see block wiring diagram), the other relevant channel is blocked for this period.

Functional description

Block wiring diagram



Functional description

The IC comprises of the functional groups as shown in the block wiring diagram which are defined in more detail below.

The following applies in standard mode:

Low level to DI means LED driver is active and therefore the LED is emitting light.

If light falls onto the photodiode, the DO driver becomes active and produces low level on DO.

Receiver component

The preamplifier in the receive component forms a current/voltage converter which converts the photocurrent from the receive diode into a voltage. The functional group peak detector ensures a signal-dependent tracking of the reference voltage and compensates destructive offset influences like dark current of the photodiode. In the Sleep mode, the receiver operates at a very low supply current. Signal wake-up sequences are integrated and if the wake-up threshold is exceeded, the active mode is switched on.

The DO output stage is a Push /Pull driver (active L, inactive H). The driver can be blocked by the transmitter component.

Transmitter component

The electrical signal to DI is inverted and sent to the LED Driver via a AND logic gate. The LED driver supplies the transmit diode with a typical current of 30mA (peak). The driver can be blocked by the receiver part.

Locking

To avoid mutual interference during data transfer, transmitter and receiver are mutually locked. During active level at its input, the functional group identified as lock in the block wiring diagram blocks the other channel. The trailing edge is delayed by t_{lock} and then releases the corresponding channel. Switching can be re-triggered. If H levels occur on both channels at the same time, the channel to be blocked is not defined. If continuous light has been detected by the receiver, the locking for the transmitting channel is released to enable transmitting even during continuous light situation.

Alarm

An alarm is detected if a pulse with pulse length t_{alarm} is recognised. The alarm output driver (Open Drain Lowside) is then statically switched on. The driver is switched off as soon as a Sync-Pulse is registered by the receiver, with PON and continuous light and in sleep mode. Alarm detection is only possible if there was a normal sync pulse received before.

Time basis and timer

An internal oscillator establishes the local time basis of the module. In order to achieve the required accuracy, the frequency is individually adjusted on each die. This tuning is made once by the chip manufacturer during the wafer measurement.

The timer unit checks all data pulses for their length and distinguishes between sync-pulses, alarm pulses and continuous light. Sync and alarm pulses must fulfil the time conditions stated under topic Operating Conditions. Continuous light is recognised at a minimum pulse duration of typical 11,4 µs. For evaluation of continuous light on time 114 pulses of the internal oscillator are counted. The time of period of the internal oscillator may be evaluated according to the following formula:

$$T_{osc} = t_{cl} / 114$$

t_{cl} = continuous light on time

pulse type	duration [ns]	max. time of period	min. time of period
alarm	2000	129,03	85,11
min	1900	122,58	80,85
max	2100	135,48	89,36
sync	3000	117,65	86,96
min	2900	113,73	84,06
max	3100	121,57	89,86

Mode control

The mode control checks and evaluates the signals of the timer unit and the power-on signal. The following actions are triggered on dependence of the result of the evaluation:

- Power-On

  When the operating voltage is applied, a PON signal is generated internally. This resets all functional units and normal mode is taken by the IC. The alarm output is inactive.

  A Power-On signal is generated at each raising of VDD2. Moreover, a Power-On signal is created when the power supply goes in the controlled mode up to VDD1 overriding a threshold of 7V. The internal reset signal is created by prolongation of the Power-On signal with 3,4 ms. DO and LEDO are locked during the reset.

- Sync pulse

  In normal mode, the sync pulse simply passes through to the output. If an alarm pulse has previously been identified, the alarm condition is cleared and the alarm output is switched off.

- Alarm pulse

  In normal mode, after an alarm pulse has been identified, the alarm condition is accepted and the alarm output is switched on. If further alarm pulses are identified, the alarm condition is sustained. It is possible to clear the alarm condition by receiving a valid sync pulse or by PON or by reached sleep mode or if continuous light is identified. In the alarm condition, data transfer takes place exactly as in normal mode. After Wake-up or PON the Alarm-Output is activated not before the recognising of the first Sync-Pulse.

- Continuous light

  If continuous light is identified on the bus (light duration > continuous light on time), the electrical output DO is blocked in order to avoid a blockade of the entire bus. An existing alarm condition is cleared. The block for DO is cleared if a valid sync or alarm pulse is identified on the electrical or optical inputs and if there is no continuous light at the receiver any more. Continuous light can only be identified by the optical receiver.

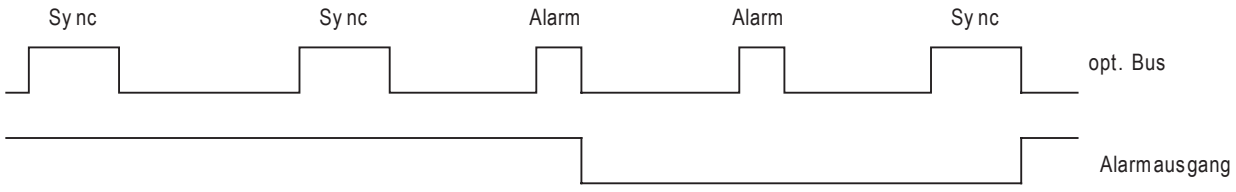
Sleep-Mode and Wake-up

After the time t_{sl}. the IC/circuit changes his internal status to the sleep mode if no light is present and also if continuous light is present. In the sleep mode, only a very slow receiver and the wake-up detector are active, in order to achieve very low power consumption.

The receiving diode integrates signals at the optical input. If the wake-up level is exceeded, the wake-up detector activates the chip. For wake-up via a optical way, continuously alternating dark/bright pulses are necessary for the duration of t_{wu}. The timing of these pulse has to be according the spec under chapter Basic Specification (parameter: bright phase wake-up impulse, dark phase wake-up impulse).

The wake-up signal has the effect of a reset and is also prolonged by 3,4 ms in order to give the analogue components enough time for switching on. This time (3,4 ms) is contained in twu. Immediately after wake up the continuous light recognition is blocked. There have to be at least 8 pulses recognised at the optical input to activate the continuous light recognition again. This is to avoid an incorrect continuous light recognition during the wake-up phase.

An immediate wake-up also occurs when a H/L flank appears at DI. Pulses at DI appear at once at LEDO (only IC internal delay). For the optical path the reset prolongation is valid at wake-up via DI. Due to the transient response of the IC, the first databits, which are transferred after activation, may be incorrect.



Photocurrent indication

The logic of the IC (internal analog diagnosis) is able to recognize photocurrents, which lie below a certain predefined value. This feature accomplishes to issue a early warning if the optical link gets worse.

In case of low photocurrent at first there is no difference to the normal receiving mode. If the module goes in transmitting mode the following warning is given:

1. The transceiver is testing if there was a pause of minimum 13 clockcycles of the internal oscillator (typ. 1,3 µs) the time ahead of the High/Low-transition on DI
2. If this break was recognized and L -level is on DI, than at DO after tddi there is a pulse of minimum 1 clock cycle of the internal oscillator (typ. 100ns). This pulse has to be detected from the connected interface module.

With this feature a low level of photocurrent can always be detected during the start sequence or during the sync pulse if the transceiver is in transmitting mode.

ESD – Protective connection

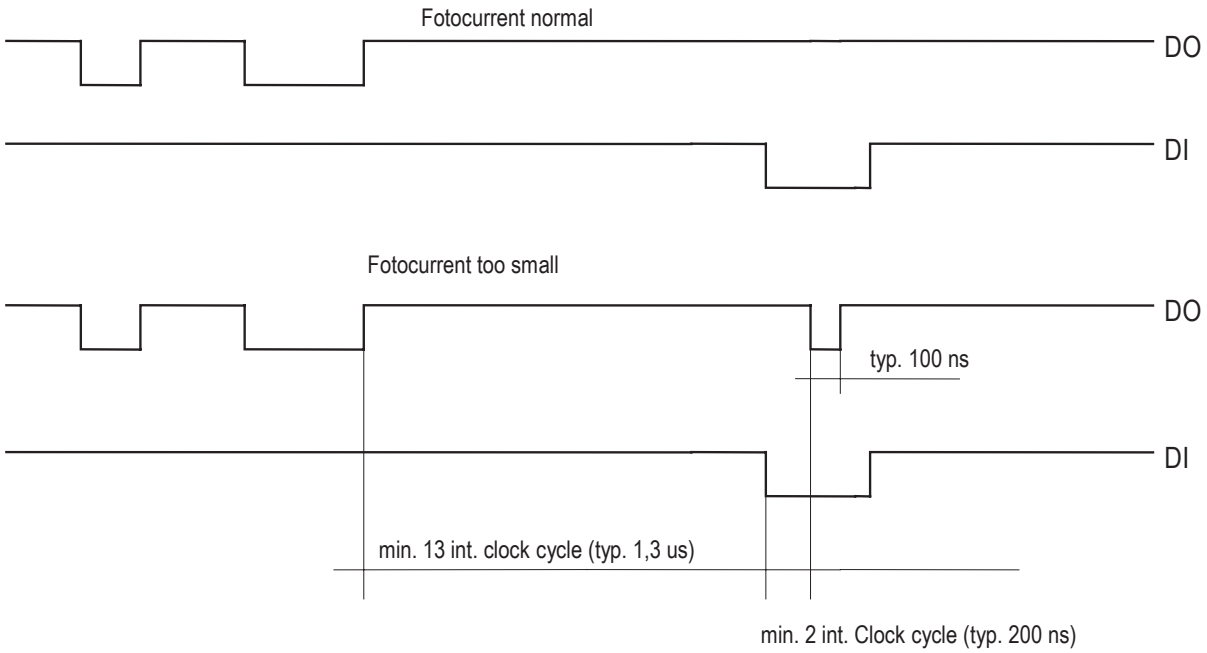
All input and output pins of the IC have protective connections internally.

ESD protective connections are tested in accordance with EOS/ESD-DS5.3 (SDM; Socketed Device Model) under the following conditions:

V_{IN} = 250/500/1000Volt

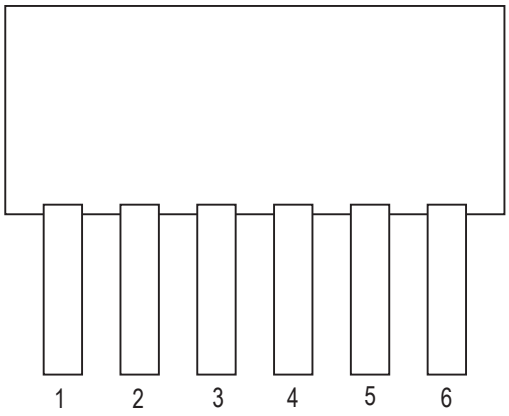
ESD protective connections are tested in accordance with EIA/JESD22-A114 (HBM Human Body Model) under the following conditions:

Vin = 500/1000/1500/2000/2500Volt



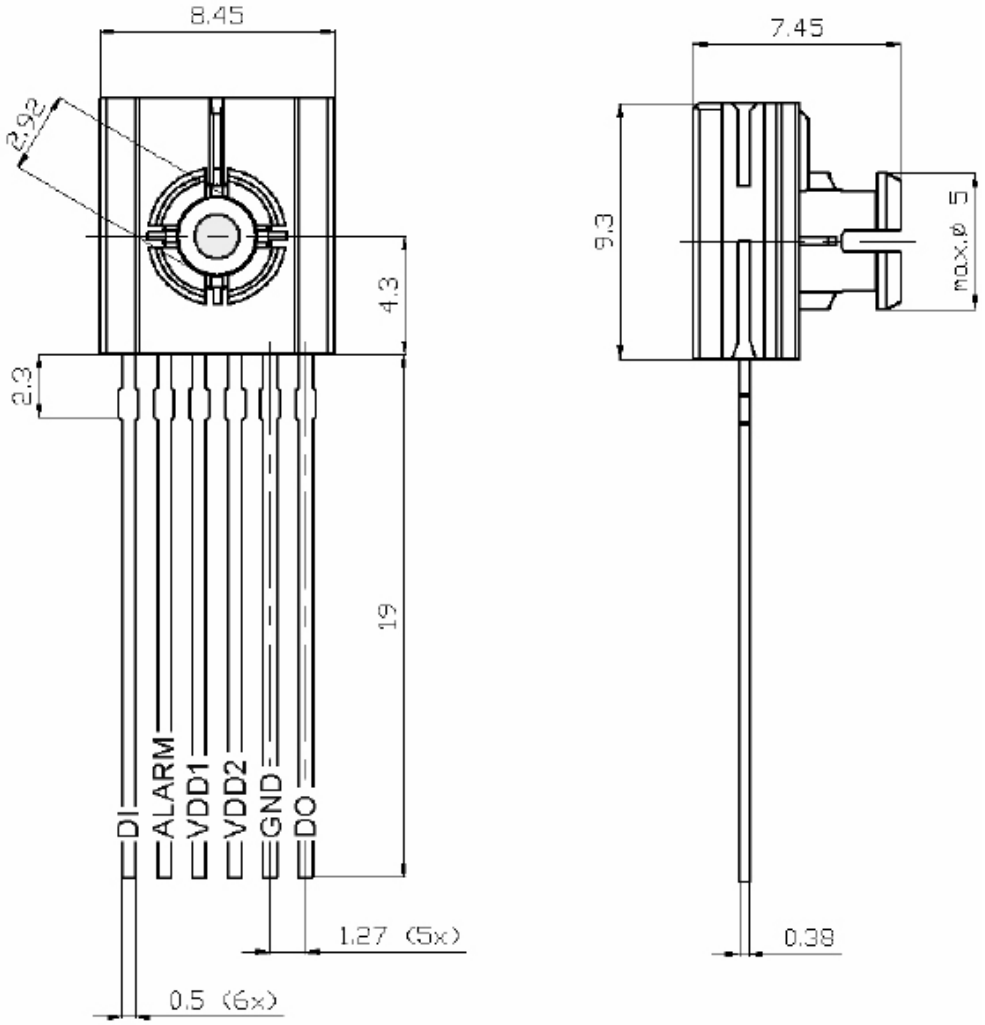
Application Circuitry

Looking to the optical interface the following application circuitry should be used:



Pin	Pin-Name	comment/requirement
1	DI	connection with 470 Kohm to V_{DD2} or 10 KOhm to external 5 V; Note: maximum signal input voltage at DI is 6 V!
2	ALARM	open drain output with minimum 2 KOhm to Vdd=9V or with minimum 1 KOhm to Vdd=5V so that maximum current at Alarm=0V is 5 mA
3	VDD1	power supply (5 V or 9 V), connected with 100 nF...1µF depending on application and 100 µF (ESR @ 120Hz < 18,6 Ohm, ESR @ 10kHz < 9,5 Ohm, over hole temperature range, critical at –40°C) block capacitors to Ground. If several BFT modules are operated in parallel, these values have to be adjusted (usually higher values have to be used) and verified within the application.
4	VDD2	connected with 220 nF....1µF (depending on application) block capacitor to Ground
5	GND	short, direct connection to System Ground
6	DO	Signal Output/Data out (push-pull)

Mechanical Design SPF BFT 003 03: CAI package (cavity as interface)



For further details refer to separate drawings.

Disclaimer

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