iC-MB4
BiSS INTERFACE MASTER

preliminary

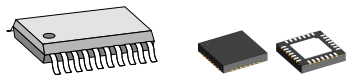
FEATURES

- Bidirectional *BiSS* communication with up to 8 slaves
- Supports SSI protocol for unidirectional data transmission
- Synchronous sensor data acquisition with cyclic transfer at data rates of up to 10 Mbit/s
- Configurable interface with TTL, CMOS, RS422 or LVDS
- Slave register operations during cyclic data transfers
- Automatic compensation of line delays and conversion times
- Data lengths of up to 64 bit for sensor data, configurable for each slave
- Data verification by CRC polynomials of up to 16 bits per slave
- Separate memory banks enable free controller access during *BiSS* sensor data transfers
- 64 bytes memory for bidirectional slave register communication
- Parallel interface with 8 bit data/address bus services Intel and Motorola devices with combined data and address bus
- Serial controller communication by SPI™-compatible mode
- Single 3 V to 5 V supply, industrial temperature range

APPLICATIONS

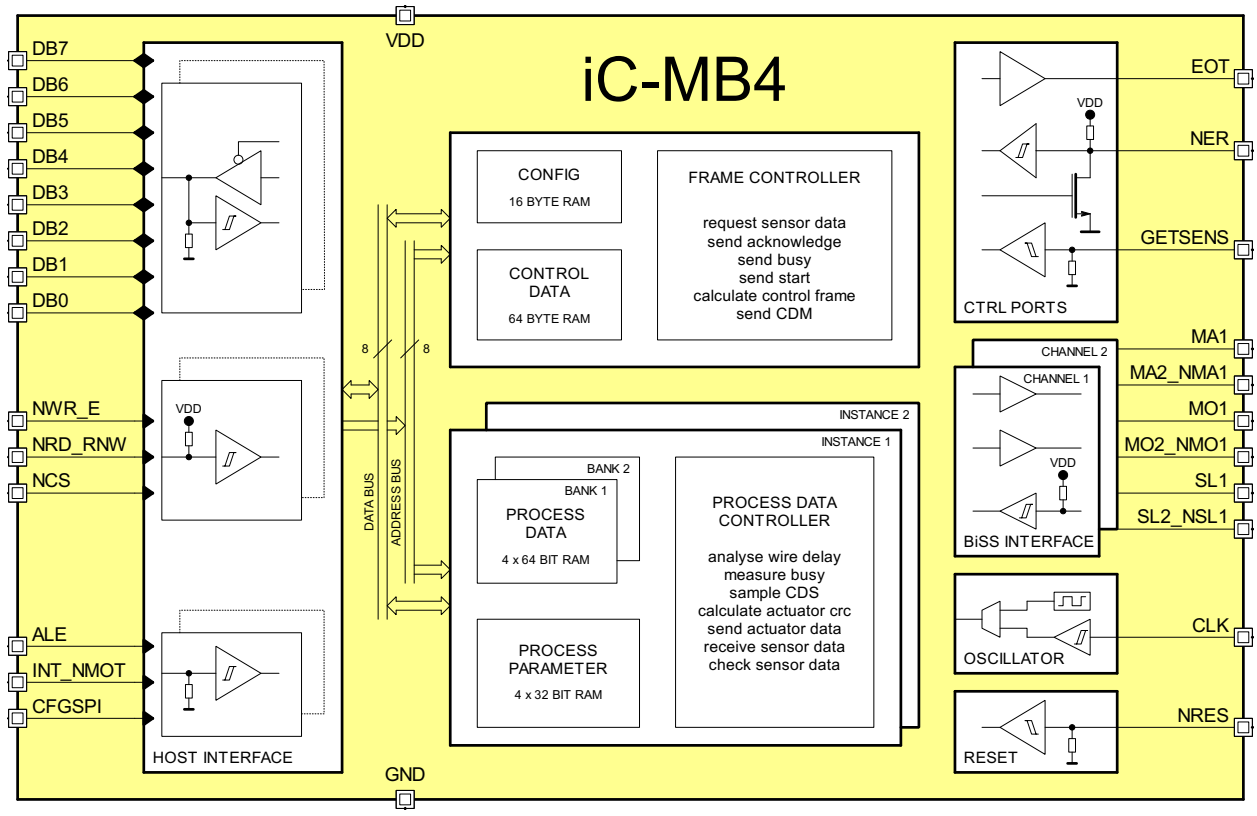
- Bidirectional communication in multi sensor systems
- Linear and rotary encoders
- Motor feedback systems
- PLC systems
- Drives

PACKAGES



TSSOP24 QFN28

BLOCK DIAGRAM



DESCRIPTION

iC-MB4 is a single-chip *BiSS*/SSI interface master controller featuring an 8 bit bus interface to industrial standard microcontrollers. Alternatively an SPI interface enables serial communication between iC-MB4 and the connected microcontroller. Up to 8 *BiSS* slaves can be accessed. The *BiSS* devices are connected to clock line MA1 and data return line SL1 using RS422 transceivers (Figure 2). The *BiSS* devices can be connected directly in noise-free environments. A maximum of 8 *BiSS* slaves is supported, each with their own configurable data sections covering:

1. Sensor data from 0 to 64 bit
   (for measurement data, flags like alarm and warning, life cycle counter, . . .)

2. Register data with 128 bytes per slave ID
   (e.g. for device parameters)

iC-MB4 provides two RAM memory banks for each slave, enabling parallel access of the microcontroller while new sensor data is being read in. A 64 byte memory supports register transfers. Sensor data acquisition is started by a microcontroller command or via pin GETSENS. Alternatively, iC-MB4 can also read in new sensor data automatically; the cycle time in this instance can be set as required. The end of sensor data acquisition and reading is signaled at pin EOT by a high; if faults occur during transmission pin NER signals a low. Errors in communication can be verified by the microcontroller via a status register; a system error message can also enter this register if bidirectional message pin NER is kept low by external intervention. iC-MB4 generates a clock signal for sensor communication using an internal 20 MHz oscillator. The clock can also be supplied externally. iC-MB4 is based on the *BiSS* master IP family MB100_X.

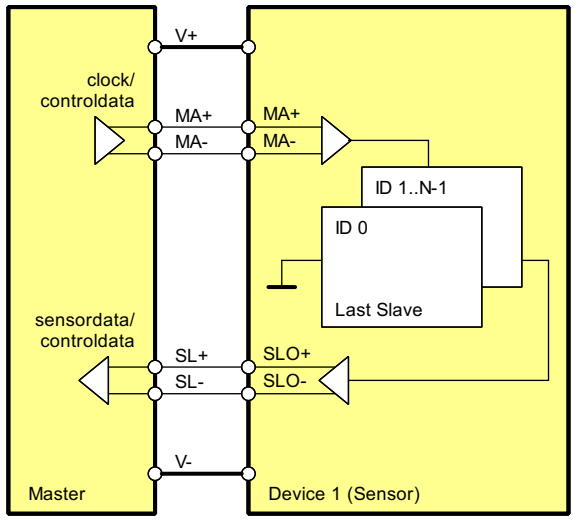


Figure 1: Point-to-point connection of iC-MB4 to one device with several slaves

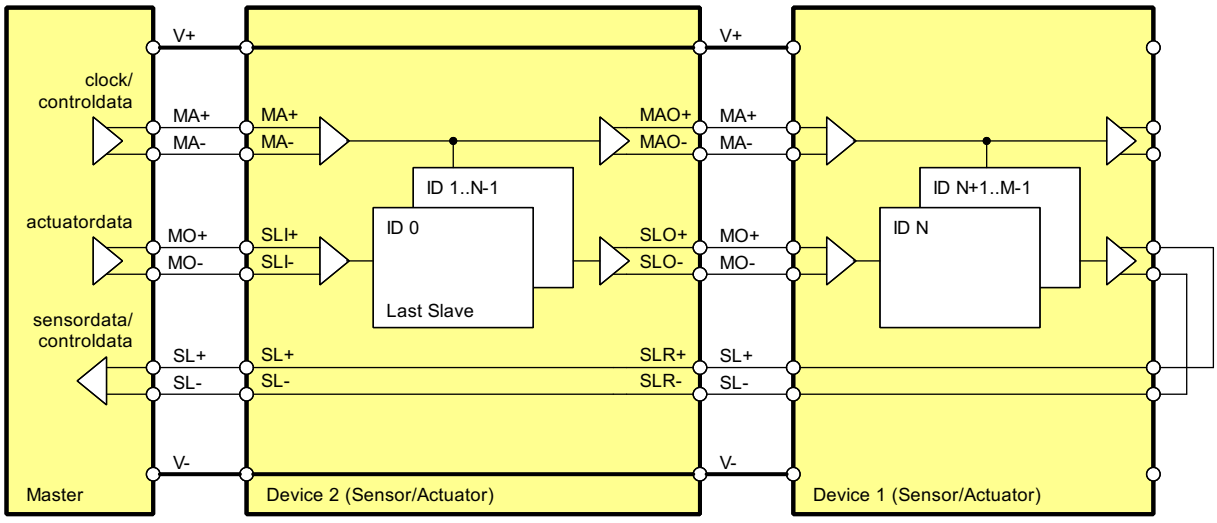
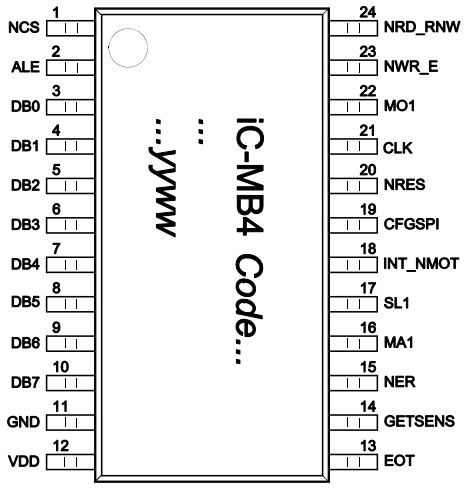


Figure 2: Example network of iC-MB4 and two devices

PACKAGING INFORMATION TO JEDEC

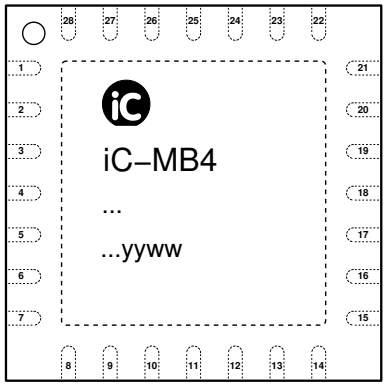
PIN CONFIGURATION TSSOP24 (topview)



PIN FUNCTIONS

No.	Name	Function
		SPI Communication Mode (CFGSPI = 1)
1	NCS	SPI Chip Select Input, active low
2	ALE	SPI Clock Input
3	DB0	SPI Serial Data Input
4	DB1	SPI Serial Data Output
7	DB4	SPI2 Chip Select Input, active low
8	DB5	SPI2 Clock Input
9	DB6	SPI2 Serial Data Input
10	DB7	SPI2 Serial Data Output
		Data Bus Communication Mode (CFGSPI = 0)
1	NCS	Chip Select Input, active low
2	ALE	Address Latch Enable Input
3	DB0	Data Bus Input/Output
4	DB1	Data Bus Input/Output
5	DB2	Data Bus Input/Output
6	DB3	Data Bus Input/Output
7	DB4	Data Bus Input/Output
8	DB5	Data Bus Input/Output
9	DB6	Data Bus Input/Output
10	DB7	Data Bus Input/Output
11	GND	Ground
12	VDD	+3 V . . . +5.5 V Supply Voltage
13	EOT	End of transmission Output
14	GETSENS	Sensor Data Request Input
15	NER	Error Message Input/Output, low active
16	MA1	BiSS Clock Line Output
17	SL1	BiSS Data Line Input
18	INT_NMOT	Communication Mode Select Input (Intel = 1, Motorola = 0)
19	CFGSPI	Serial/Parallel Mode Select Input (serial SPI = 1, parallel = 0)
20	NRES	Reset Input, low active
21	CLK	External Clock Input
22	MO1	BiSS Data Line Output
		Intel Mode (INT_NMOT = 1)
23	NWR_E	Write Input, active low
24	NRD_RNW	Read Input, active low
		Motorola Mode (INT_NMOT = 0)
23	NWR_E	Enable Input, active high
24	NRD_RNW	Read/Not-Write Select Input

PIN CONFIGURATION QFN28 5 mm x 5 mm (topview)

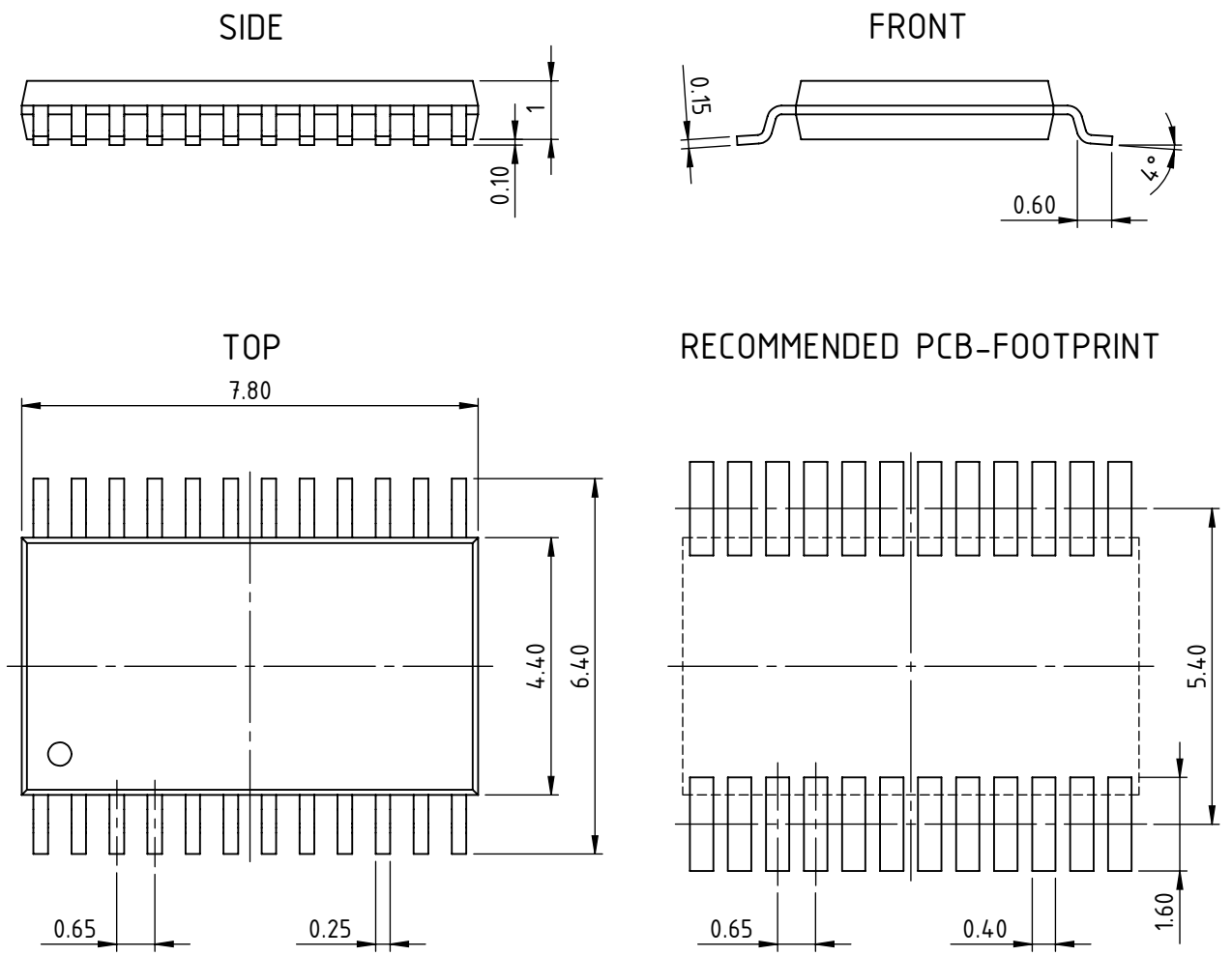


PIN FUNCTIONS

No.	Name	Function
		SPI Communication Mode (CFGSPI = 1)
27	NCS	SPI Chip Select Input, active low
28	ALE	SPI Clock Input
1	DB0	SPI Serial Data Input
2	DB1	SPI Serial Data Output
5	DB4	SPI2 Chip Select Input, active low
6	DB5	SPI2 Clock Input
7	DB6	SPI2 Serial Data Input
8	DB7	SPI2 Serial Data Output
		Data Bus Communication Mode (CFGSPI = 0)
1	DB0	Data Bus Input/Output
2	DB1	Data Bus Input/Output
3	DB2	Data Bus Input/Output
4	DB3	Data Bus Input/Output
5	DB4	Data Bus Input/Output
6	DB5	Data Bus Input/Output
7	DB6	Data Bus Input/Output
8	DB7	Data Bus Input/Output
9	GND	Ground
10	VDD	+3 V . . . +5.5 V Supply Voltage
11	EOT	End of transmission Output
12	GETSENS	Sensor Data Request Input
13	NER	Error Message Input/Output, low active
14	n.c.	not connected
15	MA1	BiSS Clock Line Output
16	MA2_NMA1	BiSS Clock Line Output Channel 2
17	SL1	BiSS Data Line Input
18	SL2_NSL1	BiSS Data Line Input Channel 2
19	INT_NMOT	Communication Mode Select Input (Intel = 1, Motorola = 0)
20	CFGSPI	Serial/Parallel Mode Select Input (serial SPI = 1, parallel = 0)
21	NRES	Reset Input, low active
22	CLK	External Clock Input
23	MO1	BiSS Data Line Output
24	MO2_NMO1	BiSS Data Line Output Channel 2
25	NWR_E	Write Input, active low (Intel) Enable Input, active high (Motorola)
26	NRD_RNW	Read Input, active low (Intel) Read/Not-Write Select Input (Motorola)
27	NCS	Chip Select Input, active low
28	ALE	Address Latch Enable Input
TP		Thermal Pad (GND)

The *Thermal Pad* must be connected to GND.

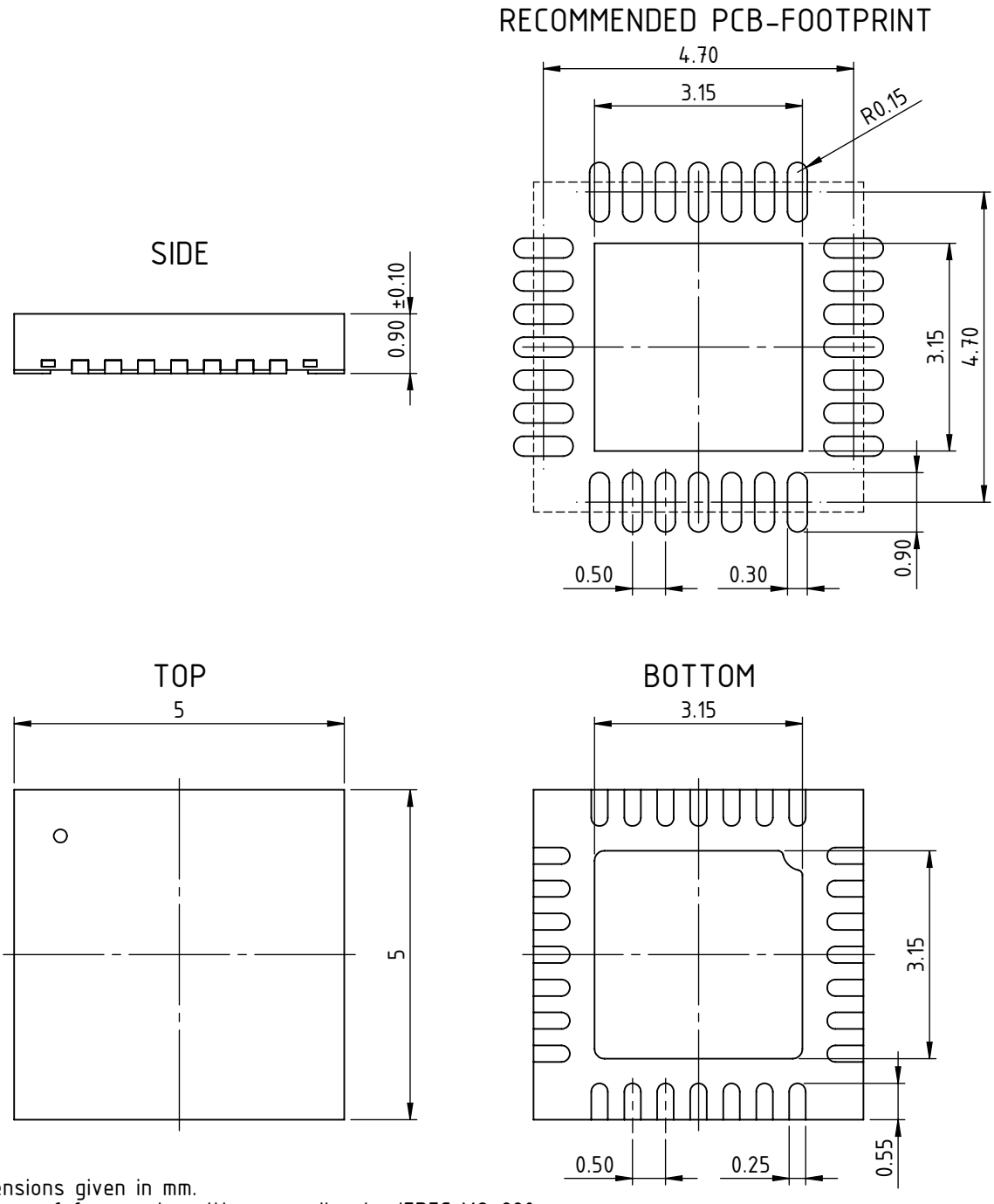
PACKAGE DIMENSIONS TSSOP24



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-153

drb_tssop24-1_pack_1, 8:1

PACKAGE DIMENSIONS QFN28 5 mm x 5 mm



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.

drc_qfn28-5x5-2_pack_1, 10:1

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Voltage at VDD		-0.3	6	V
G002	I(VDD)	Current in VDD		-20	30	mA
G003	V()	Voltage at all pins, excluding VDD and GND	V() VDD + 0.3 V	-0.3	6	V
G004	I()	Current in all pins excluding VDD and GND		-10	10	mA
G005	V_{esd}()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 Ω		2	kV
G006	Tj	Operating Junction Temperature	VDD = 3.0 V ... 4.5 V VDD = 4.5 V ... 5.5 V	-40 -40	125 140	°C °C
G007	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Operating Conditions: VDD = 3.0 V. . . 5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Standard Operating Ambient Temperature Range		-40		85	°C
T02	Ta_{ET}	Extended Operating Ambient Temperature Range	VDD = 4.5 V ... 5.5 V available on request	-40		125	°C
T03	$R_{thjaTSSOP}$	Thermal Resistance Chip to Ambient	TSSOP24 surface mounted, no special heat sink		80		K/W
T04	$R_{thjaQFN}$	Thermal Resistance Chip to Ambient	QFN28 package mounted on PCB, *thermal pad* at approx. 2 cm² cooling area		40		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0 V. . . 5.5 V, Tj = -40. . . 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD	Permissible Supply Voltage		3		5.5	V
002	I(VDD)	Supply Current in VDD	outputs not loaded, f(CLK) = 20 MHz			20	mA
003	Vc()hi	Clamp Voltage hi at all pins excluding VDD, GND, MA1, MO1, SL1	Vc()hi = V() - VDD, I() = 1 mA; outputs tristate	0.3		1.75	V
004	Vc()lo	Clamp Voltage lo at all pins excluding VDD, GND	I() = -1mA; outputs tristate	-1.6		-0.3	V
µC Interface: CFGSPI, INT_NMOT, NCS, ALE, NRD_RNW, NWR_E, DB7...0							
A01	Vs()hi	Saturation Voltage hi at DB7...0	Vs()hi = VDD - V(); VDD = 4.5 V, I() = -4 mA VDD = 3 V; I() = -2 mA			 0.4 0.4	 V V
A02	Vs()lo	Saturation Voltage lo at DB7...0	VDD = 4.5 V, I() = 4 mA VDD = 3 V, I() = 2 mA			0.4 0.4	V V
A03	Vt()hi	Threshold Voltage hi at CFGSPI, INT_NMOT, NCS, ALE, NRD_RNW, NWR_E, DB7...0				2	V
A04	Vt()lo	Threshold Voltage lo at CFGSPI, INT_NMOT, NCS, ALE, NRD_RNW, NWR_E, DB7...0		0.8			V
A05	Vt()hys	Threshold Voltage Hysteresis at CFGSPI, INT_NMOT, NCS, ALE, NRD_RNW, NWR_E, DB7...0		150	250		mV
A06	Ipd()	Pull-Down Current at CFGSPI, INT_NMOT, ALE, DB7...0	VDD = 4.5 V, V() = 1 V ... V(VDD) VDD = 3 V, V() = 1 V ... V(VDD)	6 3	30 30	60 60	µA µA
A07	Ipu()	Pull-Up Current at NCS, NRD_RNW, NWR_E	VDD = 4.5 V, V() = 0 V ... V(VDD) - 1 V VDD = 3 V, V() = 0 V ... V(VDD) - 1 V	-60 -60	-30 -30	-6 -3	µA µA
BiSS Interface							
B01	Rpu()	Pull-up Resistor at SL1, SL2_NSL1			50		kΩ
BiSS Interface: TTL/CMOS Mode (CFGIF = 00 or 01)							
B02	Vs()hi	Saturation Voltage hi at MA1, MO1, MA2_NMA1, MO2_NMO2	V() = V(VDD) - V(); VDD = 4.5 V, I() = -4 mA VDD = 3 V, I() = -2 mA			 0.4 0.4	 V V
B03	Vs()lo	Saturation Voltage lo at MA1, MO1, MA2_NMA1, MO2_NMO2	VDD = 4.5 V, I() = 4 mA VDD = 3 V, I() = 2 mA			0.4 0.4	V V
BiSS Interface: TTL Mode (CFGIF = 00)							
B04	Vt()hi	Threshold Voltage hi at SL, SL2_NSL1				2	V
B05	Vt()lo	Threshold Voltage lo at SL, SL2_NSL1		0.8			V
B06	Vt()hys	Hysteresis at at SL, SL2_NSL1		150	300		mV
BiSS Interface: CMOS Mode (CFGIF = 01)							
B07	Vt()hi	Threshold Voltage hi at SL, SL2_NSL1			62	70	%VDD
B08	Vt()lo	Threshold Voltage lo at SL, SL2_NSL1		33	39		%VDD
B09	Vt()hys	Hysteresis at at SL, SL2_NSL1		0.7	1.13		V
BiSS Interface: RS422 Mode (CFGIF = 10, VDD = 4.5 V ... 5.5 V)							
B10	Vs()hi	Saturation Voltage hi at MA1, MO1, MA2_NMA1, MO2_NMO2	V() = V(VDD) - V(); I() = -50 mA			1.2	V
B11	Vs()lo	Saturation Voltage lo at MA1, MO1, MA2_NMA1, MO2_NMO2	I() = 50 mA			1.2	V
B12	Vcom()	Input Voltage Range at SL, SL2_NSL1		0		3	V

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0 V. . . 5.5 V, Tj = -40. . . 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
B13	Vtdiff()	Threshold Voltage at SL - SL2_NSL1	V()=V(P) - V(N)	-300		300	mV
B14	Vthys()	Hysteresis Voltage at SL - SL2_NSL1	V()=V(P) - V(N)	75	150		mV
BiSS Interface: LVDS Mode (CFGIF = 11)							
B15	Vs()hi	Output Voltage hi at MA1, MO1, MA2_NMA1, MO2_NMO2	RL = 100 Ω VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	 1.25 1.0		 1.6 1.6	 V V
B16	Vs()lo	Output Voltage lo at MA1, MO1, MA2_NMA1, MO2_NMO2	RL = 100 Ω VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	 0.9 0.7		 1.125 1.125	 V V
B17	Vadiff	Differential Output Voltage at MA1 - MA2_NMA1, MO1 - MO2_NMO2	RL = 100 Ω VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	 250 220	 350 350	 450 450	 mV mV
B18	Vacm	Common Mode Output Voltage lo at MA1, MO1, MA2_NMA1, MO2_NMO2	RL = 100 Ω VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	 1.125 0.9	 1.2 1.15	 1.375 1.375	 V V
B19	Vcom()	Input Voltage Range at SL, SL2_NSL1	VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	0.8 0.8		3 1.8	V V
B20	Vtdiff()	Threshold Voltage at SL - SL2_NSL1	V()=V(P) - V(N)	-150		150	mV
B21	Vthys()	Hysteresis Voltage at SL - SL2_NSL1	V()=V(P) - V(N) VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	 25 14	 70 40		 mV mV
Ports: EOT, NER, GETSENS							
C01	Vs()hi	Saturation Voltage hi at EOT	Vs()hi = VDD - V(); VDD = 4.5 V, I() = -4 mA VDD = 3 V; I() = -2 mA			 0.4 0.4	 V V
C02	Vs()lo	Saturation Voltage lo at EOT, NER	VDD = 4.5 V, I() = 4 mA VDD = 3 V, I() = 2 mA			0.4 0.4	V V
C03	Vt()hi	Threshold Voltage hi at NER, GETSENS				2	V
C04	Vt()lo	Threshold Voltage lo at NER, GETSENS		0.8			V
C05	Vt()hys	Threshold Voltage Hysteresis at NER, GETSENS		150	250		mV
C06	Ipd()	Pull-Down Current at GETSENS	VDD = 4.5 V, V() = 1 V ... V(VDD) VDD = 3 V, V() = 1 V ... V(VDD)	6 3	30 30	60 60	µA µA
C07	Ipu()	Pull-Up Current at NER	V() = 0 V ... V(VDD) - 1 V	-950	-300	-35	µA
Oscillator: CLK							
D01	f(CLK)	Permissible Clock Rate at CLK			20	25	MHz
D02	f(CLKI)	Oscillator Clock Frequency	VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	15 10	20 15	25 22	MHz MHz
D03	Vt(CLK)hi	Threshold Voltage hi				2	V
D04	Vt(CLK)lo	Threshold Voltage lo		0.4			V
D05	Vt(CLK)hys	Threshold Voltage Hysteresis		300	500		mV
D06	Ipd()	Pull-Down Current at CLK	VDD = 4.5 V, V() = 1.5 V ... VDD VDD = 3 V, V() = 1.5 V ... VDD	6 3	30 30	60 60	µA µA

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0 V. . . 5.5 V, Tj = -40. . . 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Reset: NRES							
E01	VDDoff	Undervoltage Reset	VDD decreasing	1.4		2.6	V
E02	VDDon	Undervoltage Release	VDD increasing	1.6		2.8	V
E03	VDDhys	Undervoltage Hysteresis	VDDhys = VDDon - VDDoff	200			mV
E04	Vt()hi	Threshold Voltage hi				2	V
E05	Vt()lo	Threshold Voltage lo		0.4			V
E06	Vt()hys	Threshold Voltage Hysteresis		300	500		mV
E07	Ipd()	Pull-Down Current	V() = 1.5 V ... VDD	4	35	70	µA
E08	td()res	Required Reset Pulse Duration	At NRES	250			ns

OPERATING REQUIREMENTS: µC Interface, INTEL mode

Operating conditions: CFGSPI = 0, INT_NMOT = 1, VDD = 3.0 . . . 5.5 V, Tj = -40 . . . 125 °C
lo input level = 0 . . . 0.8 V, hi input level = 2.0 V . . . VDD, lo output level = 0 . . . 0.4 V, hi output level = 2.4 V . . . VDD
Alias: NRD = NRD_RNW, NWR = NWR_E

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I001	tsCA	Setup Time: NCS lo before ALE hi→lo		10		ns
I002	tsDA	Setup Time: Data stable before ALE hi→lo		15		ns
I003	thDA	Hold Time: Data stable after ALE hi→lo		15		ns
I004	tAh	Signal Duration: ALE at high level		10		ns
I005	tsAR	Setup Time: ALE lo before NRD hi→lo		10		ns
I006	thAR	Hold Time: ALE lo after NRD lo→hi	NCS = lo	10		ns
I007	tRl	Signal Duration: NRD at low level	NCS = lo	10		ns
I008	tpRD1	Propagation Delay: Data stable after NRD hi→lo	NCS = lo, CL = 50 pF		25	ns
I009	tpRD2	Propagation Delay: Data bus high impedance after NRD lo→hi	NCS = lo, CL = 50 pF		25	ns
I010	thCR	Hold Time: NCS lo after NRD lo→hi		10		ns
I011	tsAW	Setup Time: ALE lo before NWR hi→lo		10		ns
I012	thAW	Hold Time: ALE lo after NWR lo→hi	NCS = lo	10		ns
I013	tWl	Signal Duration: NWR at low level	NCS = lo	10		ns
I014	tsDW	Setup Time: Data stable before NWR lo→hi	NCS = lo	15		ns
I015	thDW	Hold Time: Data stable after NWR lo→hi	NCS = lo	15		ns
I016	thCW	Hold Time: NCS lo after NWR lo→hi		10		ns

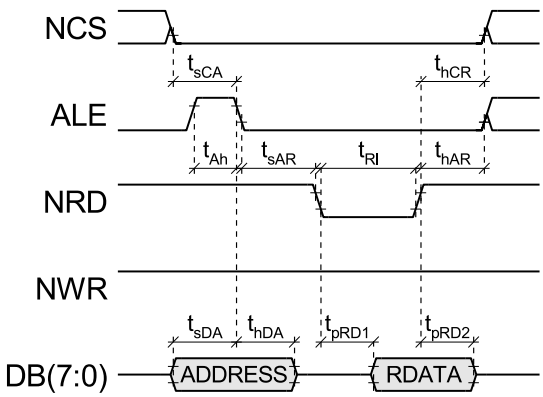


Figure 3: Read cycle (Intel mode)

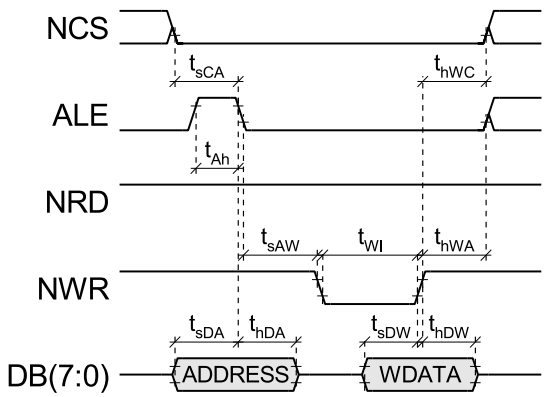


Figure 4: Write cycle (Intel mode)

OPERATING REQUIREMENTS: µC Interface, MOTOROLA mode

Operating conditions: CFGSPI = 0, INT_NMOT = 0 VDD = 3.0 . . . 5.5 V, Tj = -40 . . . 125 °C;
lo input level = 0 . . . 0.8 V, hi input level = 2.0 V . . . VDD, lo output level = 0 . . . 0.4 V, hi output level = 2.4 V . . . VDD
Alias: RNW = NRD_RNW, E = NWR_E

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I101	tsCA	Setup Time: NCS lo before ALE hi→lo		10		ns
I102	tsDA	Setup Time: Data stable before ALE hi→lo		15		ns
I103	thDA	Hold Time: Data stable after ALE hi→lo		15		ns
I104	tAh	Signal Duration: ALE at high level		10		ns
I105	tsAE	Setup Time: ALE lo before E lo→hi		10		ns
I106	thAE	Hold Time: ALE lo after E hi→lo	NCS = lo	10		ns
I107	tsRE	Setup Time: RNW stable before E lo→hi	NCS = lo	10		ns
I108	thRE	Hold Time: RNW stable after E hi→lo	NCS = lo	10		ns
I109	tEh	Signal Duration: E at high level	NCS = lo	10		ns
I110	tpED1	Propagation Delay: Data stable after E lo→hi	NCS = lo, CL = 50 pF		25	ns
I111	tpED2	Propagation Delay: Data bus high impedance after E hi→lo	NCS = lo, CL = 50 pF		25	ns
I112	tsDE	Setup Time: Data stable before E hi→lo	NCS = lo	15		ns
I113	thDE	Hold Time: Data stable after E hi→lo	NCS = lo	15		ns
I114	thCE	Hold Time: NCS lo after E hi→lo		10		ns

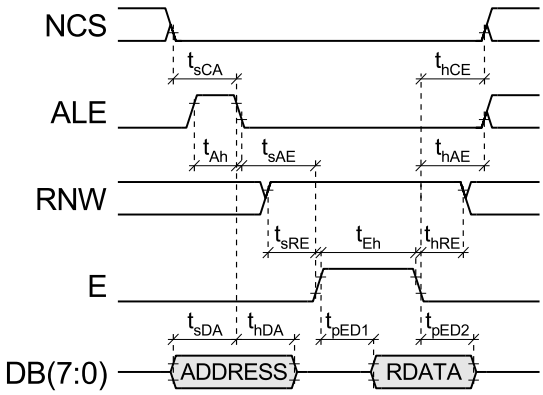


Figure 5: Read cycle (Motorola mode)

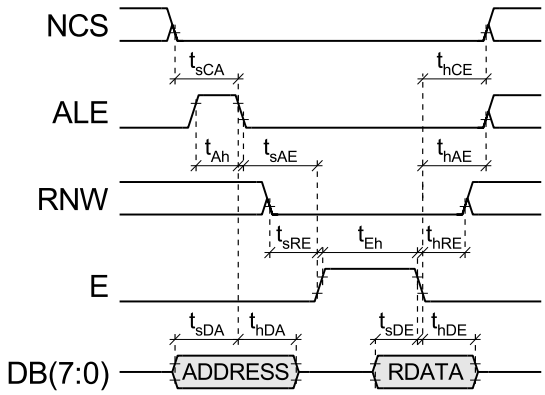


Figure 6: Write cycle (Motorola mode)

OPERATING REQUIREMENTS: µC Interface, SPI mode

Operating conditions: CFGSPI = 1 VDD = 3.0 . . . 5.5 V, Tj = -40 . . . 125 °C;
lo input level = 0 . . . 0.8 V, hi input level = 2.0 V . . . VDD, lo output level = 0 . . . 0.4 V, hi output level = 2.4 V . . . VDD
Alias: NCS = NCS/DB4, SCLK = ALE/DB5, MOSI = DB0/DB6, MISO = DB1/DB7

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I201	tsCS	Setup Time: NCS lo before SCLK lo→hi		10		ns
I202	thCS	Hold Time: NCS lo after SCLK hi→lo		10		ns
I203	tSl	Signal Duration: SCLK lo		10		ns
I204	tSh	Signal Duration: SCLK hi	 during command 'ReadData' between address and data	10 100		ns ns
I205	tsDS	Setup Time: MOSI stable before SCLK lo→hi		7.5		ns
I206	thDS	Hold Time: MOSI stable after SCLK lo→hi		7.5		ns
I207	tpSD	Propagation Delay: MISO stable after SCLK hi→lo	CL = 50 pF		25	ns
I208	tpCD	Propagation Delay: MISO high impedance after NCS lo→hi	CL = 50 pF		25	ns
I209	tCh	Signal Duration: NCS hi		10		ns

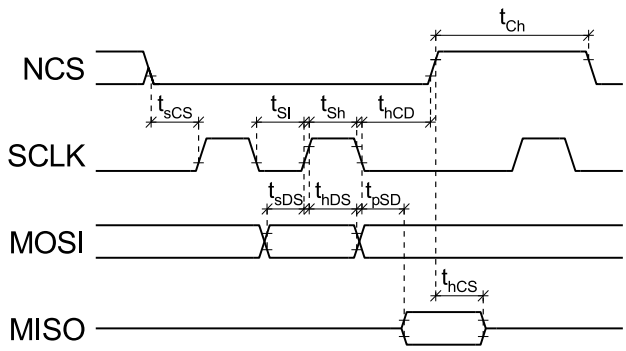


Figure 7: Read/write access (SPI mode)

OPERATING REQUIREMENTS: BiSS Interface - BiSS Frame

Operating conditions: register bit SELSSI = 0 VDD = 3.0 . . . 5.5 V, Tj = -40 . . . 125 °C
Alias: MA = MA1/MA2_NMA1, SL = SL1/SL2_NSL1

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
Sensor Data Cycle						
I301	TMAS	Clock Period	FreqSens via FREQ(4:0) selected in accordance with table 45 on page 29	2	320	1/f(CLK)
I302	tMASl	Clock Signal Lo Level Duration		50	50	% TMAS
I303	tMASh	Clock Signal Hi Level Duration		50	50	% TMAS
I304	tpLine	Permissible Line Delay		0	indefinite	
I305	Δ tpL	Permissible Propagation Delay of Subsequent Clock Cycles vs. 1st Clock Cycle	Δ tpL = max(|tpLine - tpLx|); x= 1 ... n		25	% TMAS
I306	Ttos	Permissible Timeout (Slave)		55		% TMAS

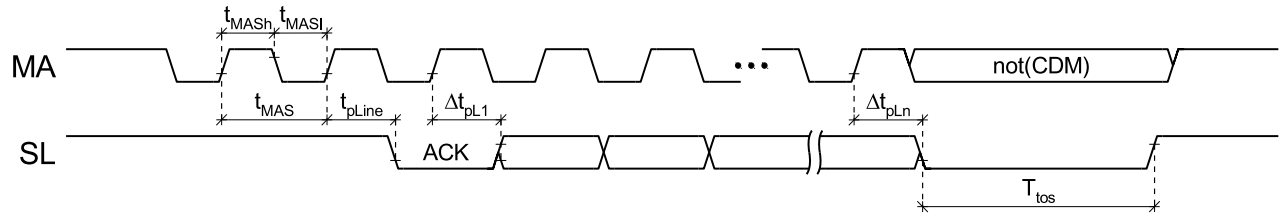


Figure 8: Timing diagram *BiSS* Frame

SLx line sampling

With BiSS line delays longer than one clock cycle are permissible, with the result that line delays during communication are negligible. The evaluation of the sensor response is delayed until the first falling edge at SLx while the clock signal continues to be output at MAx .
Within one MAx clock cycle four equally distributed sampling instances are available. Following the falling edge at SLx is the slaves acknowledge signal. The SL1 level is evaluated by two sampling instances, close to the center of the transmitted bit.

OPERATING REQUIREMENTS: BiSS Interface - Register Data Cycle (BiSS B)

Operating conditions: register bit SELSSI = 0 VDD = 3.0...5.5 V, Tj = -40...125 °C
Alias: MA = MA1/MA2_NMA1, SL = SL1/SL2_NSL1

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
Your copied rows:						
I401	TMAR	Clock Period	FreqReg via FREQ(7:5) selected in accordance with table on page XXX	2	256	TMAS
I402	tMA0h	"Logic 0" Hi Level Duration		25	25	% TMAR
I403	tMA1h	"Logic 1" Hi Level Duration		75	75	% TMAR
I404	tMAth	Clock Signal Hi Level Duration	register data readout	50	50	% TMAR
I405	tsSM	Setup Time: SL stable before MA lo→hi		30		ns
I406	thSM	Hold Time: SL stable after MA lo→hi		0		ns
I407	Ttor	Permissible Timeout (Slave)		80		% TMAR

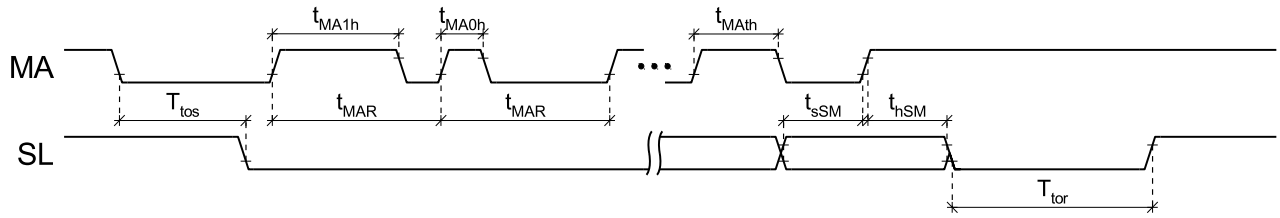


Figure 9: Timing diagram *BiSS* B register access

OPERATING REQUIREMENTS: BiSS Interface (SSI mode)

Operating conditions: register bit SELSSI = 1; VDD = 3. . . 5.5 V, Tj = -40. . . 125 °C
Alias: MA = MA1/MA2_NMA1, SL = SL1/SL2_NSL1

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I501	TMAS	Clock Period	FreqSens via FREQ(4:0) selected in accordance with table 45 on page 29	2	320	1/f(CLK)
I502	tMASh	Clock Signal Hi Level Duration		50	50	% TMAS
I503	tMASl	Clock Signal Lo Level Duration		50	50	% TMAS
I504	tsDC	Setup Time: SL stable before MA lo→hi		30		ns
I505	thDC	Hold Time: SL stable after MA lo→hi		0		ns

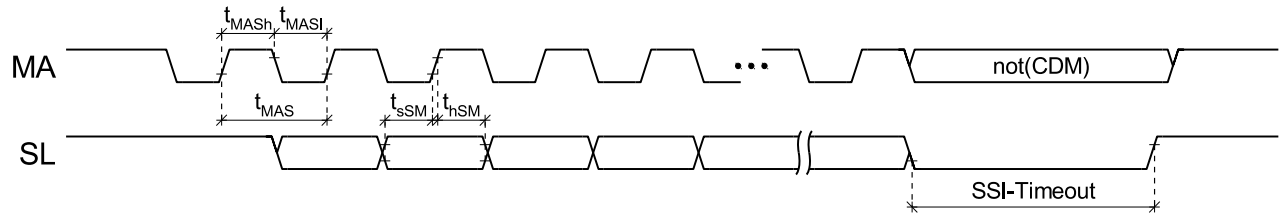


Figure 10: Timing diagram SSI mode

SLx line sampling
In SSI interface mode SL1 values are sampled with the rising edge at MA1. An overall delay of the sensor response to the clock at MA1, caused by process times in the sensor or transmission times, is permissible up to the length of one clock cycle.

PROGRAMMING

REGISTER LAYOUT, OVERVIEW

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sensor and Actuator Data								
0x00	SCDATA1(7:0)							
0x01 .. 0x07	SCDATA1(63:8)							
0x08 .. 0x3F	SCDATA2(63:0) .. SCDATA8(63:0)							
0x40 .. 0x7F	– *							
Register Data								
0x80 †	RDATA1(7:0)							
0x80 ‡	IDS(7:0)							
0x81 .. 0xBF	RDATA2(7:0) .. RDATA64(7:0)							
Configuration Slave 1								
0xC0	GRAYS1 / LSTOP1	ENSCD1	SCDLEN1(5:0)					
0xC1	SELCRCS1	SCRCLEN1(6:0) / SCRCPOLY1(7:1)						
0xC2	SCRCSTART1(7:0)							
0xC3	SCRCSTART1(15:8)							
0xC4 .. 0xDF	Configuration Slave 2(31:0) .. Configuration Slave 8(31:0)							
Control Communication Configuration								
0xE0	– *							
0xE1	– *							
0xE2	WNR	REGADR(6:0)						
0xE3	– *		REGNUM(5:0)					
0xE4	– *						CHSEL(2:1)	
0xE5 †	CTS	REGVERS	SLAVEID(2:0)			– *	EN_MO	HOLDCDM
0xE5 ‡	CTS	REGVERS	CMD(1:0)		IDA_TEST	– *	EN_MO	HOLDCDM
Master Configuration								
0xE6	FREQR(2:0)			FREQS(4:0)				
0xE7	– *						NOCRC	SINGLEBANK
0xE8	FREQAGS(7:0)							
0xE9	MO_BUSY(7:0)							
0xEA	REVISION(7:0)§							
0xEB	VERSION(7:0)§							
Channel Configuration								
0xEC	'0'	'0'	'0'	SLAVELOC5	'0'	'0'	'0'	'1'
0xED	– *				CFGCH2(1:0)		CFGCH1(1:0)	
0xEE	– *							

* Reserved or unused register bits highlighted as "–" need to be written with 0 if a byte wide register write access is required.
† Using register access in control communication.
‡ Using command/instructions in control communication.
§ Register bits with constant "0" or "1" are ROM-based values and can not be changed through writing.

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave Configuration 2								
0xEF	ACTnSENS(8:1)							
Status Information								
0xF0	nERR	nAGSERR	nDELAYERR	nSCDERR	nREGERR	REGEND	'1'	EOT
0xF1	SVALID4	'0'	SVALID3	'0'	SVALID2	'0'	SVALID1	'0'
0xF2	SVALID8	'0'	SVALID7	'0'	SVALID6	'0'	SVALID5	'0'
0xF3	CDMTIME-OUT	CDSSEL	REGBYTES(5:0)					
Instruction Register								
0xF4	BREAK	HOLDBANK	SWBANK	INIT	INSTR(2:0)			AGS
0xF5	MAVO	MAFO	MAVS	MAFS	CFGIF(1:0)		ENTEST	CLKENI
0xF6	–	–	–	–	–	–	–	–
0xF7	–	–	–	–	–	–	–	–
Status Information 2								
0xF8	0	1	0	1	CDS2	SL2	CDS1	SL1
0xF9	0	1	0	1	0	1	0	1
0xFA	–	–	–	–	–	–	–	–
0xFB	–	–	–	–	–	–	–	SWBANK-FAILS
Reserved								
0xFC . . 0xFF	–	–	–	–	–	–	–	–

Table 10: Register layout

iC-MB4 does reset all RAM registers to 0 on a power on reset.

FUNCTIONAL DESCRIPTION

BiSS C Frame

BiSS uses in the point-to-point configuration a clock line (MA) from the master to the slave and a data line (SL) from the slave to the master. A device may contain multiple slaves. The data input (SLI) of the last slave is set to low, the slaves are daisychained (SLO → SLI), and the data output (SLO) of the first slave is directed to the master. A data line from the master to the slave is not mandatory (see figure 1).

At the end of the cycle the master sends the CDM bit (inverted) on the MA clock line. After detecting the slaves timeout with SLO = 1 the master changes the MA clock line state to high. If the BiSS frame has not been clocked out finally, e.g. for a faster configuration phase and higher control data transmission rates, the HOLDCDM needs to be enabled to keep the clock line constant until the next cycle starts. The difference is explained in figures 11 and 12.

BiSS C provides the additional bus configuration with the data output line (MO) from the master to the slaves. With EN_MO = 1 the master emulates a slave without sensor data at the MO line. The parameterized processing time for sensor data (i.e. the ”start bit delay”) is configured by the MO_BUSY parameter.

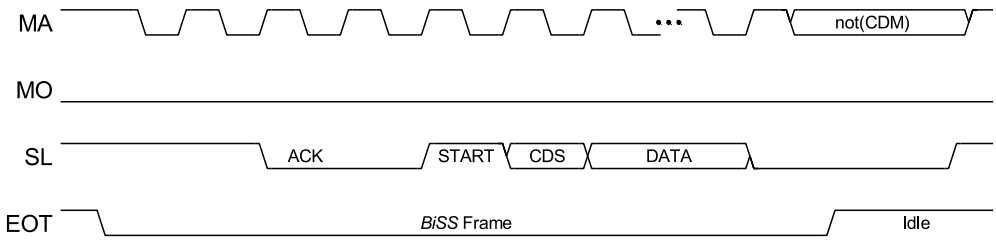


Figure 11: BiSS frame in point-to-point configuration (EN_MO = 0, HOLDCDM = 0)

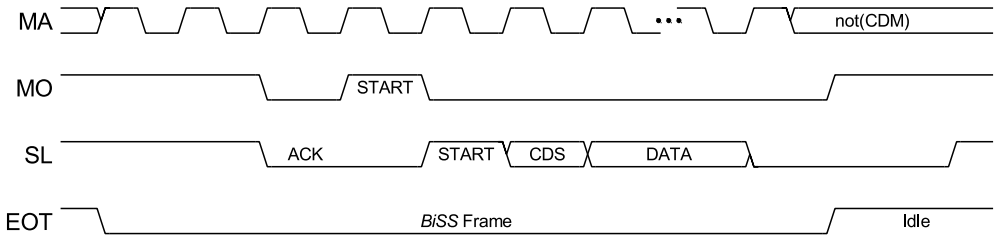


Figure 12: BiSS frame in bus configuration (EN_MO = 1, HOLDCDM = 1)

BiSS B Register Communication

In BiSS B the register communication is started by a timing condition and a handshake at the beginning of the cycle (see figure 13). Alternatively the register communication can be selected at the cycle start with the MO line. With EN_MO = 1 the slave ID ”0” remains unused.

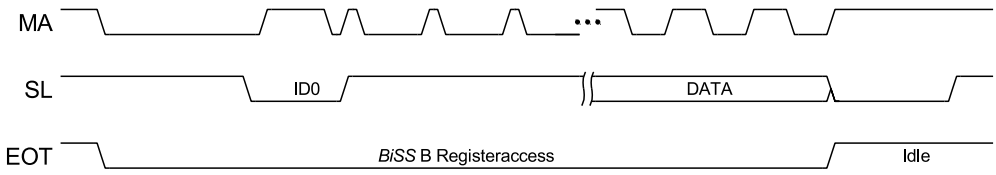


Figure 13: BiSS B register access (EN_MO = 0)

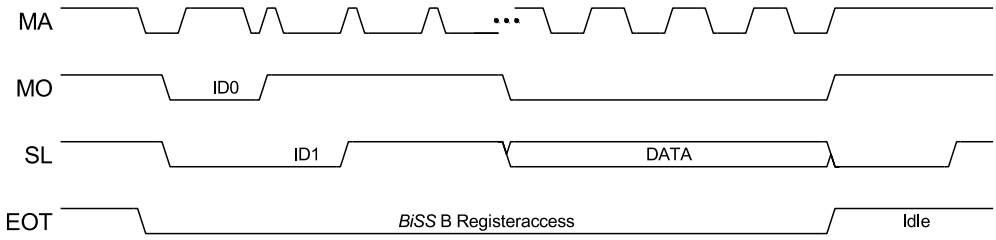


Figure 14: BiSS B register access (EN_MO = 1)

Extended SSI BiSS C Register Communication
With extended SSI the BiSS C register write access is possible to the SSI slave. The master is able to transmit a BiSS C register write access to the slave without the slaves CDS feedback. The master cannot verify if the BiSS C register write access to the slave did succeed or not. At the end of the cycle the master sends the CDM bit inverted on the MA clock line.

BiSS C Init Sequence
In the init sequence two 0 pulses are generated at MA. The slave should answer with a falling edge and after the BiSS timeout with a rising edge at SL. The gap between the second rising edge at MA and the falling edge at SL is measured as line delay and stored in the single cycle data RAM. The BiSS C init is selected with REGVERS=1 and executed with INIT = 1.

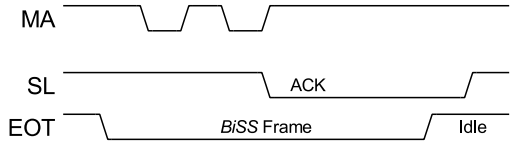


Figure 15: BiSS init sequence

With an INIT sequence the iC-MB4 does store the measured channel 1 line delay in the SCDATA1(7:0) and the channel 2 line delay in the SCDATA5(7:0).
The unit of this value is the 1/4 of the configured MA clock frequency.

$$t_{\text{Line Delay Channel 1}} = \frac{SCDATA1(7:0)}{4 * f_{MA}}$$

$$t_{\text{Line Delay Channel 2}} = \frac{SCDATA5(7:0)}{4 * f_{MA}}$$

For the INIT sequence the maximum line delay is 255. On exceeding this limit while INIT the INIT sequence is aborted and an AGSERR is set.

MICROCONTROLLER INTERFACE

With pin CFGSPI the microcontroller interface is selected between an 8 bit parallel interface or an SPI serial interface. With pin CFGSPI = 0 the 8 bit parallel microcontroller interface is selected in which the bidirectional data bus alternately transmits addresses and data in blocks of 8 bits (see figures 3). With pin INT_NMOT = 0 for an Intel 8051 controller or INT_NMOT = 1 for a 68HC11 Motorola controller communication type is selected.

CFGSPI	INT_NMOT	Mode
0	0	Motorola 68HC11
0	1	Intel 8051

Table 11: Parallel communication modes

SPI Serial Microcontroller Interface
With pin CFGSPI = 1 the SPI serial microcontroller interface is selected.

CFGSPI	INT_NMOT	Mode
1	-	SPI1 (polarity = 0, phase = 0)

Table 12: SPI communication modes

When operated in conjunction with an SPI controller, pin ALE is used as a clock input (SCK) and pin NCS as an enable input (NCS), with DB0 as the data input (SI) and DB1 as the data output (SO). Data is transmitted serially in successive blocks of 8 bits (command, address and data). Six commands are available:

- WriteData (0x02 = 0b0000 0010)
- ReadData (0x03 = 0b0000 0011)
- ReadStatus (0x05 = 0b0000 0101)
- WriteInstruction (0x07 = 0b0000 0111)
- ReadData0 (0x09 = 0b0000 1001)
- WriteData0 (0x0B = 0b0000 1011)

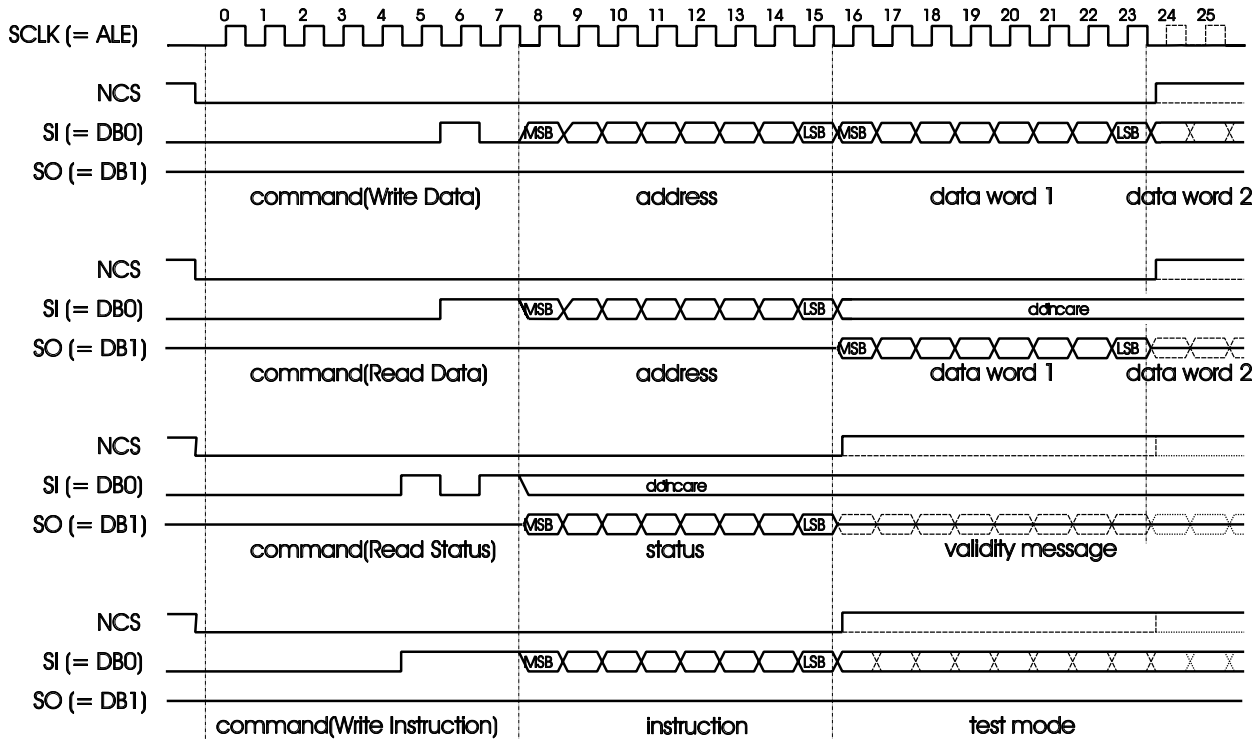


Figure 16: SPI transmission protocol (polarity 0, phase 0)

The first two commands can be used to write data to or read data from iC-MB4's registers. The latter commands are shortend write commands and read commands with a set start address. In the read data command a delay between the address and the first data is necessary.

For fast access use the SPI commands "ReadStatus", "WriteInstruction" and "ReadData0".

- ReadStatus to read the status register in 0xF0
- WriteInstruction to write the instruction register in 0xF4
- ReadData0 to read SDATA register starting at 0x00

This means that it is not necessary to give an address, with the data directly adhering to the command. With all commands it is possible to transmit several bytes of data consecutively if the NCS signal is not reset and ALE/SCK continues to be clocked. The address transmitted (240 for ReadStatus and 244 for WriteInstruction) is then the start address which is internally increased by 1 following each transmitted byte.

Additional 2nd SPI Serial Microcontroller Interface
With the active SPI serial microcontroller interface an additional SPI interface can be addressed for dedicated register access and reduced function set.

CFGSPI	NWR_E	Mode
1	0	SPI2, optional (polarity = 0, phase = 0)

Table 13: SPI communication modes

An additional SPI interface at DB4 . . . DB7 is available for exclusive read access to the SCD single cycle data RAM of the slaves 5 to 8. The 2nd SPI interface is enabled with NWR_E = 0. Access to status, instruction and parameter register is not possible.

The 2. SPI does only provide the SPI command "ReadData" with a limited address range of 0x40 . . . 0x7F.

- ReadData (0x03 = 0b0000 0011)

The 2nd SPI can neither be used to configure nor to read status.

This 2nd SPI can only be used to read SCDATA from 0x40 . . . 0x7F.

SENSOR DATA

The transmission of sensor data begins when the master outputs the clock signal at pin MA1 with the clock frequency selected by FREQ. The line delay, i.e. the transmission propagation until an acknowledgement is generated at SL1, is determined from the second falling edge onwards. While the clock continues to be output at MA1, the master waits for the slaves start bit (1) signaling the start of data transmission. Afterwards this the actual clocking out of sensor data begins, i.e. the sensors place a new bit on the SL1 line with each rising edge on the MA1 line.

The sensor data being input into the master and the subsequent sets of CRC data are written to the appropriate sensor data RAM. At the same time the new CRC value is calculated in accordance with the CRC polynomial stored in the configuration RAM. Should the system ascertain after entry of the last CRC bit, that transmission was faulty, the relevant validity message is deleted and error message nSENSERR set in the status register. At the same time the sensor data RAM banks are swapped.

In order for new sensor data to be read in during controller accesses, iC-MB4 has dual memory banks for sensor data. While sensor data is being read and written into the first RAM bank, the second RAM bank section with the prior read sensor data can be read out by the controller. The relevant sensor data memory banks are swapped at the end of the reading procedure. This can be prevented by the controller entering the command register bit HOLDBANK. Simultaneously the status information 1 (validity register in address 0xF1 . . . 0xF2) and status information 2 (CDS2 and CDS1 in address 0xF8) are also swapped.

Arrangement of Sensor Data in the RAM
The sensor data memory bank has 8 bytes of memory for each slave which can be interpreted as 64 bits of memory in the array 0bxxxx.x111 to 0bxxxx.x000. The sensor data is written to memory area [SDLEN - 1:0] with SDLEN marking the length of the relevant data. If there is space in the available memory for the processed CRC bits and NOCRC = 0, the read CRC bits are stored with the above data at positions [63:63 - (CRCLEN-1)].

SCDATA	Addr. 0x00 . . . 0x3F; bit 7:0	R/W
0x00	SCDATA1(7:0)	
0x01	SCDATA1(15:8)	
0x02	SCDATA1(23:16)	
0x03	SCDATA1(31:24)	
0x04	SCDATA1(39:32)	
0x05	SCDATA1(47:40)	
0x06	SCDATA1(55:48)	
0x07	SCDATA1(63:56)	
0x08 . . 0x0F	SCDATA2(63:0)	
0x10 . . 0x17	SCDATA3(63:0)	
0x18 . . 0x1F	SCDATA4(63:0)	
0x20 . . 0x27	SCDATA5(63:0)	
0x28 . . 0x2F	SCDATA6(63:0)	
0x30 . . 0x37	SCDATA7(63:0)	
0x38 . . 0x3F	SCDATA8(63:0)	

Table 14: Address mapping of sensor data

Example: BiSS Sensor Bus with 3 Slaves
The following example indicates the sensor data position and content in the sensor data of three slaves.

Slave 1: 19+2 bits of sensor data, 6 bits of CRC
=> total length of 27 bits

Slave 2: 12+2 bits of sensor data, 6 bits of CRC
=> total length of 20 bits

Slave 3: 13+2 bits of sensor data, 6 bits of CRC
=> total length of 21 bits

Addr.	Content
0x00 . . 0x07	Sensor data 1(63:0)
0x00	Sensor data 1(7:0)
0x01	Sensor data 1(15:8)
0x02	Sensor data 1(20:16) in bit 4:0
0x03	not changed
0x04	not changed
0x05	not changed
0x06	not changed
0x07	Received CRC of sensor data 1(5:0) in bit 7:2
0x08 . . . 0x0F	Sensor data 2(63:0)
0x08	Sensor data 2(7:0)
0x09	Sensor data 2(13:8) in bit 5:0
0x0A	not changed
0x0B	not changed
0x0C	not changed
0x0D	not changed
0x0E	not changed
0x0F	Received CRC of sensor data 2(5:0) in bit 7:2
0x10 . . . 0x17	Sensor data 3(63:0)
0x10	Sensor data 3(7:0)
0x11	Sensor data 3(14:8) in bit 6:0
0x12	Sensor data
0x13	not changed
0x14	not changed
0x15	not changed
0x16	not changed
0x17	Received CRC of sensor data 3(5:0) in bit 7:2
0x18 . . . 0x1F	not changed
0x20 . . . 0x27	not changed
0x28 . . . 0x2F	not changed
0x30 . . . 0x37	not changed
0x38 . . . 0x3F	not changed

Table 15: Address mapping of sensor data

Dual SPI Interface Operation
iC-MB4 can be operated with two SPI interfaces on a single BiSS interface. With activated second SPI (NWR_E = 0) the SCDATA range is splitted into two sections, each SPI with 4 SCD data section. The SPI2 can only access the related SCDATA. The SPI2 has no access to the configuration nor status information.

Addr.	Content
0x00	SPI1: SCDATA 1(7:0)
0x01	SPI1: SCDATA 1(15:8)
0x02	SPI1: SCDATA 1(23:16)
0x03	SPI1: SCDATA 1(31:24)
0x04	SPI1: SCDATA 1(39:32)
0x05	SPI1: SCDATA 1(47:40)
0x06	SPI1: SCDATA 1(55:48)
0x07	SPI1: SCDATA 1(63:56)
0x08 . . . 0x0F	SPI1: SCDATA 2(63:0)
0x10 . . . 0x17	SPI1: SCDATA 3(63:0)
0x18 . . . 0x1F	SPI1: SCDATA 4(63:0)
0x20 . . . 0x27	SPI2: SCDATA 1(63:0)
0x28 . . . 0x2F	SPI2: SCDATA 2(63:0)
0x30 . . . 0x37	SPI2: SCDATA 3(63:0)
0x38 . . . 0x3F	SPI2: SCDATA 4(63:0)

Table 16: Address mapping of sensor data access by SPI1 and SPI2

The second BiSS interface channel 2 is only available with iC-MB4 QFN28.

CONTROL COMMUNICATION

For the interim storage of register information read out from or writing to the slaves, iC-MB4 has an individual storage area (addresses 0x80 . . . 0xBF) which can temporarily store up to 64 bytes of data. Just one single command starts the transmission (writing to the slave or read from the slave). The slave addressed is set by the SLAVEID(2:0) and the first address for the register data access is set by REGADR. The transfer of register data may take longer than a sensor data transfer cycle, so that the content of the sensor data RAM is then often obsolete.

Configuration of Register Communication

RDATA	Addr. 0x80 . . . 0xBF; bit 7:0	R/W
0x00 . . . 0xFF	RDATA: register data (64 bytes, bidirectional)	

Table 17: Register data

REGADR	Addr. 0xE2; bit 6:0	R/W
0x00 . . . 0x7F	Register address	

Table 18: Register access start address

WNR	Addr. 0xE2; bit 7	R/W
0	Read register data	
1	Write register data	

Table 19: Register access direction

Registers start address REGADR, number of bytes REGNUM and slave ID SLAVEID stipulate from which slave register address onwards how many bytes are to be written to or read out from which specific slave. A byte count of 0 entered for REGNUM signals the transmission of a single register value; a 63 indicates the transmission of 64 register values. In the register REGBYTES a 0 is indicated and readable if register communication has proved error free. In the event of an register communication error the number of correctly read or written registers is indicated in REGBYTES.

REGNUM	Addr. 0xE3; bit 5:0	R/W
0x00	Register count = 1	
0x01 . . . 0x3F	Register count = REGNUM(5:0)+1	

Table 20: Register quantity of access(-1)

REGBYTES	Addr. 0xE3; bit 5:0	R/W
0x00	After transfer: no register communication error	
0x01 . . . 0x3F	After transfer: number of successfully transferred registers before register communication error	

Table 21: Register transmitted successfully

CHSEL(1)	Addr. 0xE4; bit 0	R/W
0	Channel 1 not used *	
1	Channel 1 used for control communication	
CHSEL(2)	Addr. 0xE4; bit 1	R/W
0	Channel 2 not used	
1	Channel 2 used for control communication †	

Table 22: Channel mapping for control communication

SLAVEID	Addr. 0xE5; bit 5:3	R/W
0 . . . 7	Slave ID that addresses the register access	

Table 23: Slave ID of accessed slave

iC-MB4 does support autonomous register communication with BiSS C and BiSS B, REGVERS is set to present protocol type. On register write access with extended SSI the BiSS C protocol type needs to be selected.

REGVERS	Addr. 0xE5; bit 6	R/W
0	Register communication BiSS A/B	
1	Register communication BiSS C	

Table 24: Type of protocol for register access

CTS	Addr. 0xE5; bit 7	R/W
0	Command/instruction communication	
1	Register communication	

Table 25: Type of control communication

The CTS parameter was called MSEL in former MB100 or iC-MB3 data sheets.

HOLDCDM	Addr. 0xE5; bit 0	R/W
0	Clock line high at end of cycle	
1	Clock line constant with CDM bit until start of next cycle	

Table 26: Length of CDM bit

* Channel 1 is selected if CHSEL(2:1)=0.
† Channel 2 is not available with iC-MB4 TSSOP24.

EN_MO	Addr. 0xE5; bit 1	R/W
0	MO forced to low	
1	Parameterized processing time by master on MO signal active (length: MO_BUSY)	

Table 27: MO control

MO_BUSY	Addr. 0xE9; bit 7:0	R/W
0x00 . . . 0xFF	Count of MA clocks as the parameterized processing time by master on MO signal **Premise:** EN_MO = 1	

Table 28: Master controlled processing time

Configuration of Command/Instruction Communication

The command/instruction communication is a subset of the control communication. iC-MB4 does support autonomous command/instruction communication only with BiSS C.

CTS	Addr. 0xE5; bit 7	R/W
0	Command/instruction communication	
1	Register communication, not applicable with Command/instruction communication	

Table 29: Type of control communication

REGVERS	Addr. 0xE5; bit 6	R/W
1	Command communication BiSS C	
0	Not applicable with command/instruction communication	

Table 30: Type of protocol for register access

IDA_TEST	Addr. 0xE5; bit 3	R/W
0	The slaves feedback (IDA) is tested before execution (EX bit after IDA, see figure 18)	
1	Immediate execution (see figure 17)	

Table 31: Command/instruction execution control

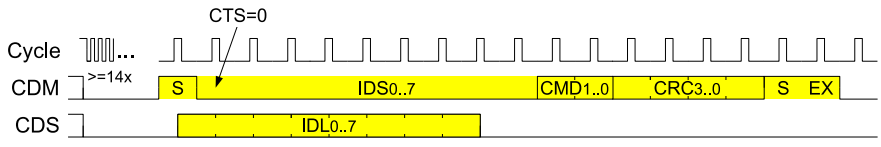
CMD(1:0)	Addr. 0xE5; bit 5:4	R/W
0x00	Command/instruction 0b00	
0x01	Command/instruction 0b01	
0x02	Command/instruction 0b10	
0x03	Command/instruction 0b11	

Table 32: Command of accessed slave

IDS(7:0)	Addr. 0x80; bit 7:0	R/W
0x00	IDS addressing data (broadcast to all IDs)	
0x01	IDS addressing data (addressing ID 0)	
0x02	IDS addressing data (addressing ID 1)	
0x04	IDS addressing data (addressing ID 2)	
0x08	IDS addressing data (addressing ID 3)	
0x10	IDS addressing data (addressing ID 4)	
0x20	IDS addressing data (addressing ID 5)	
0x40	IDS addressing data (addressing ID 6)	
0x80	IDS addressing data (addressing ID 7)	
0x03	IDS addressing data (addressing ID 0 and ID 1	
0xFF	IDS addressing data (addressing ID 0 . . . 7)	

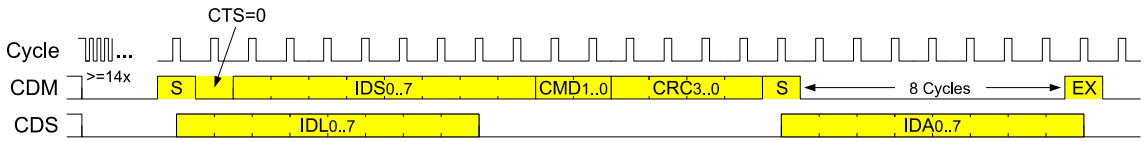
Table 33: IDS command/instruction addressing, combinable

The combination of CMD and IDS result in the total command/instruction. The command/instruction is executed by instruction INSTR = 0b100, b0110 or 0b111.



(S=Start, IDL=ID-Lock, IDS=ID-Select, CMD=Command, EX=Execute)

Figure 17: Command/instruction frame (broadcast)



(S=Start, IDL=ID-Lock, IDS=ID-Select, IDA=ID-Acknowledge, CMD=Command, EX=Execute)

Figure 18: Command/instruction frame (addressed)

INSTRUCTION REGISTER

Data transmission can be started by writing the instruction register, The data transmission is then started automatically with a constant cycle time or by the external pin GETSENS. The CDM bit (end of cycle low or high) is generated by the following table or generated automatically within a running register communication. All bits with the exception of AGS, HOLDBANK and SWBANK are independently deleted by the master once the command has been carried out. All configuration parametera must be stable during data transmission.

The transmission of sensor data can be triggered via INSTR. In both instances a new transmission process is initiated; the difference between the two commands lies in how the transmission cycle is ended. With INSTR = 0b010 the cycle finishes with a CDM = 0.
With INSTR = 0b001 the cycle finishes with a CDM = 1.
A BiSS C register access to a slave can be operated by INSTR = 0b100. A reduced protocol for a shorter BiSS C register access to a slave can be operated by INSTR = 0b111.

INSTR	Addr. 0xF4; bit 3:1	R/W - 000
010	CDM=0	
001	CDM=1	
100, 110	Register communication Condition: CDMTIMEOUT=1	
111	Register communication (reduced protocol) Condition: CDMTIMEOUT=1	

Table 34: SCD control instruction

With AGS = 0 the master starts the data transmission after finishing writing the instruction register (rising edge of NWR). A nAGSERR error will be generated if the SL line is low, TIMEOUTSENS has not exceeded. The error can be inhibited by setting FREQAGS to AGSMIN. If an AGS bit has been set sensor data is read in cyclically according to the cycle frequency set in FREQAGS without any further commands being issued by the controller.

AGS	Addr. 0xF4; bit 0	R/W - 0
0	No automatic data transmission	
1	Start of data transmission after TIMEOUTSENS Condition: FREQAGS = AGSMIN	
1	Start of data transmission triggered by pin Condition: FREQAGS = AGSINFINITE	
1	Start of data transmission after timeout	

Table 35: Automatic Get Sensordata

The sensor chain can be initiated using the command INIT.

INIT	Addr. 0xF4; bit 4	R/W - 0
0	No changes on the data channel	
1	Initialize data channel	

Table 36: Start INIT sequence

All current actions can be aborted using the BREAK command so that a defined state can be resumed if one of the sensors proves faulty, for example.
BREAK = 1 aborts the active data transmission and all status information will be reset.

BREAK	Addr. 0xF4; bit 7	R/W - 0
0	No change	
1	Abort data transmission nSCDERR, nREGER, nDELAYERR, nAGSERR = 1, REGEND = 0	

Table 37: Start BREAK sequence

To stop an AGS operation set the BREAK bit and reset the AGS bit in one instruction into instruction register 0xF4 to stop the running cycle and stop AGS.

During the readout of more than one sensor data register by the controller it is possible that the RAM banks in the master could be swapped over once a sensor data transmission is complete. So that the controller only reads related values bit HOLDBANK should be set at the start of the readout and reset at the end; this suppresses the RAM swap. With the start of a new sensor data cycle previous values are then overwritten by the new sensor data.

HOLDBANK	Addr. 0xF4; bit 6	R/W - 0
0	No bank switching lock permitted	
1	Bank switching lock permitted	

Table 38: RAM bank control

Each setting or deletion of bit SWBANK forces the sensor data banks to be swapped over. Data just input, for example, can then be read out if a cycle has ended during HOLDBANK = 1 (this is indicated by EOT in the status register switching to 1 during the suppression of the RAM swap).

SWBANK	Addr. 0xF4; bit 5	R/W - 0
0	RAM banks are not switched	
1	RAM banks are switched	

Table 39: RAM bank switching

MAFS	Addr. 0xF5; bit 4	R/W
0	Controlling selected(CHSEL) MA clock line: using MA signal	
1	Controlling selected(CHSEL) MA clock line: using MAVS level	

Table 40: Selected MA line control selection

MAVS	Addr. 0xF5; bit 5	R/W
0	Low definition of selected(CHSEL) MA clock lines	
1	High definition of selected(CHSEL) MA clock lines	

Table 41: Selected MA line control level

MAFO	Addr. 0xF5; bit 6	R/W
0	Controlling unselected(CHSEL) MA clock line: using MA signal	
1	Controlling unselected(CHSEL) MA clock line: using MAVS level	

Table 42: Not selected MA line control selection

MAVO	Addr. 0xF5; bit 7	R/W
0	Low definition of unselected(CHSEL) MA clock lines	
1	High definition of unselected(CHSEL) MA clock lines	

Table 43: Not selected MA line control level

CONFIGURATION MASTER

Master Clock MA

The master clock, either generated by the basic clock of the internal 20 MHz oscillator (CLKENI = 1) or by an external clock oscillator (CLKENI = 0) which supplies pin CLK, is set with the aid of the frequency division register FREQ (address 0xE6).

The MA clock frequency for both BiSS and SSI modes is set via FREQ(4:0) in accordance with table 44. With an external clock pulse of f(CLK) = 20 MHz clock frequencies ranging from 62.5 kHz to 10 MHz can thus be selected for sensor data transmission.

FREQS	Addr. 0xE6; bit 4:0	R/W
0x00	f_{CLK}/ 2	
0x01	f_{CLK}/ 4	
0x02	f_{CLK}/ 6	
0x03	f_{CLK}/ 8	
...	...	
0x09	f_{CLK}/ 20	
...	...	
0x0D	f_{CLK}/ 28	
0x0E	f_{CLK}/ 30	
0x0F	f_{CLK}/ 32	
0x10	"not permitted"	
0x11	f_{CLK}/ 40	
0x12	f_{CLK}/ 60	
0x13	f_{CLK}/ 80	
...	...	
0x1D	f_{CLK}/ 280	
0x1E	f_{CLK}/ 300	
0x1F	f_{CLK}/ 320	

Table 44: Sensor data clock frequency

Both BiSS and SSI devices recognize an idle bus at the end of a transmission cycle via a monoflop timeout elapsing (timeoutSENS, see BiSS protocol). The choice of possible clock frequencies is thus limited as the duration of both the high and low level may not exceed the shortest timeout of all of the connected subscribers (slaves).

BiSS B devices switch to register mode when recognizing that the bus is idle after a high-low transition at the clock input and signal this state back to the master on the data line.

The clock frequency in BiSS B register mode is set via parameter FREQ and within a range of 244 Hz to 5 MHz. The selection is also limited as a different monoflop timeout does now recognize the idle bus at the end of the cycle (timeoutREG, see BiSS B protocol).

FREQR	Addr. 0xE6; bit 7:5	R/W
0 . . 7	FreqSens/ (2 * (FREQ(7:5)+1))	
0	FreqSens / 2	
1	FreqSens / 4	
2	FreqSens / 8	
3	FreqSens / 16	
4	FreqSens / 32	
5	FreqSens / 64	
6	FreqSens / 128	
7	FreqSens / 256	

Table 45: BiSS B register data frequency

BiSS B devices typically require a minimum clock frequency (such as 250 kHz) due to the MA clock form has to be evaluated as a possible PWM signal for register communication. BiSS C devices generally permit a lower clock frequency. BiSS C devices do not use the MA clock duty cycle (PWM signal) and can be operated down to 80 kHz. SSI devices generally permit a lower clock frequency and with extended SSI the register ac-

cess is similar to BiSS C and can be operated down to 80 kHz.

The FREQAGS controls the automatic SCD timing. Automatic SCD timings are enabled by the instruction bit AGS. With FREQAGS the cycle rate can be set to a dedicated ratio of the f_{CLK}. For the fastest possible cycle rate FREQAGS is set to AGSMIN. For the cycle rate that is controlled externally by GETSENS, FREQAGS is set to AGSINFINITE.

With an external clock of 20 MHz sensor data request cycles ranging from 1 µs to 4 ms are possible. FREQAGS must be set in a way that the distance between two requests for data is greater than a complete cycle; this consists of the transmission of a request, an acknowledge signal (including any line delays), a start bit (including process times), a register bit (optional), the sensor and CRC bits of each slave and the longest sensor timeout of all the slaves.

FREQAGS	Addr. 0xE8; bit 7:0	R/W
0x00 .. 0x7B	f_{CLK}/ (20 * (FREQAGS(6:0)+1))	
0x7C	AGSMIN	
0x7D .. 0x7F	AGSINFINITE	
0x80 .. 0xFF	f_{CLK}/ (625 * (FREQAGS(6:0)+1))	

Table 46: AutoGetSens frequency

AGSMIN
With AGSMIN the master automatically restarts the next cycle after the prior was finished. AGSMIN is the fastest SCD rate with complete SCD cycles. The rate depends on the configured master clock frequency, the total slave configuration, slaves processing time and the total system line delay.

AGSINFINITE
With AGSINFINITE the master does not automatically restart the next cycle after the prior one was finished. AGSINFINITE requires a trigger event to start the next SCD cycle. Possible trigger events are a GETSENS signal or an INST instruction that start a cycle.

The RAM location for the received and processed CRC bits are the most significant bits each slaves SCDATA.

NOCRC	Addr. 0xE7; bit 1	R/W
0	CRC of SCD is stored RAM (only applicable with active CRC verification and CRC polynome > 0)	
1	CRC of SCD not to be stored in RAM	

Table 47: All Slave CRC RAM copy

The buffering of the received SCD and the access to the SCD can use two or one RAM bank. When using only a single RAM bank, the access to prior SCD needs to be coordinated with a possible update of new SCD.

SINGLEBANK	Addr. 0xE7; bit 1	R/W
0	Two RAM banks are used for SCD	
1	One RAM bank is used for SCD	

Table 48: Usage of single RAM bank for SCD

BiSS Master Device Identification

The BiSS master device is identifiable with the two register VERSION and REVISION. A host software can use VERSION and REVISION to identify the present device and verify the compatibility of software and device.

VERSION	Addr. 0xEB; bit 7:0	R
0x83	iC-MB3	
0x84	iC-MB4	
...	...	
0xFF		

Table 49: iC-MB version

REVISION	Addr. 0xEA; bit 7:0	R
0x10	Z(first revision)	
0x11	Z1	
0x20	Y	
...		
0xFF		

Table 50: iC-MBx redesign ID

The MB100 BiSS IP´s do also provide a version and revision for identification.

VERSION	Addr. 0xEB; bit 7:0	R
0x41	BiSS IP MB101	
...	...	
0x49	BiSS IP MB109	
...	...	
0x82		

Table 51: MB100 version

REVISION	Addr. 0xEA; bit 7:0	R
0x02	Z(first revision)	
0x03	Y	
0x04	Y1	
0x05	X	
...	...	
0xFF		

Table 52: MB100 redesign ID

ENTEST	Addr. 0xF5; bit 1	R/W
0	Device in normal operation mode	

Table 53: Enable device factory test mode

The device factory test may not be activated.

CONFIGURATION CHANNEL

SLAVELOC5	Addr. 0xEC; bit 4	R/W
0	Slaves 5-8 are connected to channel 1	
1	Slaves 5-8 are connected to channel 2*	

Table 54: Slave location

CFGIF	Addr. 0xF5; bit 3:2	R/W
0x00	TTL	
0x01	CMOS	
0x02	RS422* † ‡	
0x03	LVDS* †	

Table 55: Configure physical interface

The configuration of both channels control the type of protocol that is applied by each channel.

CFGCH1	Addr. 0xED; bit 1:0	R/W
CFGCH2*	Addr. 0xED; bit 3:2	R/W
0x00	*BiSS* B	
0x01	*BiSS* C	
0x02	SSI	
0x03	Channel is not used	

Table 56: Channel configuration

In previous MB100 or iC-MB3 data sheets this configuration was applied by the former parameter SELSSI and BISSMOD.

CONFIGURATION SLAVE

ENSCD1	Addr. 0xC0; bit 6	R/W
ENSCD2	Addr. 0xC4; bit 6	R/W
ENSCD3	Addr. 0xC8; bit 6	R/W
ENSCD4	Addr. 0xCC; bit 6	R/W
ENSCD5	Addr. 0xD0; bit 6	R/W
ENSCD6	Addr. 0xD4; bit 6	R/W
ENSCD7	Addr. 0xD8; bit 6	R/W
ENSCD8	Addr. 0xDC; bit 6	R/W
0	Single cycle data not available	
1	Single cycle data available	

Table 57: Enable SCDx

SCDLEN1	Addr. 0xC0; bit 5:0	R/W
SCDLEN2	Addr. 0xC4; bit 5:0	R/W
SCDLEN3	Addr. 0xC8; bit 5:0	R/W
SCDLEN4	Addr. 0xCC; bit 5:0	R/W
SCDLEN5	Addr. 0xD0; bit 5:0	R/W
SCDLEN6	Addr. 0xD4; bit 5:0	R/W
SCDLEN7	Addr. 0xD8; bit 5:0	R/W
SCDLEN8	Addr. 0xDC; bit 5:0	R/W
0	Single cycle data length = 1	
1	Single cycle data length = 2	
2	Single cycle data length = 3	
...	Single cycle data length = SCDLENx +1	
62	Single cycle data length = 63	
63	Single cycle data length = 64	

Table 58: Length of SCDx (-1)

GRAYS1	Addr. 0xC0; bit 7	R/W
GRAYS2	Addr. 0xC4; bit 7	R/W
GRAYS3	Addr. 0xC8; bit 7	R/W
GRAYS4	Addr. 0xCC; bit 7	R/W
GRAYS5	Addr. 0xD0; bit 7	R/W
GRAYS6	Addr. 0xD4; bit 7	R/W
GRAYS7	Addr. 0xD8; bit 7	R/W
GRAYS8	Addr. 0xDC; bit 7	R/W
0	SSI single cycle data binary coded	
1	SSI single cycle data gray coded	

Table 59: SSI format is Gray code

LSTOP1	Addr. 0xC0; bit 7	R/W
LSTOP2	Addr. 0xC4; bit 7	R/W
LSTOP3	Addr. 0xC8; bit 7	R/W
LSTOP4	Addr. 0xCC; bit 7	R/W
LSTOP5	Addr. 0xD0; bit 7	R/W
LSTOP6	Addr. 0xD4; bit 7	R/W
LSTOP7	Addr. 0xD8; bit 7	R/W
LSTOP8	Addr. 0xDC; bit 7	R/W
0	No leading STOP bit on single cycle actuator data	
1	Leading STOP bit on single cycle actuator data	

Table 60: Actuator stop bit control

* The second BiSS interface channel 2 is only available with iC-MB4 QFN28.
† RS422 and LVDS interfaces are only available with iC-MB4 QFN28.
‡ RS422 interfaces are only operatable with VDD = 4.5 V ... 5.5 V

SELCRCS1	Addr. 0xC1; bit 7	R/W
SELCRCS2	Addr. 0xC5; bit 7	R/W
SELCRCS3	Addr. 0xC9; bit 7	R/W
SELCRCS4	Addr. 0xCD; bit 7	R/W
SELCRCS5	Addr. 0xD1; bit 7	R/W
SELCRCS6	Addr. 0xD5; bit 7	R/W
SELCRCS7	Addr. 0xD9; bit 7	R/W
SELCRCS8	Addr. 0xDD; bit 7	R/W

0	CRC bit length in SCRCLENx apply dedicated CRC polynomials
1	CRC polynomial(7:1) in SCRCPOLYx SELCRCSx = 0b1 not applicable with CRC polynomial SCRCPOLYx(7:1) = 0x00

Table 61: CRC polynomial selection

SCRCLEN1(6:0)	Addr. 0xC1; bit 6:0	R/W
SCRCLEN2(6:0)	Addr. 0xC5; bit 6:0	R/W
SCRCLEN3(6:0)	Addr. 0xC9; bit 6:0	R/W
SCRCLEN4(6:0)	Addr. 0xCD; bit 6:0	R/W
SCRCLEN5(6:0)	Addr. 0xD1; bit 6:0	R/W
SCRCLEN6(6:0)	Addr. 0xD5; bit 6:0	R/W
SCRCLEN7(6:0)	Addr. 0xD9; bit 6:0	R/W
SCRCLEN8(6:0)	Addr. 0xDD; bit 6:0	R/W

0	CRC for single cycle data not present, CRC verification deactivated, SELCRCSx = 0b0
3	CRC polynomial 0b1011 = 0xB
4	CRC polynomial 0b1.0011 = 0x13
5	CRC polynomial 0b10.0101 = 0x25
6	CRC polynomial 0b100.0011 = 0x43
7	CRC polynomial 0b1000.1001 = 0x89
8	CRC polynomial 0b1.0010.1111 = 0x12F
16	CRC polynomial 0b1.1001.0000.1101.1001 = 0x190D9
. . .	Other CRC lengths in SCRCLENx are not permitted with SELCRCSx = 0b0 .

Table 62: CRC length with predefined CRC polynomial

SCRCPOLY1(7:1)	Addr. 0xC1; bit 6:0	R/W
SCRCPOLY2(7:1)	Addr. 0xC5; bit 6:0	R/W
SCRCPOLY3(7:1)	Addr. 0xC9; bit 6:0	R/W
SCRCPOLY4(7:1)	Addr. 0xCD; bit 6:0	R/W
SCRCPOLY5(7:1)	Addr. 0xD1; bit 6:0	R/W
SCRCPOLY6(7:1)	Addr. 0xD5; bit 6:0	R/W
SCRCPOLY7(7:1)	Addr. 0xD9; bit 6:0	R/W
SCRCPOLY8(7:1)	Addr. 0xDD; bit 6:0	R/W

0x00	CRC polynomial 0x00 not applicable with SELCRCSx = 0b1
0x01 . . 0x7F	CRC polynomial for single cycle data = SCRCPOLYx(7:1) + '0x01'

Table 63: CRC polynomial(n:1)

SCRCSTART1(7:0)	Addr. 0xC2; bit 7:0	R/W
SCRCSTART1(15:8)	Addr. 0xC3; bit 7:0	R/W
SCRCSTART2(7:0)	Addr. 0xC6; bit 7:0	R/W
SCRCSTART2(15:8)	Addr. 0xC7; bit 7:0	R/W
SCRCSTART3(7:0)	Addr. 0xCA; bit 7:0	R/W
SCRCSTART3(15:8)	Addr. 0xCB; bit 7:0	R/W
SCRCSTART4(7:0)	Addr. 0xCE; bit 7:0	R/W
SCRCSTART4(15:8)	Addr. 0xCF; bit 7:0	R/W
SCRCSTART5(7:0)	Addr. 0xD2; bit 7:0	R/W
SCRCSTART5(15:8)	Addr. 0xD3; bit 7:0	R/W
SCRCSTART6(7:0)	Addr. 0xD6; bit 7:0	R/W
SCRCSTART6(15:8)	Addr. 0xD7; bit 7:0	R/W
SCRCSTART7(7:0)	Addr. 0xDA; bit 7:0	R/W
SCRCSTART7(15:8)	Addr. 0xDB; bit 7:0	R/W
SCRCSTART8(7:0)	Addr. 0xDE; bit 7:0	R/W
SCRCSTART8(15:8)	Addr. 0xDF; bit 7:0	R/W

Table 64: CRC calculation start value

The CRC start value does affect the CRC result. The CRC start value can be used to safely differentiate between two SCD data words e.g. two position words provided by two different sensors. The same CRC start value that is used in the sensor needs to be applied in the master to check the received single cycle data. A typical default slave CRC start value is 0x0000.

iC-MB4 can read sensors and control actuators. The ACTnSENS parameter defines the functionality of each BiSS slave on the BiSS bus.

ACTnSENS	Addr. 0xEF; bit 7:0	R/W
0x00	All slaves are sensors	
0x01	Slave 1 is actuator	
0x02	Slave 2 is actuator	
0x04	Slave 3 is actuator	
0x08	Slave 4 is actuator	
0x10	Slave 5 is actuator	
0x20	Slave 6 is actuator	
0x40	Slave 7 is actuator	
0x80	Slave 8 is actuator	
0xFF	All slaves are actuators	

Table 65: Slave functionality control

Actuator control requires the MO signal.

STATUS INFORMATION 1

In sensor mode the validity of data is stored separately for each slave in the validity message register. In the event of error the appropriate validity message is deleted and nSENSERR set to 0 in the status register. The error is signaled at pin NER.

EOT	Addr. 0xF0; bit 0	R - 1
0	Data transmission active	
1	Data transmission finished	

Table 66: End of transmission

In register mode a register error (nREGERR = 0) or a slave start signal missed at least 4096 MA1 clock pulses results in an error message at NER.

REGEND	Addr. 0xF0; bit 2	R - 0
0	No valid register data available	
1	Register data transmission completed	

Table 67: End of register communication

A register watchdog error is also triggered if a slave response is lacking during the transmission of register data. This has two possible causes: either a slave does not respond to the first falling edge with a low or the slave fails to generate a start bit.

nREGERR	Addr. 0xF0; bit 3	R - 1
0	Error in last register data transmission	
1	No error in last register data transmission	

Table 68: Register communication error

The nREGERR bit is reset by writing BREAK = 1 into instruction register 0xF4 or writing INIT = 1 into instruction register 0xF4. If a register data error is generated the number of bytes transmitted correctly before the error occurred can be determined by reading out the register message REGBYTES (address 0xF3, bits 5...0). In the event of error the transmission of data is terminated.

If a sensor data error is signaled the faulty sensor can be verified by reading out address 0xF1 (validity message).

nSCDERR	Addr. 0xF0; bit 4	R - 1
0	Error in last single cycle data transmission	
1	No error in last single cycle data transmission	

Table 69: SCD transmission error

The nSCDERR bit is reset by writing BREAK = 1 into instruction register 0xF4.

An AGS watchdog error nAGSERR is set during the automatic transmission of sensor data if no new cycle could be initiated; bit AGS in the command register is reset and the automatic request for sensor data aborted. During the transmission of register data a watchdog error is triggered if the slave shows no response, i.e. if it does not answer the first falling master edge with a low or fails to generate a start bit.

nAGSERR	Addr. 0xF0; bit 6	R - 1
0	AGS watchdog error	
1	No AGS watchdog error	

Table 70: AGS error

The nAGSERR bit is reset by writing into instruction register 0xF4. Typically a BREAK=1 and AGS=0 instruction is written into register 0xF4.

It is possible to connect other components to pin NER which can also generate an error message; this can then be read out via bit nERR in the status register.

nERR	Addr. 0xF0; bit 7	R - 1
0	Error	
1	No error	

Table 71: Transmission error

nDELAYERR	Addr. 0xF0; bit 5	R - 1
0	Delay error	
1	No Delay error	

Table 72: Delay error

The SVALIDx bit indicates the validity of each slaves SCD CRC verification. A prior set SVALIDx bit can be reset by writing 0 into the register.

SVALID1	Addr. 0xF1;	bit 1	R/W - 0
SVALID2	Addr. 0xF1;	bit 3	R/W - 0
SVALID3	Addr. 0xF1;	bit 5	R/W - 0
SVALID4	Addr. 0xF1;	bit 7	R/W - 0
SVALID5	Addr. 0xF2;	bit 1	R/W - 0
SVALID6	Addr. 0xF2;	bit 3	R/W - 0
SVALID7	Addr. 0xF2;	bit 5	R/W - 0
SVALID8	Addr. 0xF2;	bit 7	R/W - 0
0	SCD invalid		
1	SCD valid		

Table 73: SCDATAx validity indication

With BiSS C register communication the count of SCD cycles with CDM = 0 is relevant for a manual register communication by host control. Therefore the CDM-TIMEOUT bit indicates that $\geq$ 14 SCD cycles with CDM = 0 have been sent before.

CDMTIMEOUT (Register vaild)	Addr. 0xF3; bit 7	R - 1
0	CDMTIMEOUT not reached	
1	CDMTIMEOUT reached	

Table 74: CDM timeout reached

CDSSEL	Addr. 0xF3; bit 6	R - 1
	CDS from the selected channel	

Table 75: CDS bit from the selected channel

STATUS INFORMATION 2

SL1	Addr. 0xF8;	bit 0	R - 1
SL2	Addr. 0xF8;	bit 2	R - 1
SL3*	Addr. 0xF8;	bit 4	R - 1
SL4*	Addr. 0xF8;	bit 6	R - 1
SL5*	Addr. 0xF9;	bit 0	R - 1
SL6*	Addr. 0xF9;	bit 2	R - 1
SL7*	Addr. 0xF9;	bit 4	R - 1
SL8*	Addr. 0xF9;	bit 6	R - 1
0	SL line level low		
1	SL line level high		

Table 76: SL input line state

CDS1	Addr. 0xF8;	bit 1	R - 1
CDS2	Addr. 0xF8;	bit 3	R - 1
CDS3†	Addr. 0xF8;	bit 5	R - 1
CDS4†	Addr. 0xF8;	bit 7	R - 1
CDS5†	Addr. 0xF9;	bit 1	R - 1
CDS6†	Addr. 0xF9;	bit 3	R - 1
CDS7†	Addr. 0xF9;	bit 5	R - 1
CDS8†	Addr. 0xF9;	bit 7	R - 1
0	CDS = 0		
1	CDS = 1		

Table 77: CDS bit of channel

SWBANKFAILS Bank switching SCD not successful	Addr. 0xFB; bit 0	R - 1
0	Bank switching (SCD) successful	
1	Bank switching (SCD) not successful	

Table 78: Bank switching status

* SL3 . . . SL8 are not available with iC-MB4.
† CDS3 . . . CDS8 are not available with iC-MB4.

APPLICATION DESIGN TRANSFER FROM iC-MB3 TSSOP24 TO iC-MB4 TSSOP24

In order to transfer iC-MB3 TSSOP24 applications to iC-MB4 applications the following items need to be verified:

- Related details on PCB
- Configurations
- Operational sequences

Pin compatibility

As both devices are register and pin compatible* the iC-MB4 TSSOP24 is a drop in replacement possibility to iC-MB3 TSSOP24.

All pins keep their function except one pin that typically was not used by former iC-MB3 TSSOP24 users:

- iC-MB3 TSSOP24:
  pin 22: CLKOUT clock output
- iC-MB4 TSSOP24:
  pin 22: MO1 BiSS data line output

The internal oscillator of the iC-MB3 TSSOP24 is typically not used as a clock source. With the updated MB100_X BiSS master IP the control of the MO line is possible with iC-MB3 TSSOP24. As most of on the market available encoder are point-to-point encoder the signal MO is such applications not required. The parameter "EN_MO" in address 0xE5; bit 1 controls the level:

- 0 MO to low
- 1 parameterized processing time by master on MO signal active (length: MO_BUSY).

In typical point-to-point applications there is no MO at the sensor required/used and the sensors SLI = 0 (often constant level inside sensor) = MO (if required and connected).

BiSS C register access functionality

The iC-MB3 TSSOP24 can only perform BiSS B register access with the REGADR, REGNUM, ... , not BiSS C. To perform BiSS C register access a sequence of CDM bits for the register access is needed (read or write) and with the appropriate command (GETSENS0 or GETSENS1) the SCD cycle is triggered, the CDS bit of this cycle is captured and the CDM bit is output on the MA line (please check BiSS AN 4). iC-MB3 TSSOP24 with host support support is also BiSS C capable and designs on iC-MB3 TSSOP24 can be upgraded with iC-MB4 TSSOP24. iC-MB4 is full BiSS B and BiSS C register access capable.

Differing operational sequences on BiSS B and BiSS C register access

The operational sequence to perform a BiSS B register access differs to the operational sequence to perform a BiSS C register access. On BiSS B the SCD transfer was stopped and the BiSS B register access was executed. With BiSS C the SCD transfer is required to perform the BiSS C register access. Adaptions of an existing BiSS B register access the operational sequence for BiSS C register access need to be verified.

Disabeling SCD CRC verification

To deactivate the SCD CRC verification select:

- SELCRCSx = 0b0
- CRC bit length in SCRCLENx = 0 .
- Extend the SCDLEN by the length of the present CRC that is subject to be ignored.

A CRC polynome SCRCPOLYx = 0x00 is not applicable with SELCRCSx = 0b1.

Obsolete MCD functions removed

Multi Cycle Data (MCD) functions have completely been removed in iC-MB4 TSSOP24. This covers functions, parameters, data and status. Former iC-MB3 TSSOP24 configurations and operational sequences that applied MCD need to be verified, removed or adapted.

* Not using CLKOUT as a clock source within application.

DESIGN REVIEW

Function Notes

iC-MB4 Z1		
No.	Function, Parameter/Code	Description and Application Notes
1	**MO_BUSY**	Control communication max fail, if MO_BUSY /= 0 and output MO is **not** connected to slave input SLI.
2	**Actuatordata**	Transmission of actuatordata on both channels with different length fail, if CDM = 0.
3	**BiSS C Init Sequence**	Line delay measurement fails, if line delay of one channel is bigger than line delay plus timeout of the other channel.

Table 79: Notes on chip functions regarding iC-MB4 chip release Z1.

All listed Chip functions are adjusted with iC-MB4 chip release Y.

REVISION HISTORY

Rel.	Rel. Date	Chapter	Modification	Page
A1	14-06-24		Initial Release.	

Rel.	Rel. Date	Chapter	Modification	Page
B1	14-11-20	PACKAGING INFORMATION	Function text on pin 25 NWR_E swapped with Function text on pin 26 NRD_RNW: • NWR_E: Read Input, active low (Intel) Read/Not-Write Select Input (Motorola). • NRD_RNW: Write Input, active low (Intel) Enable Input, active high (Motorola).	4
		ELECTRICAL CHARACTERISTICS	Vc()hi Clamp Voltage hi MAX updated from 1.65 V to 1.75 V	8
		ELECTRICAL CHARACTERISTICS	f(CLKI) Oscillator Clock Frequency VDD = 3.0 V ... 3.6 V MAX updated from 20 MHz to 22 MHz	9
		FUNCTIONAL DESCRIPTION	INIT = 1 updated.	21
		INSTRUCTION REGISTER	"All configuration parametera must be stable during data transmission" added.	28
		CONFIGURATION MASTER	AUTOMATIC REQUEST FOR SENSOR DATA moved into chapter CONFIGURATION MASTER	29
		CONFIGURATION CHANNEL	CFGIF footnote added: RS422 interfaces are only operatable with VDD = 4.5 V ... 5.5 V	31
		CONFIGURATION SLAVE	Slave Configuration CRC Verification: • CRC for single cycle data not present, CRC verification deactivated, SELCRCSx = 0b0. • CRC polynomial(7:1) in SCRCPOLYx SELCRCSx = 0b1 not applicable with CRC polynomial SCRCPOLYx(7:1) = 0x00. • CRC polynomial 0x00 not applicable with SELCRCSx = 0b1. • Other CRC lengths in SCRCLENx are not permitted with SELCRCSx = 0b0.	32
		STATUS INFORMATION 1	Bit address of nDELAYERR 0xF0 updated to 5	35
		APPLICATION DESIGN TRANSFER FROM iC-MB3 TSSOP24 TO iC-MB4 TSSOP24	Disabeling SCD CRC verification To deactivate the SCD CRC verification select: • SELCRCSx = 0b0 • CRC bit length in SCRCLENx = 0 . • Extend the SCDLEN by the length of the present CRC that is subject to be ignored. A CRC polynomial SCRCPOLYx = 0x00 is not applicable with SELCRCSx = 0b1.	38
		DESIGN REVIEW	Chapter DESIGN REVIEW added.	39
		FUNCTIONAL DESCRIPTION	Measuring the Line Delay on channel 1 and channe l, measuring unit added	21

Rel.	Rel. Date	Chapter	Modification	Page
B2	2015-07-07	DESCRIPTION	BiSS BUA added	2
		FUNCTIONAL DESCRIPTION	Maximum line delay while INIT = 255, overflow abort and AGERR is set	21
		INSTRUCTION REGISTER	All configuration parameter must be stable during SCD data transmission	28

ORDERING INFORMATION

Type	Package	Order Designation
iC-MB4	TSSOP24	iC-MB4 TSSOP24
iC-MB4	QFN28-5x5	iC-MB4 QFN28-5x5
Evaluation Board		iC-MB4 EVAL MB4_1D

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