Product Specification

PE97240

Radiation Tolerant UltraCMOS® Integer-N Frequency Synthesizer for Low Phase Noise Applications

Features

- Frequency range
  - 5 GHz in 10/11 prescaler modulus
  - 4 GHz in 5/6 prescaler modulus
- Phase noise floor figure of merit: –230 dBc/Hz
- Low power: 75 mA @ 2.7V
- Serial or direct mode access
- Packaged in a 44-lead CQFP
- 100 kRad(Si) total dose

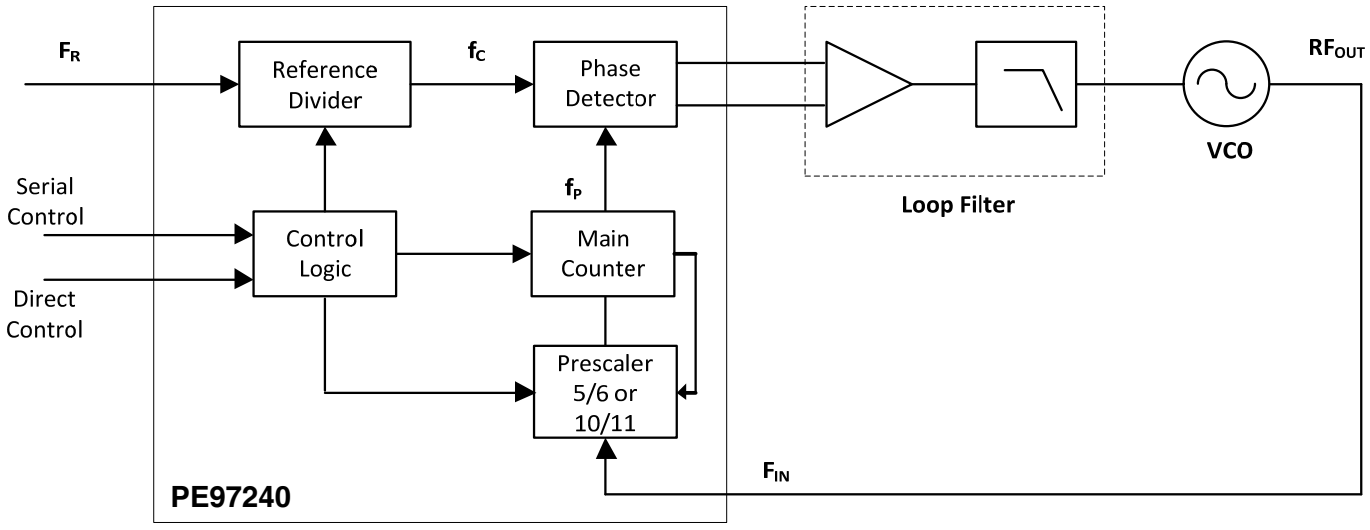
Product Description

Peregrine's PE97240 is a radiation tolerant high-performance Integer-N PLL capable of frequency synthesis up to 5 GHz. The device is designed for commercial space applications and optimized for superior phase noise performance.

The PE97240 features a selectable prescaler modulus of 5/6 or 10/11, counters and a phase comparator as shown in *Figure 1*. Counter values are programmable through either a serial interface or directly hard-wired.

The PE97240 is available in a 44-lead CQFP and is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering excellent RF performance and intrinsic radiation tolerance.

Figure 1. Functional Diagram



©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

Figure 2. Pin Configurations (Top View)

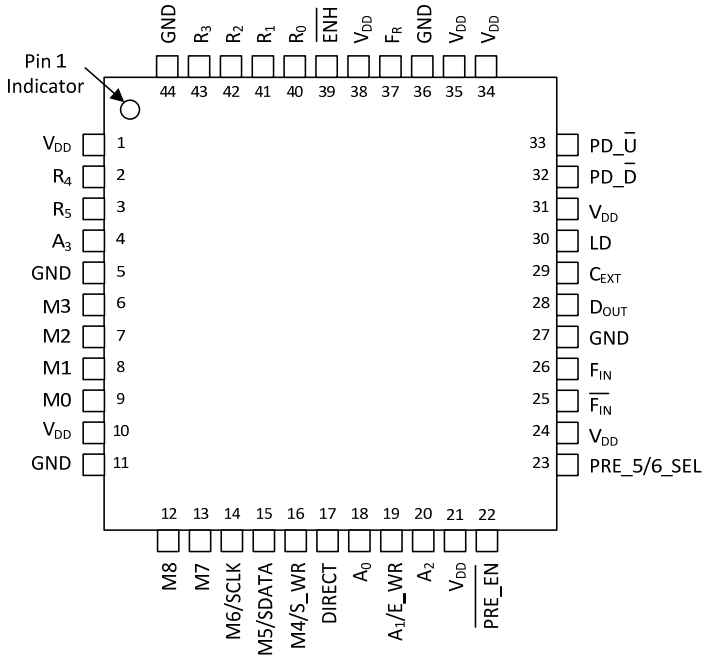


Figure 3. Package Type

44-lead CQFP

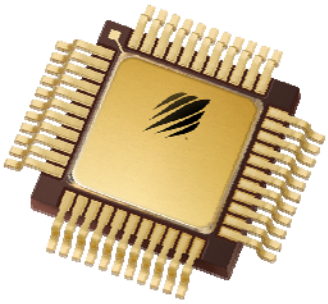


Table 1. Pin Descriptions

Pin #	Pin Name	Interface Mode	Type	Description
1	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.6–2.8V. Bypassing recommended.
2	R4	Direct	Input	R counter bit4
3	R5	Direct	Input	R counter bit5
4	A3	Direct	Input	A counter bit3
5	GND	Both		Ground
6	M3	Direct	Input	M counter bit3
7	M2	Direct	Input	M counter bit2
8	M1	Direct	Input	M counter bit1
9	M0	Direct	Input	M counter bit0
10	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.6–2.8V. Bypassing recommended.
11	GND	Both		Ground
12	M8	Direct	Input	M counter bit8
13	M7	Direct	Input	M counter bit7
14	SCLK	Serial	Input	Serial clock input. SDATA is clocked serially into the 21-bit primary register (E_WR “low”) or the 8-bit enhancement register (E_WR “high”) on the rising edge of SCLK.
	M6	Direct	Input	M counter bit6
15	SDATA	Serial	Input	Binary serial data input. Input data entered MSB first.
	M5	Direct	Input	M counter bit5
16	S_WR	Serial	Input	Serial load enable input. While S_WR is “low”, SDATA can be serially clocked. Primary register data is transferred to the secondary register on S_WR or Hop_WR rising edge.
	M4	Direct	Input	M counter bit4

©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

Table 1. Pin Descriptions (continued)

Pin No.	Pin Name	Interface Mode	Type	Description
17	Direct	Direct	Input	Select “High” enables Direct Mode. Select “Low” enables Serial Mode.
18	A0	Direct	Input	A counter bit0
19	A1	Direct	Input	A counter bit1
	E_WR	Serial	Input	Enhancement register write enable. While E_WR is “high”, SDATA can be serially clocked into the enhancement register on the rising edge of SCLK.
20	A2	Direct	Input	A counter bit2
21	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.6–2.8V. Bypassing recommended.
22	$\overline{Pre_en}$	Direct	Input	Prescaler enable, active “low”. When “high”, F_{IN} bypasses the prescaler.
23	Pre_5/6_Sel	Direct	Input	5/6 modulus select, active “High.” When “Low,” 10/11 modulus selected.
24	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.6–2.8V. Bypassing recommended.
25	$\overline{F_{IN}}$	Both	Input	Prescaler complementary input. A 22 pF bypass capacitor should be placed as close as possible to this pin and be connected in series with a 50Ω resistor to ground.
26	F_{IN}	Both	Input	Prescaler input from the VCO, 5.0 GHz max frequency. A 22 pF coupling capacitor should be placed as close as possible to this pin and be connected in shunt to a 50Ω resistor to ground.
27	GND	Both		Ground
28	D_{OUT}	Serial	Output	Data Out. The MSEL signal and the raw prescaler output are available on Dout through enhancement register programming.
29	C_{EXT}	Both	Output	Logical “NAND” of PD_$\overline{D}$ and PD_$\overline{U}$ terminated through an on chip, 2 kΩ series resistor. Connecting Cext to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD.
30	LD	Both	Output	Lock detect and open drain logical inversion of C_{EXT}. When the loop is in lock, LD is high impedance, otherwise LD is a logic low (“0”).
31	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.6V to 2.8V. Bypassing recommended.
32	PD_$\overline{D}$	Both	Output	PD_$\overline{D}$ is pulse down when f_p leads f_c
33	PD_$\overline{U}$	Both	Output	PD_$\overline{U}$ is pulse down when f_c leads f_p
34	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.6–2.8V. Bypassing recommended.
35	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.6–2.8V. Bypassing recommended.
36	GND	Both		Ground
37	F_R	Both	Input	Reference frequency input
38	V_{DD}	Both	Note 1	Power supply input. Input may range from 2.6–2.8V. Bypassing recommended.
39	$\overline{ENH}$	Serial	Input	Enhancement mode. When asserted low (“0”), enhancement register bits are functional.
40	R0	Direct	Input	R counter bit0
41	R1	Direct	Input	R counter bit1
42	R2	Direct	Input	R counter bit2
43	R3	Direct	Input	R counter bit3
44	GND	Both		Ground

Notes: 1. V_{DD} pins 1, 10, 21, 24, 31, 34, 35 and 38 are connected by diodes and must be supplied with the same positive voltage level.
2. All digital input pins have 70 kΩ pull-down resistors to ground.

©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

Table 2. Operating Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	2.6	2.8	V
Operating ambient temperature range	T_A	–40	+85	°C

Table 3. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	–0.3	3.3	V
Voltage on any input	V_I	–0.3	V_{DD} + 0.3	V
DC into any input	I_I	–10	+10	mA
DC into any output	I_O	–10	+10	mA
RF input power, CW 50 MHz–5 GHz	P_{MAX_CW}		10	dBm
Thermal resistance	T_{JC}		33.4	°C/W
Junction temperature	T_J		+125	°C
Storage temperature range	T_{ST}	–65	+150	°C
ESD voltage HBM[1] All pins except pin 28	V_{ESD_HBM}		1000	V
ESD voltage HBM[1,2] On pin 28			300	V

Notes: 1. Human Body Model (MIL-STD-883 Method 3015).
2. Pin 28 is not used in normal operation.

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-Up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

ELDRS

UltraCMOS devices do not include bipolar minority carrier elements, and therefore do not exhibit enhanced low dose rate sensitivity.

Table 4. Single Event Effects[1]

SEE Mode	Effective Linear Energy Transfer (LET)[2]
SEL	86 MeV•cm^2/mg
SEFI	86 MeV•cm^2/mg
SEU	86 MeV•cm^2/mg
SET	30 MeV•cm^2/mg [3]

Notes: 1. Testing performed using serial programming mode.
2. SEE testing was conducted with Au, Ho, Xe, Kr, Cu ion species at 0° incidence.
3. Minor transients (phase errors) observed resulting in self-recovering operation without intervention.

©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

Table 5. DC Characteristics @ V_{DD} = 2.7V, –40 °C < T_A < +85 °C, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD}	Operational supply current	Prescaler disabled, f_C = 50 MHz, F_{IN} = 500 MHz V_{DD} = 2.6–2.8V		34	50	mA
		5/6 prescaler, f_C = 50 MHz, F_{IN} = 3 GHz V_{DD} = 2.6–2.8V		72	105	mA
		10/11 prescaler, f_C = 50 MHz, F_{IN} = 3 GHz V_{DD} = 2.6–2.8V		74	110	mA
Digital Inputs: All except F_R, F_{IN}, $\overline{F_{IN}}$						
V_{IH}	High level input voltage	V_{DD} = 2.6–2.8V	0.7 x V_{DD}			V
V_{IL}	Low level input voltage	V_{DD} = 2.6–2.8V			0.3 x V_{DD}	V
I_{IH}	High level input current	V_{IH} = V_{DD} = 2.8V			70	µA
I_{IL}	Low level input current	V_{IL} = 0, V_{DD} = 2.8V	–10			µA
Reference Divider input: F_R						
I_{IHR}	High level input current	V_{IH} = V_{DD} = 2.8V			300	µA
I_{ILR}	Low level input current	V_{IL} = 0, V_{DD} = 2.8V	–300			µA
Counter and phase detector outputs: PD_$\overline{D}$, PD_$\overline{U}$						
V_{OLD}	Output voltage LOW	I_{out} = 6 mA			0.4	V
V_{OHD}	Output voltage HIGH	I_{out} = –3 mA	V_{DD} – 0.4			V
Lock detect outputs: C_{EXT}, LD						
V_{OLC}	Output voltage LOW, C_{EXT}	I_{out} = 100 µA			0.4	V
V_{OHC}	Output voltage HIGH, C_{EXT}	I_{out} = –100 µA	V_{DD} – 0.4			V
V_{OLLD}	Output voltage LOW, LD	I_{out} = 1 mA			0.4	V

©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

Table 6. AC Characteristics @ V_{DD} = 2.7V, –40 °C < T_A < +85 °C, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Control interface and latches (see *Figures 16* and *17*)[1]						
f_{Clk}	Serial data clock frequency[2]				10	MHz
t_{ClkH}	Serial clock HIGH time		30			ns
t_{ClkL}	Serial clock LOW time		30			ns
t_{DSU}	SDATA set-up time after SCLK rising edge		10			ns
t_{DHLD}	SDATA hold time after SCLK rising edge		10			ns
t_{PW}	S_WR pulse width		30			ns
t_{CWR}	SCLK rising edge to S_WR rising edge		30			ns
t_{CE}	SCLK falling edge to E_WR transition		30			ns
t_{WRC}	S_WR falling edge to SCLK rising edge		30			ns
t_{EC}	E_WR transition to SCLK rising edge		30			ns
Main divider 5/6 (including prescaler)						
F_{IN}	Operating frequency		800		4000	MHz
P_{F_IN}	Input level range	External AC coupling 800 MHz–4 GHz	–5[3]		7	dBm
Main divider 10/11 (including prescaler)						
F_{IN}	Operating frequency		800		5000	MHz
P_{F_IN}	Input level range	External AC coupling 800 MHz–<4 GHz 4–5 GHz	–5[3] 2		7 7	dBm dBm
Main divider (prescaler bypassed)						
F_{IN}	Operating frequency		50		800	MHz
P_{F_IN}	Input level range	External AC coupling	–5[3]		7	dBm
Reference divider						
F_R	Operating frequency				100	MHz
P_{F_R}	Reference input power[4]	Single-ended input	–5[5]		7	dBm
Phase detector						
f_c	Comparison frequency				100	MHz

©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

Table 6. AC Characteristics @ V_{DD} = 2.7V, –40 °C < T_A < +85 °C, unless otherwise specified (continued)

Symbol	Parameter	Condition	Min	Typical	Max	Unit
SSB phase noise 5/6 prescaler (F_{IN} = 3 GHz, P_{F_R} = +5 dBm, f_C = 50 MHz, LBW = 500 kHz)						
Φ_N	Phase noise	100 Hz offset		–100	–92	dBc/Hz
Φ_N	Phase noise	1 kHz offset		–109	–103	dBc/Hz
Φ_N	Phase noise	10 kHz offset		–116	–110	dBc/Hz
Φ_N	Phase noise	100 kHz offset		–118	–115	dBc/Hz
SSB phase noise 10/11 prescaler (F_{IN} = 3 GHz, P_{F_R} = +5 dBm, f_C = 50 MHz, LBW = 500 kHz)						
Φ_N	Phase noise	100 Hz offset		–98	–91	dBc/Hz
Φ_N	Phase noise	1 kHz offset		–104	–98	dBc/Hz
Φ_N	Phase noise	10 kHz offset		–111	–107	dBc/Hz
Φ_N	Phase noise	100 kHz offset		–117	–113	dBc/Hz
Phase noise figure of merit (FOM)[6]						
$FOM_{flicker}$	Flicker figure of merit	5/6 prescaler		–268	–265	dBc/Hz
		10/11 prescaler		–263	–259	dBc/Hz
FOM_{floor}	Floor figure of merit	5/6 prescaler		–230	–227	dBc/Hz
		10/11 prescaler		–229	–225	dBc/Hz
$FOM_{flicker}$	$PN_{flicker} = FOM_{flicker} + 20\log(F_{IN}) - 10\log(f_{offset})$					dBc/Hz
FOM_{floor}	$PN_{floor} = FOM_{floor} + 10\log(f_c) + 20\log(F_{IN}/f_c)$					dBc/Hz
FOM_{total}	$PN_{total} = 10\log(10\,[PN_{flicker}/10] + 10\,[PN_{floor}/10])$					dBc/Hz

Notes: 1. Timing parameters are guaranteed through design characterization and not tested in production.
2. f_{clk} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify f_{clk} specification.
3. 0 dBm minimum is recommended for improved phase noise performance when sine-wave is applied.
4. CMOS logic levels can be used to drive the reference input. If the V_{DD} of the CMOS driver matches the V_{DD} of the PLL IC, then the reference input can be DC coupled. Otherwise, the reference input should be AC coupled. For sine-wave inputs, the minimum amplitude needs to be 0.5 V_{PP}. The maximum level should be limited to prevent ESD diodes at the pin input from turning on. Diodes will turn on at one forward-bias diode drop above V_{DD} or below GND. The DC voltage at the Reference input is $V_{DD}/2$.
5. +2 dBm or higher is recommended for improved phase noise performance.
6. The phase noise can be separated into two normalized specifications: a floor figure of merit and a flicker figure of merit. To accurately measure the phase noise floor without the contribution of the flicker noise, the loop bandwidth is set to 500 kHz and the phase noise is measured at a frequency offset near 100 kHz. The flicker noise is measured at a frequency offset ≤ 1000 Hz. The formula assumes a –10 dB/decade slope versus frequency offset.

©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

Figure 4. Equivalent Input Diagram: Digital Input

Digital Input

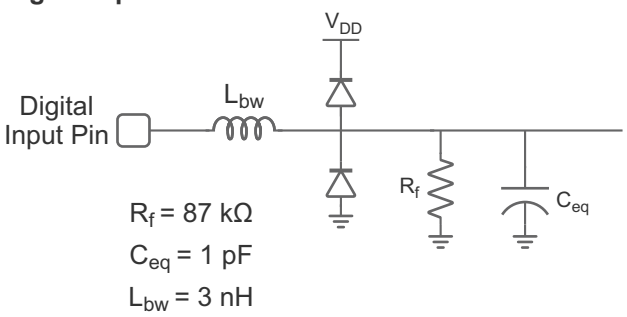


Figure 5. Equivalent Input Diagram: Reference Input

Reference Input

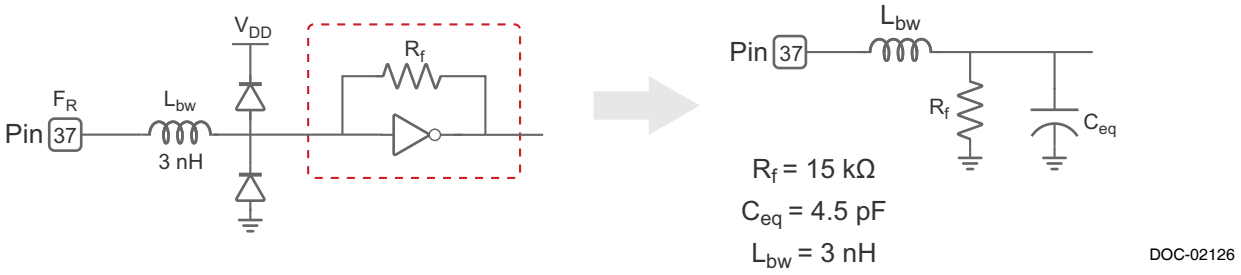
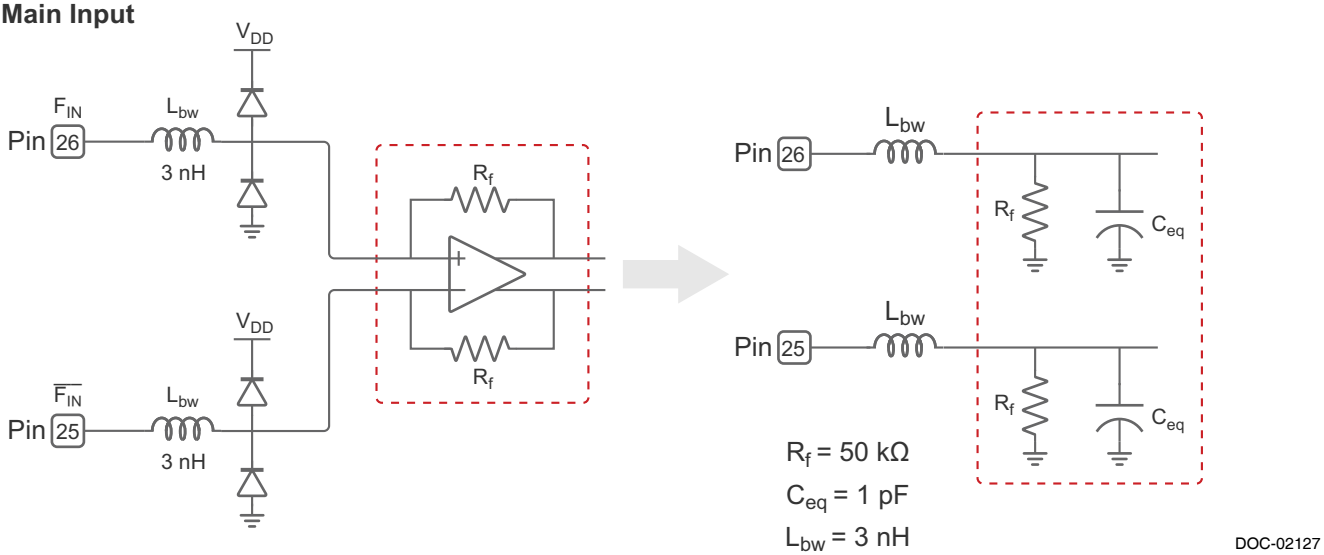


Figure 6. Equivalent Input Diagram: Main Input

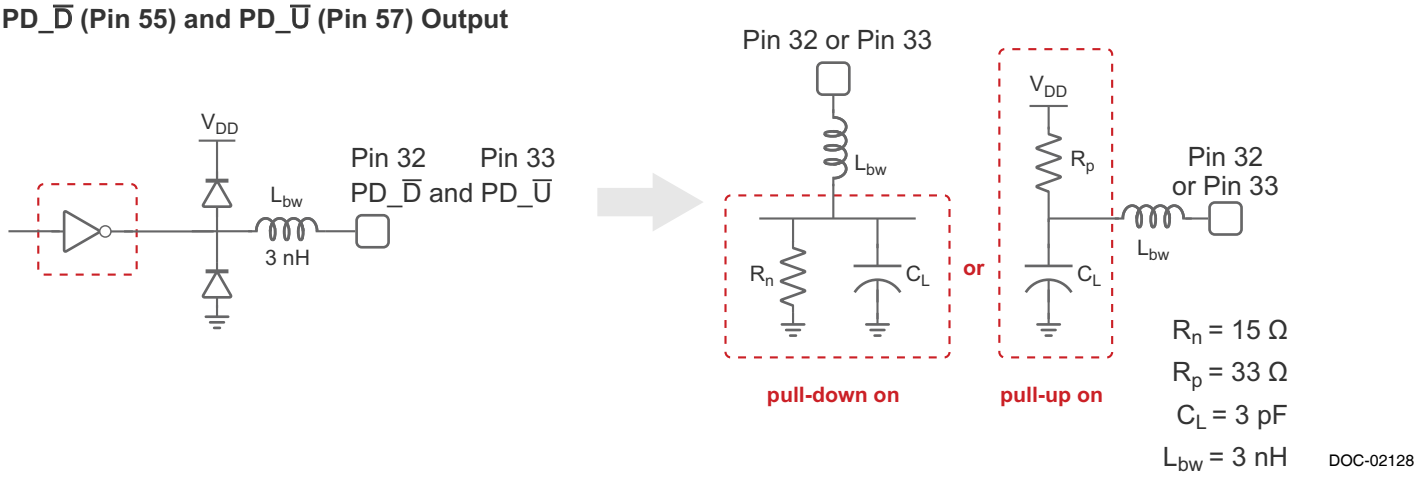
Main Input



©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

Figure 7. Equivalent Output Diagram

PD_$\overline{D}$ (Pin 55) and PD_$\overline{U}$ (Pin 57) Output



©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

Typical Performance Data@ V_{DD} = 2.6–2.8V, –40 °C < T_A < +85 °C, f_c = 50 MHz and F_{IN} = 3 GHz

Figure 8. Typical Phase Noise 5/6 Prescaler
F_{IN} = 3 GHz, V_{DD} = 2.7V, Loop Bandwidth = 500 kHz, +25 °C

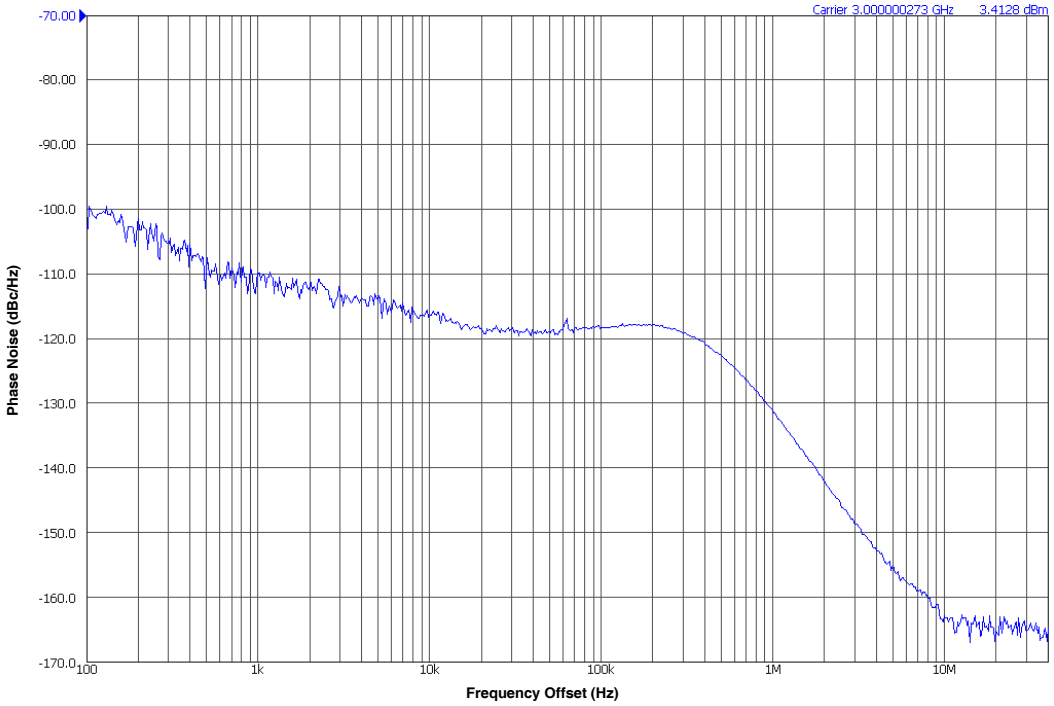
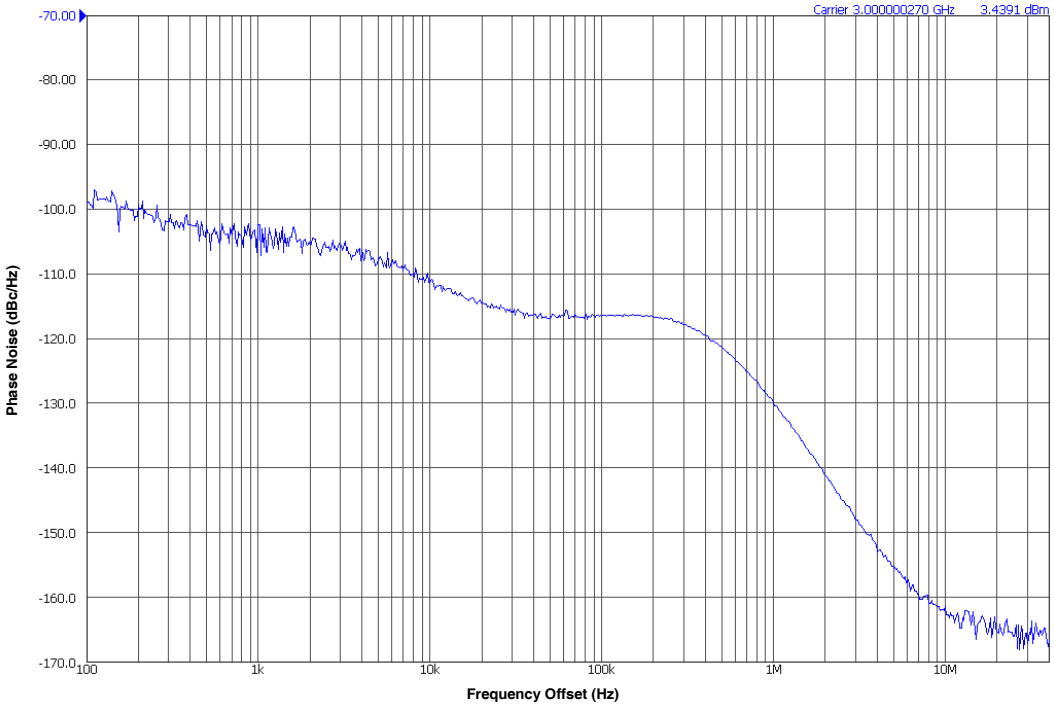


Figure 9. Typical Phase Noise 10/11 Prescaler
F_{IN} = 3 GHz, V_{DD} = 2.7V, Loop Bandwidth = 500 kHz, +25 °C



©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

Typical Performance Data @ V_{DD} = 2.6–2.8V, –40 °C < T_A < +85 °C, f_C = 50 MHz and F_{IN} = 3 GHz

Figure 10. FOM vs. Reference Power and Temp (5/6 Prescaler, V_{DD} = 2.7V)

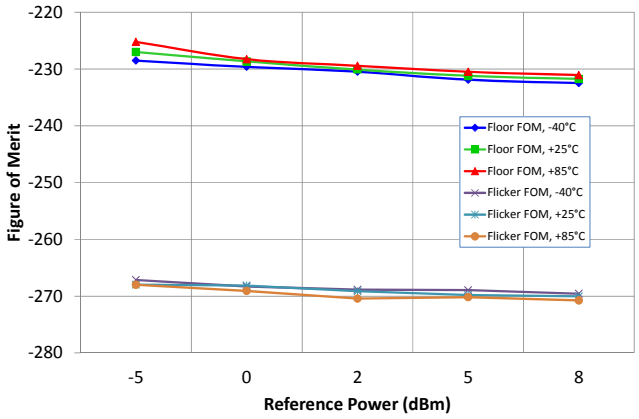


Figure 11. FOM vs. Reference Power and Temp (10/11 Prescaler, V_{DD} = 2.7V)

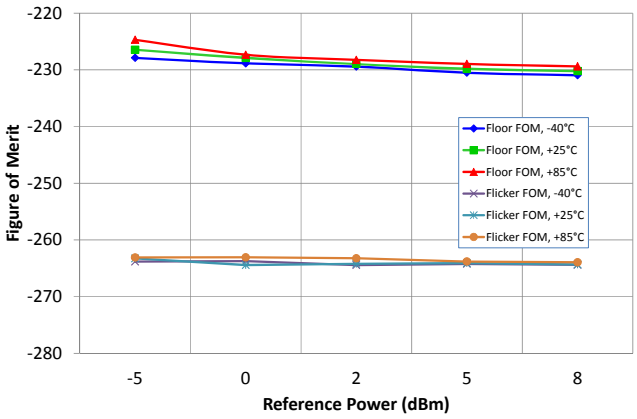


Figure 12. FOM vs. Temp and Supply Voltage (5/6 Prescaler, P_{F_IN} = 2 dBm)

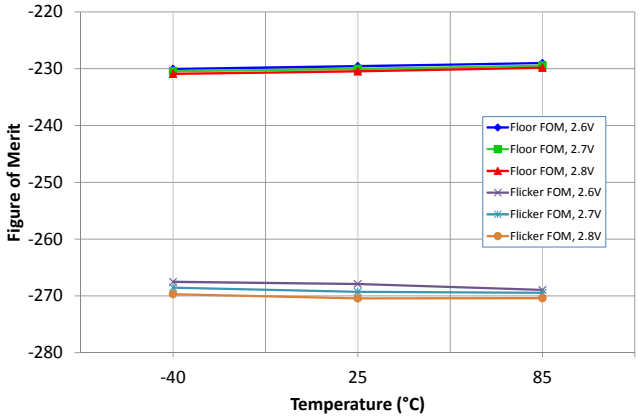


Figure 13. FOM vs. Temp and Supply Voltage (10/11 Prescaler, P_{F_IN} = 2 dBm)

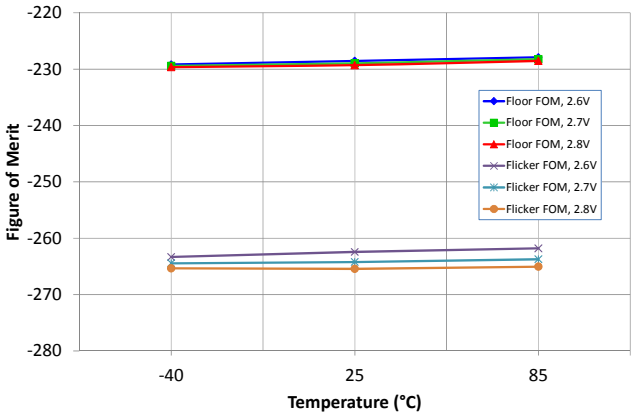


Figure 14. RF Sensitivity vs. F_{IN} and Temp (5/6 Prescaler, V_{DD} = 2.6V)*

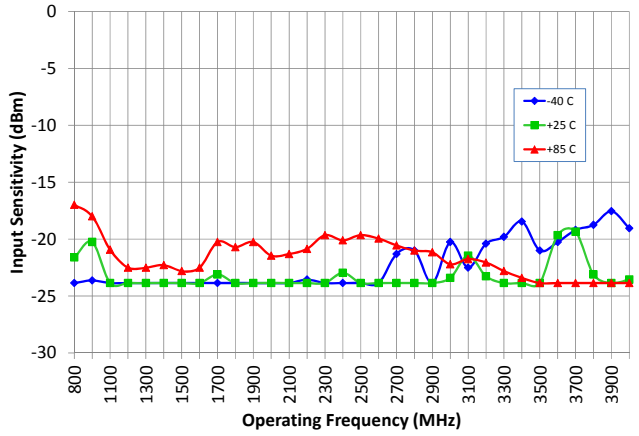
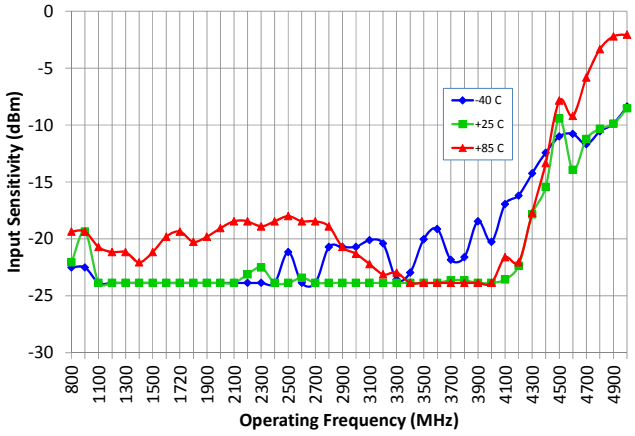


Figure 15. RF Sensitivity vs. F_{IN} and Temp (10/11 Prescaler, V_{DD} = 2.6V)*



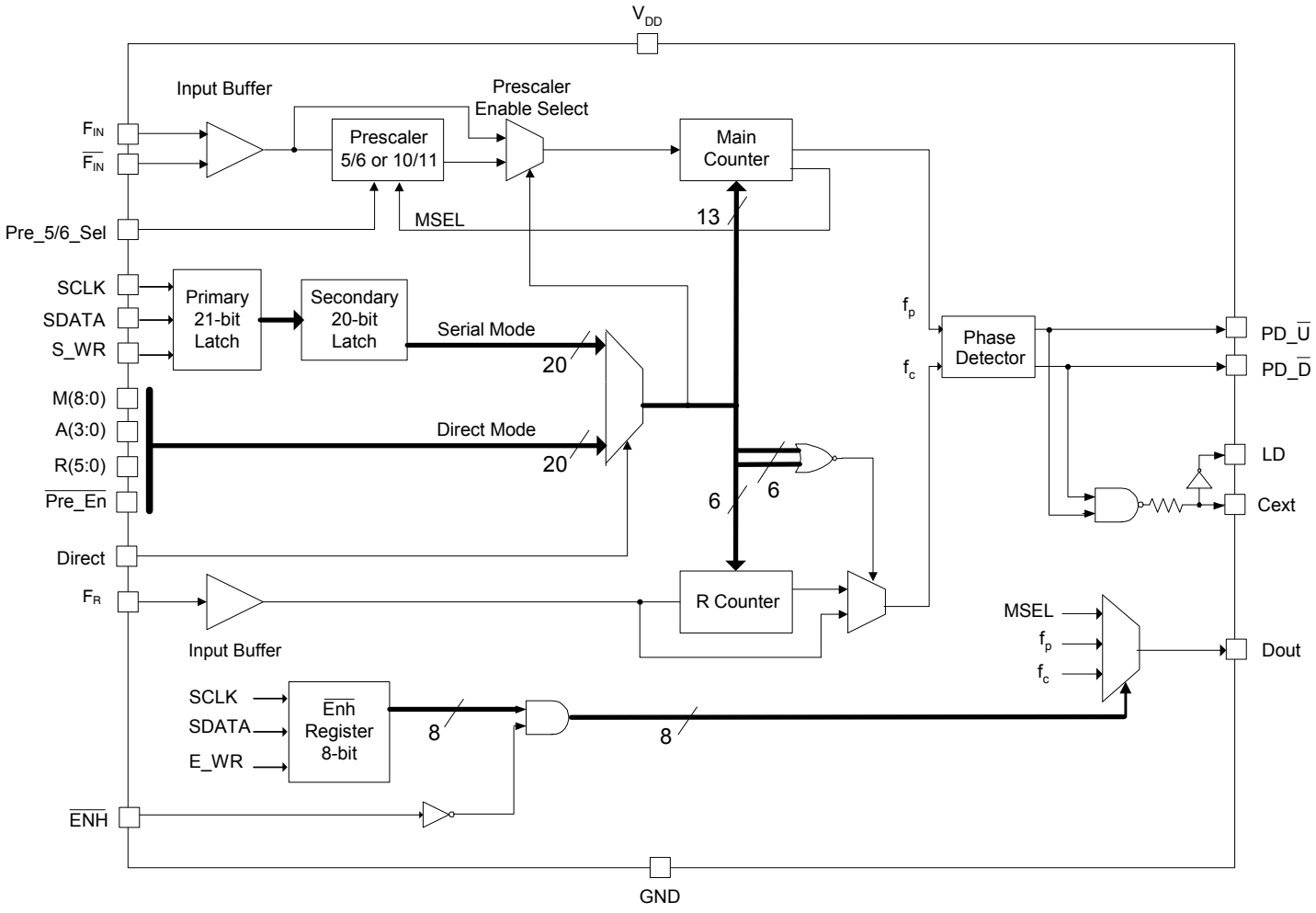
Note: * RF sensitivity is the minimum input power level required for the PLL to maintain lock. Operating at these levels does not guarantee the SSB phase noise performance in *Table 6.*

©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

Functional Description

The PE97240 consists of a prescaler, counters, a phase detector, and control logic. The dual modulus prescaler divides the VCO frequency by either 5/6 or 10/11, depending on the value of the modulus select. Counters “R” and “M” divide the reference and prescaler output, respectively, by integer values stored in a 21-bit register. An additional counter (“A”) is used in the modulus select logic. The phase-frequency detector generates up and down frequency control signals. The control logic includes a selectable chip interface. Data can be written via serial bus or hardwired directly to the pins. There are also various operational and test modes and a lock detect output.

Figure 16. Functional Block Diagram



©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

Main Counter Chain

Normal Operating Mode

The main counter chain divides the RF input frequency, F_{IN}, by an integer derived from the user-defined values in the "M" and "A" counters. It is composed of the 5/6 or 10/11 selectable modulus prescaler, modulus select logic, and 9-bit M counter. The prescaler can be set to either 5/6 or 10/11 based on the Pre_5/6_SEL pin. Setting $\overline{\text{Pre_en}}$ "low" enables the 5/6 or 10/11 prescaler. Setting $\overline{\text{Pre_en}}$ "high" allows F_{IN} to bypass the prescaler and powers down the prescaler.

The output from the main counter chain, f_p, is related to the VCO frequency, F_{in}, by the following equation:

$$f_p = F_{IN} / [10 \times (M + 1) + A] \quad (1)$$

where $A \leq M + 1,\ 1 \leq M \leq 511$

Or

$$f_p = F_{IN} / [5 \times (M + 1) + A]$$

where $A \leq M + 1,\ 1 \leq M \leq 511$

When the loop is locked, F_{IN} is related to the reference frequency, F_R, by the following equation:

$$F_{IN} = [10 \times (M + 1) + A] \times [F_R / (R + 1)] \quad (2)$$

where $A \leq M + 1,\ 1 \leq M \leq 511$

Or

$$F_{IN} = [5 \times (M + 1) + A] \times [F_R / (R + 1)]$$

where $A \leq M + 1,\ 1 \leq M \leq 511$

A consequence of the upper limit on A is that in Integer-N mode, to obtain contiguous channels,

F_{IN} **must be = 90 x [F_R / (R + 1)] with 10/11 modulus**

F_{IN} **must be = 20 x [F_R / (R + 1)] with 5/6 modulus**

The A counter can accept values as high as 15, but in typical operation it will cycle from 0 to 9 between increments in M. Programming the M counter with the minimum allowed value of "1" will result in a minimum M counter divide ratio of "2".

Prescaler Bypass Mode

Setting $\overline{\text{Pre_en}}$ "high" allows F_{IN} to bypass and power down the prescaler. In this mode, the 5/6 or 10/11 prescaler and A register are not active, and the input VCO frequency is divided by the M counter directly. The following equation relates F_{in} to the reference frequency, F_R:

$$F_{IN} = (M + 1) \times [F_R / (R + 1)] \quad (3)$$

where $1 \leq M \leq 511$

Reference Counter

The reference counter chain divides the reference frequency, F_R, down to the phase detector comparison frequency, f_c.

The output frequency of the 6-bit R counter is related to the reference frequency by the following equation:

$$f_c = F_R / (R + 1) \quad (4)$$

where $0 \leq R \leq 63$

Note that programming R with "0" will pass the reference frequency, F_R, directly to the phase detector.

©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

Serial Interface Mode

While the E_WR input is "low" and the S_WR input is "low", serial input data (SDATA input), B_0 to B_{20}, is clocked serially into the primary register on the rising edge of SCLK, MSB (B_0) first. The contents from the primary register are transferred into the secondary register on the rising edge of S_WR according to the timing diagram shown in *Figure 17*. Data is transferred to the counters as shown in *Table 7*.

While the E_WR input is "high" and the S_WR input is "low", serial input data (SDATA input), B_0 to B_7, is clocked serially into the enhancement register on the rising edge of SCLK, MSB (B_0) first. The enhancement register is double buffered to prevent inadvertent control changes during serial loading, with buffer capture of the serially-entered data performed on the falling edge of E_WR according to the timing diagram shown in *Figure 17*. After the falling edge of E_WR, the data provides control bits as shown in *Tables 8 and 9* with bit functionality enabled by asserting the $\overline{ENH}$ input "low".

Direct Interface Mode

Direct Interface Mode is selected by setting the Direct input "high".

Counter control bits are set directly at the pins as shown in *Table 7*.

Table 7. Primary Register Programming

Interface Mode	$\overline{ENH}$	R_5	R_4	M_8	M_7	$\overline{Pre_en}$	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0	ADDR
Serial*	1	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	B_{13}	B_{14}	B_{15}	B_{16}	B_{17}	B_{18}	B_{19}	B_{20}
Direct	1	R_5	R_4	M_8	M_7	$\overline{Pre_en}$	M_6	M_5	M_4	M_3	M_2	M_1	M_0	R_3	R_2	R_1	R_0	A_3	A_2	A_1	A_0	0

Note: * Serial data clocked serially on SCLK rising edge while E_WR "low" and captured in secondary register on S_WR rising edge.

MSB (first in) (last in) LSB

Table 8. Enhancement Register Programming

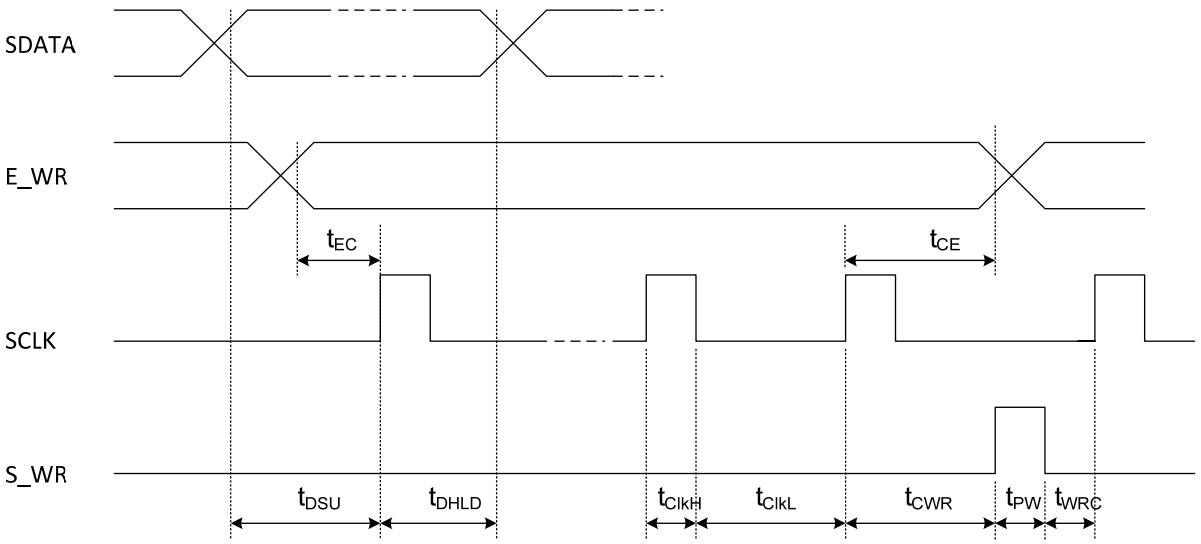
Interface Mode	$\overline{ENH}$	Direct	Reserved	Reserved	f_p output	Power Down	Counter load	MSEL output	f_c output	LD Disable
Serial*	0	0	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7

Note: * Serial data clocked serially on SCLK rising edge while E_WR "high" and captured in the double buffer on E_WR falling edge.

MSB (first in) (last in) LSB

©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

Figure 17. Serial Interface Mode Timing Diagram



Enhancement Register

The functions of the enhancement register bits are shown below with all bits active “high”.

Table 9. Enhancement Register Bit Functionality

Bit Function		Description
Bit 0	Reserve*	Reserved.
Bit 1	Reserve*	Reserved.
Bit 2	f_p output	Drives the M counter output onto the D_{OUT} output.
Bit 3	Power down	Power down of all functions except programming interface.
Bit 4	Counter load	Immediate and continuous load of counter programming.
Bit 5	MSEL output	Drives the internal dual modulus prescaler modulus select (MSEL) onto the D_{OUT} output.
Bit 6	f_c output	Drives the reference counter output onto the D_{OUT} output.
Bit 7	LD Disable	Disables the LD pin for quieter operation.

Note: * Program to 0.

©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

Phase Detector

The phase detector is triggered by rising edges from the main Counter (f_p) and the reference counter (f_c). It has two outputs, namely PD_$\overline{U}$, and PD_$\overline{D}$. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), PD_$\overline{D}$ pulses “low”. If the divided reference leads the divided VCO in phase or frequency (f_r leads f_p), PD_$\overline{U}$ pulses “low”. The width of either pulse is directly proportional to phase offset between the two input signals, f_p and f_c. The phase detector gain is 400 mV/radian.

PD_$\overline{U}$ and PD_$\overline{D}$ are designed to drive an active loop filter which controls the VCO tune voltage. PD_$\overline{U}$ pulses result in an increase in VCO frequency and PD_$\overline{D}$ results in a decrease in VCO frequency.

A lock detect output, LD is also provided, via the pin C_{EXT}. C_{EXT} is the logical “NAND” of PD_$\overline{U}$ and PD_$\overline{D}$ waveforms, which is driven through a series 2 kΩ resistor. Connecting C_{EXT} to an external shunt capacitor provides integration. C_{EXT} also drives the input of an internal inverting comparator with an open drain output. Thus LD is an “AND” function of PD_$\overline{U}$ and PD_$\overline{D}$. See *Figure 16* for a functional block diagram of this circuit.

©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

Evaluation Board

The PE97240 evaluation board was designed to demonstrate optimal phase noise performance when using an external and stable low noise reference source. The device may be programmed serially using the USB interface board with the applications software or directly by using jumpers to set the register values. Additionally, an external VCO may be used for specific operating frequencies.

The evaluation board consists of a four layer stack with two outer layers made of Rogers 4350B (ε_r = 3.48) and two inner layers of FR406 (ε_r = 4.80). The 12 mil (0.30 mm) thick inner layers provide ground planes for the RF transmission lines. The total thickness of the board is 62 mils (1.57 mm).

Figure 18. Evaluation Kit

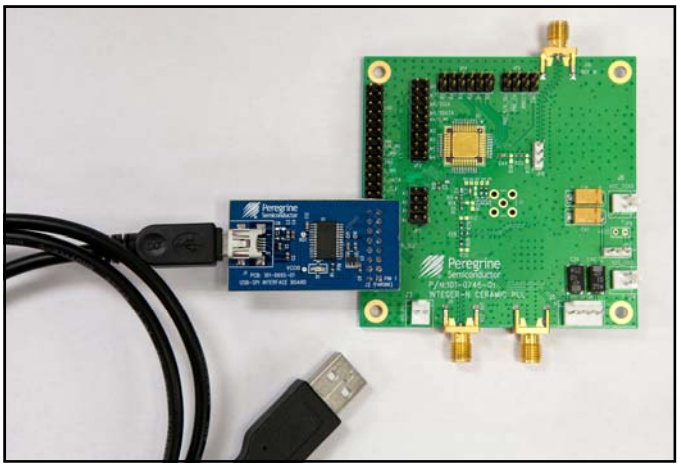
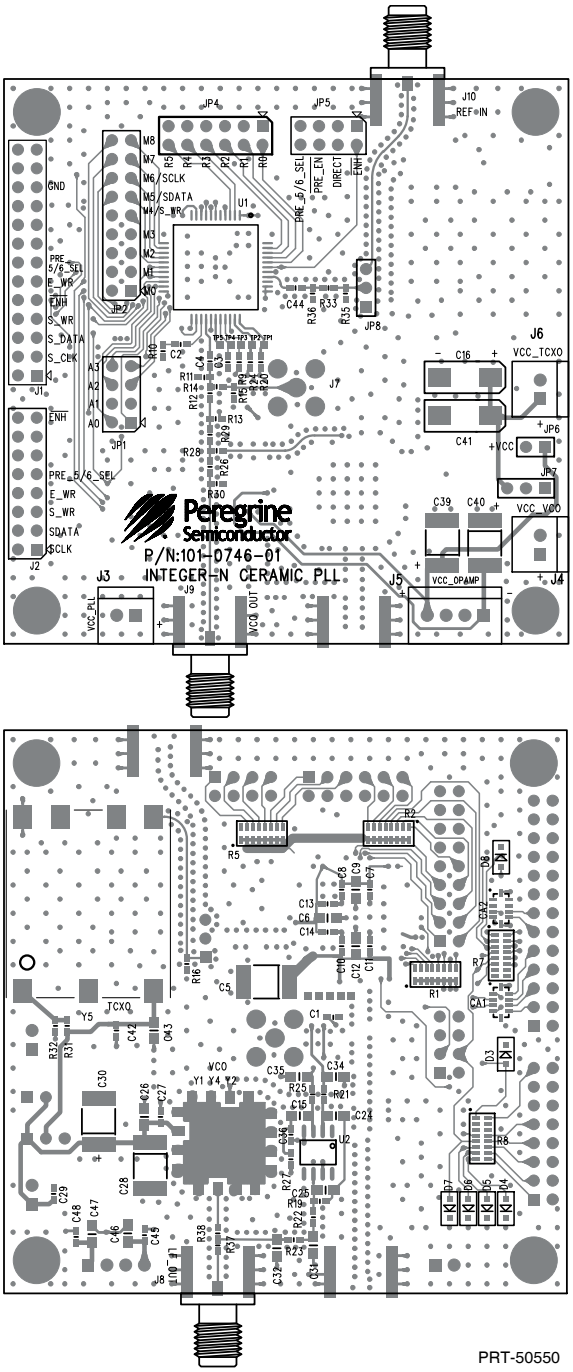


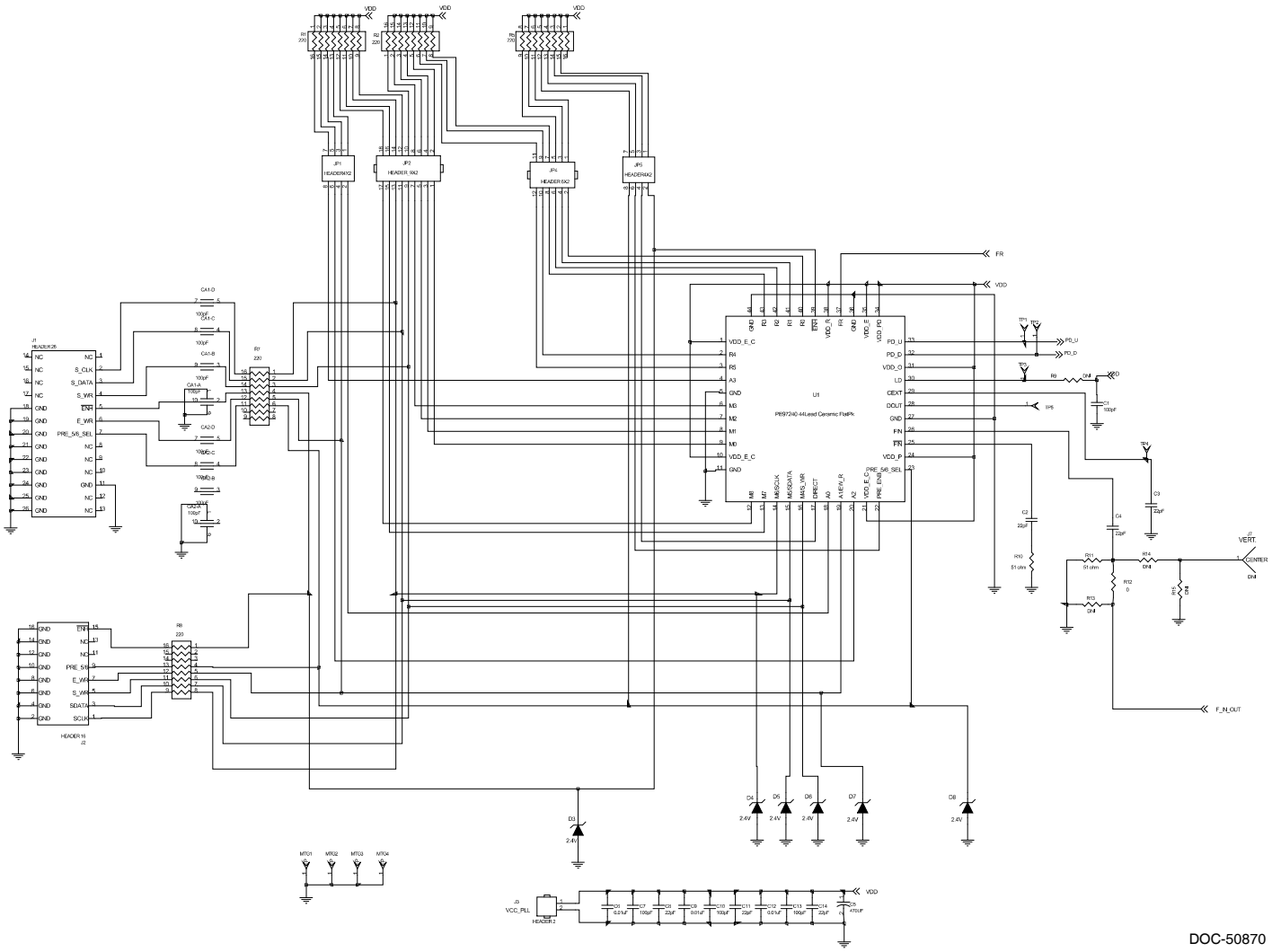
Figure 19. Evaluation Board Layout



PRT-50550

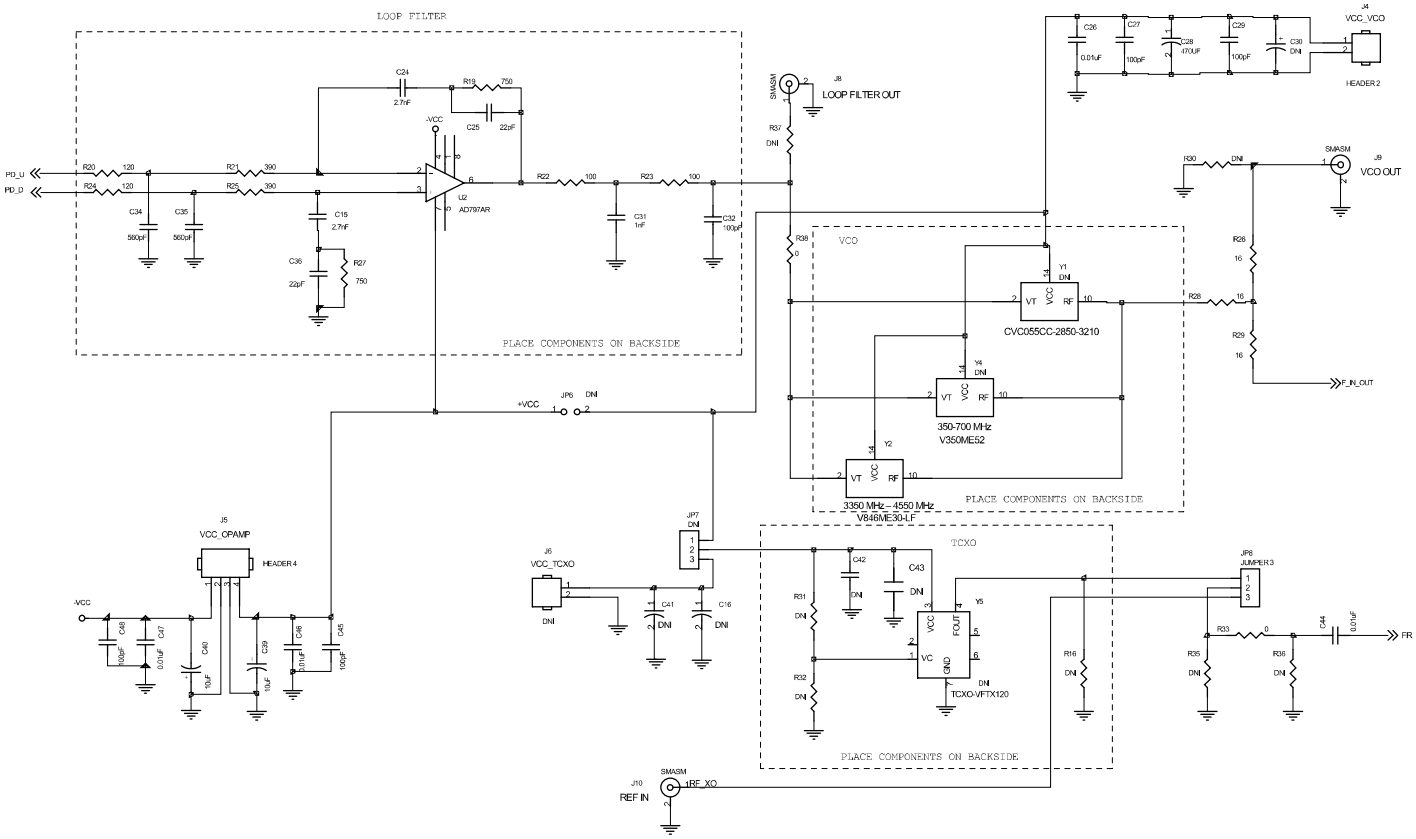
©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

Figure 20. Evaluation Board Schematic



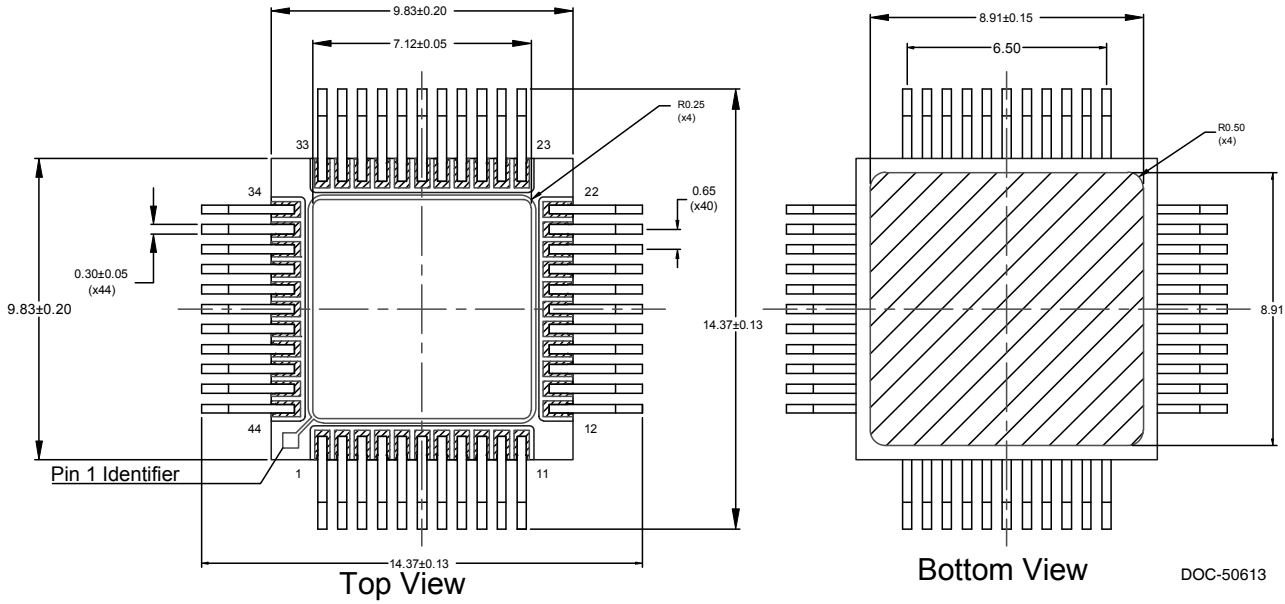
©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

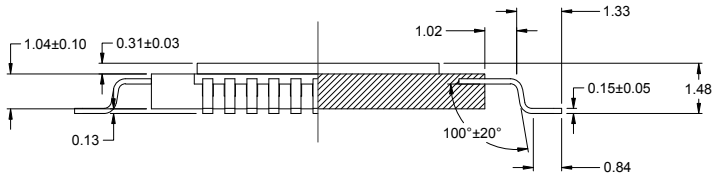
Figure 20. Evaluation Board Schematic (continued)



©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

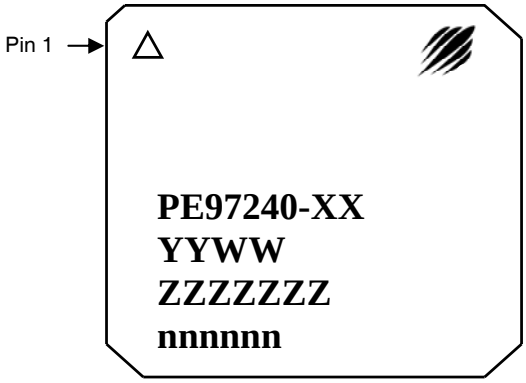
Figure 21. Package Drawing
44-lead CQFP





©2010-2015 Peregrine Semiconductor Corp. All rights reserved.

Figure 22. Top Marking Specifications



PRT-55218

△ = Pin 1 indicator
97240-XX = Part number (XX will be specified by the PO and/or the assembly instructions)
YYWW = Date Code, last two digits of the year and work week
ZZZZZZZ = Lot Code (up to seven digits)
nnnnnn = Serial number of the part (up to six digits)

Table 10. Ordering Information

Order Code	Description	Package	Shipping Method
97240-01*	Engineering samples	44-lead CQFP	40 units/tray
97240-11	Flight units	44-lead CQFP	40 units/tray
97240-00	Evaluation kit	Evaluation kit	1/box

Note: * The PE97240-01 devices are ES (Engineering Sample) prototype units intended for use as initial evaluation units for customers of the PE97240-11 flight units. The PE97240-01 device provides the same functionality and footprint as the PE97240-11 space qualified device, and intended for engineering evaluation only. They are tested at +25 °C only and processed to a non-compliant flow (e.g. No burn-in, non-hermetic, etc). These units are non-hermetic and are not suitable for qualification, production, radiation testing or flight use.

Sales Contact and Information

Contact Information:
e2v ~ http://www.e2v-us.com ~ inquiries @e2v-us.com

Advance Information: The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification: The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product. ***Product Specification:*** The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

The information in this datasheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.
No patent rights or licenses to any circuits described in this datasheet are implied or granted to any third party. Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.
The Peregrine name, logo, UltraCMOS and UTSi are registered trademarks and HaRP, MultiSwitch and DuNE are trademarks of Peregrine Semiconductor Corp. Peregrine products are protected under one or more of the following U.S. Patents: http://patents.psemi.com.

©2010-2015 Peregrine Semiconductor Corp. All rights reserved.