Application Report

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High-Vin, High-Efficiency Power Solution Using DC/DC Converter With DVFS

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ABSTRACT

This reference design is intended for users designing with the TMS320C6742, TMS320C6746, TMS320C6748, or OMAP-L138 processor. Using sequenced power supplies, this reference design describes a system having a 12-V input voltage and a high-efficiency dc/dc converter with integrated FETs and dynamic voltage and frequency scaling (DVFS) for a small, simple design.

Sequenced power supply architectures are becoming commonplace in high-performance microprocessor and digital signal processor (DSP) systems. To save power and increase processing speeds, processor cores have smaller geometry cells and require lower supply voltages than the system bus voltages. Power management in these systems requires special attention. This application report addresses these topics and suggests solutions for output voltage sequencing.

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1 Introduction

In dual voltage architectures, coordinated management of power supplies is necessary to avoid potential problems and ensure reliable performance. Power supply designers must consider the timing and voltage differences between core and input/output (I/O) voltage supplies during power-up and power-down operations.

Sequencing refers to the order, timing, and differential in which the two voltage rails are powered up and down. A system designed without proper sequencing may be at risk for two types of failures. The first of these represents a threat to the long-term reliability of the dual voltage device, whereas the second is more immediate, with the possibility of damaging interface circuits in the processor or system devices such as memory, logic, or data converter integrated circuits (IC).

Another potential problem with improper supply sequencing is bus contention. Bus contention is a condition in which the processor and another device both attempt to control a bidirectional bus during power up. Bus contention may also affect I/O reliability. Power supply designers must check the requirements regarding bus contention for individual devices.

The power-on sequencing for the OMAP-L138, TMS320C6742, TMS320C6746, and TMS320C6748 are shown in Table 1. None of the supplies for these devices require a specific voltage ramp rate as long as the 3.3-V rail does not exceeds the 1.8-V rail by more than 2 V.

In order to reduce the power consumption of the processor core, dynamic voltage and frequency scaling (DVFS) is used in the reference design. DVFS is a power management technique used while active processing is going on in the system-on-chip (SoC), which matches the operating frequency of the hardware to the performance requirement of the active application scenario. Whenever clock frequencies are lowered, operating voltages are also lowered to achieve power savings. In the reference design, the TPS62353 is used, which can scale its output voltage.

2 Power Requirements

The power requirements are as specified in the following table.

Table 1. General Requirements

	PIN NAME	VOLTAGE [1] [2] (V)	Imax (mA)	TOLERANCE	SEQUENCING ORDER	TIMING DELAY
I/O	RTC_CVDD	1.2	1	–25%, +10%	1[3]	
Core	CVDD[4]	1.0 / 1.1 / 1.2	600	–9.75%, +10%	2	
I/O	RVDD, PLL0_VDDA, PLL1_VDDA, SATA_VDD, USB_CVDD, USB0_VDDA12	1.2	200	–5%, +10%	3	
I/O	USB0_VDDA18, USB1_VDDA18, DDR_DVDD18, SATA_VDDR, DVDD18	1.8	180	±5%	4	
I/O	USB0_VDDA33, USB1_VDDA33	3.3	24	±5%	5	
I/O	DVDD3318_A, DVDD3318_B, DVDD3318_C	1.8 / 3.3	50 / 90[5]	±5%	4 / 5	

(1) If 1.8-V LVCMOS is used, power rails up with the 1.8-V rails. If 3.3-V LVCMOS is used, power it up with the ANALOG33 rails (VDDA33_USB0/1).

(2) No specific voltage ramp rate is required for any of the supplies LVCMOS33 (USB0_VDDA33, USB1_VDDA33) as long as STATIC18 (USB0_VDDA18, USB1_VDDA18, DDR_DVDD18, SATA_VDDR, DVDD18) never exceeds more than 2 V.

(3) If RTC is not used/maintained on a separate supply, it can be included in the STATIC12 (fixed 1.2 V) group.

(4) If using CVDD at fixed 1.2 V, all 1.2-V rails may be combined.

(5) If DVDD3318_A, B, and C are powered independently, maximum power for each rail is 1/3 above maximum power.

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3 Features

The design uses the following high-efficiency dc/dc converters with integrated FETs.

	HIGH EFFICIENCY (With DVFS)
INPUT VOLTAGE	**~12 V/3.3 V**
OUTPUT VOLTAGES	
Core 1.2 V at 600 mA	TPS62353
Fixed 1.2 V + VRTC at 251 mA	TPS62232
1.8 V at 230 mA	TPS62231
3.3 V at 115 mA	TPS62111

In the preceding table, VRTC is included in the STATIC12 (fixed 1.2-V) group.

TPS62353

- 88% efficiency at 3-MHz operation
- Output peak current up to 800 mA
- 3-MHz fixed frequency operation
- *Best in class* load and line transient
- ±2% PWM dc voltage accuracy
- Efficiency optimized Power-Save mode
- Transient optimized Power-Save mode
- Fixed 1.2-V output eliminates need for external voltage-setting resistors
- Available in a 10-pin QFN (3 × 3 mm) 12-pin NanoFree™ (CSP) packaging

TPS62231 and TPS62232

- 3-MHz switch frequency
- Up to 94% efficiency
- Output peak current up to 500 mA
- Small external output filter components (1 μH/4.7 μF)
- Small 1 × 1,5 × 0,6 mm 3 SON package
- Fixed 1.8-V and 1.2-V output, respectively, eliminates need for external voltage-setting resistors

TPS62111

- High-efficiency synchronous step-down converter with up to 95% efficiency
- Up to 1.5-A output current
- High efficiency over a wide load-current range due to PFM/PWM operation mode
- Fixed 3.3-V output eliminates need for external voltage-setting resistors

More information on the devices can be found in the data sheets.

- TPS62111, SLVS585
- TPS62231 and TPS62232, SLVS941
- TPS62353, SLVS540

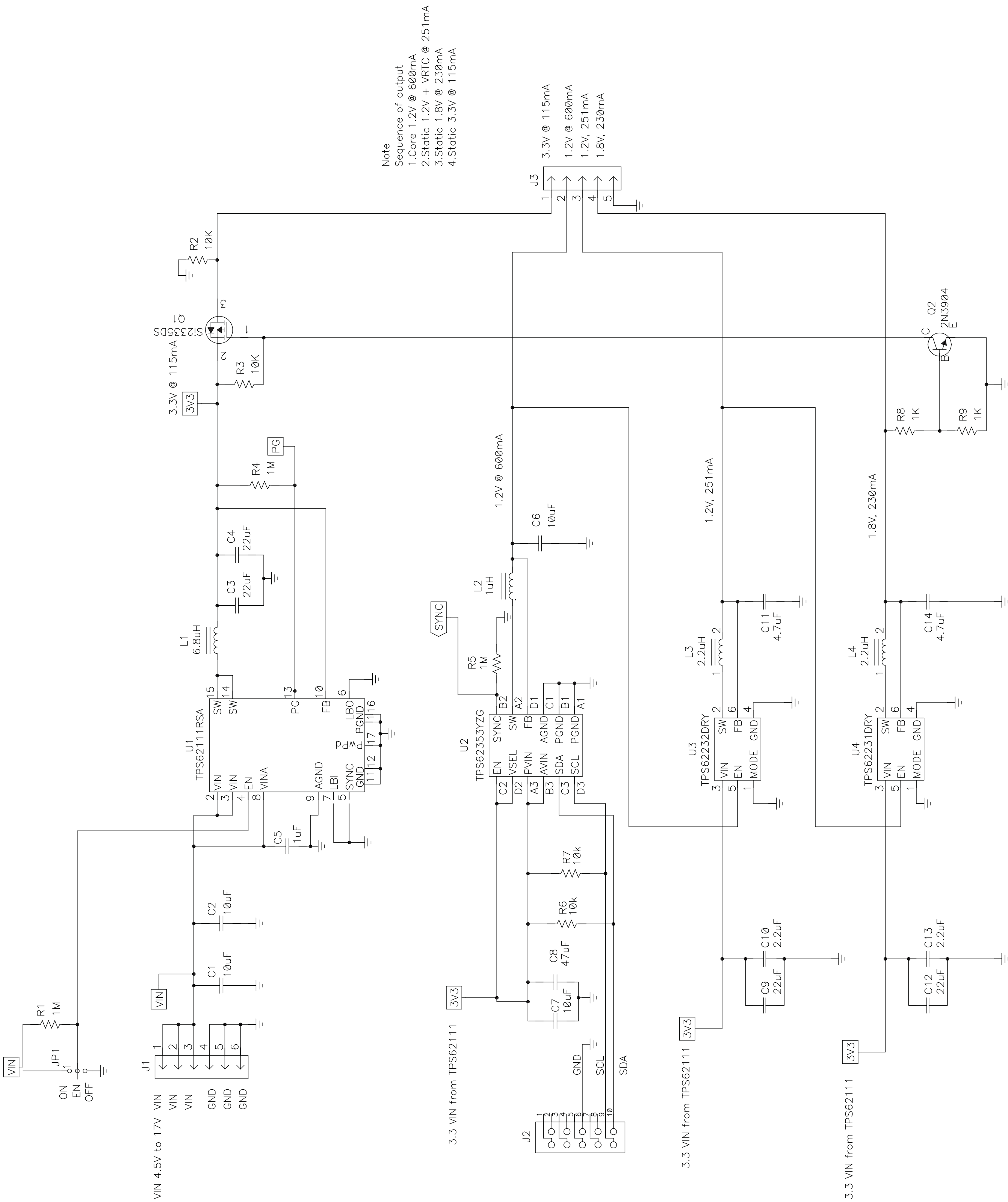
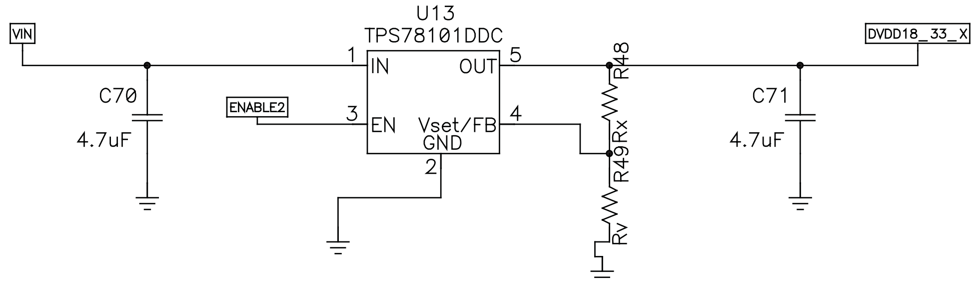


Figure 1. PMP4976 Reference Design Schematic

Proper sequencing is ensured in the design with the use of a NPN transistor and a P-channel MOSFET. As required, Core 1.2 V at 600 mA comes first, and is followed by Static 1.2 V + VRTC at 251 mA. Then comes Static 1.8 V at 230 mA, which in turn pulls down the gate of a P-channel MOSFET with the use of a NPN transistor. Last, Static 3.3 V at 115 mA comes up.



(1) Use three such LDOs to power up DVDDA, DVDDB, and DVDDC. (It can be either 1.8 V or 3.3 V.)

(2) Rx = 0.499 MΩ, Ry = 1 MΩ for Vout = 1.8 V

(3) Rx = 1.8 MΩ, Ry = 1 MΩ for Vout = 3.3 V

(4) For proper sequencing of output, the enable of the LDOs are fed either from a 1.2-V output from TPS62232 if DVDDX is 1.8 V or from a 1.8-V output from TPS62231 if DVDDX is 3.3 V.

Figure 2. Optional Circuit for DVDD_A, DVDD_B, and DVDD_C

4 Bill of Materials

Table 2. PMP4976 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR	AREA
2	C1	10 µF	Capacitor, Ceramic, 25V, X5R, 20%	1206	C3216X5R1E106	TDK	15390
	C2	10 µF	Capacitor, Ceramic, 25V, X5R, 20%	1206	C3216X5R1E106	TDK	15390
2	C3	22 µF	Capacitor, Ceramic, 10V, X5R, 20%	1206	C3216X5R1A226	TDK	15390
	C4	22 µF	Capacitor, Ceramic, 10V, X5R, 20%	1206	C3216X5R1A226	TDK	15390
1	C5	1 µF	Capacitor, Ceramic, 25V, X7R, 10%	603	C1608X7R1E105K	TDK	5650
2	C6	10 µF	Capacitor, Ceramic, 6.3V, X5R, 10%	603	C1608X5R0J106KT	TDK	5650
	C7	10 µF	Capacitor, Ceramic, 6.3V, X5R, 10%	603	C1608X5R0J106KT	TDK	5650
1	C8	47 µF	Capacitor, Ceramic, 10V, X5R, 20%	1812	C4532X5R1A476M	TDK	43,360
2	C9	22 µF	Capacitor, Ceramic, 10V, X5R, 20%	1210	Std	Std	83,600
2	C10	2.2 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	402	JDK105BJ225MV	Taiyo Yuden	2800
2	C11	4.7 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	402	JDK105BJ475MV	Taiyo Yuden	2800
	C12	22 µF	Capacitor, Ceramic, 10V, X5R, 20%	1210	Std	Std	83,600
	C13	2.2 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	402	JDK105BJ225MV	Taiyo Yuden	2800
	C14	4.7 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	402	JDK105BJ475MV	Taiyo Yuden	2800
1	J1	PTC36SAAN	Header, Male 6-pin, 100mil spacing, (36-pin strip)	0.100 inch × 6	PTC36SAAN	Sullins	70000
1	J2	2510-6002UB	Connector, Male Straight 2×10 pin, 100mil spacing, 4 Wall	0.338 × 0.788	2510-6002UB	3M	301.02 4
1	J3	PEC36SAAN	Header, Male 5-pin, 100mil spacing, (36-pin strip)	0.100 inch × 5	PEC36SAAN	Sullins	60000
1	JP1	PTC36SAAN	Header, 3-pin, 100mil spacing, (36-pin strip)	0.100 × 3	PTC36SAAN	Sullins	34100
1	L1	6.8 µH	Inductor, SMT, 3.0A, 97 mΩ	0.276 × 0.276 inch	HA3808-AL	Coiltronics	90000
1	L2	1 µH	Inductor, SMT, 1.6A, ±30%	0.118 × 0.118	LPS3010-102NLC	Coilcraft	26,560
2	L3	2.2 µH	Inductor, SMT, 0.7A, 230-mΩ	805	MIPSZ20120D2R2	FDK	10160
	L4	2.2 µH	Inductor, SMT, 0.7A, 230-mΩ	805	MIPSZ20120D2R2	FDK	10160
1	Q1	Si2335DS	MOSFET, P-ch, -12 V, 4 A, 51 mΩ	SOT23	Si2335DS	Vishay	14105
1	Q2	2N3904	Transistor, NPN, 40V, 200mA, 625mW	TO-92	2N3904	Fairchild	37800
1	R1	1M	Resistor, Chip, 1/16-W, 1%	603	Std	Std	9100
2	R2	10K	Resistor, Chip, 1/16W, x%	603	Std	Std	5,650
	R3	10K	Resistor, Chip, 1/16W, x%	603	Std	Std	5,650
1	R4	1M	Resistor, Chip, 1/16W, x%	603	Std	Std	5,650
1	R5	1M	Resistor, Chip, 1/16W, 1%	603	Std	Std	5650
2	R6	10k	Resistor, Chip, 1/16W, 1%	603	Std	Std	5650
	R7	10k	Resistor, Chip, 1/16W, 1%	603	Std	Std	5650
2	R8	1K	Resistor, Chip, 1/16W, x%	603	Std	Std	5,650
	R9	1K	Resistor, Chip, 1/16W, x%	603	Std	Std	5,650
1	U1	TPS62111RSA	IC, Synchronous Step-Down Converter, 17V, 1.2A	QFN-16	TPS62111RSA	TI	54289
1	U2	TPS62353YZG	IC, 3MHz Synchronous Step Down Converter with I^2C, 800mA	CSP-12	TPS62353YZG	TI	12,000
1	U3	TPS62232DRY	IC, 3MHz Ultra Small Step Down Converter, x.x V	QFN	TPS62232DRY	TI	6020
1	U4	TPS62231DRY	IC, 3MHz Ultra Small Step Down Converter, x.x V	QFN	TPS62232DRY	TI	6020

Notes:
1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Failure to use clean flux is unacceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Reference designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

4.1 Test Result

The start-up waveform Figure 3 specifies the sequencing order that is required.

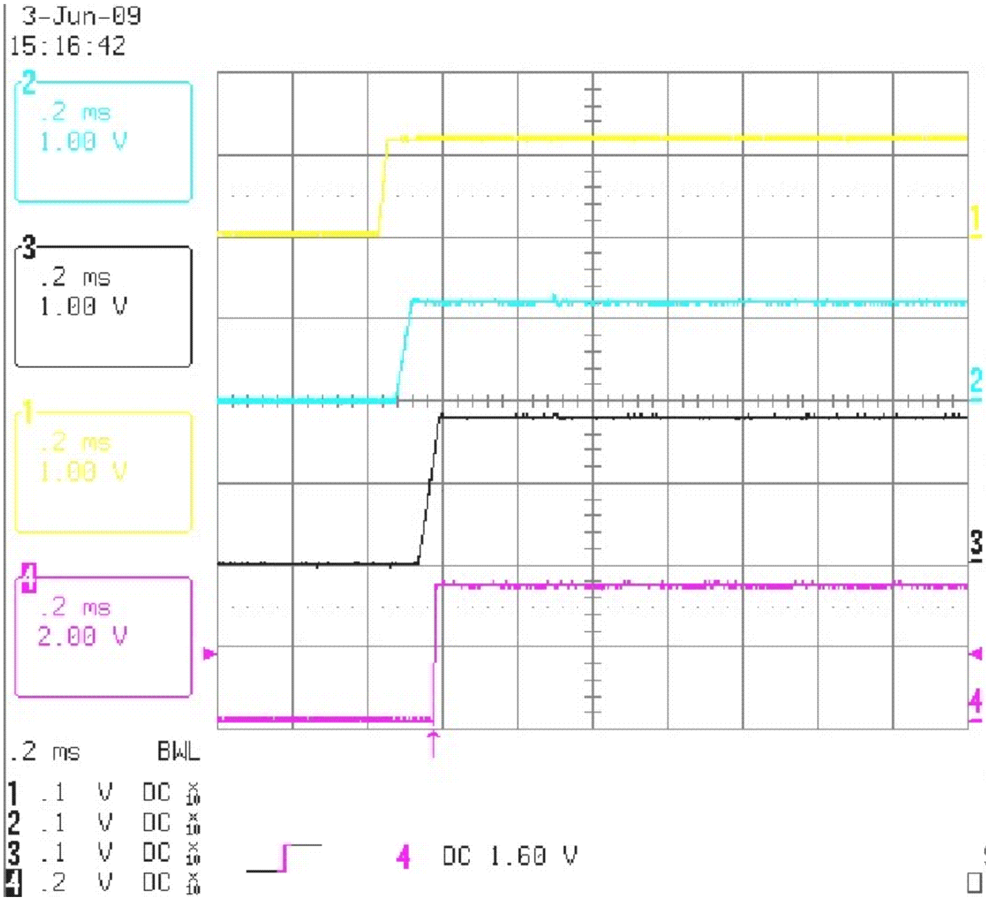


Figure 3. Sequencing in Start-up Waveform

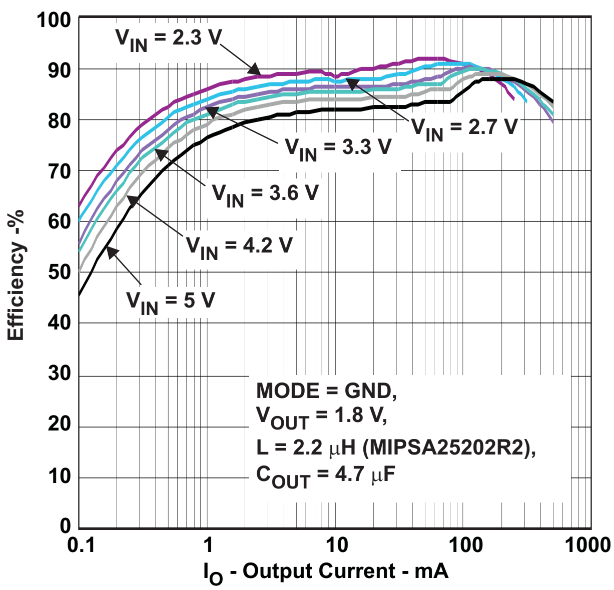


Figure 4. Efficiency vs Output Current

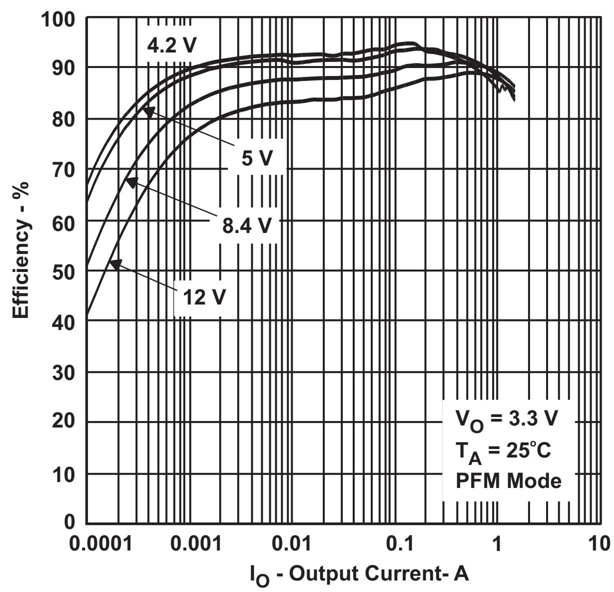


Figure 5. Efficiency vs Output Current

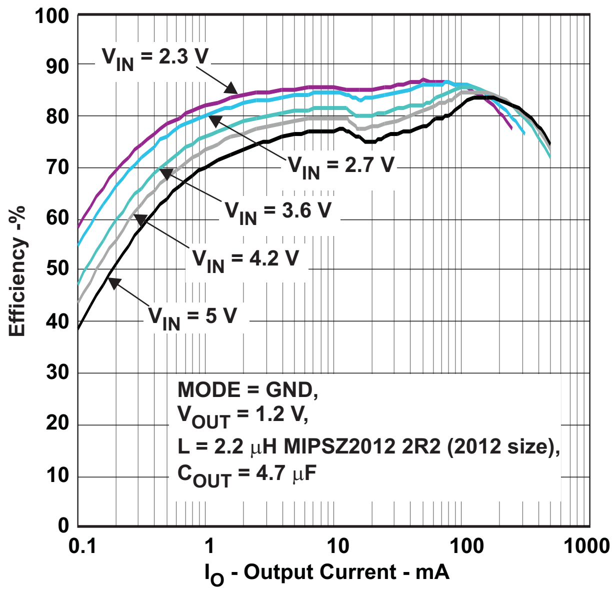


Figure 6. Efficiency vs Output Current

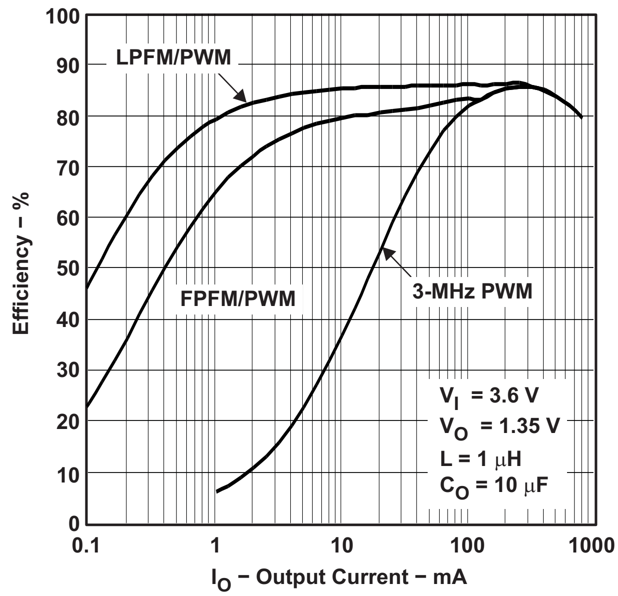


Figure 7. Efficiency vs Output Current