PRELIMINARY - December 7, 1999 TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

DESCRIPTION

The SC1205 is a cost effective Dual MOSFET Driver designed for switching High and Low side Power MOSFETs. Each driver is capable of driving a 3000pF load in 20ns rise/fall time and has a 20ns max propagation delay from input transition to the gate of the power FET's. An internal Overlap Protection Circuit prevents shoot-through from Vin to GND in the main switching and synchronous MOSFET's. The Overlap Protection circuit ensures the Bottom FET does not turn on until the Top FET source has reached a voltage low enough to prevent cross-conduction.

The high current drive capability (2A peak) allows fast switching, thus reducing switching losses at high (1MHz) PWM frequencies. The high voltage CMOS process allows operation from 5-25 Volts at top MOSFET drain, thus making SC1205 suitable for battery powered applications. Connecting Enable pin (EN) to logic low shuts down both drives and reduces operating current to less than 10uA.

An Under-Voltage-Lock-Out circuit is included to guarantee that both driver outputs are low when the 5V logic level is less than or equal to 4.4V (typ) at supply ramp up (4.35V at supply ramp down). An Internal temperature sensor shuts down all drives in the event of overtemperature. SC1205 is fabricated utilizing CMOS technology for low quiescent current. The SC1205 is offered in a standard SO-8 package.

FEATURES

- Fast rise and fall times (15ns typical with 3000pf load)
- 2Amp peak drive current
- 14ns max Propagation delay (BG going low)
- Adaptive Non-overlapping Gate Drives provide shoot-through protection
- Floating top drive switches up to 25V
- Under-Voltage lock-out
- Overtemperature protection
- Less than 10uA supply current when EN is low
- Low cost

APPLICATIONS

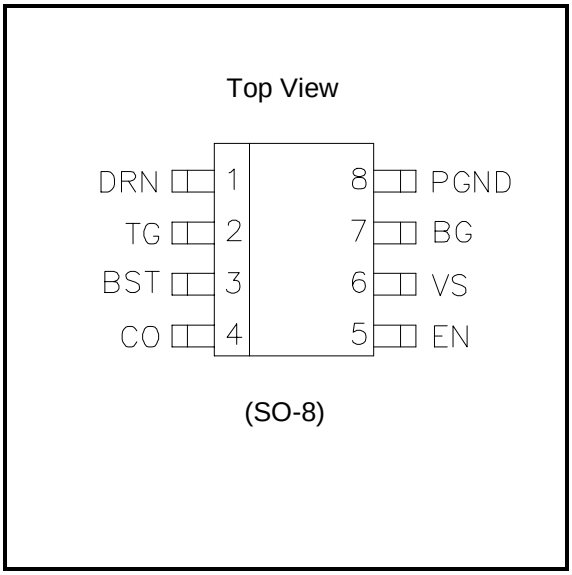
- High Density sunchronous power supplies
- Motor Drives/Class-D amps/Half bridge drivers
- High frequency (to 1.2 MHz) operation allows use of small inductors and low cost caps in place of electrolytics
- Portable computers
- Battery powered applications

ORDERING INFORMATION

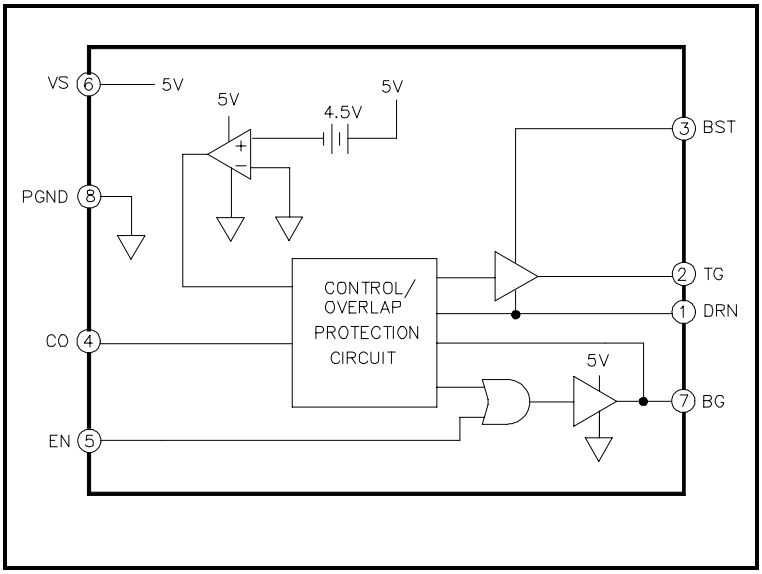
DEVICE(1)	PACKAGE	TEMP. RANGE (T_J)
SC1205CS	SO-8	0 - 125°C

Note:
(1) Add suffix 'TR' for tape and reel.

PIN CONFIGURATION



BLOCK DIAGRAM



 652 MITCHELL ROAD NEWBURY PARK CA 91320

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Maximum	Units
V_{CC} Supply Voltage	V_{MAX5V}		7	V
BST to PGND	$VMAX_{BST-PGND}$		30	V
BST to DRN	$VMAX_{BST-DRN}$		7	V
DRN to PGND	$VMAX_{DRN-PGN}$		25	V
OVP_S to PGND	$VMAX_{OVP\_S-PGND}$		10	V
Input pin	CO		-0.3 to 7.3	V
Continuous Power Dissipation	Pd	Tamb = 25°C, T_J = 125°C Tcase = 25°C, T_J = 125°C	0.66 2.56	W
Thermal Resistance Junction to Case	$\theta\vartheta X$		40	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}		150	°C/W
Operating Temperature Range	T_J		0 to +125	°C
Storage Temperature Range	T_{STG}		-65 to +150	°C
Lead Temperature (Soldering) 10 sec	T_{LEAD}		300	°C

NOTE:

(1) Specification refers to application circuit in Figure 1.

ELECTRICAL CHARACTERISTICS (DC OPERATING SPECIFICATIONS)

Unless specified: -0 < θ_J < 125°C; V_{CC} = 5V; 4V ≤ V_{BST} ≤ 26V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage	V_{CC}	V_{CC}	4.15	5	6.0	V
Quiescent Current, operating	Iq_op	V_{CC} = 5V, CO = 0V		1		ma
Quiescent Current	Iq_stby	EN = 0V			10	µA
UNDER-VOLTAGE LOCKOUT						
Start Threshold	V_{START}		4.2	4.4	4.6	V
Hysteresis	$Vhys_{UVLO}$			0.05		V
Logic Active Threshold	V_{ACT}				1.5	V

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ELECTRICAL CHARACTERISTICS (DC OPERATING SPECIFICATIONS) Cont.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CO						
High Level Input Voltage	V_{IH}		2.0			V
Low Level Input Voltage	V_{IL}				0.8	V
THERMAL SHUTDOWN						
Over Temperature Trip Point	T_{OTP}			165		°C
Hysteresis	T_{HYST}			10		°C
HIGH-SIDE DRIVER						
Peak Output Current	I_{PKH}			2		A
Output Resistance	$Rsrc_{TG}$ $Rsink_{TG}$	duty cycle < 2%, tpw < 100µs, T_J = 125°C, V_{BST} - V_{DRN} = 4.5V, V_{TG} = 4.0V (src)+V_{DRN} or V_{TG} = 0.5V (sink)+V_{DRN}		1 .7		Ω Ω
LOW-SIDE DRIVER						
Peak Output Current	I_{PKL}			2		A
Output Resistance	$Rsrc_{BG}$ $Rsink_{BG}$	duty cycle < 2%, tpw < 100µs, T_J = 125°C V_{V_5} = 4.6V, V_{BG} = 4V (src), or V_{LOWDR} = 0.5V (sink)		1.2 1.0		Ω Ω

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AC OPERATING SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-SIDE DRIVER						
rise time	tr_{TG},	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V, **T_J = 125°C**		14	**23**	ns
fall time	tf_{TG}	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V, **T_J = 125°C**		12	**19**	ns
propagation delay time, TG going high	$tpdh_{TG}$	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V, **T_J = 125°C**		20	**32**	ns
propagation delay time, TG going low	$tpdl_{TG}$	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V, **T_J = 125°C**		15	**24**	ns
LOW-SIDE DRIVER						
rise time	tr_{BG}	Cl = 3nF, V_{V_5} = 4.6V, **T_J = 125°C**		15	**24**	ns
fall time	tr_{BG}	Cl = 3nF, V_{V_5} = 4.6V, **T_J = 125°C**		13	**21**	ns
propagation delay time BG going high	$tpdh_{BGHI}$	Cl = 3nF, V_{V_5} = 4.6V, **T_J = 125°C**, DRN ≤ 1V		12	**19**	ns
progagation delay time BG going low	$tpdl_{BG}$	Cl = 3nF, V_{V_5} = 4.6V, **T_J = 125°C**		7	**12**	ns
UNDER-VOLTAGE LOCKOUT						
V_5 ramping up	$tpdh_{UVLO}$	EN is High			10	us
V_5 ramping down	$tpdl_{UVLO}$	EN is High			10	us

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PIN DESCRIPTION

Pin #	Pin Name	Pin Function
1	DRN	This pin connects to the junction of the switching and synchronous MOSFET's. This pin can be subjected to a -2V minimum relative to PGND without affecting operation.
2	TG	Output gate drive for the switching (high-side) MOSFET.
3	BST	Bootstrap pin. A capacitor is connected between BST and DRN pins to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically between 0.1µF and 1µF (ceramic).
4	CO	TTL-level input signal to the MOSFET drivers.
5	EN	When high, this pin enables the internal circuitry of the device. When low, TG, BG and PRDY are forced low and the supply current (5V) is less than 10µA.
6	VS	+5V supply. A .22-1µF ceramic capacitor should be connected from 5V to PGND very close to this pin.
7	BG	Output drive for the synchronous MOSFET.
8	PGND	Ground.

NOTE:

(1) All logic level inputs and outputs are open collector TTL compatible.

TIMING DIAGRAM

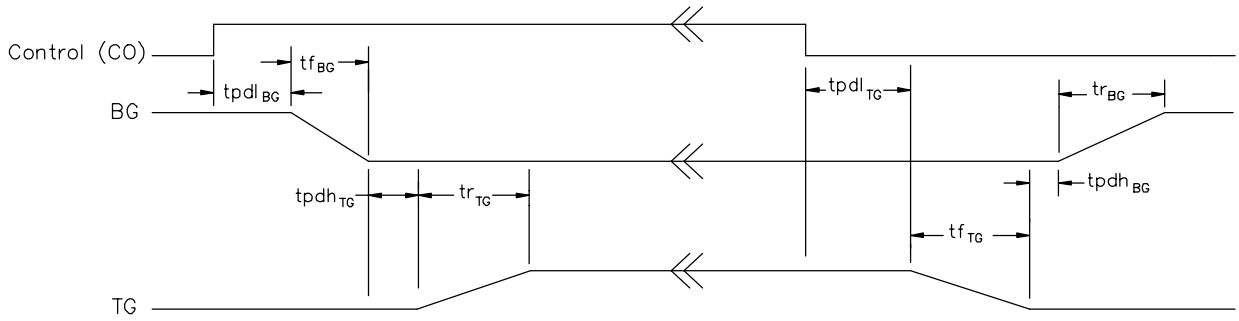
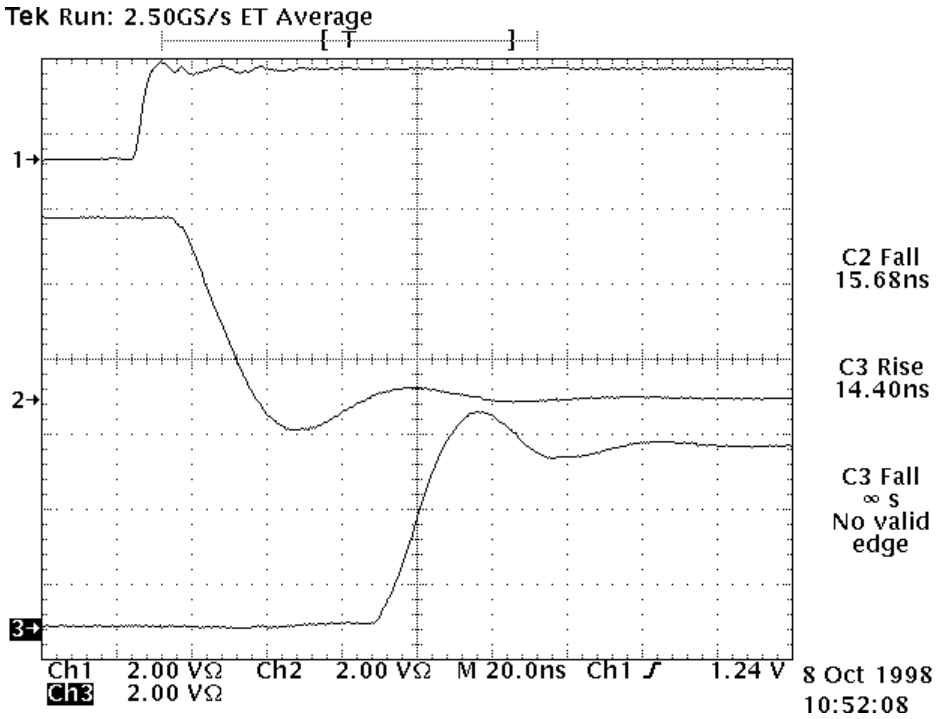


Figure 1 - Timing characteristics while driving a 3nf load at Tamb = 125°C after CO low to high transition.

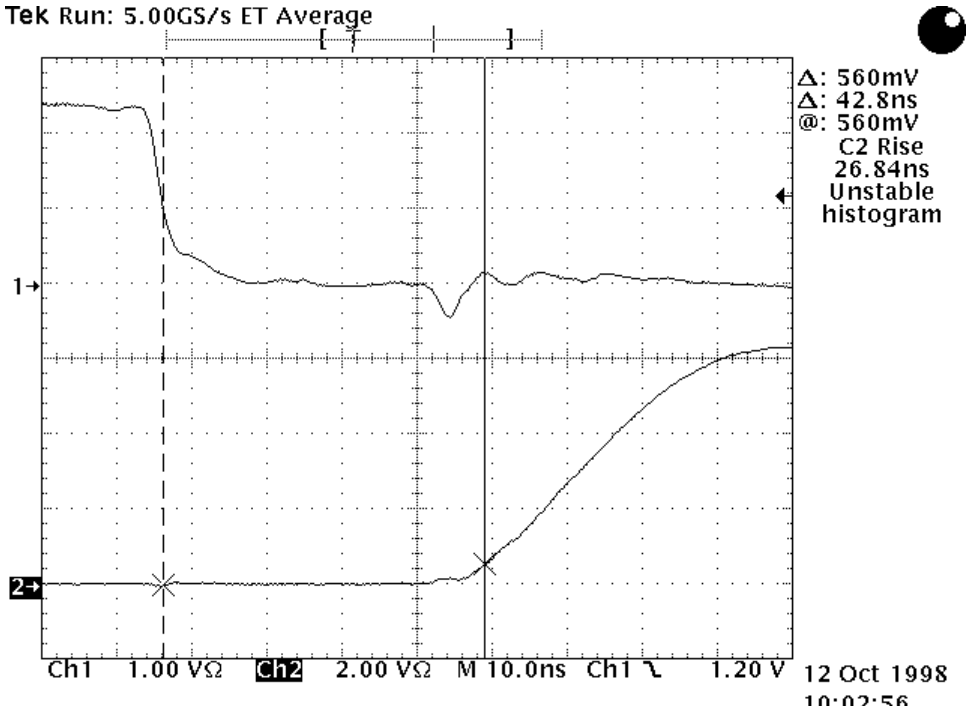


Ch1. CO input going high (start of cycle)

Ch2. BG drive

Ch3. TG drive

Cload = 3 nf
C_delay = 0



Ch1. DRN (phase node) voltage going low

Ch2. BG going high

Cload = 3 nf
C_delay = 0

Figure 2-Timing characteristics while driving a 3nf load at Tamb = 125°C after DRN voltage transition to a low voltage (DRN <1V)

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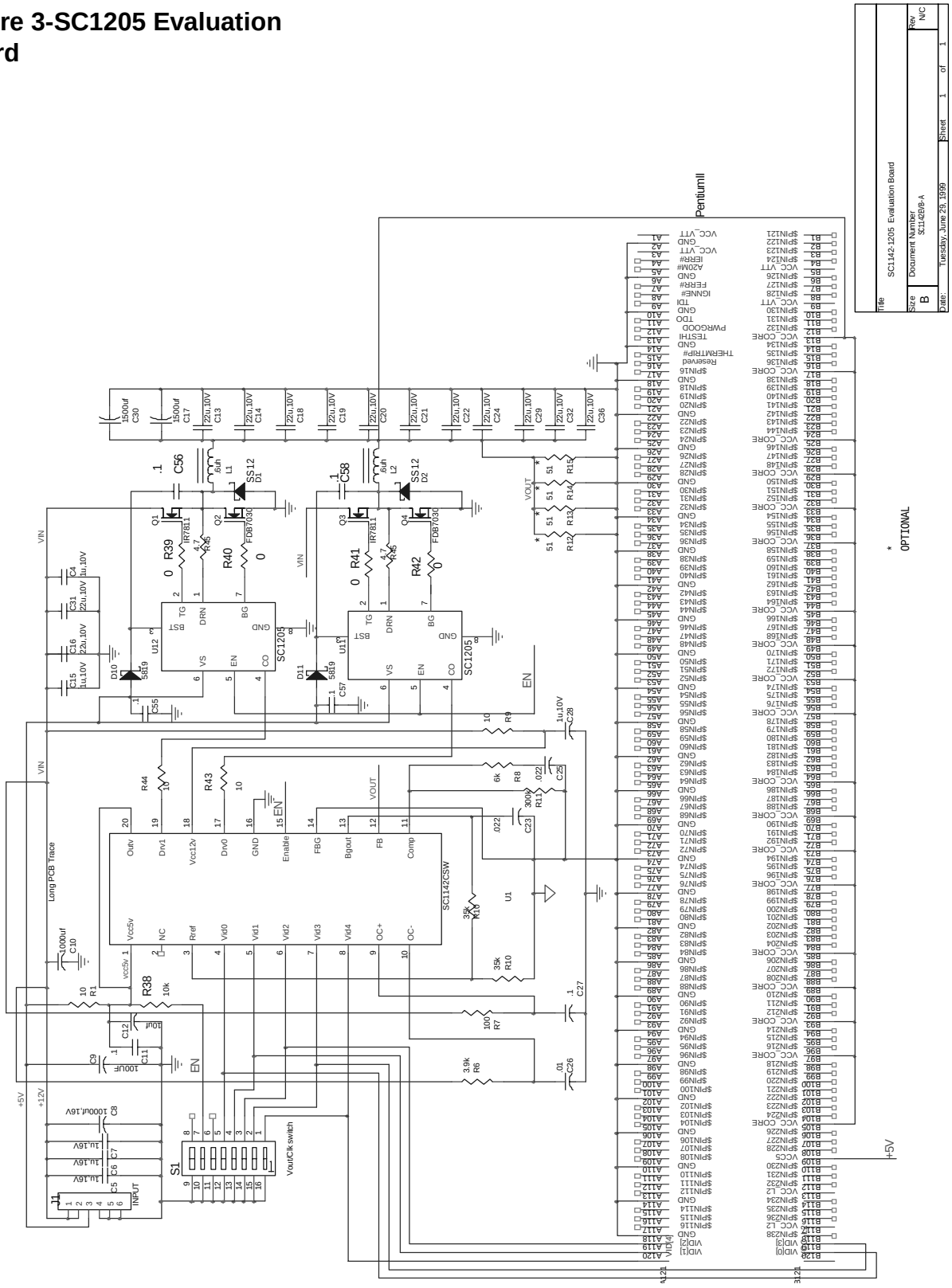
Figure 3-SC1205 Evaluation Board



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BILL OF MATERIAL

Item	Qty	Reference	Value	Manufacturer
1	3	C4,C15,C28	1u,10V, Cer.	AVX, Murata
2	3	C5,C6,C7	1u,16V, Cer.	AVX, Murata
3	1	C8	1000uF, 16V	Nichicon, any
4	1	C9	100uF	Nichicon, any
5	1	C10	1000uf	Nichicon, any
7	1	C12	10uF	Nichicon, any
8	13	C13,C14,C16,C18,C19,C20,C21,C22,C24,C29,C31,C32, C36	22u, 10V	Murata (GRM235Y5V226Z010)
9	2	C17,C30	1500uf	Nichicon, Sanyo
10	2	C23,C25	.022	Avx, any
11	1	C26	.01	Avx, any
12	6	C11,C27,C55,C56,C57,C58	.1	Avx, any
13				
14	2	D1,D2	SS12	General Instruments, any
15	2	D10,D11	5819	General Instruments, any
16	1	J1	Input	
17	2	L1,L2	.6uh	Falco, P/N: TO2508 or SDIP0804-608M (305) 662-9076
18	2	Q1,Q3	IR7811	Int. Rectifier (310) 252-7099
19	2	Q2,Q4	FDB7030	Fairchild Semi. (408) 822-2000
20	4	R1,R9,R43,R44	10	any
21	1	R6	3.9k	any
22	1	R7	100	any
23	1	R8	6k	any
24	1	R10	35k	any
25	1	R11	300k	any
26	4	R12,R13,R14,R15	51	any, Required in asynch. operation
27	1	R38	10K	any
28	4	R39,R40,R41,R42	0	any
29	1	R45	4.7	any
30	1	S1	Vout/Clk switch	Digikey
31	1	U2	Pentium II™	Slot 1 Connector
32	1	U1	SC1142CSW	Semtech, (805) 499-2111
33	2	U11,U12	SC1205S	Semtech, (805) 499-2111

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APPLICATION INFORMATION:

SC1205 is a high speed, smart dual MOSFET driver. It is designed to drive Low Rds_On power MOSFET's with ultra-low rise/fall times and propagation delays. As the switching frequencies of PWM controllers is increased to reduce power supply and Class-D amplifier volume and cost, fast rise and fall times are necessary to minimize switching losses (TOP MOSFET) and reduce Dead-time (BOTTOM MOSFET). While Low Rds_On MOSFET's present a power saving in I^2R losses, the MOSFET's die area is larger and thus the effective input capacitance of the MOSFET is increased. Often a 50% decrease in Rds_On more than doubles the effective input gate charge, which must be supplied by the driver. The Rds_On power savings can be offset by the switching and dead-time losses with a sub-optimum driver. While discrete solution can achieve reasonable drive capability, implementing shoot-through, programmable delay and other housekeeping functions necessary for safe operation can become cumbersome and costly. The SC120X family of parts presents a total solution for the high-speed, high power density applications. Wide input supply range of 4.5V-25V allows use in battery powered applications, new high voltage, distributed power servers as well as Class-D amplifiers.

THEORY OF OPERATION

The control input (CO) to the SC1205 is typically supplied by a PWM controller that regulates the power supply output. (See Application Evaluation Schematic, Figure 3). The timing diagram demonstrates the sequence of events by which the top and bottom drive signals are applied. The shoot-through protection is implemented by holding the bottom FET off until the voltage at the phase node (intersection of top FET source, the output inductor and the bottom FET drain) has dropped below 1V. This assures that the top FET has turned off and that a direct current path does not exist between the input supply and ground, a condition which both the top and bottom FET's are on momentarily. The top FET is also prevented from turning on until the bottom FET is off. This time is internally set to 20ns.

LAYOUT GUIDELINES

As with any high speed , high current circuit, proper layout is critical in achieving optimum performance of the SC1205. The Evaluation board schematic (Refer to figure 3) shows a two-phase synchronous design with all surface mountable components.
While components connecting to EN are relatively non-critical, tight placement and short,wide traces must be used in layout of The Drives, DRN, and especially PGND pin. The top gate driver supply voltage is provided by bootstrapping the +5V supply and adding it the phase node voltage (DRN). Since the bootstrap capacitor supplies the charge to the top gate, it must be less than .5" away from the SC1205. Ceramic X7R capacitors are a good choice for supply bypassing near the chip. The Vcc pin capacitor must also be less than .5" away from the SC1205. The ground node of this capacitor, the SC1205 PGND pin and the Source of the bottom FET must be very close to each other, preferably with common PCB copper land with multiple vias to the ground plane (if used). The parallel Shottkey must be physically next to the Bottom FETS Drain and source. Any trace or lead inductance in these connections will drive current way from the Shottkey and allow it to flow through the FET's Body diode, thus reducing efficiency.

PREVENTING INADVERTENT BOTTOM FET TURN-ON

At high input voltages, (12V and greater) a fast turn-on of the top FET creates a positive going spike on the Bottom FET's gate through the Miller capacitance, crss of the bottom FET. The voltage appearing on the gate due to this spike is:

Vspike=Vin*crss/(Crass+ciss)

Where Ciss is the input gate capacitance of the bottom FET. This is assuming that the impedance of the drive path is too high compared to the instantaneous impedance of the capacitors. (since dV/dT and thus the effective frequency is very high). If the BG pin of the SC1205 is very close to the bottom FET, Vspike will be reduced depending on trace inductance, rate of rise of current,etc.

While not shown in Figure 3, a capacitor may be added from the gate of the Bottom FET to its source, preferably less than .1" away. This capacitor will be added to Ciss in the above equation to reduce the effective spike voltage, Vspike.
The selection of the bottom MOSFET must be done with attention paid to the Crss/Ciss ratio. A low ratio reduces the Miller feedback and thus reduces Vspike. Also MOSFETs with higher Turn-on threshold voltages will conduct at a higher voltage and will not turn on during the spike. The MOSFET shown in the schematic (figure 3) has a 2 volt threshold and will require approximately 4.5 volts Vgs to be conducting, thus reducing the possibility of shoot-through. A zero ohm bottom FET gate resistor will obviously help keeping the gate voltage low.
Ultimately, slowing down the top FET by adding gate resistance will reduce di/dt which will in turn make the effective impedance of the capacitors higher, thus allowing the BG driver to hold the bottom gate voltage low. It does this at the expense of increased switching times (and switching losses) for the top FET.

RINGING ON THE PHASE NODE

The top MOSFET source must be close to the bottom MOSFET drain to prevent ringing and the possibility of the phase node going negative. This frequency is determined by:

F_{ring} =1/(2¶* Sqrt(L_{st}*Coss))

Where:

L_{st} = The effective stray inductance of the top FET added to trace inductance of the connection between top FET's source and the bottom FET's drain added to the trace resistance of the bottom FET's ground connection.
Coss=Drain to source capacitance of bottom FET. If there is a Shottkey used, the capacitance of the Shottkey is added to the value.

Although this ringing does not pose any power losses due to a fairly high Q, it could cause the phase node to go too far negative, thus causing improper operation, double pulsing or at worst driver damage. On the SC1205, the drain node, DRN, can go as far as 2V below ground without affecting operation or sustaining damage.
The ringing is also an EMI nuisance due to its high resonant frequency. Adding a capacitor, typically 1000-2000pf, in parallel with Coss of the bottom FET can often eliminate the EMI issue. If double pulsing is caused due to excessive ringing, placing 4.7-10 ohm resistor between the phase node and the DRN pin of the SC1205 should eliminate the double pulsing. Proper layout will guarantee minimum ringing and eliminate the need for external components. Use of SO-8 or other surface mount MOSFETs while increasing thermal resistance, will reduce lead inductance as well as radiated EMI.

OVER TEMP SHUTDOWN

The SC1205 will shutdown by pulling both driver if its junction temperature, Tj, exceeds 165 °C.

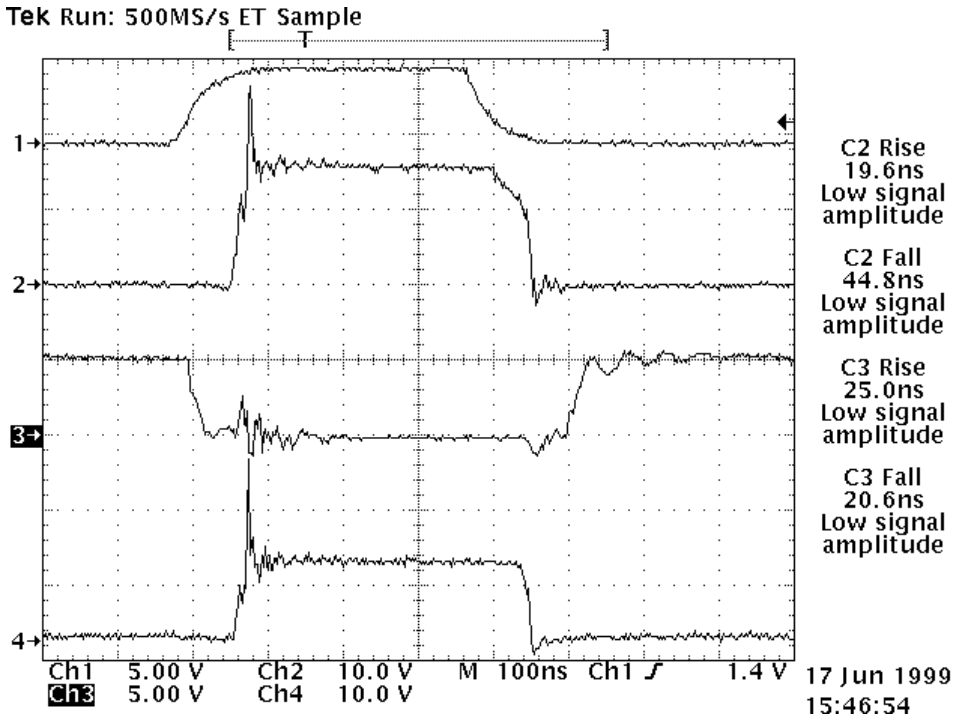

Figure 4-Timing diagram:

Ch1:CO input

Ch2:TG drive

Ch3:BG non-overlap drive

Ch4:phase node
Iout=20A (10A/phase)
Refer to Eval. Schematic (fig.3)

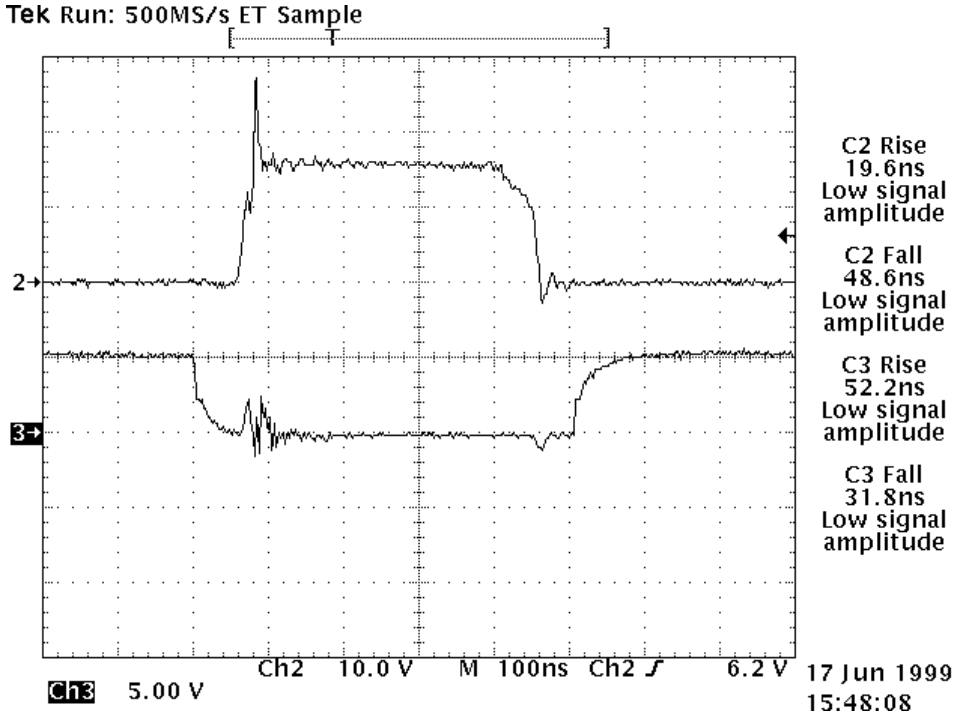

Figure 5-Timing diagram: Rise/Fall times

Ch1:TG drive

Ch2:BG drive

Cursor:$Tpdh_{TG}$

Iout=20A (10A/phase)
Refer to Eval. Schematic (fig.3)

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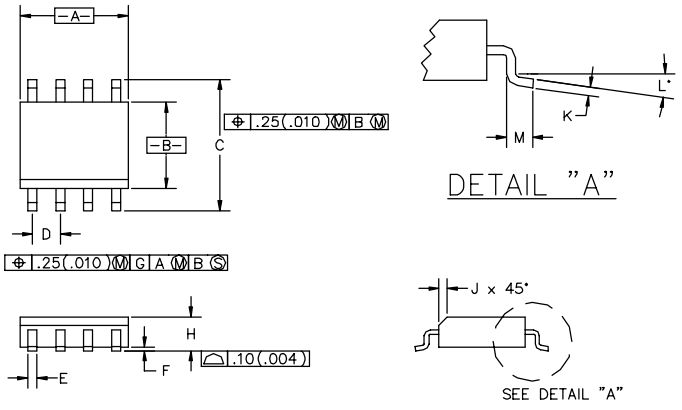
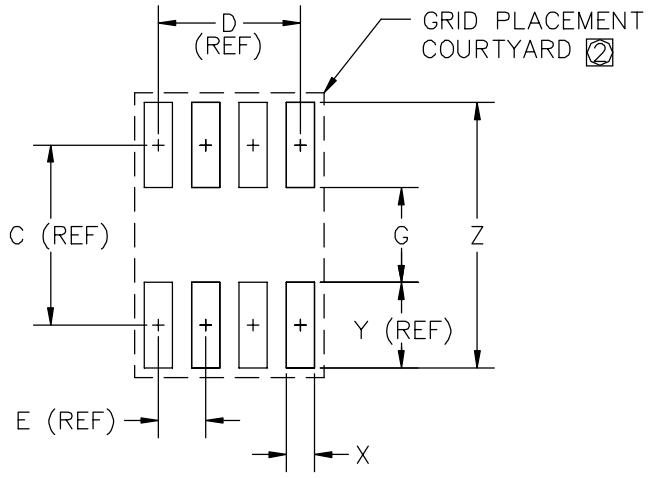
OUTLINE DRAWING - SO-8



JEDEC
REF: MS-012AA

DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.188	.197	4.80	5.00	
B	.149	.158	3.80	4.00	
C	.228	.244	5.80	6.20	
D	.050	BSC	1.27	BSC	
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.011	.019	0.28	0.48	
K	.007	.010	.19	.25	
L	0°	8°	0°	8°	
M	.016	.050	0.40	1.27	

LAND PATTERN - SO-8



DIMENSIONS (1)					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.19	–	5.00	–
D	–	.15	–	3.81	–
E	–	.05	–	1.27	–
G	.10	.11	2.60	2.80	–
X	.02	.03	.60	.80	–
Y	–	.09	–	2.40	–
Z	–	.29	7.20	7.40	–

(2) GRID PLACEMENT COURTYARD IS 12x16 ELEMENTS (6 mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

(1) CONTROLLING DIMENSION: MILLIMETERS

ECN99-742