

DLP5531-Q1 0.55 2:1 1.3-MP Automotive DMD

1 Features

- Qualified for Automotive Applications
 - -40°C to 105°C Operating DMD Array Temperature Range
- Optical Light Switching Component for the DLP5531-Q1 Automotive Chipset:
 - DLP5531-Q1 DMD
 - DLPC230-Q1 DMD Controller
 - TPS99000-Q1 System Management and Illumination Controller
- 0.55-inch Diagonal Micromirror Array
 - $7.6\text{-}\mu\text{m}$ Micromirror Pitch
 - $\pm 12^{\circ}$ Micromirror Tilt Angle (Relative to Flat State)
 - Bottom Illumination for Optimal Efficiency and Optical Engine Size
 - 1.3-Megapixel Array Configured in 2:1 Aspect Ratio Enabling High Resolution and Wide Aspect Ratio Automotive Applications
 - Compatible With LED or Laser
- DMD Interface
 - 600-MHz Sub-LVDS DMD Interface for Low Power and Emission
 - 10-kHz DMD Refresh Rate Over Temperature Extremes
- Thermally Efficient Hermetic Package Provides Low Thermal Resistance of 1.3°C/W From Array to Back of Package

2 Applications

- High Resolution Headlight

3 Description

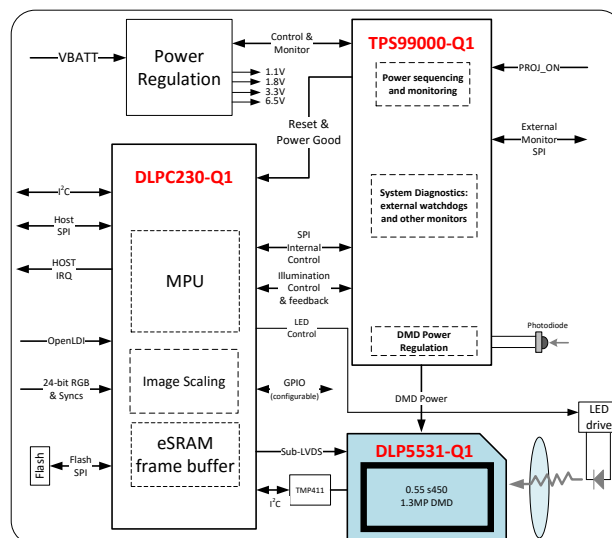
The DLP5531-Q1 Automotive DMD, combined with the DLPC230-Q1 DMD controller and TPS99000-Q1 system management and illumination controller, provides the capability to achieve high performance high resolution headlight systems. The 2:1 aspect ratio supports very wide aspect ratio designs, and the 1.3-megapixel resolution enables high resolution symbol projection and adaptive driving beam applications. The DLP5531-Q1 has more than 3 times the optical throughput than the preceding DLP3030-Q1 Automotive DMD. The DLP5531-Q1 Automotive DMD micromirror array is configured for bottom illumination which enables highly efficient and more compact optical engine designs. The S450 package has low thermal resistance to the DMD array to enable more efficient thermal solutions. Note, this datasheet pertains to the specifications and application use of this DMD in the Headlight application. Please see the DLP5530-Q1 datasheet (DLPS073) for HUD specification and application information.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP5531-Q1	FYK (149)	22.30 mm × 32.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

DLP® DLP5531-Q1 Chipset System Block Diagram



4 Device and Documentation Support

4.1 Device Support

4.1.1 Device Nomenclature

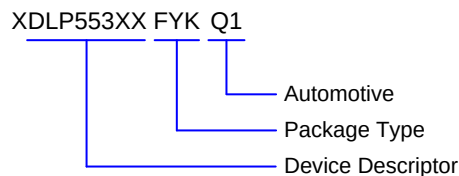


Figure 1. Part Number Description

4.1.2 Device Markings

The device marking includes the legible character string GHJJJK DLP5531XFYKQ1. GHJJJK is the lot trace code. DLP5531XFYKQ1 is the device marking.

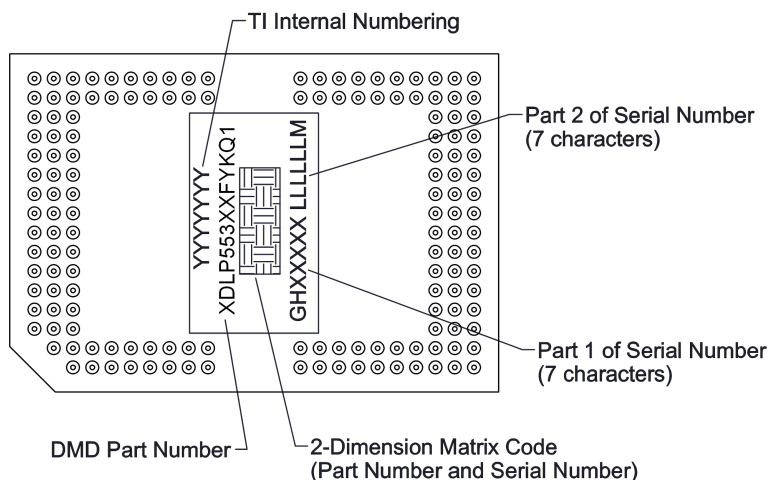


Figure 2. DMD Marking

4.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DLP5531-Q1	TBD	TBD	TBD	TBD	TBD
DLPC230-Q1	TBD	TBD	TBD	TBD	TBD
TPS99000-Q1	TBD	TBD	TBD	TBD	TBD

4.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

4.4 Trademarks

E2E is a trademark of Texas Instruments.

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All other trademarks are the property of their respective owners.

4.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

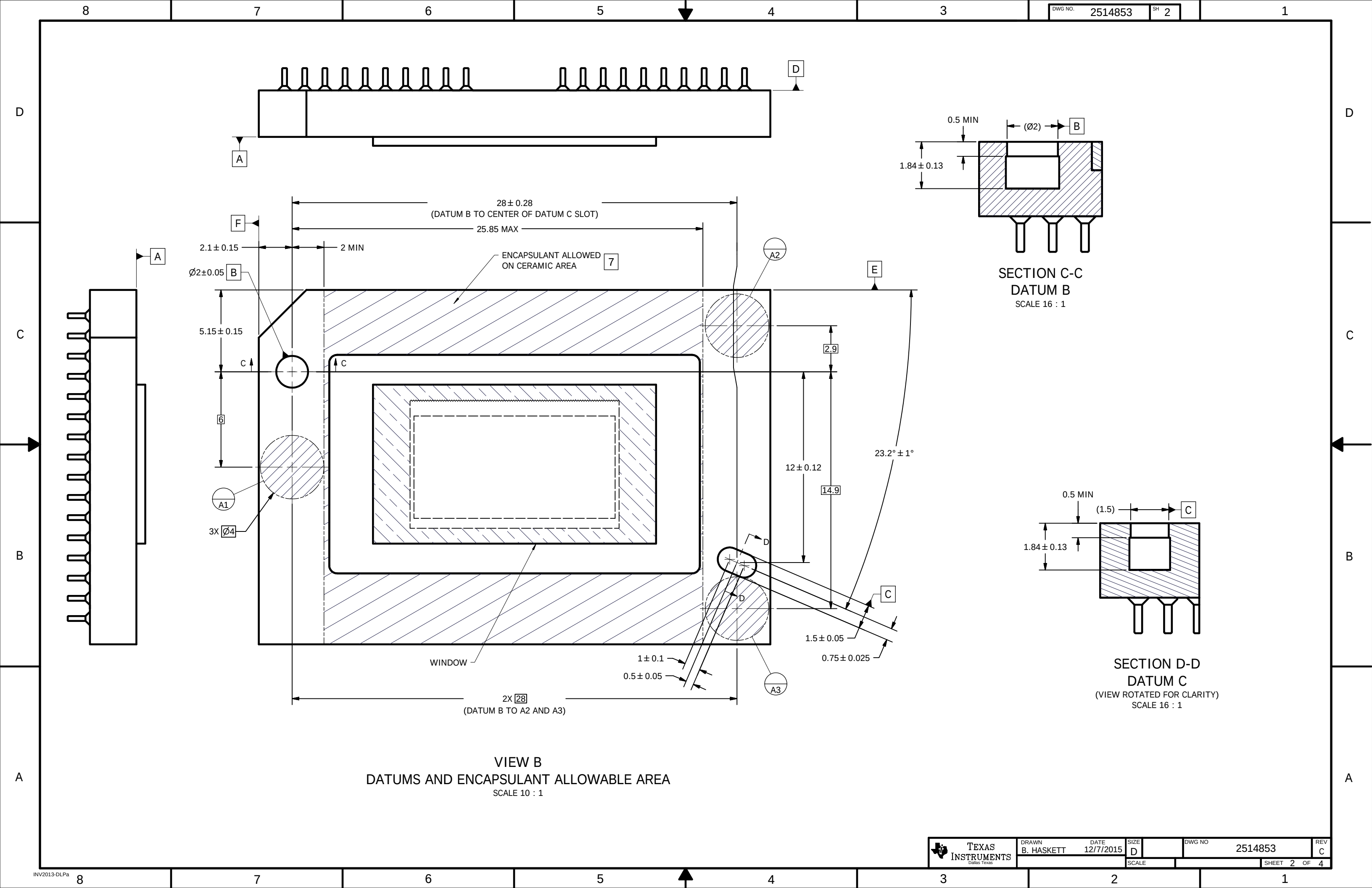
4.6 Glossary

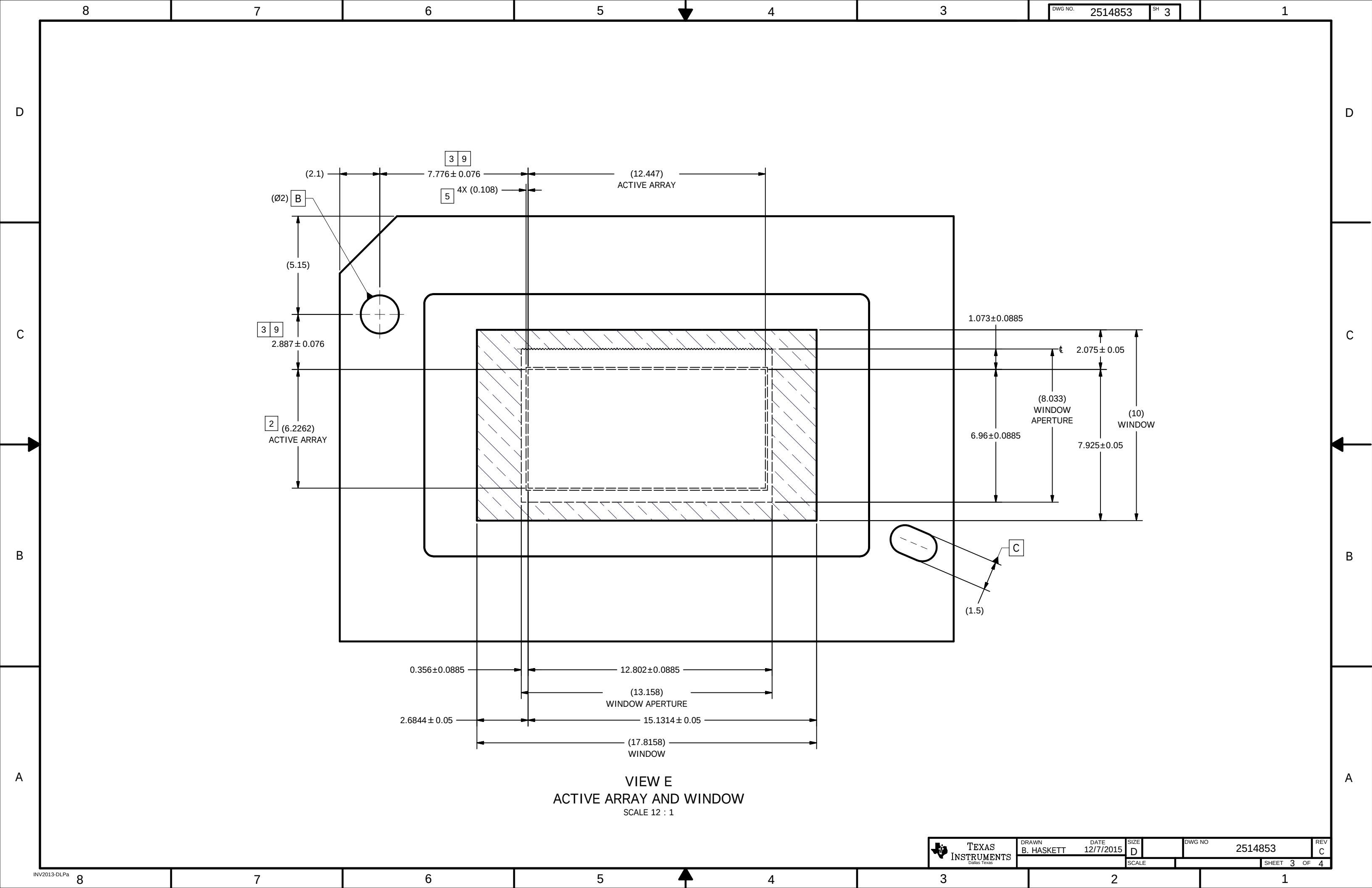
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.





VIEW E
ACTIVE ARRAY AND WINDOW
SCALE 12 : 1

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DWG NO. 2514853

SH 4

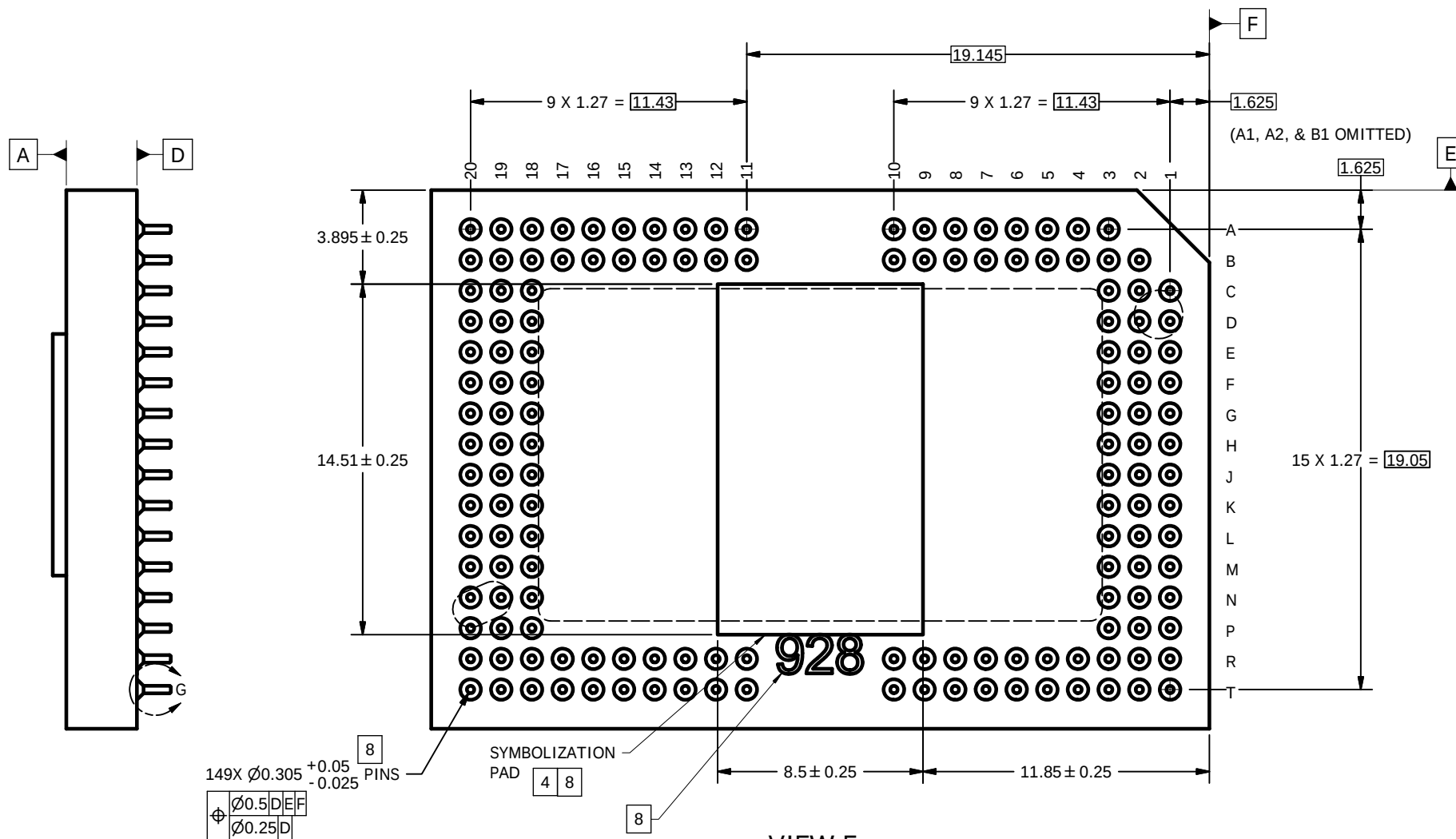
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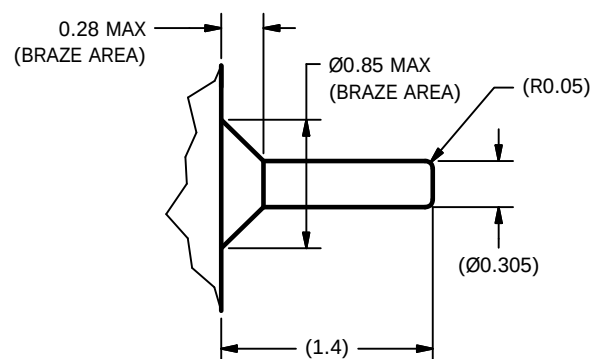
C

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VIEW F
PINS AND SYMBOLIZATION PAD
SCALE 8 : 1



DETAIL G
PIN AND BRAZE DIMENSIONS
149 PLACES
SCALE 40 : 1

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP5531AFYKQ1	PREVIEW	CPGA	FYK	149	33	RoHS & Green			-40 to 105		
XDLP553XBFYKQ1	ACTIVE	CPGA	FYK	149	1	RoHS & Green			-40 to 105		Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

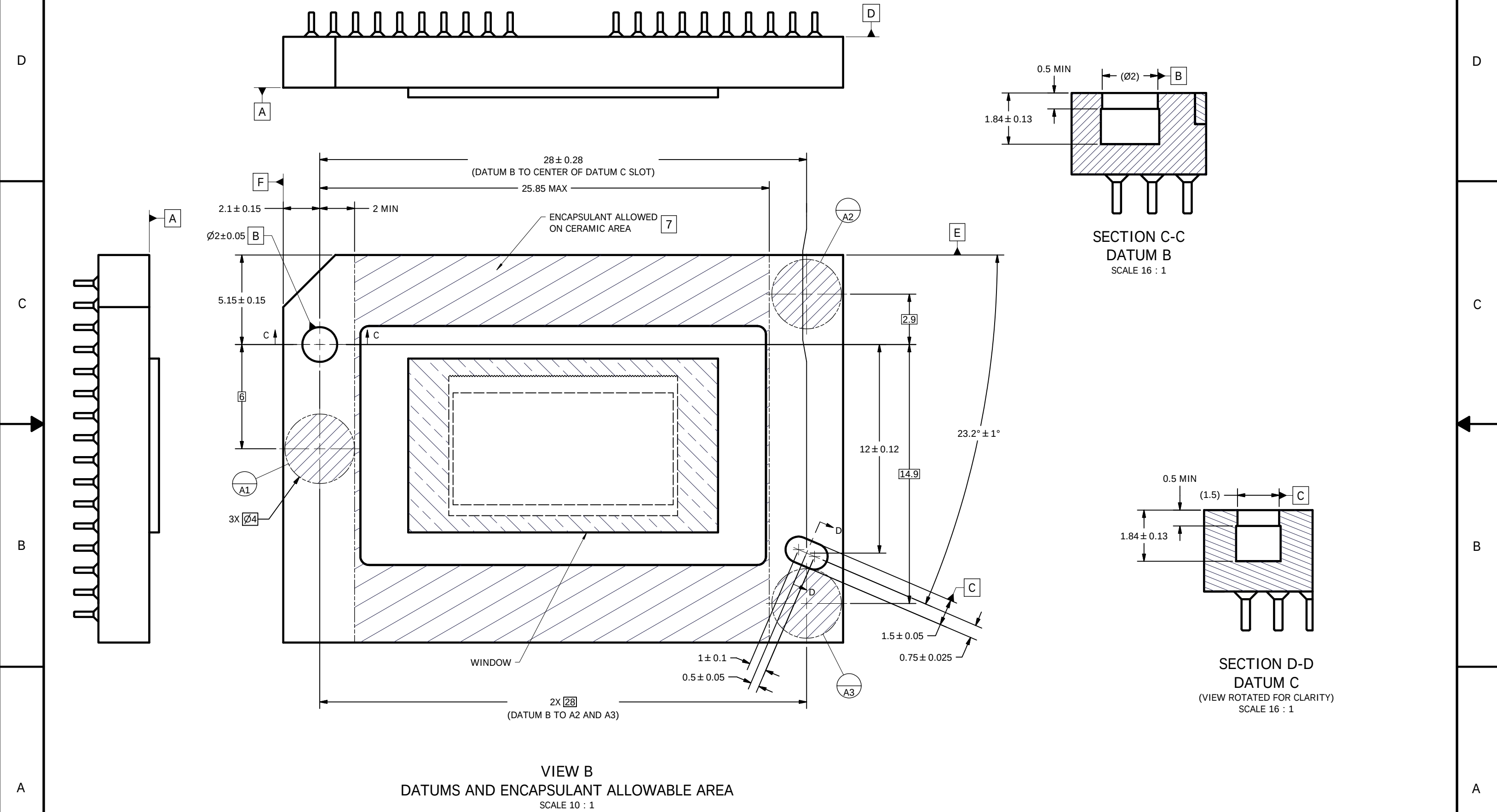
⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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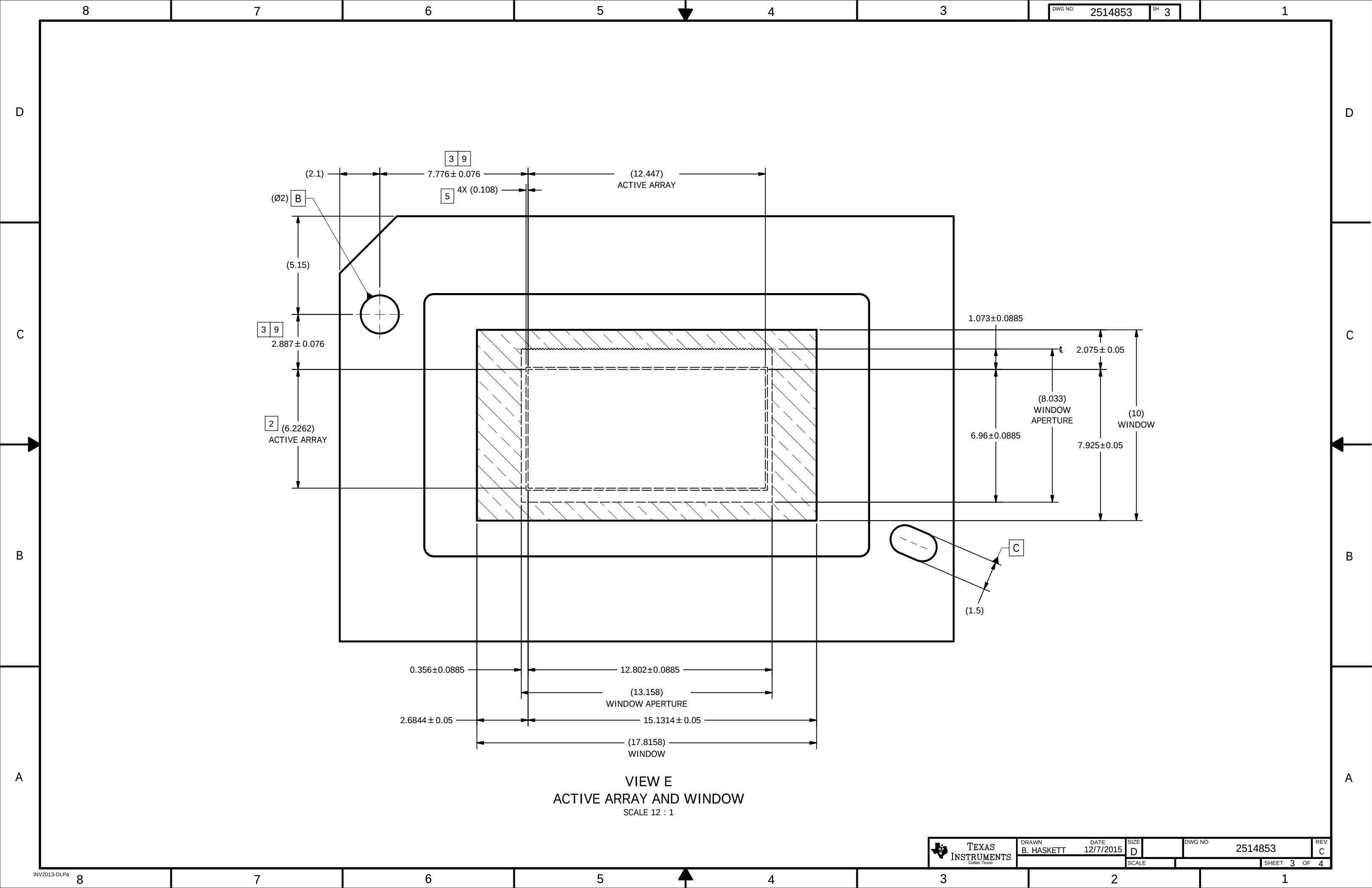
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SECTION C-C
DATUM B
SCALE 16 : 1

SECTION D-D
DATUM C
(VIEW ROTATED FOR CLARITY)
SCALE 16 : 1

VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 10 : 1



VIEW E
ACTIVE ARRAY AND WINDOW
SCALE 12 : 1

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DWG NO. 2514853

SH 4

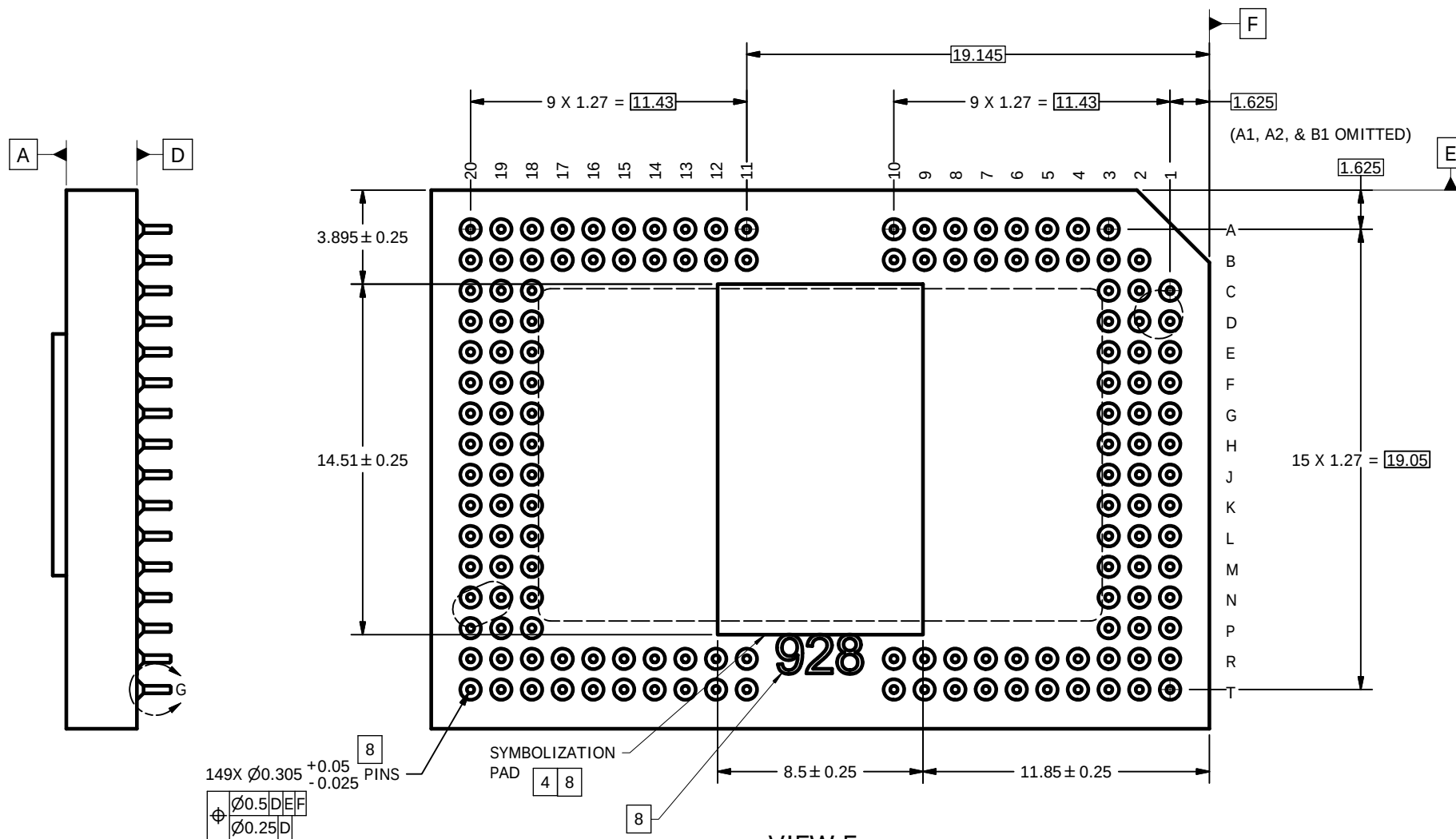
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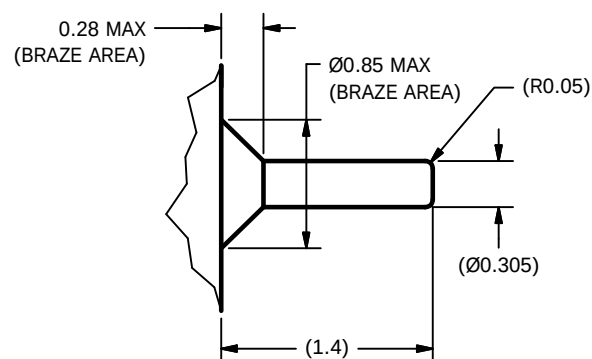
C

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VIEW F
PINS AND SYMBOLIZATION PAD
SCALE 8 : 1



DETAIL G
PIN AND BRAZE DIMENSIONS
149 PLACES
SCALE 40 : 1

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