Unipolar 2-Phase Microstepping Motor Driver IC

Features and Benefits

- Power supply voltage, V_{BB}, 46 V maximum, 10 to 44 V normal operating range
- 18.6 × 9.9 mm package footprint
- Logic supply voltage, V_{DD}, 3.3 to 5.5 V
- Maximum output current: 1.5 A
- Four NMOS output MOSFETs, $R_{DS(on)}$ = 0.25 Ω typical
- Built-in sequencer
- Simplified clock-in stepping control
- Full- and half-stepping and $^1/_4$, $^1/_8$, and $^1/_{16}$ microstepping
- Surface mount type 44-pin molded package for automatic assembly and low profile
- Self-excitation PWM current control with fixed off-time
- Microstepping off-time adjusted automatically by step

Continued on the next page…

Package: 44-pin HSOP surface mount

Not to scale

Description

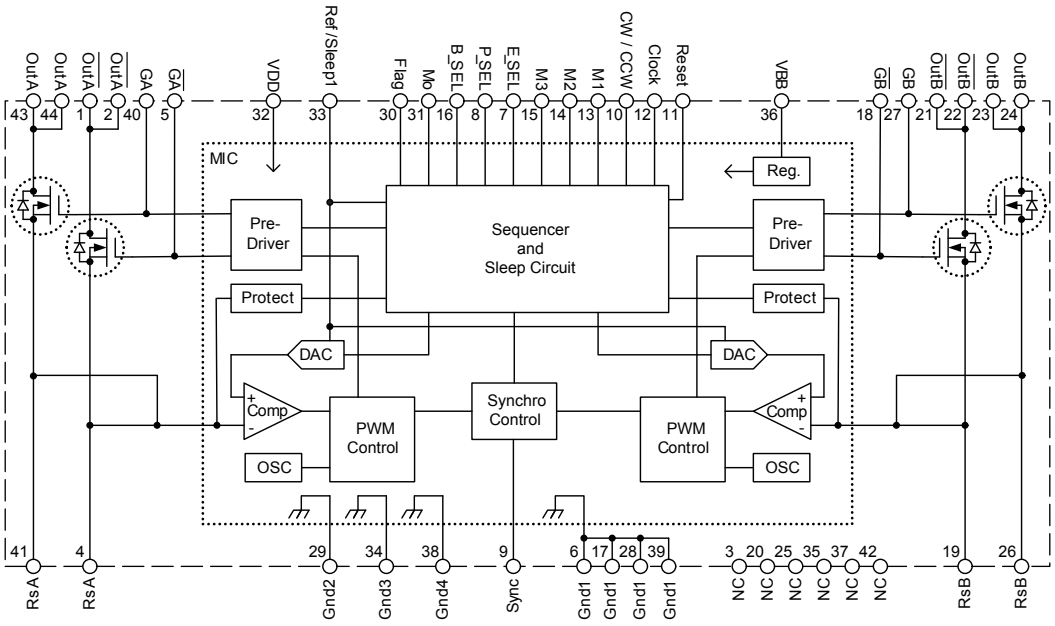
The SI-7321M constant-current mode motor driver IC features efficient unipolar driver design for full- and half-step operation, and $^1/_4$, $^1/_8$, and $^1/_{16}$ microstepping. The clock-in type input interface allows simplified control logic, with the flexibility of sequencer timing using either rising Clock edge only or both rising and falling edges. Additional flexibility is provided by user-configurable blanking time, and load circuit short or open protection (patents granted in Japan and the U.S.A.). Along with inputs for built-in sense current detection, these features minimize power losses.

The device has a multi-chip internal structure for lower thermal resistance. The control IC (MIC) and the four power elements (MOSFET) are all separate ICs. The package (HSOP) provides wide output terminals at each corner, further enhancing device thermal dissipation.

The built-in excitation distribution circuit (sequencer) allows motor control using only the Clock signal for simple operations (forward, reverse, hold), with motor speed control by frequency input into Clock pin, and rotation direction control by a dedicated logic input. This eliminates logic signal lines required for conventional phase-input methods, and reduces demand on heavily-used CPUs.

Low-power sleep mode, as well as reduced power during PWM off-time maximize energy savings.

Functional Block Diagram



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http://www.sanken-ele.co.jp/en/

Features and Benefits (continued)

reference current ratio
- Built-in synchronous rectifying circuit reduces losses at PWM switch-off
- Synchronous PWM chopping function prevents motor noise in Hold mode
- Built-in current sensing for each phase, set externally
- Dual sleep modes reduce IC input current in stand-by state
- Built-in protection against motor coil opens and shorts
- User-configurable operation options, set by external logic input:
  - Blanking time: 1.8 µs or 3.6 µs
  - Sequencer timing on Clock input rising (POS) edge or both rising and falling (POS/NEG) edges
  - Protection features enable or disable

Selection Guide

Part Number	Package	Packing
SI-7321M	SOP 44-pin surface mount	2000 pieces/ 13-in. reel

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_M		46	V
Main Power Supply Voltage	V_{BB}		46	V
Logic Supply Voltage	V_{DD}		6	V
Output Current	I_O	Current ratio mode F; output current rating may be limited by duty cycle, ambient temperature, and heat sinking; under any set of conditions, do not exceed the specified junction temperature, T_J	1.5	A
Logic Input Voltage	V_{IN}		–0.3 to V_{DD}+0.3	V
REF Input Voltage	V_{REF}		–0.3 to V_{DD}+0.3	V
Sense Voltage	V_{RS}	t_w < 1 µs not considered (t_w = dead time after the sense voltage exceeds ±2 V)	±2	V
Power Dissipation	P_D	Using Sanken evaluation board at 25°C; rating significantly affected by the application PCB layout	3.5	W
Junction Temperature	T_J		150	°C
Ambient Temperature	T_A		–20 to 80	°C
Storage Temperature	T_{stg}		–30 to 150	°C

Recommended Operating Conditions

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Load Supply Voltage	V_M		–	–	44	V
Main Power Supply Voltage	V_{BB}		10	–	44	V
Logic Supply Voltage	V_{DD}	Surge voltage at VDD pin should be less than ±0.5 V to avoid malfunctioning in operation	3.3	–	5.5	V
REF Input Voltage	V_{REF}	Protection features disabled	0.04	–	1.0	V
		Protection features enabled	0.04	–	0.5	V
Case Temperature	T_C	Measured at center of case on branded side	–	–	85	°C

All performance characteristics given are typical values for circuit or system baseline design only and are at the nominal operating voltage and an ambient temperature, T_A, of 25°C, unless otherwise stated.

ELECTRICAL CHARACTERISTICS, valid at T_A = 25°C, V_{BB} = 24 V, V_{DD} = 5 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Main Power Supply Current	I_{BB}	Normal operation	–	–	15	mA
	I_{BBS}	Sleep1 or Sleep2 modes	–	–	100	µA
Logic Supply Current	I_{DD}		–	–	5	mA
MOSFET Breakdown Voltage	V_{DSS}	V_{BB} = 44 V, I_{DS} = 1 mA	100	–	–	V
MOSFET Output On-Resistance	$R_{DS(on)}$	I_{DS} = 1.5 A	–	0.25	0.4	Ω
MOSFET Body Diode Forward Voltage	V_F	I_F = 1.5 A	–	0.95	1.2	V
Maximum Clock Frequency[1]	f_{clk}	Clock duty cycle = 50%, at rising clock edge	250	–	–	kHz
Logic Input Voltage	V_{IL}		–	–	0.25 × V_{DD}	V
	V_{IH}		0.75 × V_{DD}	–	–	V
Logic Input Current	I_{IL}		–	±1	–	µA
	I_{IH}		–	±1	–	µA
REF Input Voltage Range[2]	V_{REF}	Protection functions disabled	0.04	–	1.5	V
		Protection functions enabled	0.04	–	0.6	V
	V_{REFS}	Sleep1 mode, output off, sequencer enabled, I_{BBS} within specification	2.0	–	V_{DD}	V
REF Input Current	I_{REF}	V_{REF} = 0 to V_{DD}	–	±10	–	µA
SENSE Voltage	V_{SENSE}	V_{REF} = 0.2 V, current ratio mode F	–	0.2	–	V
SENSE Current	I_{SENSE}		–	±10	–	µA
Overcurrent Protection Threshold Voltage	V_{OCP}	Motor coil short circuit, $V_{SENSE} \geq V_{OCP}$	0.65	0.7	0.75	V
Flag Pin Logic Output Voltage	V_{FLAGL}	I_{FLAGL} = 1.25 mA	–	–	1.25	V
	V_{FLAGH}	I_{FLAGH} = –1.25 mA	V_{DD} – 1.25	–	–	V
Flag Pin Logic Output Current[3]	I_{FLAGL}		–	–	1.25	mA
	I_{FLAGH}		– 1.25	–	–	mA
Mo Pin Logic Output Voltage	V_{MOL}	I_{MOL} = 1.25 mA	–	–	1.25	V
	V_{MOH}	I_{MOH} = –1.25 mA	V_{DD} – 1.25	–	–	V
Mo Pin Logic Output Current[3]	I_{MOL}		–	–	1.25	mA
	I_{MOH}		– 1.25	–	–	mA

[1]Operation at a step frequency greater than the specified minimum value is possible but not warranted.
[2]V_{REF} setting range affected by whether or not protection features are enabled.
[3]Negative current is defined as coming out of the specified pin.

STEPPING CHARACTERISTICS valid at T_A = 25°C, V_{BB} = 24 V, V_{DD} = 5 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Step Reference Current Ratio	Mode F	V_{REF} = V_{RSx} = 100 %, V_{REF} = 0.04 to 1.5 V	–	100.0	–	%
	Mode E		–	98.1	–	%
	Mode D		–	95.7	–	%
	Mode C		–	92.4	–	%
	Mode B		–	88.2	–	%
	Mode A		–	83.1	–	%
	Mode 9		–	77.3	–	%
	Mode 8		–	70.7	–	%
	Mode 7		–	63.4	–	%
	Mode 6		–	55.5	–	%
	Mode 5		–	47.1	–	%
	Mode 4		–	38.2	–	%
	Mode 3		–	29.0	–	%
	Mode 2		–	19.5	–	%
	Mode 1		–	9.8	–	%
Sleep-Enable Recovery Time	t_{SE}	Sleep1 and Sleep2 modes	100	–	–	µs
Switching Time	t_{con}	Measured from Clock edge to output on	–	2.0	–	µs
	t_{coff}	Measured from Clock edge to output off	–	1.5	–	µs
PWM Minimum On-Time	$t_{on(min)}$	B_SEL = low	–	1.8	–	µs
		B_SEL = high	–	3.6	–	µs
PWM Off-Time	t_{off1}	Current ratio modes 8 through F	–	13	–	µs
	t_{off2}	Current ratio modes 4 through 7	–	9.5	–	µs
	t_{off3}	Current ratio modes 1 through 3	–	7.5	–	µs
Load Disconnection Undetected Time	t_{opp}	Measured from PWM off	1.5	2	2.5	µs

Temperature Increase Relationship

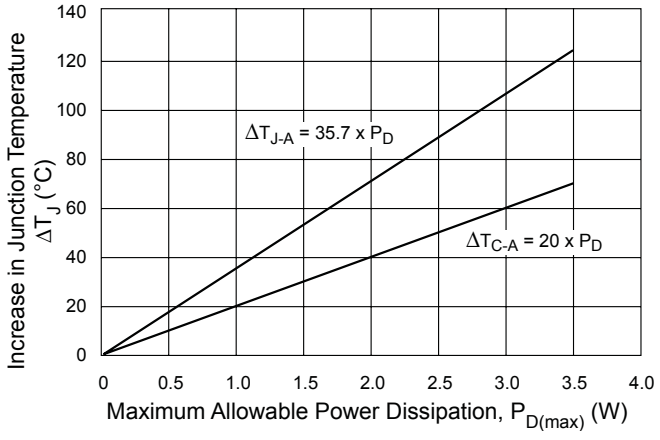


Table 1. Truth Table for Common Input Pins

Pin Name	Logic Level	
	Low	High
Reset	Normal operation	Logic reset
CW/CCW	Forward	Reverse
M1	Commutation / Sleep2 function (see table 2)	
M2		
M3		
Ref/Sleep1	Normal operation / Sleep1 function (see Reference Voltage Ranges section)	
Sync	Asynchronous PWM control	Synchronous PWM control
B_SEL	Short Blanking Time (1.8 µs)	Long Blanking Time (3.6 µs)
E_SEL	Clock input: POS/NEG edge 	Clock input: POS edge 
P_SEL	Protection circuits enabled	Protection circuits disabled

Table 2. Truth Table for Commutation/Sleep2 Function

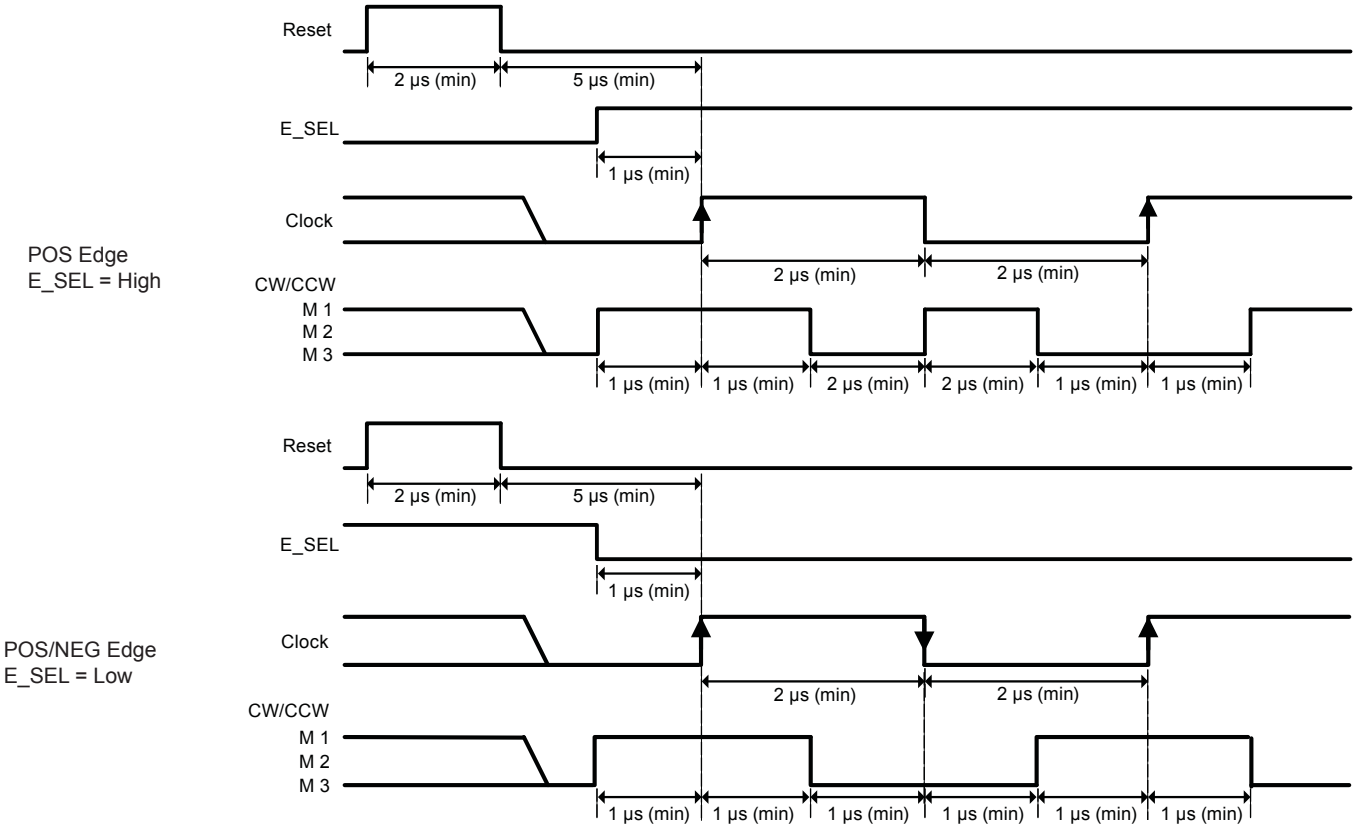
Input Pins			Operation Mode		Current Ratio Mode
M1	M2	M3	Phases*	Stepping	
L	L	L	2	Full	8 only
H	L	L	2	Full	F only
L	H	L	1-2	Half	8, F
H	H	L	1-2	Half	F
L	L	H	W1-2	Quarter	4, 8, C, F
H	L	H	2W1-2	Eighth	2, 4, 6, 8, A, C, E, F
L	H	H	4W1-2	Sixteenth	1 through F
H	H	H	Sleep2 Mode Enable		–

*W means "double"

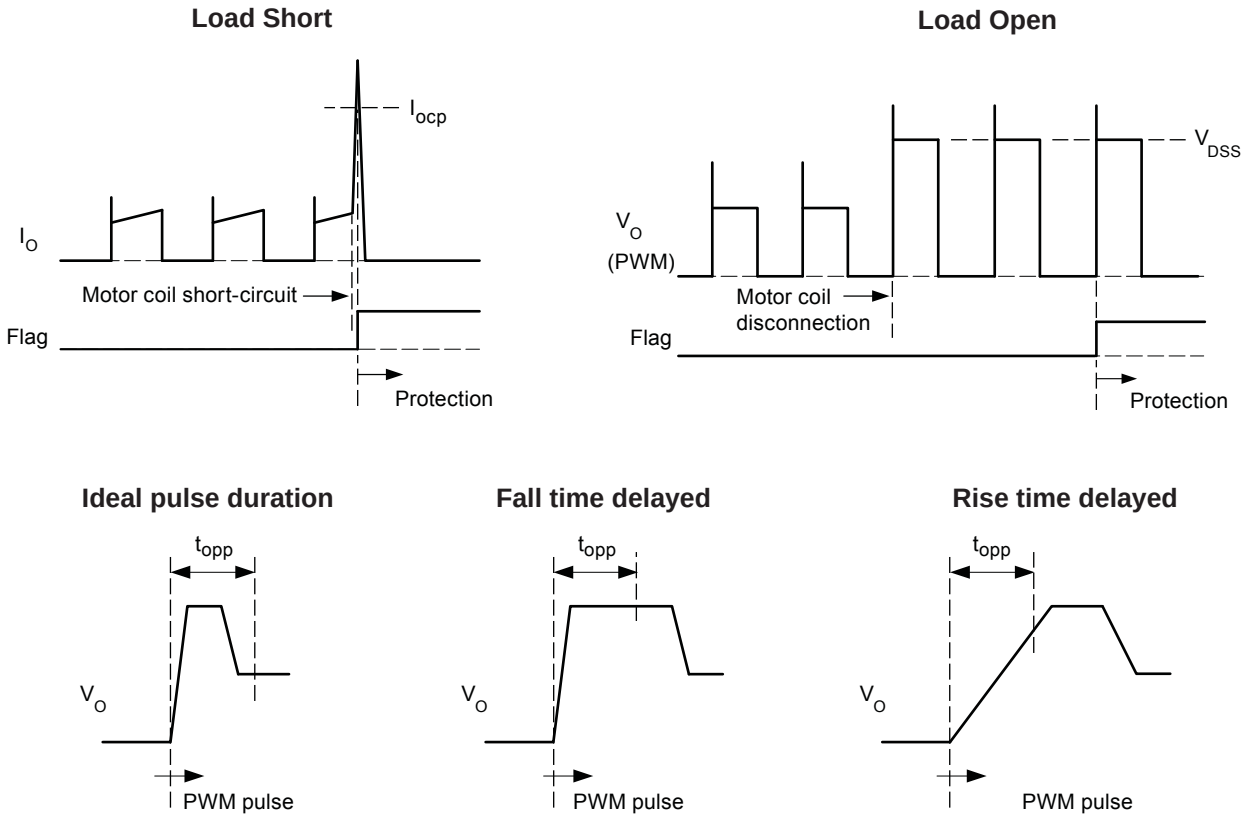
Table 3. Truth Table for Monitor Outputs

Pin Name	Low Level	High Level
Mo	Not operating in 2-Phase Excitation	Operating in 2-Phase Excitation
Flag	Normal operation	Protection circuit operating

Step Timing Options



Protection Circuits Operation



The protection functions could operate even if the fault has not occurred; for example, if the load has not actually been disconnected. This can happen when the negative edge of the PWM pulse occurs after the Load Disconnection Undetected Time, t_{opp}, because the negative edge has been boosted by the surge noise generated after PWM is turned off (center panel). It can also occur when the rise time of the pulse is delayed long enough that t_{opp} occurs before the pulse has reached full amplitude (right panel).

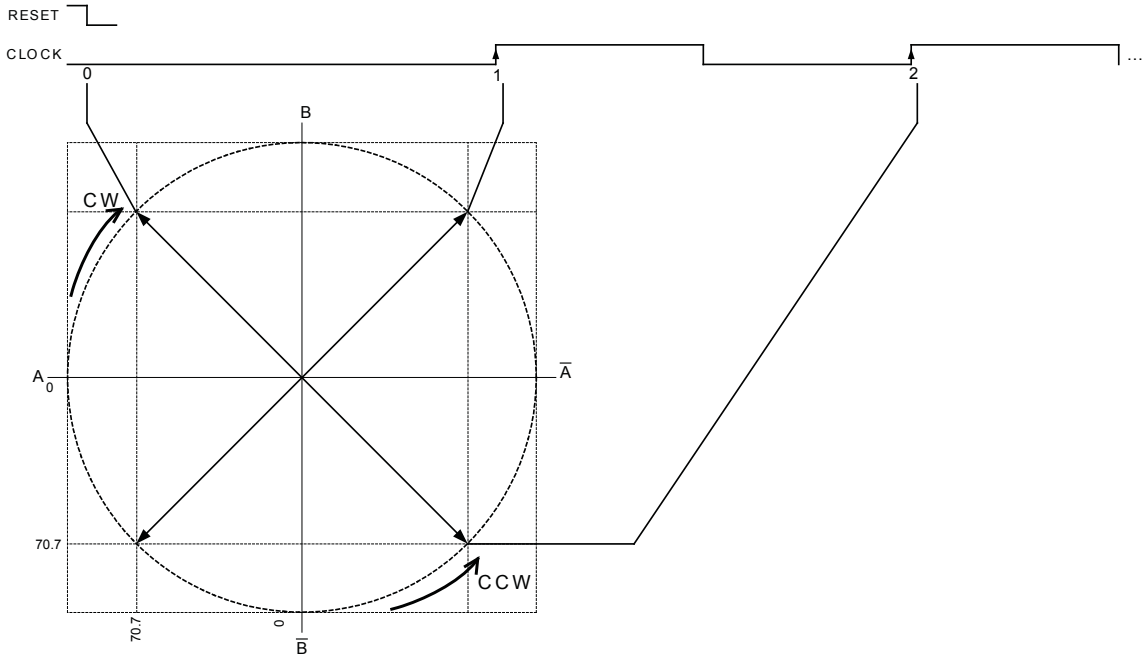
To prevent this, please evaluate the application design to optimize inductance of the motor harness and PCB traces so that the transmission and slew rates of the output pulse enable it to be completed before t_{opp} has expired.

The problem does not arise when the negative edge of the pulse fails to transition the full pulse amplitude. Moreover, the device may continue in normal operation if a surge suppressor capacitor is connected between the output pins (Ox) and power ground.

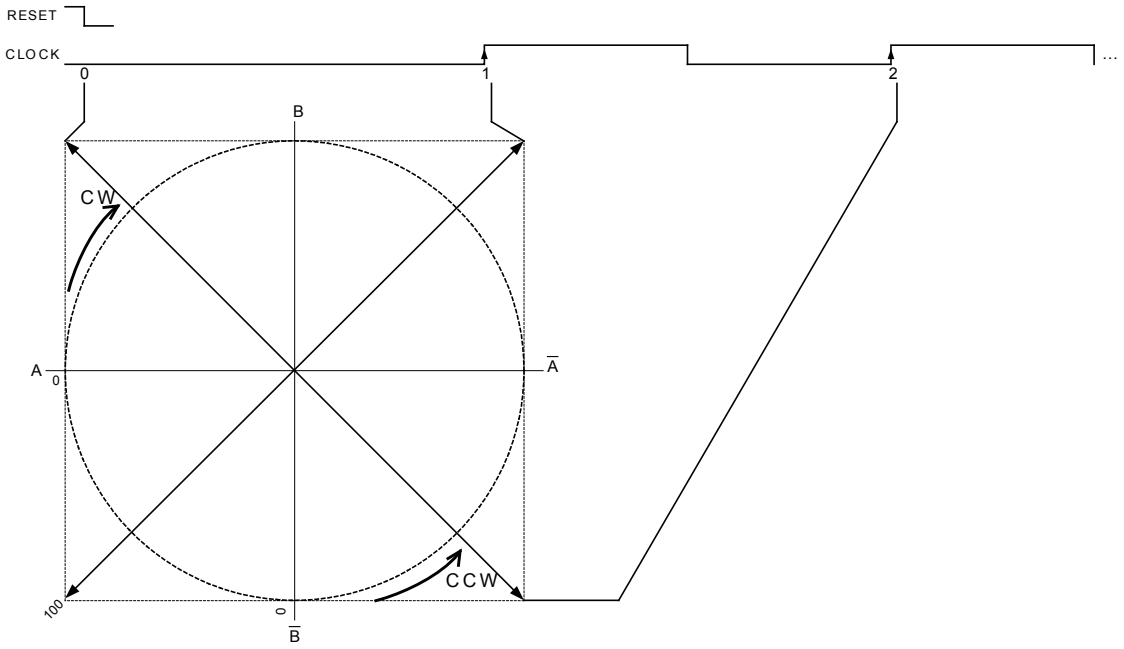
Step Sequencing

All illustrations in this section are based on step sequencing using the POS edge option. When the POS/NEG edge option is used, step sequences occur at both the rising edge and the falling edge of the Clock pulse.

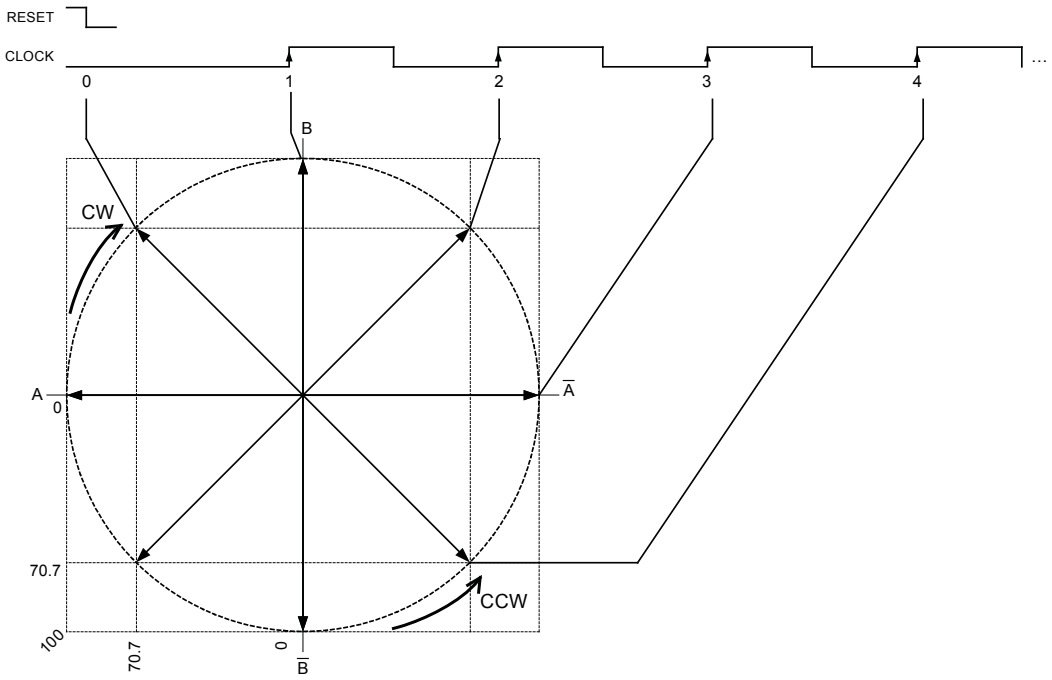
Full step
M1: Low, M2: Low, M3: Low (Current ratio mode 8)



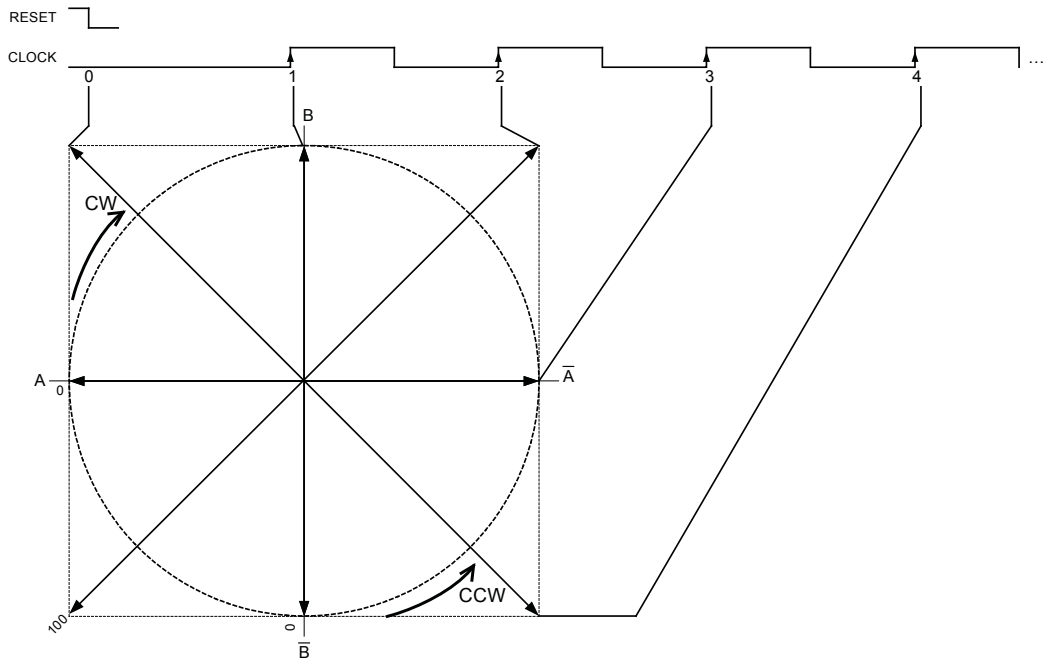
M1: High, M2: Low, M3: Low (Current ratio mode F)



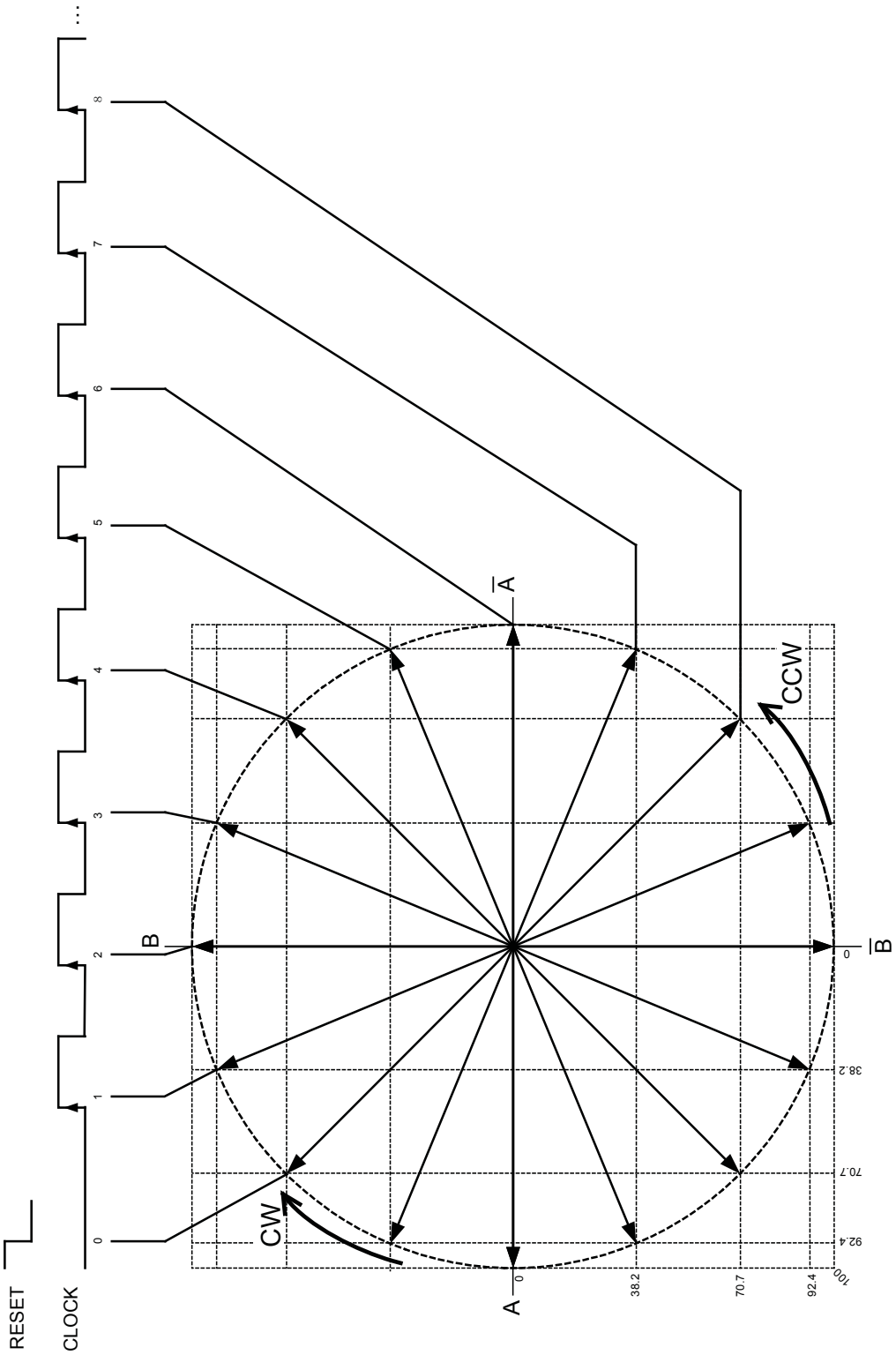
Half step
M1: Low, M2: High, M3: Low (Current ratio modes 8, F)



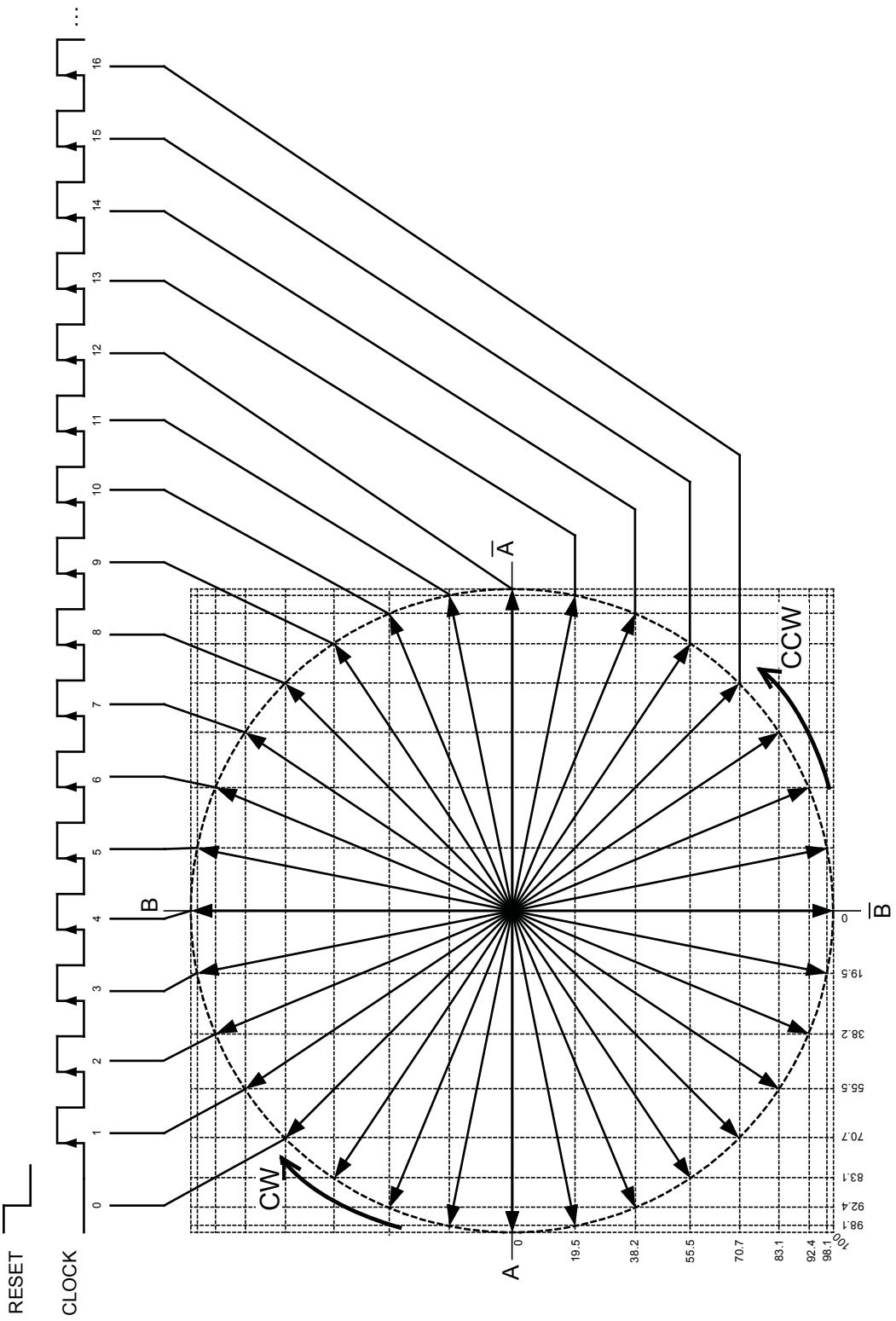
M1: High, M2: High, M3: Low (Current ratio mode F)



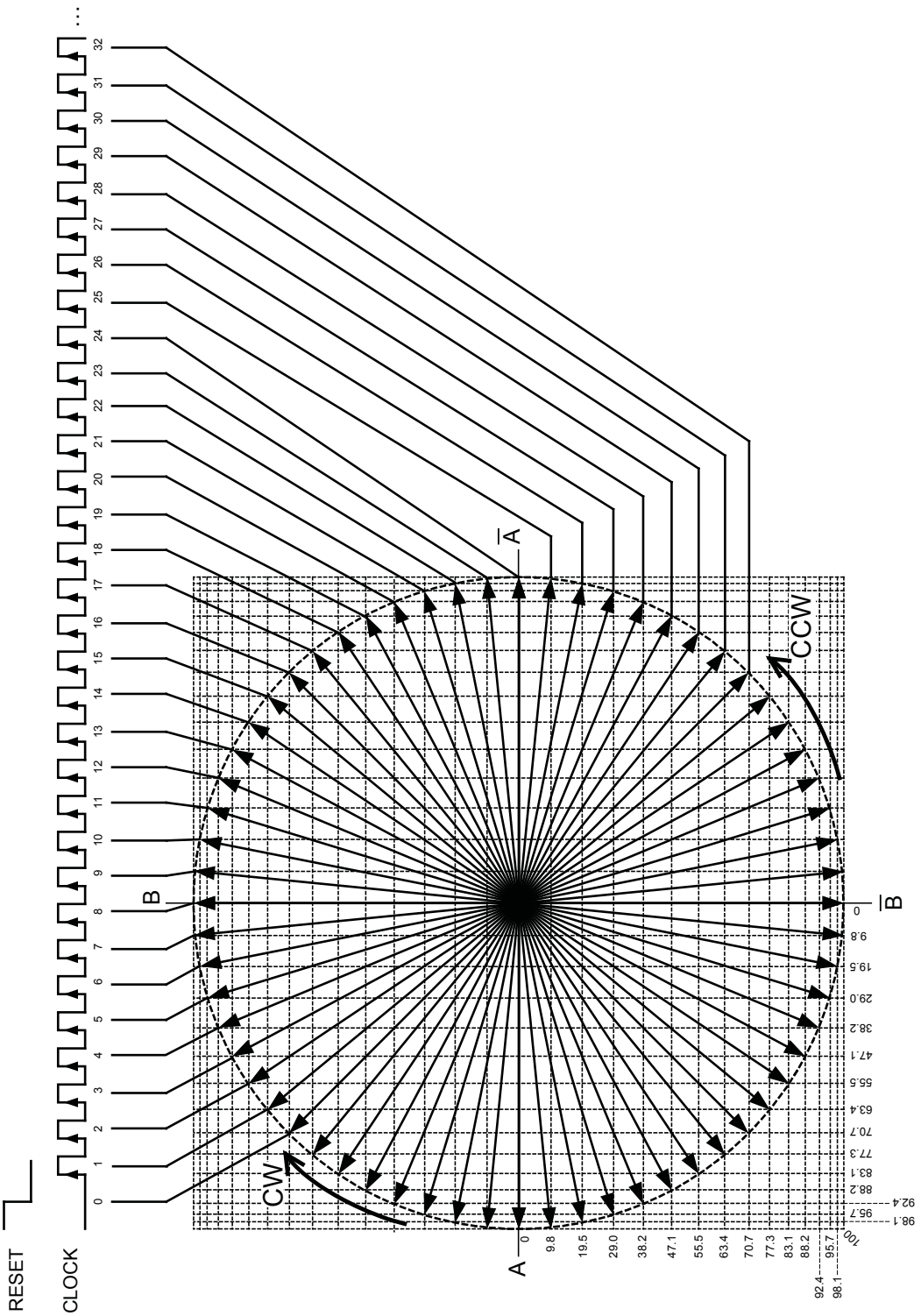
Quarter step
M1: Low, M2: Low, M3: High



Eighth step
M1: High, M2: Low, M3: High



Sixteenth step
M1: Low, M2: High, M3: High



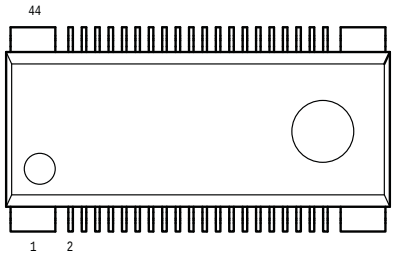
Excitation Current Ratio Mode State Table[a]

Direction	Internal Sequence State				Step Sequencing						
	Phase A		Phase B		Full Step		Half Step		1/4 Step	1/8 Step	1/16 Step
	PWM	Mode	PWM	Mode	Mode 8	Mode F	Mode 8, F	Mode F			
	A	8	B	8	X	X[b]	X	X[b]	X	X	X
	A	7	B	9							X
	A	6	B	A						X	X
	A	5	B	B							X
	A	4	B	C					X	X	X
CCW	A	3	B	D							X
▲	A	2	B	E						X	X
	A	1	B	F							X
	–	–	B	F			X	X	X	X	X
	$\overline{A}$	1	B	F							X
	$\overline{A}$	2	B	E						X	X
	$\overline{A}$	3	B	D							X
	$\overline{A}$	4	B	C					X	X	X
	$\overline{A}$	5	B	B							X
	$\overline{A}$	6	B	A						X	X
	$\overline{A}$	7	B	9							X
	$\overline{A}$	8	B	8	X	X[b]	X	X[b]	X	X	X
	$\overline{A}$	9	B	7							X
	$\overline{A}$	A	B	6						X	X
	$\overline{A}$	B	B	5							X
	$\overline{A}$	C	B	4					X	X	X
	$\overline{A}$	D	B	3							X
	$\overline{A}$	E	B	2						X	X
	$\overline{A}$	F	B	1							X
	$\overline{A}$	F	–	–			X	X	X	X	X
	$\overline{A}$	F	$\overline{B}$	1							X
	$\overline{A}$	E	$\overline{B}$	2						X	X
	$\overline{A}$	D	$\overline{B}$	3							X
	$\overline{A}$	C	$\overline{B}$	4					X	X	X
	$\overline{A}$	B	$\overline{B}$	5							X
	$\overline{A}$	A	$\overline{B}$	6						X	X
	$\overline{A}$	9	$\overline{B}$	7							X
	$\overline{A}$	8	$\overline{B}$	8	X	X[b]	X	X[b]	X	X	X
	$\overline{A}$	7	$\overline{B}$	9							X
	$\overline{A}$	6	$\overline{B}$	A						X	X
	$\overline{A}$	5	$\overline{B}$	B							X
	$\overline{A}$	4	$\overline{B}$	C					X	X	X
	$\overline{A}$	3	$\overline{B}$	D							X
	$\overline{A}$	2	$\overline{B}$	E						X	X
	$\overline{A}$	1	$\overline{B}$	F							X
	–	–	$\overline{B}$	F			X	X	X	X	X
	A	1	$\overline{B}$	F							X
	A	2	$\overline{B}$	E						X	X
	A	3	$\overline{B}$	D							X
	A	4	$\overline{B}$	C					X	X	X
	A	5	$\overline{B}$	B							X
	A	6	$\overline{B}$	A						X	X
	A	7	$\overline{B}$	9							X
	A	8	$\overline{B}$	8	X	X[b]	X	X[b]	X	X	X
	A	9	$\overline{B}$	7							X
	A	A	$\overline{B}$	6						X	X
	A	B	$\overline{B}$	5							X
	A	C	$\overline{B}$	4					X	X	X
	A	D	$\overline{B}$	3							X
	A	E	$\overline{B}$	2						X	X
	A	F	$\overline{B}$	1							X
▼	A	F	–	–			X	X	X	X	X
	A	F	B	1							X
CW	A	E	B	2						X	X
	A	D	B	3							X
	A	C	B	4					X	X	X
	A	B	B	5							X
	A	A	B	6						X	X
	A	9	B	7							X

[a]The change behavior is determined by the settings of the excitation pins (M1, M2, and M3) before and after the Clock edge.

[b]Sequence state is Mode 8, but step reference current ratio is Mode F. Mode F has step reference current ratio of 100%, and PWM off-time of 14 µs.

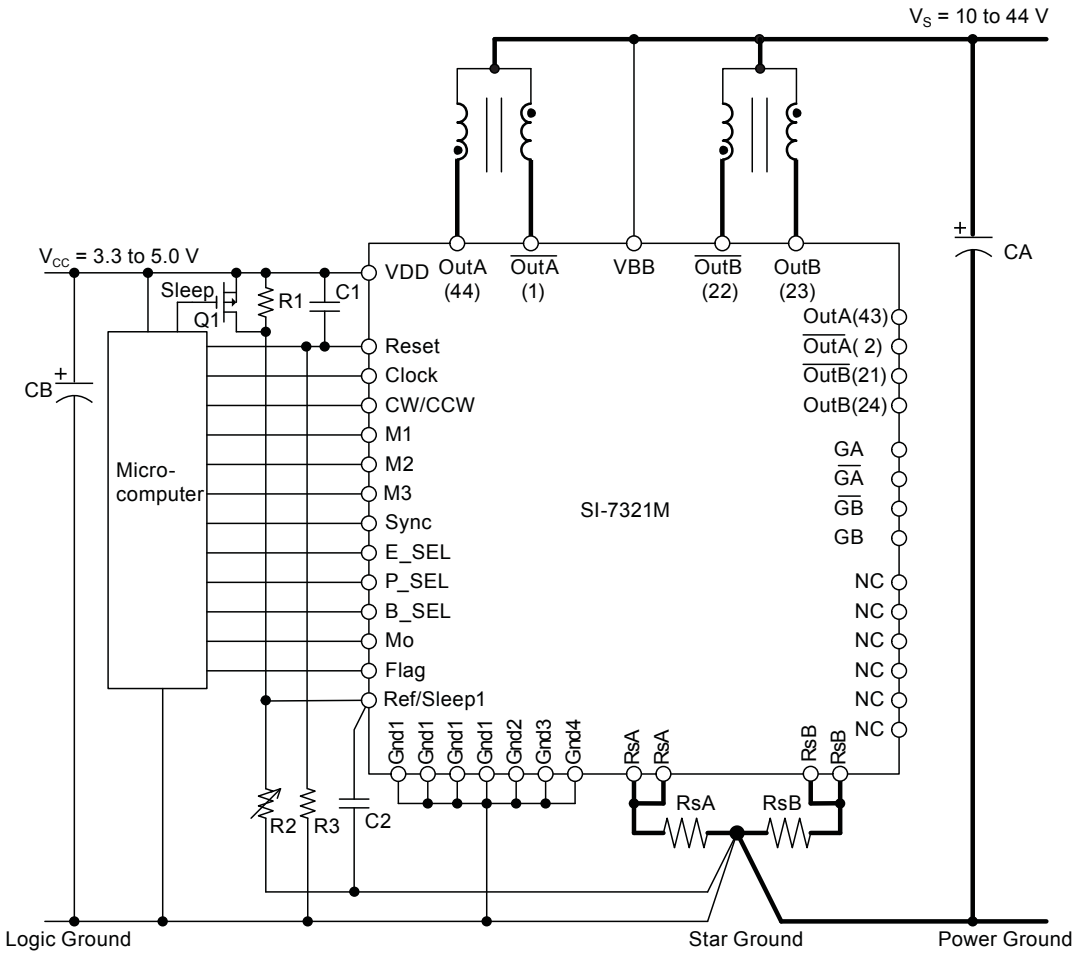
Pin-out Diagram



Terminal List Table

Number	Name	Function	Number	Name	Function
1	$\overline{\text{OutA}}$	Output of phase $\overline{\text{A}}$	23	OutB	Output of phase B
2	$\overline{\text{OutA}}$	Output of phase $\overline{\text{A}}$	24	OutB	Output of phase B
3	NC	Non connected pin	25	NC	Non connected pin
4	RsA	Phase A sense resistor connection	26	RsB	Phase B sense resistor connection
5	$\overline{\text{GA}}$	Phase $\overline{\text{A}}$ MOSFET Gate	27	GB	Phase B MOSFET gate
6	Gnd1	Gnd1	28	Gnd1	Gnd1
7	E_SEL	Edge select input	29	Gnd2	Gnd2
8	P_SEL	Protection enable/disable input	30	Flag	Output of protection circuit monitor
9	Sync	PWM control switch input	31	Mo	Output from monitor of 2-phase excitation status
10	CW/CCW	Sequence rotation switch	32	VDD	Power supply to logic
11	Reset	Reset for internal logic	33	Ref/Sleep1	V_{REF} PWM control input / Sleep1 enable input
12	Clock	Stepping clock input	34	Gnd3	Gnd3
13	M1	Commutation and Sleep2 setting	35	NC	Non connected pin
14	M2		36	VBB	Main power supply (for motor)
15	M3		37	NC	Non connected pin
16	B_SEL	Blanking time select input	38	Gnd4	Gnd4
17	Gnd1	Gnd1	39	Gnd1	Gnd1
18	$\overline{\text{GB}}$	Phase $\overline{\text{A}}$ MOSFET Gate	40	GA	Phase A MOSFET gate
19	RsB	Phase $\overline{\text{B}}$ sense resistor connection	41	RsA	Phase A sense resistor connection
20	NC	Non connected pin	42	NC	Non connected pin
21	$\overline{\text{OutB}}$	Output of phase $\overline{\text{B}}$	43	OutA	Output of phase A
22	$\overline{\text{OutB}}$	Output of phase $\overline{\text{B}}$	44	OutA	Output of phase A

Application Information



Typical application circuit

- Take precautions to avoid noise on the V_{DD} line; noise levels greater than 0.5 V on the V_{DD} line may cause device malfunction. Noise can be reduced by separating the Logic Ground and the Power Ground on the PCB, and connect them at Gnd pins.
- Unused logic input pins (CW/CCWR, M1, M2, M3, E_SEL, P_SEL, B_SEL, Reset, and Sync) *must* be pulled up/down to V_{DD} or ground. If those unused pins are left open, the device malfunctions.
- Unused logic output pins (Mo, Flag) *must* be kept open.
- Constants, for reference use only:*

  R1, R3 = 10 kΩ — CA = 100 µF / 50 V

  R2 = 1 kΩ (VR) — CB = 10 µF / 10 V

  C1, C2 = 0.1 µF

  Sense Resistor, R_S (Loss: $P \approx I_O^2 \times R_S$)
  - When not using the protection circuit: R_S = 0.1 to 0.68 Ω (3 W)
  - When using the protection circuit: R_S = 0.1 to 0.33 Ω (2 W)

  *Select the values in consideration of overcurrent protection, V_{OCP}

- The SI-7321M control current, I_O, (at Mode F) is calculated as follows:

  $$I_O = V_{REF} / R_S \ .$$

  Moreover, setting V_{REF} more than 2 V initiates Sleep1 mode, which sets all outputs in the off state, however, the internal logic circuit remains active.

- The timing of the following input signals should be synchronized:

  The rising edge of CW/CCW, M1, M2, M3, E_SEL with that of the Clock input.

  The Reset pin release (the falling edge of the Reset input pulse) and the rising edge of the Clock input.

  If these signals are not synchronized, the device may operate in an undefined manner.

- The logic inputs (Reset, Clock, CW/CCW, M1, M2, M3, Sync E_SEL, B_SEL, and P_SEL) should not be left open. If any of these are not used, be sure to connect them to VDD or GND.

  If any of the logic inputs remain open, a malfunction may occur due to external noise.

- When a logic output (Mo or Flag) is not used, be sure to keep it open.

  In case it is connected to VDD or GND, it may cause device deterioration and/or breakdown.

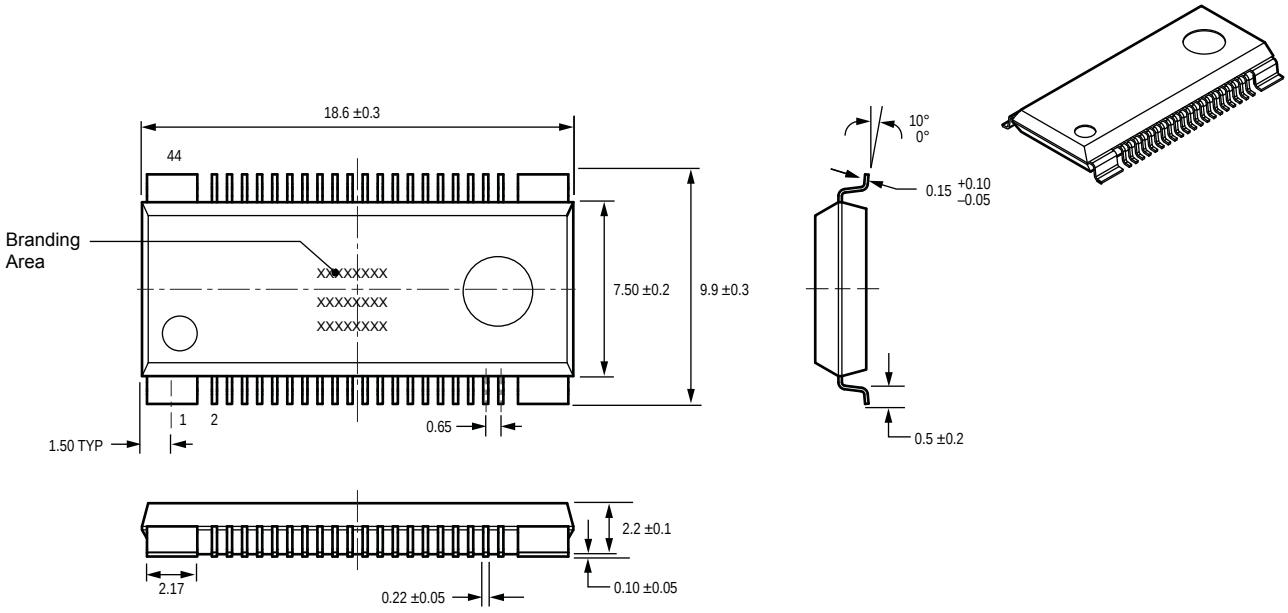
- The SI-7321M includes motor coil short-circuit and motor coil open protection circuits. Protection is activated by sensing voltage on the Rsx inputs, with the threshold level determined by external sense resistors, Rs. Therefore, an overcurrent condition cannot be detected which results from the OUTx pins or Rsx pins, or both, shorting to Gnd.

- This driver has CMOS inputs.

  When static electricity is a problem, care should be taken to properly control the room humidity. This is particularly true in the winter when static electricity is most troublesome.

  Care should be taken with device leads and with assembly sequencing to avoid applying static charges to IC leads. PC board pins should be shorted together to keep them at the same potential to avoid this kind of trouble.

Package Outline Drawing, HSOP-44



Terminal core material: Cu
Terminal treatment: Ni plating and Pb-free solder dip
Package: HSOP-44

Dimensions in millimeters

Appearance: The body shall be clean and shall not bear any stain, rust, or flaw

Branding codes (exact appearance at manufacturer discretion):
1st line, type: SI7321M
2nd line, lot: SK *YMW*
Where: Y is the last digit of the year of manufacture
M is the month (*1* to *9, O, N, D*)
W is the week
3rd line, tracking code: *NNNN*

Marking: The type number and lot number shall be clearly marked in white

Device composition 100% lead (Pb) free

Because reliability can be affected adversely by improper storage environments and handling methods, please observe the following cautions.

Cautions for Storage

- Ensure that storage conditions comply with the standard temperature (5°C to 35°C) and the standard relative humidity (around 40 to 75%); avoid storage locations that experience extreme changes in temperature or humidity.
- Avoid locations where dust or harmful gases are present and avoid direct sunlight.
- Reinspect for rust on leads and solderability of products that have been stored for a long time.

Cautions for Testing and Handling

When tests are carried out during inspection testing and other standard test periods, protect the products from power surges from the testing device, shorts between adjacent products, and shorts to the heatsink.

Soldering

- When soldering the products, please be sure to minimize the working time, within the following limits:

  260°C +0/–10°C, 10 s

Electrostatic Discharge

- When handling the products, operator must be grounded. Grounded wrist straps worn should have at least 1 MΩ of resistance to ground to prevent shock hazard.
- Workbenches where the products are handled should be grounded and be provided with conductive table and floor mats.
- When using measuring equipment such as a curve tracer, the equipment should be grounded.
- When soldering the products, the head of soldering irons or the solder bath must be grounded in other to prevent leak voltages generated by them from being applied to the products.
- The products should always be stored and transported in our shipping containers or conductive containers, or be wrapped in aluminum foil.

- The contents in this document are subject to changes, for improvement and other purposes, without notice. Make sure that this is the latest revision of the document before use.
- Application and operation examples described in this document are quoted for the sole purpose of reference for the use of the products herein and Sanken can assume no responsibility for any infringement of industrial property rights, intellectual property rights or any other rights of Sanken or any third party which may result from its use.
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  In addition, it should be noted that since power devices or IC's including power devices have large self-heating value, the degree of derating of junction temperature affects the reliability significantly.
- When using the products specified herein by either (i) combining other products or materials therewith or (ii) physically, chemically or otherwise processing or treating the products, please duly consider all possible risks that may result from all such uses in advance and proceed therewith at your own responsibility.
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