12-Bit, 600ksps Sampling A/D Converter with Shutdown

FEATURES

- **Single Supply 5V or ±5V Operation**
- **Sample Rate: 600ksps**
- **70dB S/(N + D) and 74dB THD at Nyquist**
- **Power Dissipation: 60mW Typ**
- Power Shutdown with Instant Wake-Up
- Internal Reference Can Be Overdriven Externally
- Internal Synchronized Clock; No Clock Required
- High Impedance Analog Input
- Input Range: 0V to 5V or ±2.5V
- New Flexible, Friendly Parallel Interface Eases Connections to DSPs and FIFOs
- 24-Pin SO Wide Package

APPLICATIONS

- High Speed Data Acquisition
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- Audio and Telecom Processing
- Spectrum Analysis

DESCRIPTION

The LTC®1279 is a 1.4µs, 600ksps, sampling 12-bit A/D converter which draws only 60mW from a single 5V or ±5V supplies. This easy-to-use device comes complete with a 160ns sample-and-hold, a precision reference and an internally trimmed clock. Unipolar and bipolar conversion modes add to the flexibility of the ADC. The low power dissipation is reduced even more, drawing only 8.5mW in power shutdown mode. Instant wake-up from power shutdown allows the converter to be powered down even during brief inactive periods.

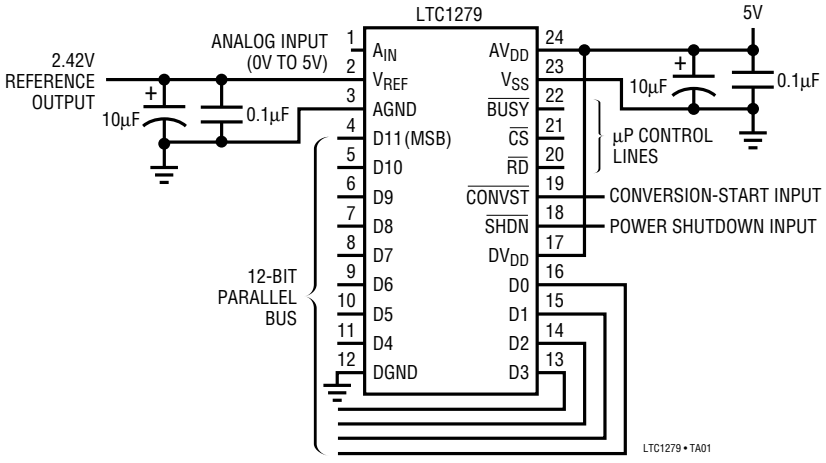
The LTC1279 converts 0V to 5V unipolar inputs from a single 5V supply and ±2.5V bipolar inputs from ±5V supplies. Maximum DC specs include ±1LSB INL and ±1LSB DNL. Outstanding guaranteed AC performance includes 70dB S/(N + D) and 78dB THD at the input frequency of 100kHz over temperature.

The internal clock is trimmed for 1.4µs conversion time. The clock automatically synchronizes to each sample command, eliminating problems with asynchronous clock noise found in competitive devices. A separate conversion start input and a data-ready signal ($\overline{BUSY}$) ease connections to FIFOs, DSPs and microprocessors.

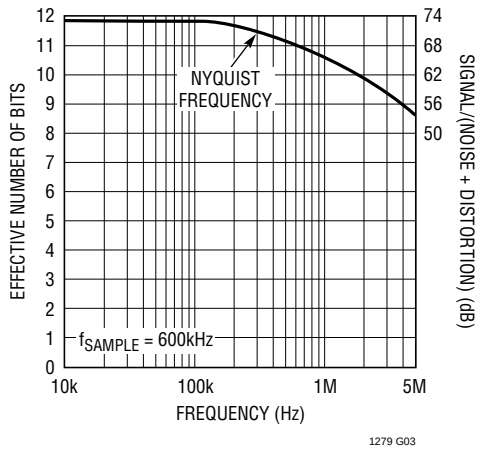
LT, LTC and LT are registered trademarks of Linear Technology Corporation.

TYPICAL APPLICATION

Single 5V Supply, 600kHz, 12-Bit Sampling A/D Converter



Effective Bits and Signal-to-(Noise + Distortion) vs Input Frequency

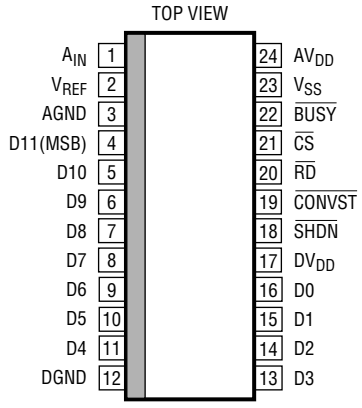


ABSOLUTE MAXIMUM RATINGS

AV_{DD} = DV_{DD} = V_{DD} (Notes 1, 2)

Supply Voltage (V_{DD}) 7V
Negative Supply Voltage (V_{SS})
  Bipolar Operation Only ..... –6V to GND
Total Supply Voltage (V_{DD} to V_{SS})
  Bipolar Operation Only 12V
Analog Input Voltage (Note 3)
  Unipolar Operation ..... – 0.3V to V_{DD} + 0.3V
  Bipolar Operation..... V_{SS} – 0.3V to V_{DD} + 0.3V
Digital Input Voltage (Note 4)
  Unipolar Operation ..... –0.3V to 12V
  Bipolar Operation..... V_{SS} – 0.3V to 12V
Digital Output Voltage
  Unipolar Operation ..... –0.3V to V_{DD} + 0.3V
  Bipolar Operation..... – 0.3V to V_{DD} + 0.3V
Power Dissipation..... 500mW
Operating Temperature Range
  LTC1279C..... 0°C to 70°C
  LTC1279I..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



SW PACKAGE
24-LEAD PLASTIC SO WIDE

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER*
LTC1279CSW
LTC1279ISW

*Consult factory for plastic DIP package.
Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

With Internal Reference (Notes 5, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 7)	●			±1	LSB
Differential Linearity Error		●			±1	LSB
Bipolar Offset Error	(Note 8)	 ●			±4 ±6	LSB LSB
Unipolar Offset Error		 ●			±6 ±8	LSB LSB
Gain Error					±15	LSB
Gain Error Tempco	$I_{OUT(REF)}$ = 0	●		±10	±45	ppm/°C

ANALOG INPUT (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9)	4.95V ≤ V_{DD} ≤ 5.25V (Unipolar) 4.75V ≤ V_{DD} ≤ 5.25V, –5.25V ≤ V_{SS} ≤ –2.45V (Bipolar)	● ●		0 to 5 ±2.5		V V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions (Sample Mode) During Conversions (Hold Mode)			25 5		pF pF

DYNAMIC ACCURACY (Notes 5, 10)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	100kHz Input Signal 300kHz Input Signal	● 	70	72 70		dB dB
THD	Total Harmonic Distortion First 5 Harmonics	100kHz Input Signal 300kHz Input Signal	● 		–82 –74	–78	dB dB
	Peak Harmonic or Spurious Noise	100kHz Input Signal 300kHz Input Signal	● 		–82 –80	–78	dB dB
IMD	Intermodulation Distortion	f_{IN1} = 94.189kHz, f_{IN2} = 97.705kHz 2nd Order Terms 3rd Order Terms			 –81 –78		 dB dB
		f_{IN1} = 299.26kHz, f_{IN2} = 305.12kHz 2nd Order Terms 3rd Order Terms			 –77 –74		 dB dB
	Full Power Bandwidth				5		MHz
	Full Linear Bandwidth (S/(N + D) ≥ 68dB)				500		kHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.400	2.420	2.440	V
V_{REF} Output Tempco	I_{OUT} = 0	●		±10	±45	ppm/°C
V_{REF} Line Regulation	4.95V ≤ V_{DD} ≤ 5.25V –5.25V ≤ V_{SS} ≤ –4.95V			0.01 0.01		LSB/V LSB/V
V_{REF} Load Regulation	–5mA ≤ I_{OUT} ≤ 800µA			2		LSB/mA

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.95V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.95V I_O = –10µA I_O = –200µA	 ●	 4.0	 4.9 		 V V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.95V I_O = 160µA I_O = 1.6mA	 ●		 0.05 0.10	 0.4	 V V
I_{OZ}	High-Z Output Leakage D11 to D0	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	High-Z Output Capacitance D11 to D0	$\overline{CS}$ High (Note 9)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage (Notes 11, 12)	Unipolar Bipolar		4.95 4.75		5.25 5.25	V V
V_{SS}	Negative Supply Voltage (Note 11, 12)	Bipolar Only		–2.45		–5.25	V
I_{DD}	Positive Supply Current	f_{SAMPLE} = 600ksps $\overline{SHDN}$ = 0V	● ●		12 1.7	24 3	mA mA
I_{SS}	Negative Supply Current	f_{SAMPLE} = 600ksps, V_{SS} = –5V	●		0.12	0.30	mA
P_D	Power Dissipation	f_{SAMPLE} = 600ksps $\overline{SHDN}$ = 0V	● ●		60 8.5	120 15	mW mW

TIMING CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency		●	600			kHz
$t_{SAMPLE(MIN)}$	Minimum Throughput Time (Acquisition Time Plus Conversion Time)		●			1.66	µs
t_{CONV}	Conversion Time		●		1.4	1.6	µs
t_{ACQ}	Acquisition Time				160		ns
t_1	$\overline{CS}\downarrow$ to $\overline{RD}\downarrow$ Setup Time	(Notes 9, 11)	●	0			ns
t_2	$\overline{CS}\downarrow$ to $\overline{CONVST}\downarrow$ Setup Time	(Notes 9, 11)	●	20			ns
t_3	$\overline{SHDN}\uparrow$ to $\overline{CONVST}\downarrow$ Wake-Up Time	(Note 11)			350		ns
t_4	$\overline{CONVST}$ Low Time	(Notes 11, 13)	●	40			ns
t_5	$\overline{CONVST}\downarrow$ to $\overline{BUSY}\downarrow$ Delay	C_L = 100pF Commercial Industrial	 ● ●		50	110 130 140	ns ns ns
t_6	Data Ready Before $\overline{BUSY}\uparrow$	C_L = 20pF	●	20	40		ns
t_7	Wait Time $\overline{RD}\downarrow$ After $\overline{BUSY}\uparrow$	Mode 2, (See Figure 14) (Note 9)	●	–20			ns
t_8	Data Access Time After $\overline{RD}\downarrow$	C_L = 20pF (Note 9) Commercial Industrial	 ● ●		35	90 110 120	ns ns ns
		C_L = 100pF Commercial Industrial	 ● ●		50	125 150 170	ns ns ns
t_9	Bus Relinquish Time	(3k and 10pF Connected as Shown in Test Circuits) Commercial Industrial	 ● ●	 10 10	 30	 75 85 90	 ns ns ns
t_{10}	$\overline{RD}$ Low Time	(Note 9)	●	t_8			ns
t_{11}	$\overline{CONVST}$ High Time	(Notes 9, 13)	●	40			ns
t_{12}	Aperture Delay of Sample-and-Hold	Jitter <50ps			12		ns

TIMING CHARACTERISTICS (Note 5)

The ● indicates specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together (unless otherwise noted).

Note 3: When the analog input voltage is taken below V_{SS} (ground for unipolar mode) or above V_{DD}, it will be clamped by internal diodes. This product can handle input currents greater than 80mA below V_{SS} (ground for unipolar mode) or above V_{DD} without latch-up.

Note 4: When these pin voltages are taken below V_{SS} (ground for unipolar mode), they will be clamped by internal diodes. This product can handle input currents greater than 60mA below V_{SS} (ground for unipolar mode) without latch-up. These pins are not clamped to V_{DD}.

Note 5: AV_{DD} = DV_{DD} = V_{DD} = 5V, (V_{SS} = –5V for bipolar mode), f_{SAMPLE} = 600kHz, t_r = t_f = 5ns unless otherwise specified.

Note 6: Linearity, offset and full scale specifications apply for unipolar and bipolar modes.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the offset voltage measured from –1/2LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

Note 9: Guaranteed by design, not subject to test.

Note 10: The AC test is for bipolar mode. The signal-to-noise plus distortion ratio is about 1dB lower for unipolar mode, so the typical S/(N + D) at 100kHz in unipolar mode is 71dB.

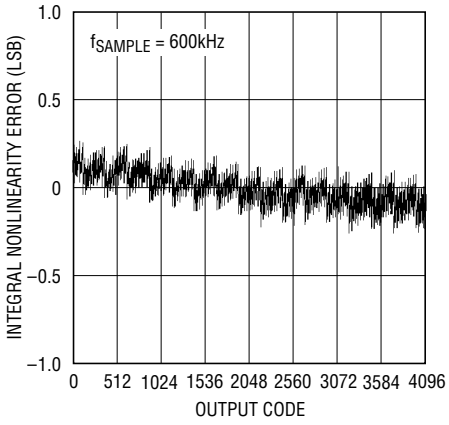
Note 11: Recommended operating conditions.

Note 12: A_{IN} must not exceed V_{DD} or fall below V_{SS} by more than 50mV for specified accuracy. Therefore the minimum supply voltage for the unipolar mode is 4.95V. The minimum for the bipolar mode is 4.75V, –2.45V.

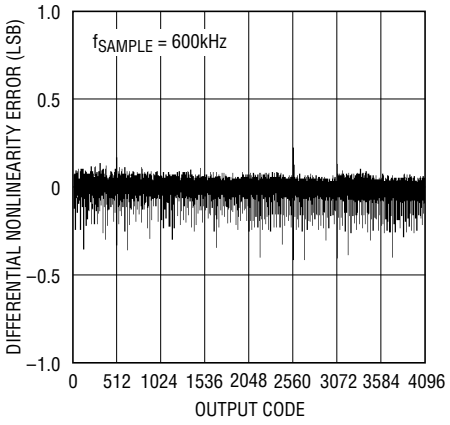
Note 13: The falling $\overline{\text{CONVST}}$ edge starts a conversion. If $\overline{\text{CONVST}}$ returns high at a bit decision point during the conversion it can create small errors. For best performance ensure that $\overline{\text{CONVST}}$ returns high either within 120ns after conversion start (i.e., before the first bit decision) or after $\overline{\text{BUSY}}$ rises (i.e., after the last bit test). See mode 1a and 1b (Figures 12 and 13) timing diagrams.

TYPICAL PERFORMANCE CHARACTERISTICS

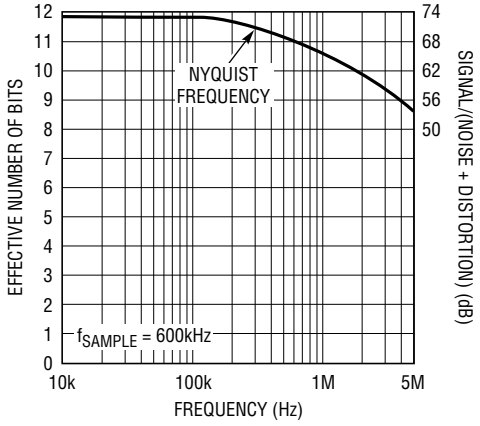
Integral Nonlinearity vs Output Code



Differential Nonlinearity vs Output Code

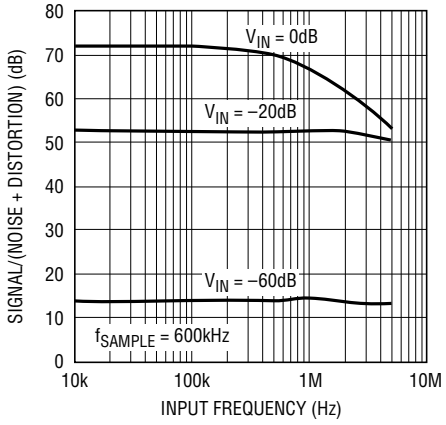


ENOBs and S/(N + D) vs Input Frequency

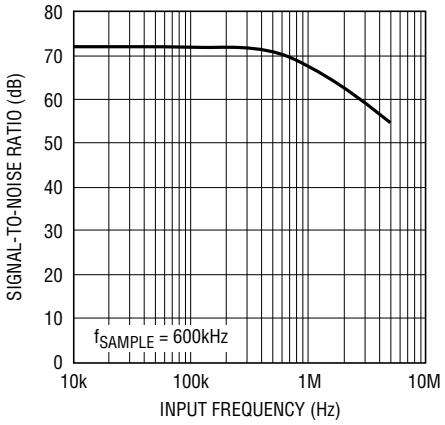


TYPICAL PERFORMANCE CHARACTERISTICS

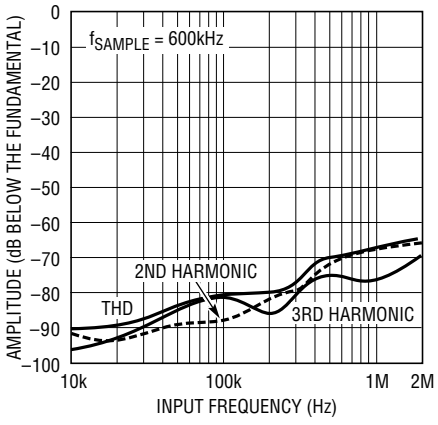
S/(N + D) vs Input Frequency and Amplitude



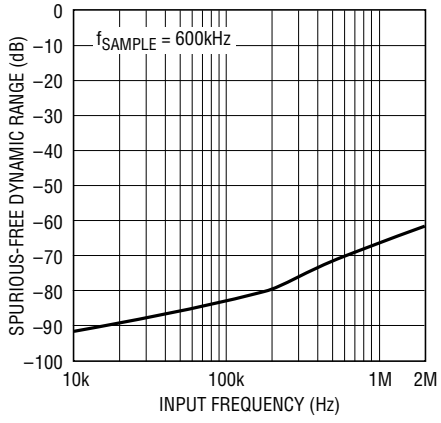
Signal-to-Noise Ratio (Without Harmonics) vs Input Frequency



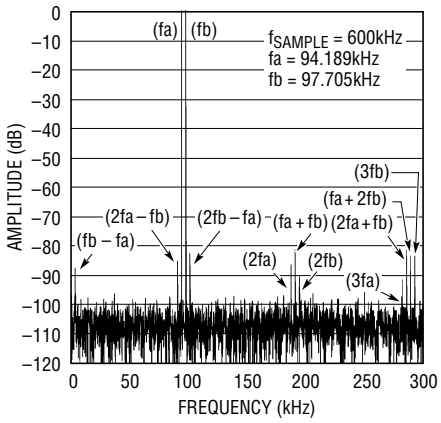
Distortion vs Input Frequency



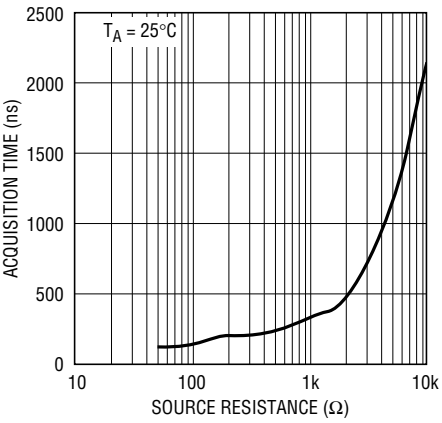
Peak Harmonic or Spurious Noise vs Input Frequency



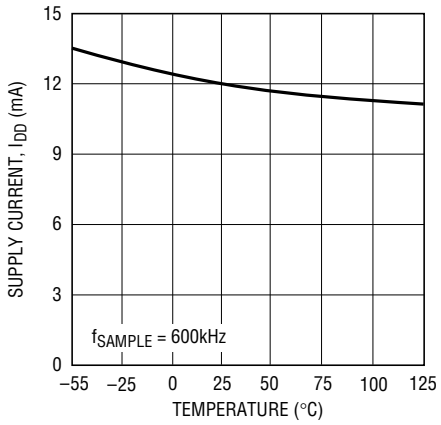
Intermodulation Distortion Plot



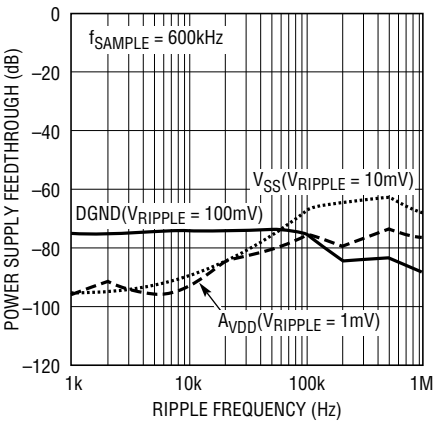
Acquisition Time vs Source Impedance



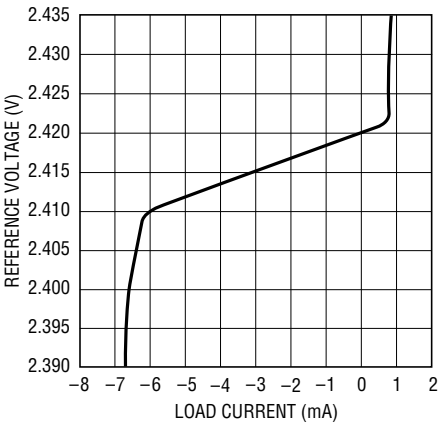
Supply Current vs Temperature



Power Supply Feedthrough vs Ripple Frequency



Reference Voltage vs Load Current



PIN FUNCTIONS

A_{IN} (Pin 1): Analog Input. 0V to 5V (Unipolar), ±2.5V (Bipolar).

V_{REF} (Pin 2): 2.42V Reference Output. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

AGND (Pin 3): Analog Ground.

D11 to D4 (Pins 11 to 4): Three-State Data Outputs. D11 is the Most Significant Bit.

DGND (Pin 12): Digital Ground.

D3 to D0 (Pins 13 to 16): Three-State Data Outputs.

DV_{DD} (Pin 17): Digital Power Supply, 5V. Tie to AV_{DD} pin.

$\overline{SHDN}$ (Pin 18): Power Shutdown. The LTC1279 powers down when $\overline{SHDN}$ is low.

$\overline{CONVST}$ (Pin 19): Conversion Start Input. It is active low. The falling edge of the $\overline{CONVST}$ signal initiates a conversion. The LTC1279 responds to $\overline{CONVST}$ signal only if the signal applied to $\overline{CS}$ is a logic low.

$\overline{RD}$ (Pin 20): READ Input. A logic low signal applied to this pin enables the output data drivers when the signal applied to the $\overline{CS}$ pin is a logic low.

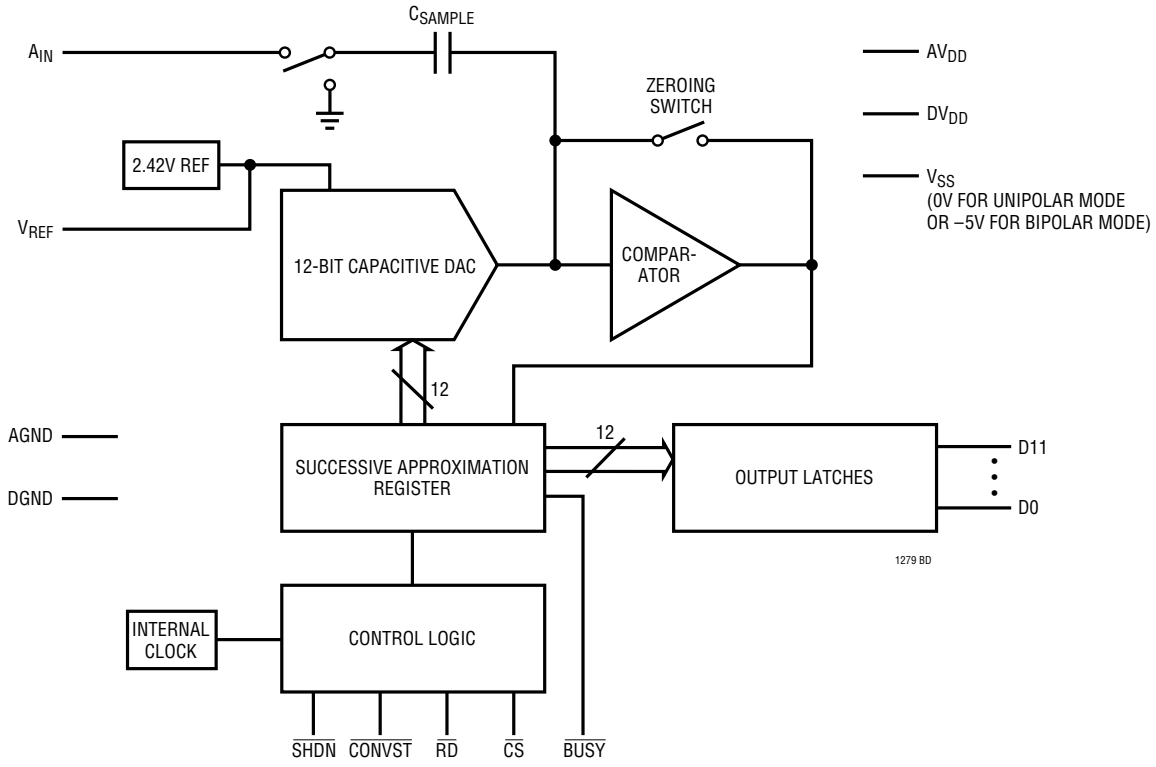
$\overline{CS}$ (Pin 21): The CHIP SELECT input must be a logic low for the ADC to recognize the signals applied to the $\overline{CONVST}$ and $\overline{RD}$ inputs.

$\overline{BUSY}$ (Pin 22): The $\overline{BUSY}$ output shows the converter status. It is a logic low during a conversion.

V_{SS} (Pin 23): Negative Supply. –5V will select bipolar operation. Bypass to AGND with 0.1µF ceramic. Tie to analog ground to select unipolar operation.

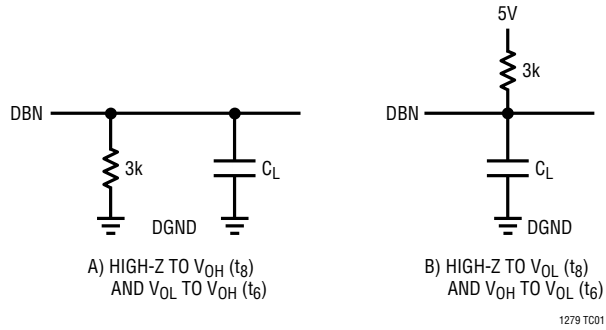
AV_{DD} (Pin 24): Positive Supply, 5V. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS

Load Circuits for Access Timing

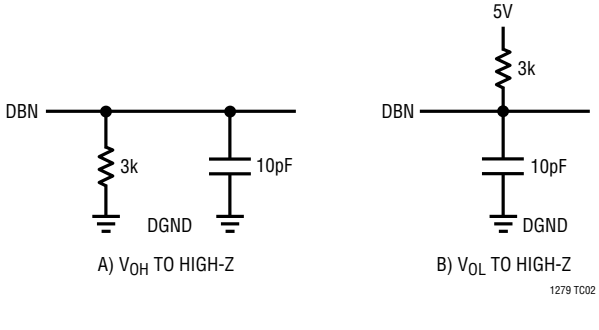


A) HIGH-Z TO V_{OH} (t_8) AND V_{OL} TO V_{OH} (t_6)

B) HIGH-Z TO V_{OL} (t_8) AND V_{OH} TO V_{OL} (t_6)

1279 TC01

Load Circuits for Output Float Delay



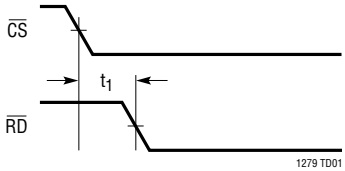
A) V_{OH} TO HIGH-Z

B) V_{OL} TO HIGH-Z

1279 TC02

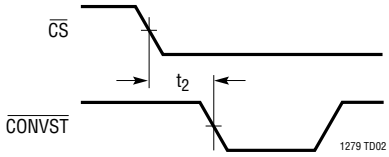
TIMING DIAGRAMS

$\overline{CS}$ to $\overline{RD}$ Setup Timing



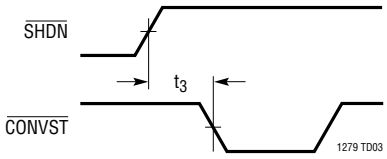
1279 TD01

$\overline{CS}$ to $\overline{CONVST}$ Setup Timing



1279 TD02

$\overline{SHDN}$ to $\overline{CONVST}$ Wake-Up Timing



1279 TD03

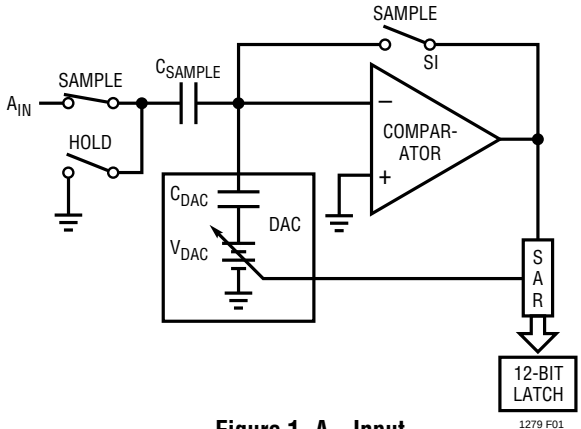
APPLICATIONS INFORMATION

CONVERSION DETAILS

The LTC1279 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 12-bit parallel output. The ADC is complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. (Please refer to the Digital Interface section for the data format.)

Conversion start is controlled by the $\overline{CS}$ and $\overline{CONVST}$ inputs. At the start of conversion the successive approximation register (SAR) is reset. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the A_{IN} input connects to the sample-and-hold capacitor during the acquire phase, and the comparator offset is nulled by the feedback switch. In this acquire phase, a minimum delay of 160ns will provide enough time for the sample-and-hold capacitor to acquire the analog signal. During the convert phase, the comparator feedback switch opens, putting the comparator into the compare mode. The input switch switches C_{SAMPLE} to ground, injecting the analog input charge onto the summing junction. This input charge is successively com-



1279 F01

Figure 1. A_{IN} Input

APPLICATIONS INFORMATION

pared with the binary-weighted charges supplied by the capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the DAC output balances the A_{IN} input charge. The SAR contents (a 12-bit data word) which represent the A_{IN} are loaded into the 12-bit output latches.

DYNAMIC PERFORMANCE

The LTC1279 has excellent high speed sampling capability. FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figures 2a and 2b show typical LTC1279 FFT plots.

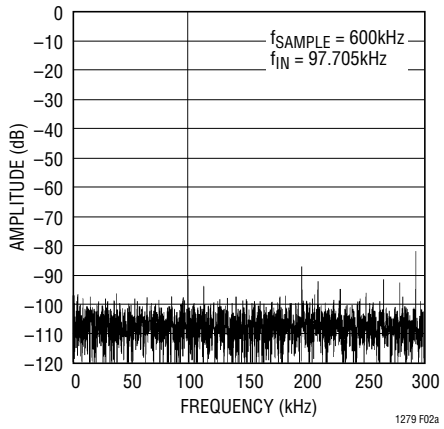


Figure 2a. LTC1279 Nonaveraged, 4096 Point FFT Plot with 100kHz Input Frequency

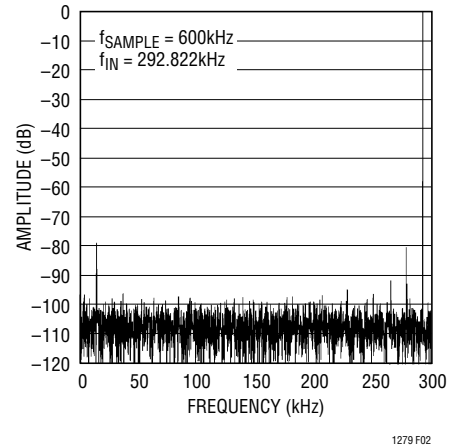


Figure 2b. LTC1279 Nonaveraged, 4096 Point FFT Plot with 300kHz Input Frequency

Signal-to-Noise Ratio

The Signal-to-Noise plus Distortion Ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies above DC and below half the sampling frequency. Figure 2a shows a typical spectral content with a 600kHz sampling rate and a 100kHz input. The dynamic performance is excellent for input frequencies up to the Nyquist limit of 300kHz as shown in Figure 2b.

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$N = [S/(N + D) – 1.76]/6.02$$

where N is the Effective Number of Bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 600kHz the LTC1279 maintains very good ENOBs up to the Nyquist input frequency of 300kHz. Refer to Figure 3.

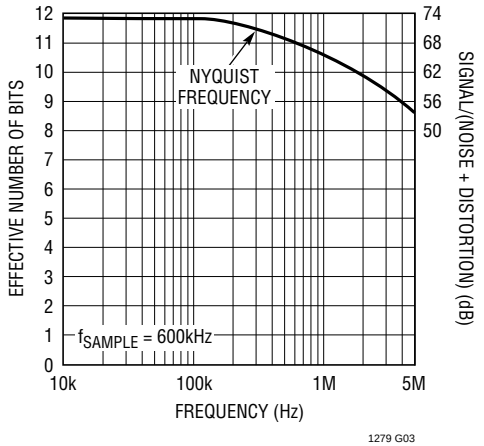


Figure 3. Effective Bits and Signal/(Noise + Distortion) vs Input Frequency

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

APPLICATIONS INFORMATION

$$THD = 20\log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \ldots + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics. THD versus input frequency is shown in Figure 4. The LTC1279 has good distortion performance up to the Nyquist frequency and beyond.

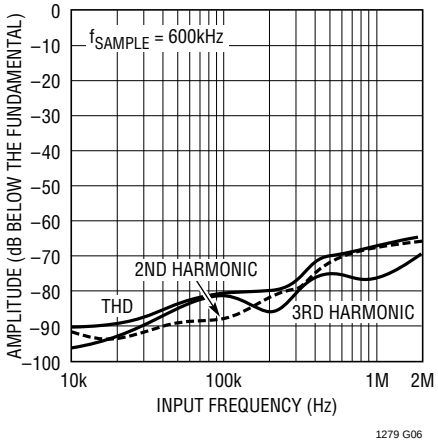


Figure 4. Distortion vs Input Frequency

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa + fb) and (fa – fb) while the 3rd order IMD terms include (2fa + fb), (2fa – fb), (fa + 2fb), and (fa – 2fb). If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

$$IMD\ (fa \pm fb) = 20\log \frac{\text{Amplitude at } (fa \pm fb)}{\text{Amplitude at fa}}$$

Figure 5 shows the IMD performance at a 100kHz input.

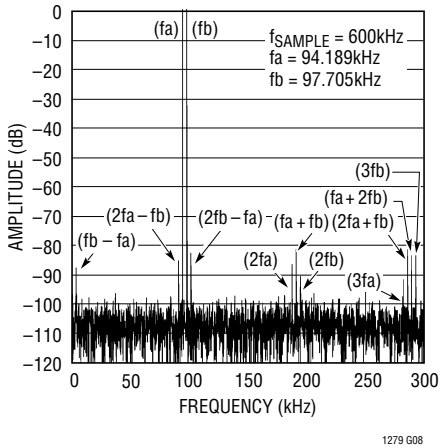


Figure 5. Intermodulation Distortion Plot

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full scale input signal.

Full Power and Full Linear Bandwidth

The full power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

The full linear bandwidth is the input frequency at which the S/(N + D) has dropped to 68dB (11 effective bits). The LTC1279 has been designed to optimize input bandwidth, allowing ADC to undersample input signals with frequencies above the converter's Nyquist Frequency. The noise floor stays very low at high frequencies; S/(N + D) becomes dominated by distortion at frequencies far beyond Nyquist.

Driving the Analog Input

The LTC1279's analog input is easy to drive. It draws only one small current spike while charging the sample-and-hold capacitor at the end of conversion. During conversion the analog input draws no current. The only requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion starts. Any op amp that settles in 160ns to small current transients will allow maximum speed operation. If slower

APPLICATIONS INFORMATION

op amps are used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADC's A_{IN} input include the LT®1360, LT1220, LT1223 and LT1224 op amps.

Internal Reference

The LTC1279 has an on-chip, temperature compensated, curvature corrected, bandgap reference that is factory trimmed to 2.42V. It is internally connected to the DAC and is available at pin 2 to provide up to 800µA current to an external load.

For minimum code transition noise, the reference output should be decoupled with a capacitor to filter wideband noise from the reference (10µF tantalum in parallel with a 0.1µF ceramic).

The V_{REF} pin can be driven with a DAC or other means to provide input span adjustment in bipolar mode. The V_{REF} pin must be driven to at least 2.45V to prevent conflict with the internal reference. The reference should be driven to no more than 4.8V to keep the input span within the ±5V supplies.

Figure 6 shows an LT1006 op amp driving the V_{REF} pin. (In the unipolar mode, the input span is already 0V to 5V with the internal reference so driving the reference is not recommended, since the input span will exceed the supply and codes will be lost at the full scale.) Figure 7 shows a typical reference, the LT1019A-2.5 connected to the LTC1279. This will provide an improved drift (equal to the LT1019A-2.5's maximum of 5ppm/°C) and a ±2.582V full scale.

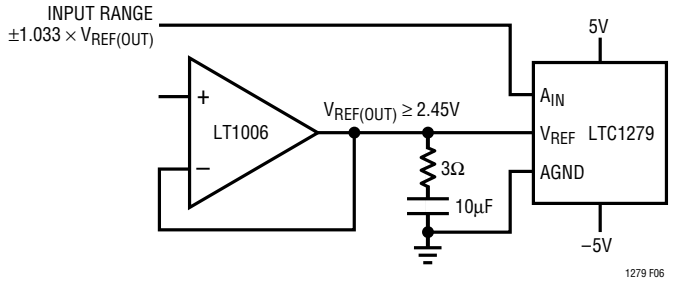


Figure 6. Driving the V_{REF} with the LT1006 Op Amp

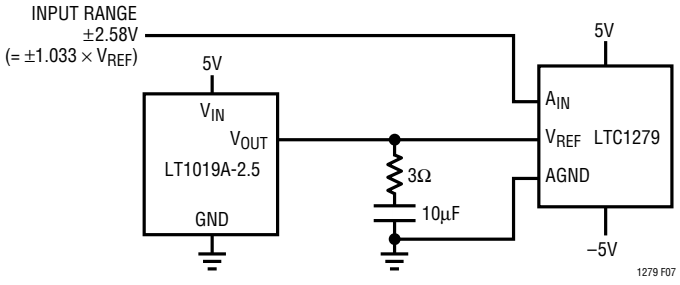


Figure 7. Supplying a 2.5V Reference Voltage to the LTC1279 with the LT1019A-2.5

UNIPOLAR/BIPOLAR OPERATION AND ADJUSTMENT

Figure 8a shows the ideal input/output characteristics for the LTC1279. The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB, ... FS – 1.5LSB). The output code is naturally binary with 1LSB = FS/4096 = 5V/4096 = 1.22mV. Figure 8b shows the input/output transfer characteristics for the bipolar mode in two's complement format.

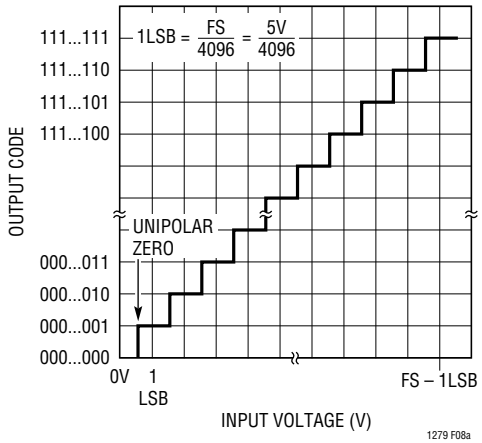


Figure 8a. LTC1279 Unipolar Transfer Characteristics

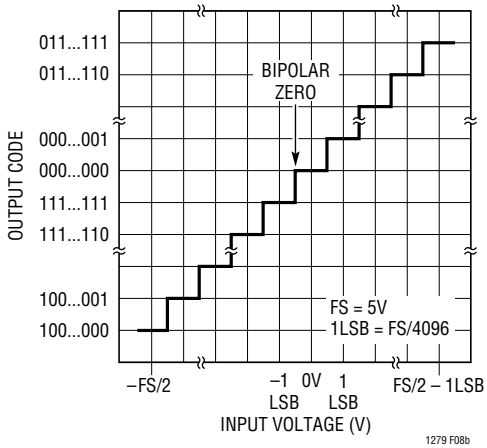


Figure 8b. LTC1279 Bipolar Transfer Characteristics

APPLICATIONS INFORMATION

Unipolar Offset and Full-Scale Error Adjustments

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 9a shows the extra components required for full-scale error adjustment. If both offset and full-scale adjustments are needed, the circuit in Figure 9b can be used. For zero offset error apply 0.61mV (i.e., 0.5LSB) at the input and adjust the offset trim until the LTC1279 output code flickers between 0000 0000 0000 and 0000 0000 0001. For zero full-scale error apply an analog input of 4.99817V (i.e., FS – 1.5LSB or last code transition) at the input and adjust R5 until the LTC1279 output code flickers between 1111 1111 1110 and 1111 1111 1111.

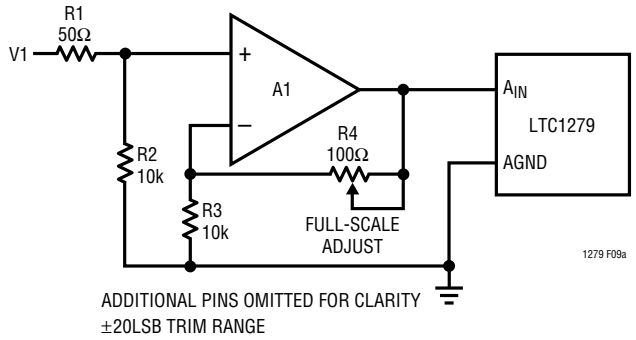


Figure 9a. Full-Scale Adjust Circuit

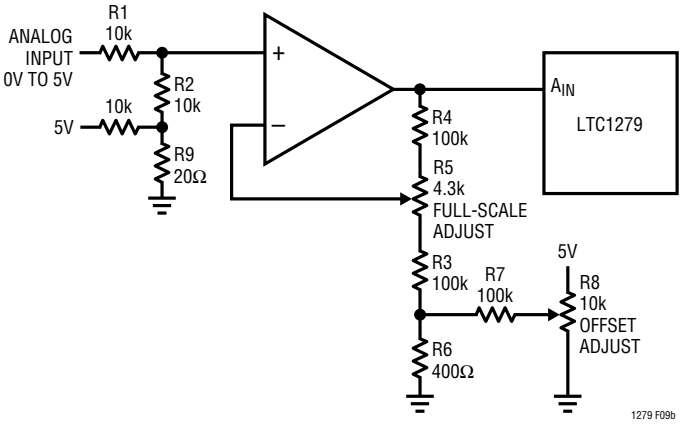


Figure 9b. LTC1279 Unipolar Offset and Full-Scale Adjust Circuit

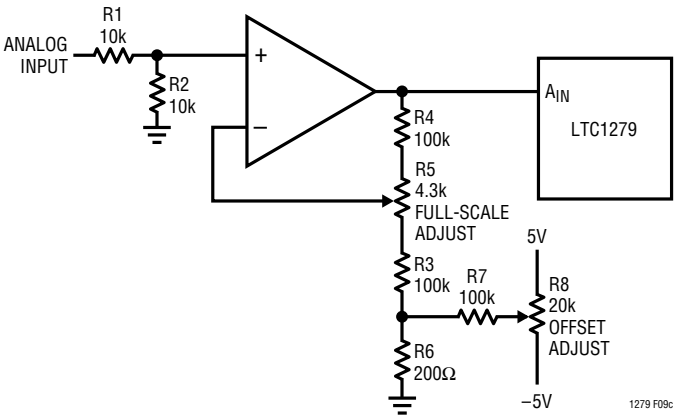


Figure 9c. LTC1279 Bipolar Offset and Full-Scale Adjust Circuit

Bipolar Offset and Full-Scale Error Adjustments

Bipolar offset and full-scale errors are adjusted in a similar fashion to the unipolar case. Again, bipolar offset must be adjusted before full-scale error. Bipolar offset error adjustment is achieved by trimming the offset of the op amp driving the analog input of the LTC1279 while the input voltage is 0.5LSB below ground. This is done by applying an input voltage of –0.61mV (–0.5LSB) to the input in Figure 9c and adjusting the R8 until the ADC output code flickers between 0000 0000 0000 and 1111 1111 1111. For full scale adjustment, an input voltage of 2.49817V (FS – 1.5LSBs) is applied to the input and R5 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

BOARD LAYOUT AND BYPASSING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1279, a printed circuit board is required. The printed circuit board's layout should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital trace alongside an analog signal trace or underneath the ADC. The analog input should be screened by AGND.

High quality tantalum and ceramic bypass capacitors should be used at the AV_{DD} and V_{REF} pins as shown in Figure 10. For the bipolar mode, a 0.1μF ceramic provides

APPLICATIONS INFORMATION

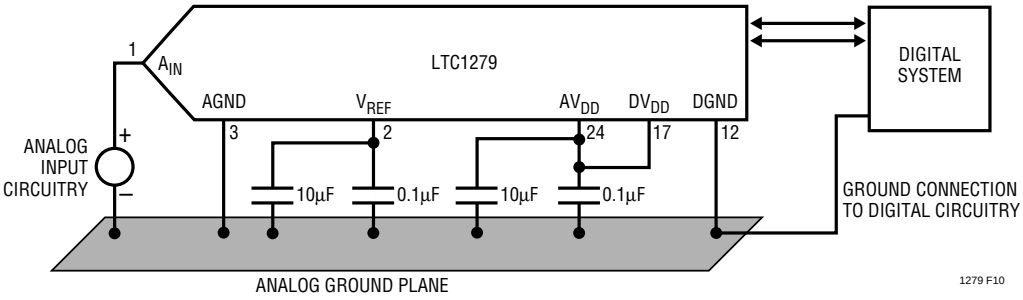


Figure 10. Power Supply Grounding Practice

adequate bypassing for the V_{SS} pin. The capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

Input signal traces to A_{IN} (pin 1) and signal return traces from AGND (pin 3) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible, a shielded cable between the signal source and ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

A single point analog ground, separate from the logic system ground, should be established with an analog ground plane at pin 3 (AGND) or as close as possible to the ADC. Pin 12 (DGND) and all other analog grounds should be connected to this single analog ground point. No other digital grounds should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion or by using three-state buffers to isolate the ADC data bus.

DIGITAL INTERFACE

The A/D converter is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. A separate $\overline{CONVST}$ is used to initiate a conversion.

Internal Clock

The A/D converter has an internal clock that eliminates the need of synchronization between the external clock and the $\overline{CS}$ and $\overline{RD}$ signals found in other ADCs. The internal clock is factory trimmed to achieve a typical conversion time of 1.4µs. No external adjustments are required, and with the typical acquisition time of 160ns, throughput performance of 600ksps is assured.

Power Shutdown

The LTC1279 provides a power shutdown feature that saves power when the ADC is in inactive periods. To power down the ADC, pin 18 ($\overline{SHDN}$) needs to be driven low. When in power shutdown mode, the LTC1279 will not start a conversion even though the $\overline{CONVST}$ goes low. All the power is off except the Internal Reference which is still active and provides 2.42V output voltage to the other circuitry. In this mode the ADC draws 8.5mW instead of 60mW (for minimum power, the logic inputs must be within 600mV of the supply rails). The wake-up time from the power shutdown to active state is 350ns.

APPLICATIONS INFORMATION

Timing and Control

Conversion start and data read operations are controlled by three digital inputs: $\overline{CS}$, $\overline{CONVST}$ and $\overline{RD}$. Figure 11 shows the logic structure associated with these inputs. A logic "0" for $\overline{CONVST}$ will start a conversion after the ADC has been selected (i.e., $\overline{CS}$ is low). Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output, and this is low while conversion is in progress.

Figures 12 through 16 show several different modes of operation. In modes 1a and 1b (Figures 12 and 13) $\overline{CS}$ and $\overline{RD}$ are both tied low. The falling $\overline{CONVST}$ starts the conversion. The data outputs are always enabled and data can be latched with the $\overline{BUSY}$ rising edge. Mode 1a shows operation with a narrow logic low $\overline{CONVST}$ pulse. Mode 1b shows a narrow logic high $\overline{CONVST}$ pulse.

In mode 2 (Figure 14) $\overline{CS}$ is tied low. The falling $\overline{CONVST}$ signal again starts the conversion. Data outputs are in three-state until read by MPU with the $\overline{RD}$ signal. Mode 2 can be used for operation with a shared MPU databus.

In Slow memory and ROM modes (Figures 15 and 16) $\overline{CS}$ is tied low and $\overline{CONVST}$ and $\overline{RD}$ are tied together. The MPU starts conversion and reads the output with the $\overline{RD}$ signal. Conversions are started by the MPU or DSP (no external sample clock).

In Slow memory mode the processor applies a logic low to $\overline{RD}$ (= $\overline{CONVST}$), starting the conversion. $\overline{BUSY}$ goes low, forcing the processor into a WAIT state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; $\overline{BUSY}$ goes high, releasing the processor; the processor applies a logic high to $\overline{RD}$ (= $\overline{CONVST}$) and reads the new conversion data.

In ROM mode, the processor applies a logic low to $\overline{RD}$ (= $\overline{CONVST}$), starting a conversion and reading the previous conversion result. After the conversion is complete, the processor can read the new result (which will initiate another conversion).

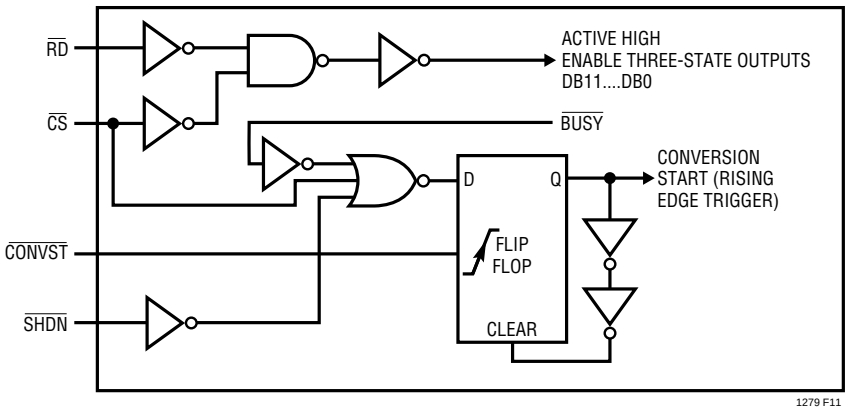


Figure 11. Internal Logic for Control Inputs $\overline{CS}$, $\overline{RD}$, $\overline{CONVST}$ and $\overline{SHDN}$

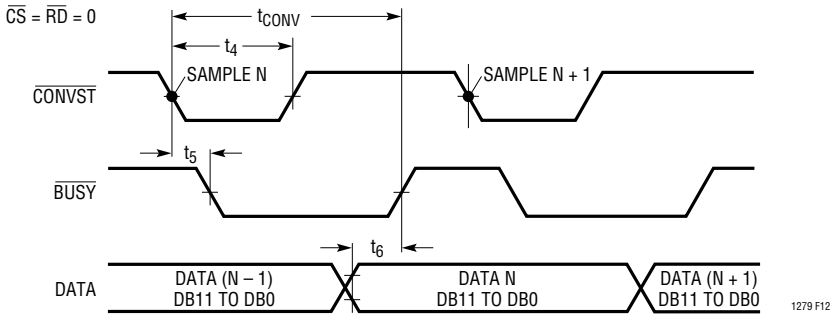


Figure 12. Mode 1a. $\overline{CONVST}$ Starts a Conversion. Data Ouputs Always Enabled. ($\overline{CONVST}$ = ⊓⊔⊓)

APPLICATIONS INFORMATION

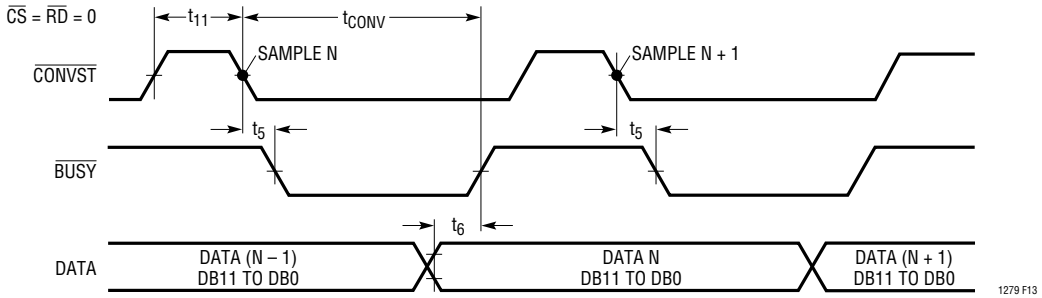


Figure 13. Mode 1b. $\overline{\text{CONVST}}$ Starts a Conversion. Data Outputs Always Enabled.($\overline{\text{CONVST}}$ = ⎍⎍)

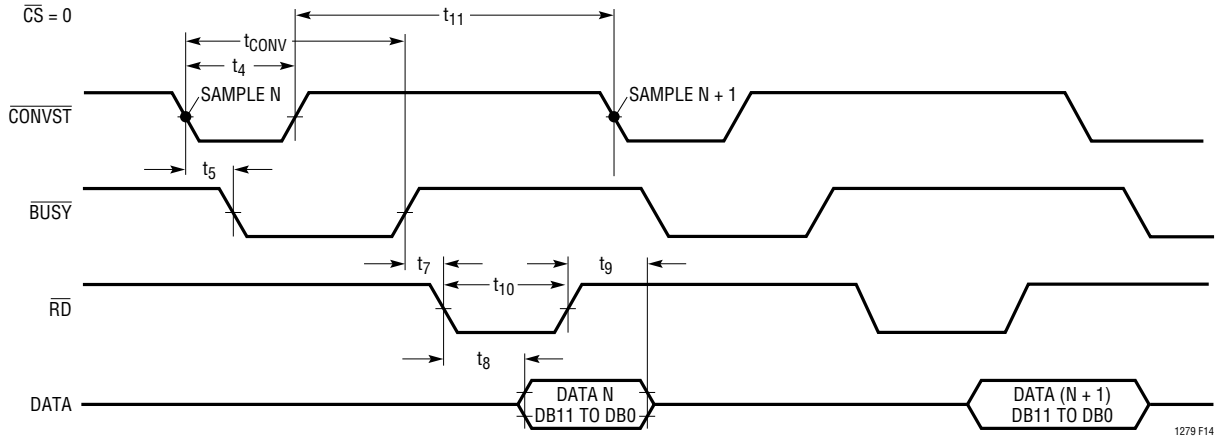


Figure 14. Mode 2. $\overline{\text{CONVST}}$ Starts a Conversion. Data is Read by $\overline{\text{RD}}$

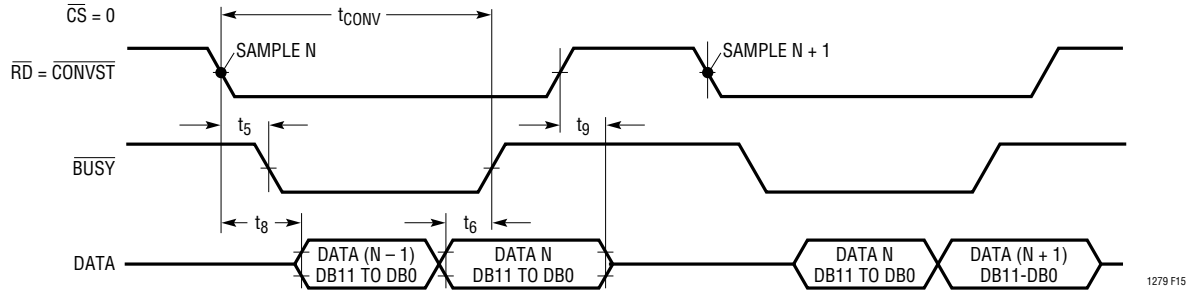


Figure 15. Slow Memory Mode

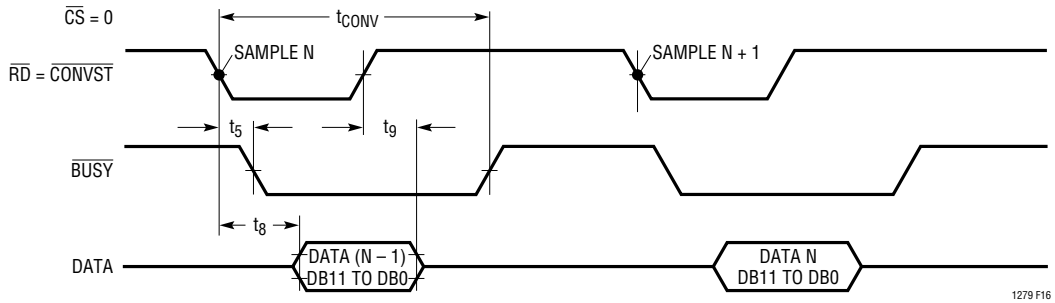
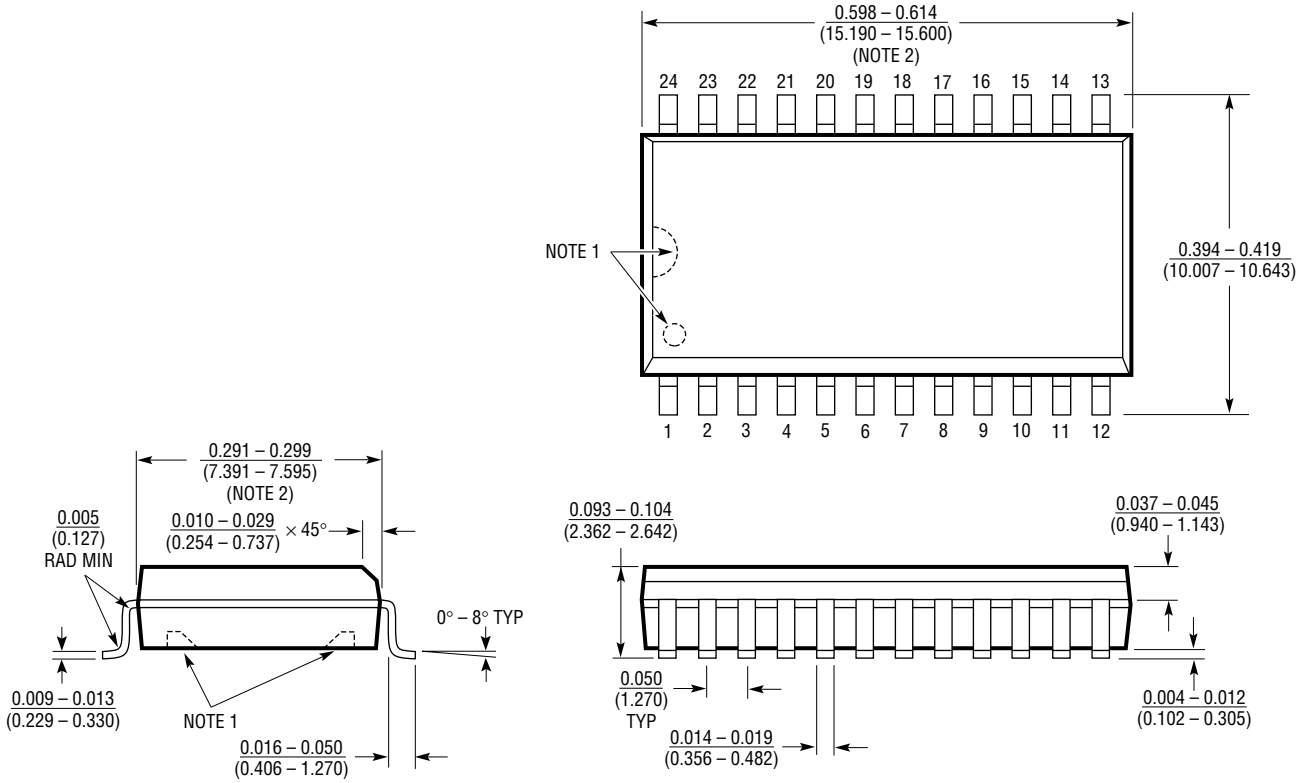


Figure 16. ROM Mode Timing

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

S Package
24-Lead Plastic SOL



SOL24 0392

NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.
2. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

RELATED PARTS (12 Bit)

PART NUMBER	DESCRIPTION	COMMENTS
LTC1272	12-Bit, 3µs, 250kHz Sampling A/D Converter	Single 5V, Sampling 7572 Upgrade
LTC1273/LTC1275/LTC1276	12-Bit, 300ksps Sampling A/D Converters with Reference	Complete with Clock, Reference
LTC1274/LTC1277	12-Bit, 10mW, 100ksps A/D Converters with 1µA Shutdown	Complete with Clock, Reference
LTC1278	12-Bit, 500ksps Sampling A/D Converter with Shutdown	70dB SINAD at Nyquist, Low Power
LTC1282	3V, 140ksps 12-Bit Sampling A/D Converter with Reference	3V or ±3V ADC with Reference, Clock
LTC1409	12-Bit, 800ksps Sampling A/D Converter with Shutdown	Fast, Complete Low Power ADC
LTC1410	12-Bit, 1.25Msps Sampling A/D Converter with Shutdown	Fast, Complete, Wideband ADC

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7487
(408) 432-1900 • FAX: (408) 434-0507 • TELEX: 499-3977

LT/GP 0495 10K • PRINTED IN USA

© LINEAR TECHNOLOGY CORPORATION 1995