ISL6744

Intermediate Bus PWM Controller

FN9147
Rev.8.00
September 22, 2005

The ISL6744 is a low cost, primary side, double-ended controller intended for applications using full and half-bridge topologies for unregulated DC/DC converters. It is a voltage-mode PWM controller designed for half-bridge and full-bridge power supplies. It provides precise control of switching frequency, adjustable soft-start, precise deadtime control with deadtimes as low as 35ns, and overcurrent shutdown.

Low start-up and operating currents allow for easy biasing in both AC/DC and DC/DC applications. This advanced BiCMOS design features low start-up and operating currents, adjustable switching frequency up to 1MHz, 1A FET drivers, and very low propagation delays for a fast response to overcurrent faults.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6744AU	-40 to 105	8 Ld MSOP	M8.118
ISL6744AUZ (Note)	-40 to 105	8 Ld MSOP (Pb-free)	M8.118
ISL6744AB	-40 to 105	8 Ld SOIC	M8.15
ISL6744ABZ (Note)	-40 to 105	8 Ld SOIC (Pb-free)	M8.15

Add “-T” suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

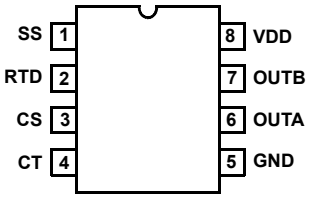
- Precision Duty Cycle and Deadtime Control
- 100µA Start-up Current
- Adjustable Delayed Overcurrent Shutdown and Restart
- Adjustable Oscillator Frequency Up to 2MHz
- 1A MOSFET Gate Drivers
- Adjustable Soft-Start
- Internal Over Temperature Protection
- 35ns Control to Output Propagation Delay
- Small Size and Minimal External Component Count
- Input Undervoltage Protection
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

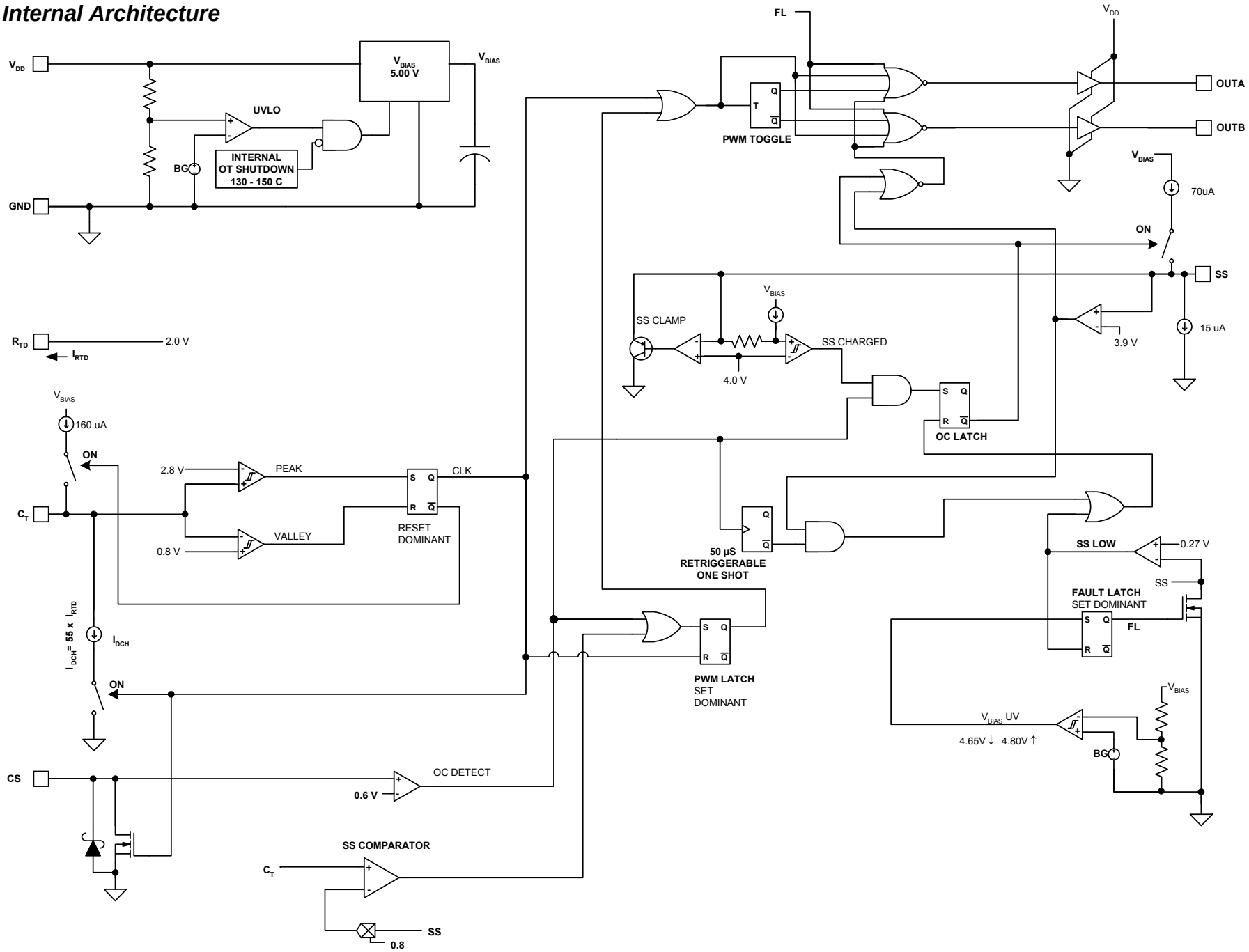
- Telecom and Datacom Isolated Power
- DC Transformers
- Bus Converters

Pinout

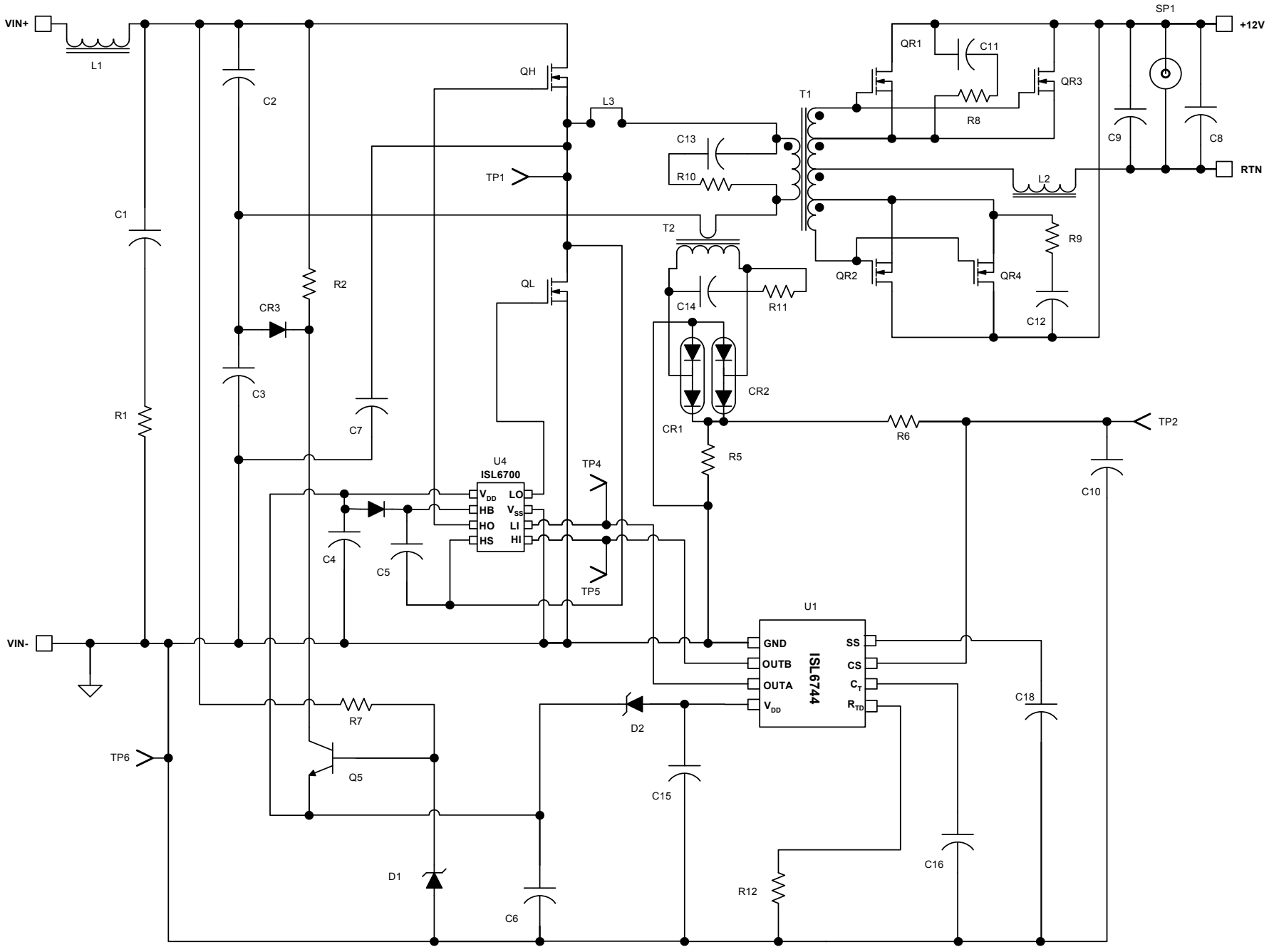
ISL6744 (SOIC, MSOP)
TOP VIEW



Internal Architecture



Typical Application using ISL6744 - 48V Input DC Transformer, 12V @ 8A Output



Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . GND - 0.3V to +20.0V
OUTA, OUTB . . . . . GND - 0.3V to V_{DD}
Signal Pins . . . . . GND - 0.3V to 5V
Peak GATE Current 1A
ESD Classification
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 2000V
Machine Model (Per EIAJ ED-4701 Method C-111) 100V
Charged Device Model (Per EOS/ESD DS5.3, 4/14/93) . . . 1000V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
8 Lead MSOP	128
8 Lead SOIC	98

Maximum Junction Temperature . . . . . -55°C to 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Operating Conditions

Temperature Range
ISL6744AU . . . . . -40°C to 105°C
Supply Voltage Range (Typical) . . . . . 9-16 VDC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. All voltages are to be measured with respect to GND, unless otherwise specified.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application schematic. 9V < V_D < 16V, R_{TD} = 51.1kΩ, C_T = 470pF, T_A = -40°C to 105°C (Note 4), Typical values are at T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE					
Start-Up Current, I_{DD}	V_{DD} < START Threshold	-	-	175	µA
Operating Current, I_{DD}	R_{LOAD}, $C_{OUTA,B}$ = 0	-	2.89	-	mA
	$C_{OUTA,B}$ = 1nF	-	5	8.5	mA
UVLO START Threshold		5.9	6.3	6.6	V
UVLO STOP Threshold		5.3	5.7	6.3	V
Hysteresis		-	0.6	-	V
CURRENT SENSE					
Current Limit Threshold		0.55	0.6	0.65	V
CS to OUT Delay	(Note 4)	-	35	-	ns
CS Sink Current		8	10	-	mA
Input Bias Current		-1	-	1	µA
PULSE WIDTH MODULATOR					
Minimum Duty Cycle	V_{ERROR} < C_T Offset	-	-	0	%
Maximum Duty Cycle	C_T = 470pF, R_{TD} = 51.1kΩ	-	94	-	%
	C_T = 470pF, R_{TD} = 1.1kΩ (Note 4)	-	99	-	%
C_T to SS Comparator Input Gain	(Note 4)	-	1	-	V/V
SS to SS Comparator Input Gain	(Note 4)	-	0.8	-	V/V

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application schematic. 9V < V_D < 16V, R_{TD} = 51.1kΩ, C_T = 470pF, T_A = -40°C to 105°C (Note 4), Typical values are at T_A = 25°C **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR					
Charge Current		143	156	170	µA
R_{TD} Voltage		1.925	2	2.075	V
Discharge Current Gain		45	-	65	µA/µA
C_T Valley Voltage		0.75	0.8	0.85	V
C_T Peak Voltage		2.70	2.80	2.90	V
SOFT-START					
Charging Current		45	-	68	µA
SS Clamp Voltage		3.8	4.0	4.2	V
Overcurrent Shutdown Threshold Voltage	(Note 4)	-	3.9	-	V
Overcurrent Discharge Current		12	15	23	µA
Reset Threshold Voltage	(Note 4)	0.25	0.27	0.30	V
OUTPUT					
High Level Output Voltage (VOH)	V_{DD} - V_{OUTA} or V_{OUTB}, I_{OUT} = -100mA	-	0.5	2.0	V
Low Level Output Voltage (VOL)	I_{OUT} = 100mA	-	0.5	1.0	V
Rise Time	C_{GATE} = 1nF, V_{DD} = 12V	-	17	60	ns
Fall Time	C_{GATE} = 1nF, V_{DD} = 12V	-	20	60	ns
THERMAL PROTECTION					
Thermal Shutdown	(Note 4)	-	145	-	°C
Thermal Shutdown Clear	(Note 4)	-	130	-	°C
Hysteresis, Internal Protection	(Note 4)	-	15	-	°C

NOTES:

3. Specifications at -40°C are guaranteed by design, not production tested.
4. Guaranteed by design, not 100% tested in production.

Typical Performance Curves

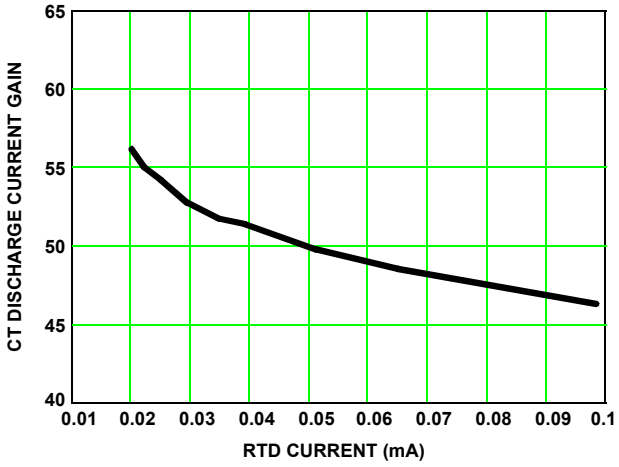


FIGURE 1. OSCILLATOR CT DISCHARGE CURRENT GAIN

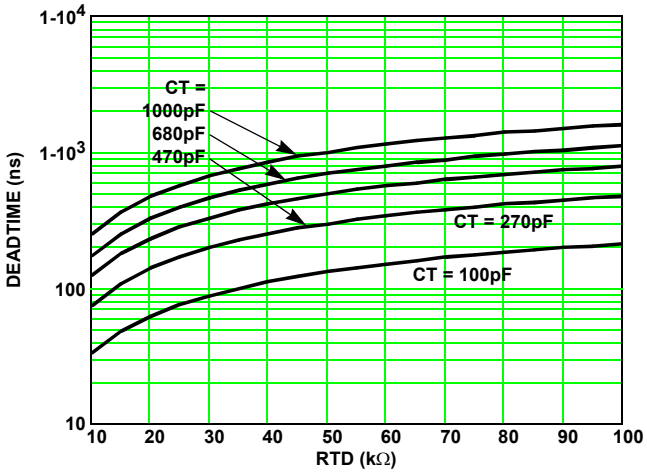


FIGURE 2. DEADTIME vs CAPACITANCE

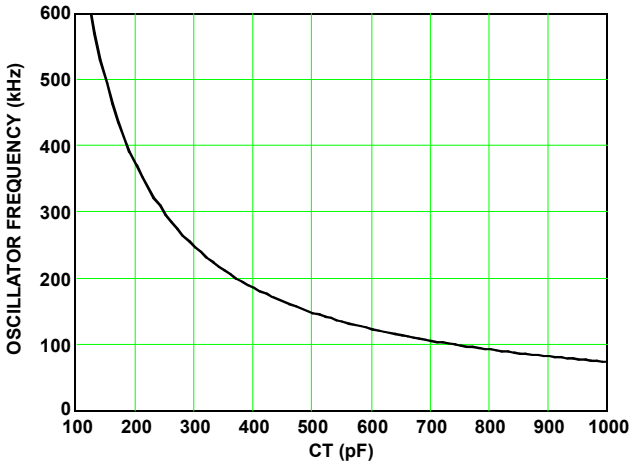


FIGURE 3. CAPACITANCE vs OSCILLATOR FREQUENCY (RTD = 49.9kΩ)

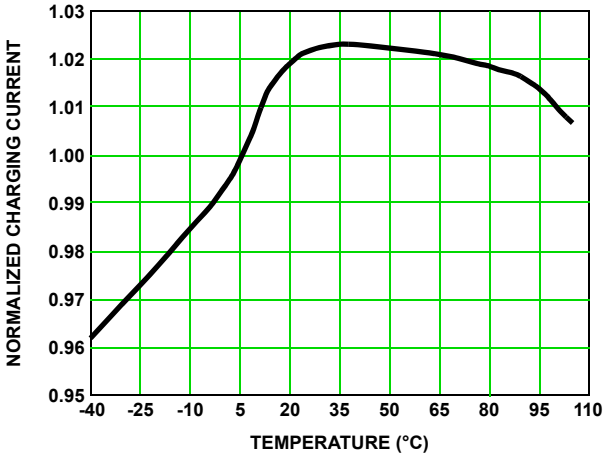


FIGURE 4. CHARGE CURRENT vs TEMPERATURE

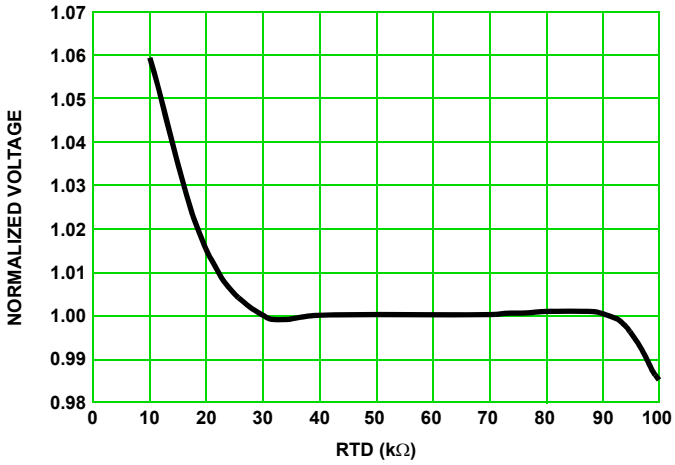


FIGURE 5. TIMING CAPACITOR VOLTAGE vs RTD

Pin Descriptions

V_{DD} - V_{DD} is the power connection for the IC. To optimize noise immunity, bypass V_{DD} to GND with a ceramic capacitor as close to the V_{DD} and GND pins as possible.

The total supply current, I_{DD}, will be dependent on the load applied to outputs OUTA and OUTB. Total I_{DD} current is the sum of the quiescent current and the average output current. Knowing the operating frequency, Fsw, and the output loading capacitance charge, Q, per output, the average output current can be calculated from:

$$I_{OUT} = 2 \bullet Q \bullet Fsw \quad \text{(EQ. 1)}$$

R_{TD} - This is the oscillator timing capacitor discharge current control pin. A resistor is connected between this pin and GND. The current flowing through the resistor determines the magnitude of the discharge current. The discharge current is nominally 55x this current. The PWM deadtime is determined by the timing capacitor discharge duration.

C_T - The oscillator timing capacitor is connected between this pin and GND.

CS - This is the input to the overcurrent protection comparator. The overcurrent comparator threshold is set at 0.600V nominal. The CS pin is shorted to GND at the end of each switching cycle. Depending on the current sensing source impedance, a series input resistor may be required due to the delay between the internal clock and the external power switch.

Exceeding the overcurrent threshold will start a delayed shutdown sequence. Once an overcurrent condition is detected, the soft-start charge current source is disabled. The soft-start capacitor begins discharging through a 15µA current source, and if it discharges to less than 3.9V (Sustained Overcurrent Threshold), a shutdown condition occurs and the OUTA and OUTB outputs are forced low. When the soft-start voltage reaches 0.27V (Reset Threshold) a soft-start cycle begins.

If the overcurrent condition ceases, and then an additional 50µs period elapses before the shutdown threshold is reached, no shutdown occurs. The SS charging current is re-enabled and the soft-start voltage is allowed to recover.

GND - Reference and power ground for all functions on this device. Due to high peak currents and high frequency operation, a low impedance layout is necessary. Ground planes and short traces are highly recommended.

OUTA and OUTB - Alternate half cycle output stages. Each output is capable of 1A peak currents for driving power MOSFETs or MOSFET drivers. Each output provides very low impedance to overshoot and undershoot.

SS - Connect the soft-start timing capacitor between this pin and GND to control the duration of soft-start. The value of the capacitor determines the rate of increase of the duty cycle during start-up, controls the overcurrent shutdown delay, and the overcurrent and short circuit hiccup restart period.

Functional Description

Features

The ISL6744 PWM is an excellent choice for low cost bridge topologies for applications requiring accurate frequency and deadtime control. Among its many features are 1A FET drivers, adjustable soft-start, overcurrent protection and internal thermal protection, allowing a highly flexible design with minimal external components.

Oscillator

The ISL6744 has an oscillator with a frequency range to 2MHz, programmable using a resistor R_{TD} and capacitor C_T.

The switching period may be considered to be the sum of the timing capacitor charge and discharge durations. The charge duration is determined by C_T and the internal current source (assumed to be 160µA in the formula). The discharge duration is determined by R_{TD} and C_T.

$$T_C \approx 1.25 \times 10^4 \bullet C_T \quad s \quad \text{(EQ. 2)}$$

$$T_D \approx \frac{1}{CTDischargeCurrentGain} \bullet R_{TD} \bullet C_T \quad s \quad \text{(EQ. 3)}$$

$$T_{OSC} = T_C + T_D = \frac{1}{F_{OSC}} \quad s \quad \text{(EQ. 4)}$$

where T_C and T_D are the approximate charge and discharge times, respectively, T_{OSC} is the oscillator free running period, and F_{OSC} is the oscillator frequency. One output switching cycle requires two oscillator cycles. The actual times will be slightly longer than calculated due to internal propagation delays of approximately 5ns/transition. This delay adds directly to the switching duration, and also causes overshoot of the timing capacitor peak and valley voltage thresholds, effectively increasing the peak-to-peak voltage on the timing capacitor. Additionally, if very low charge and discharge currents are used, there will be an increased error due to the input impedance at the C_T pin.

The above formulae help with the estimation of the frequency. Practically, effects like stray capacitances that affect the overall C_T capacitance, variation in R_{TD} voltage and charge current over temperature, etc. exist, and are best evaluated in-circuit. Equation 2 follows from the basic capacitor current equation, $i = C \times \frac{dV}{dt}$. In this case, with variation in dV with R_{TD} (Figure 5), and in charge current (Figure 4), results from Equation 2 would differ from the calculated frequency. The typical performance curves may be used as a tool along with the above equations as a more accurate tool to estimate the operating frequency more accurately.

The maximum duty cycle, D, and deadtime, DT, can be calculated from:

$$D = T_C / T_{OSC} \quad \text{(EQ. 5)}$$

$$DT = (1 - D) \cdot T_{OSC} \quad s \quad \text{(EQ. 6)}$$

Soft-Start Operation

The ISL6744 features a soft-start using an external capacitor in conjunction with an internal current source. Soft-start reduces stresses and surge currents during start-up.

The oscillator capacitor signal, C_T, is compared to the soft-start voltage, SS, in the SS comparator which drives the PWM latch. While the SS voltage is less than 3.5V, duty cycle is limited. The output pulse width increases as the soft-start capacitor voltage increases up to 3.5V. This has the effect of increasing the duty cycle from zero to the maximum pulse width during the soft-start period. When the soft-start voltage exceeds 3.5V, soft-start is completed. Soft-start occurs during start-up and after recovery from an overcurrent shutdown. The soft-start voltage is clamped to 4V.

Gate Drive

The ISL6744 is capable of sourcing and sinking 1A peak current, and may also be used in conjunction with a MOSFET driver such as the ISL6700 for level shifting. To limit the peak current through the IC, an external resistor may be placed between the totem-pole output of the IC (OUTA or OUTB pin) and the gate of the MOSFET. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance.

Overcurrent Operation

Overcurrent delayed shutdown is enabled once the soft-start cycle is complete. If an overcurrent condition is detected, the soft-start charging current source is disabled and the soft-start capacitor is allowed to discharge through a 15µA source. At the same time a 50µs retriggerable one-shot timer is activated. It remains active for 50µs after the overcurrent condition ceases. If the soft-start capacitor discharges to 3.9V, the output is disabled. This state continues until the soft-start voltage reaches 270mV, at which time a new soft-start cycle is initiated. If the overcurrent condition stops at least 50µs prior to the soft-start voltage reaching 3.9V, the soft-start charging currents revert to normal operation and the soft-start voltage is allowed to recover.

Thermal Protection

An internal temperature sensor protects the device should the junction temperature exceed 145°C. There is approximately 15°C of hysteresis.

Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. V_{DD} should be bypassed directly to GND with good high frequency capacitance.

Typical Application

The Typical Application Schematic features the ISL6744 in an unregulated half-bridge DC/DC converter configuration, often referred to as a DC Transformer or Bus Converter.

The input voltage is 48V ±10% DC. The output is a nominal 12V when the input voltage is at 48V. Since this is an unregulated topology, the output voltage will vary proportionately with input voltage. The load regulation is a function of resistance between the source and the converter output. The output is rated at 8A.

Circuit Elements

The converter design is comprised of the following functional blocks:

Input Filtering: L1, C1, R1

Half-Bridge Capacitors: C2, C3

Isolation Transformer: T1

Primary Snubber: C13, R10

Start Bias Regulator: CR3, R2, R7, C6, Q5, D1

Supply Bypass Components: C15, C4

Main MOSFET Power Switch: QH, QL

Current Sense Network: T2, CR1, CR2, R5, R6, R11, C10, C14

Control Circuit: U1, C18, C16, D2

Output Rectification and Filtering: QR1, QR2, QR3, QR4, L2, C9, C8

Secondary Snubber: R8, R9, C11, C12

FET Driver: U4

Bootstrap components for driver: CR4, C5

ZVS Resonant Delay (Optional): L3, C7

Design Specifications

The following design requirements were selected for evaluation purposes:

Switching Frequency, Fsw: 235kHz

V_{IN}: 48 ± 10% V

V_{OUT}: 12V (nominal)

I_{OUT}: 8A (steady state)

P_{OUT}: 100W

Efficiency: 95%

Ripple: 1%

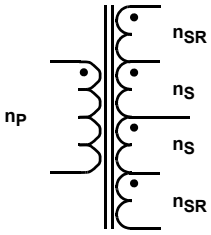


FIGURE 6. TRANSFORMER SCHEMATIC

Transformer Design

The design of a transformer for a half-bridge application is a straightforward affair, although iterative. It is a process of many compromises, and even experienced designers will produce different designs when presented with identical requirements. The iterative design process is not presented here for clarity.

The abbreviated design process follows:

- Select a core geometry suitable for the application. Constraints of height, footprint, mounting preference, and operating environment will affect the choice.
- Determine the turns ratio.
- Select suitable core material(s).
- Select maximum flux density desired for operation.
- Select core size. Core size will be dictated by the capability of the core structure to store the required energy, the number of turns that have to be wound, and the wire gauge needed. Often the window area (the space used for the windings) and power loss determine the final core size.
- Determine maximum desired flux density. Depending on the frequency of operation, the core material selected, and the operating environment, the allowed flux density must be determined. The decision of what flux density to allow is often difficult to determine initially. Usually the highest flux density that produces an acceptable design is used, but often the winding geometry dictates a larger core than is indicated based on flux density alone.
- Determine the number of primary turns.
- Select the wire gauge for each winding.
- Determine winding order and insulation requirements.
- Verify the design.

For this application we have selected a planar structure to achieve a low profile design. A PQ style core was selected because of its round center leg cross section, but there are many suitable core styles available.

Since the converter is operating open loop at nearly 100% duty cycle, the turns ratio, N, is simply the ratio of the input voltage to the output voltage divided by 2.

$$N = \frac{V_{IN}}{V_{OUT} \bullet 2} = \frac{48}{12 \bullet 2} = 2 \qquad \text{(EQ. 7)}$$

The factor of 2 in the denominator is due to the half-bridge topology. Only half of the input voltage is applied to the primary of the transformer.

A PC44HPQ20/6 “E-Core” plus a PC44PQ20/3 “I-Core” from TDK were selected for the transformer core. The ferrite material is PC44.

The core parameter of concern for flux density is the effective core cross-sectional area, Ae. For the PQ core pieces selected:

Ae = 0.62cm^2 or 6.2e -5m^2

Using Faraday’s Law, V = N dΦ/dt, the number of primary turns can be determined once the maximum flux density is set. An acceptable Bmax is ultimately determined by the allowable power dissipation in the ferrite material and is influenced by the lossiness of the core, core geometry, operating ambient temperature, and air flow. The TDK datasheet for PC44 material indicates a core loss factor of ~400mW/cm^3 with a ± 2000 gauss 100kHz sinusoidal excitation. The application uses a 235kHz square wave excitation, so no direct comparison between the application and the data can be made. Interpolation of the data is required. The core volume is approximately 1.6cm^3, so the estimated core loss is

$$P_{loss} \approx \frac{mW}{cm^3} \bullet cm^3 \bullet \frac{f_{act}}{f_{meas}} = 0.4 \bullet 1.6 \bullet \frac{200kHz}{100kHz} = 1.28 \quad W \qquad \text{(EQ. 8)}$$

1.28W of dissipation is significant for a core of this size. Reducing the flux density to 1200 gauss will reduce the dissipation by about the same percentage, or 40%. Ultimately, evaluation of the transformer’s performance in the application will determine what is acceptable.

From Faraday’s Law and using 1200 gauss peak flux density (ΔB = 2400 gauss or 0.24 tesla)

$$N = \frac{V_{IN} \bullet T_{ON}}{2 \bullet A_e \bullet \Delta B} = \frac{53 \bullet 2 \bullet 10^{-6}}{2 \bullet 6.2 \bullet 10^{-5} \bullet 0.24} = 3.56 \quad \text{turns} \qquad \text{(EQ. 9)}$$

Rounding up yields 4 turns for the primary winding. The peak flux density using 4 turns is ~1100 gauss. From EQ. 7, the number of secondary turns is 2.

The volts/turn for this design ranges from 5.4V at V_{IN} = 43V to 6.6V at V_{IN} = 53V. Therefore, the synchronous rectifier (SR) windings may be set at 1 turn each with proper FET selection. Selecting 2 turns for the synchronous rectifier

windings would also be acceptable, but the gate drive losses would increase.

The next step is to determine the equivalent wire gauge for the planar structure. Since each secondary winding conducts for only 50% of the period, the RMS current is

$$I_{RMS} = I_{OUT} \bullet \sqrt{D} = 10 \bullet \sqrt{0.5} = 7.07 \quad A \qquad \text{(EQ. 10)}$$

where D is the duty cycle. Since an FR-4 PWB planar winding structure was selected, the width of the copper traces is limited by the window area width, and the number of layers is limited by the window area height. The PQ core selected has a usable window area width of 0.165 inches. Allowing one turn per layer and 0.020 inches clearance at the edges allows a maximum trace width of 0.125 inches. Using 100 circular mils(c.m.)/A as a guideline for current density, and from EQ. 10, 707c.m. are required for each of the secondary windings (a circular mil is the area of a circle 0.001 inches in diameter). Converting c.m. to square mils yields $555mils^2$ (0.785 sq. mils/c.m.). Dividing by the trace width results in a copper thickness of 4.44mils (0.112mm). Using 1.3mils/oz. of copper requires a copper weight of 3.4oz. For reasons of cost, 3oz. copper was selected.

One layer of each secondary winding also contains the synchronous rectifier winding. For this layer the secondary trace width is reduced by 0.025 inches to 0.100 inches(0.015 inches for the SR winding trace width and 0.010 inches spacing between the SR winding and the secondary winding).

The choice of copper weight may be validated by calculating the DC copper losses of the secondary winding. Ignoring the terminal and lead-in resistance, the resistance of each layer of the secondary may be approximated using EQ. 11.

$$R = \frac{2\pi\rho}{t \bullet \ln\left(\frac{r_2}{r_1}\right)} \quad \Omega \qquad \text{(EQ. 11)}$$

where

R = Winding resistance

ρ = Resistivity of copper = 669e-9Ω-inches at 20°C

t = Thickness of the copper (3 oz.) = 3.9e-3 inches

r_2 = Outside radius of the copper trace = 0.324 or 0.299 inches

r_1 = Inside radius of the copper trace = 0.199 inches

The winding without the SR winding on the same layer has a DC resistance of 2.21mΩ. The winding that shares the layer with the SR winding has a DC resistance of 2.65mΩ. With the secondary configured as a 4 turn center tapped winding (2 turns each side of the tap), the total DC power loss for the secondary at 20°C is 486mW.

The primary windings have an RMS current of approximately 5 A (I_{OUT} x N_S/N_P at ~ 100% duty cycle). The primary is configured as 2 layers, 2 turns per layer to minimize the winding stack height. Allowing 0.020 inches edge clearance and 0.010 inches between turns yields a trace width of 0.0575 inches. Ignoring the terminal and lead-in resistance, and using EQ. 11, the inner trace has a resistance of 4.25mΩ, and the outer trace has a resistance of 5.52mΩ. The resistance of the primary then is 19.5mΩ at 20°C. The total DC power loss for the primary at 20°C is 489mW.

Improved efficiency and thermal performance could be achieved by selecting heavier copper weight for the windings. Evaluation in the application will determine its need.

The order and geometry of the windings affects the AC resistance, winding capacitance, and leakage inductance of the finished transformer. To mitigate these effects, interleaving the windings is necessary. The primary winding is sandwiched between the two secondary windings. The winding layout appears below.

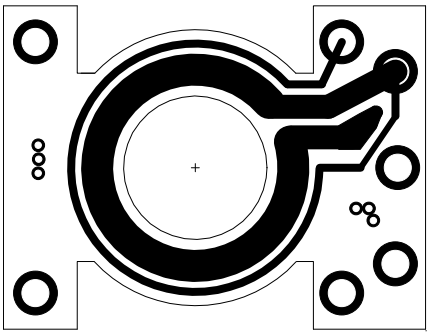


FIGURE 7A. TOP LAYER: 1 TURN SECONDARY AND SR WINDINGS

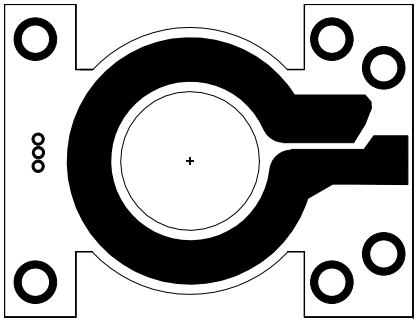


FIGURE 7B. INT. LAYER 1: 1 TURN SECONDARY WINDING

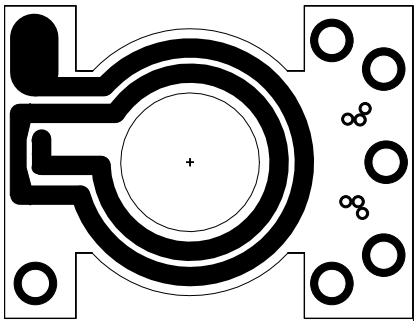


FIGURE 7C. INT. LAYER 2: 2 TURNS PRIMARY WINDING

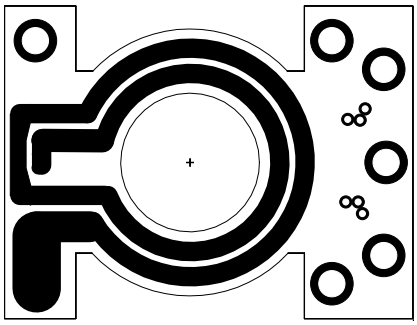


FIGURE 7D. INT. LAYER 3: 2 TURNS PRIMARY WINDING

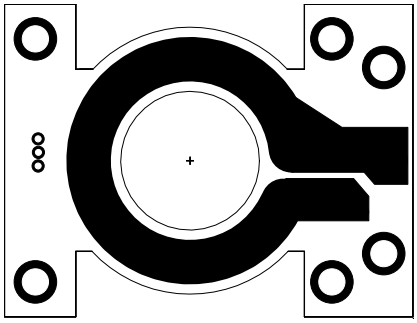


FIGURE 7E. INT. LAYER 4: 1 TURN SECONDARY WINDING

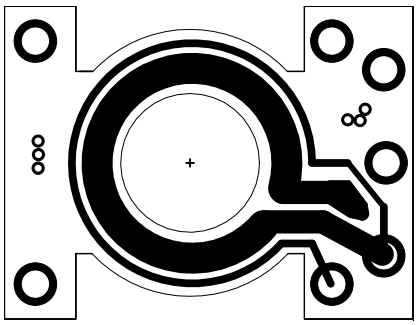


FIGURE 7F. BOTTOM LAYER: 1 TURN SECONDARY AND SR WINDINGS

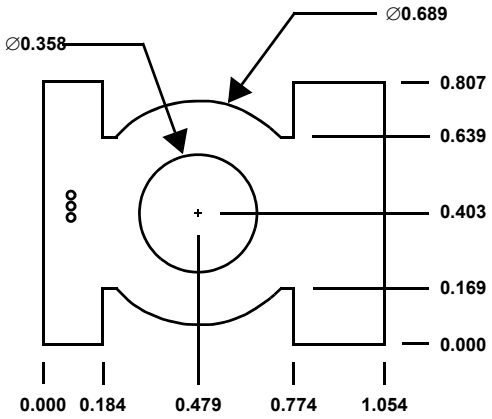


FIGURE 7G. PWB DIMENSIONS

MOSFET Selection

The criteria for selection of the primary side half-bridge FETs and the secondary side synchronous rectifier FETs is largely based on the current and voltage rating of the device. However, the FET drain-source capacitance and gate charge cannot be ignored.

The zero voltage switch (ZVS) transition timing is dependent on the transformer's leakage inductance and the capacitance at the node between the upper FET source and the lower FET drain. The node capacitance is comprised of the drain-source capacitance of the FETs and the transformer parasitic capacitance. The leakage inductance and capacitance form an LC resonant tank circuit which determines the duration of the transition. The amount of energy stored in the LC tank circuit determines the transition voltage amplitude. If the leakage inductance energy is too low, ZVS operation is not possible and near or partial ZVS operation occurs. As the leakage energy increases, the voltage amplitude increases until it is clamped by the FET body diode to ground or V_{IN}, depending on which FET conducts. When the leakage energy exceeds the minimum required for ZVS operation, the voltage is clamped until the energy is transferred. This behavior increases the time window for ZVS operation. This behavior is not without consequences, however. The transition time and the period of time during which the voltage is clamped reduces the effective duty cycle.

The gate charge affects the switching speed of the FETs. Higher gate charge translates into higher drive requirements and/or slower switching speeds. The energy required to drive the gates is dissipated as heat.

The maximum input voltage, V_{IN}, plus transient voltage, determines the voltage rating required. With a maximum input voltage of 53V for this application, and if we allow a 10% adder for transients, a voltage rating of 60V or higher will suffice.

The RMS current through each primary side FET can be determined from EQ. 10, substituting 5A of primary current for I_{OUT} (assuming 100% duty cycle). The result is 3.5A RMS. Fairchild FDS3672 FETs, rated at 100V and 7.5A ($r_{DS(ON)}$ = 22mΩ), were selected for the half-bridge switches.

The synchronous rectifier FETs must withstand approximately one half of the input voltage assuming no switching transients are present. This suggests that a device capable of withstanding at least 30V is required. Empirical testing in the circuit revealed switching transients of 20V were present across the device indicating a rating of at least 60V is required.

The RMS current rating of 7.07A for each SR FET requires a low $r_{DS(ON)}$ to minimize conduction losses, which is difficult to find in a 60V device. It was decided to use two devices in parallel to simplify the thermal design. Two Fairchild FDS5670 devices are used in parallel for a total of four SR FETs. The FDS5670 is rated at 60V and 10A ($r_{DS(ON)}$ = 14mΩ).

Oscillator Component Selection

The desired operating frequency of 235kHz for the converter was established in the ***Design Criteria*** section. The oscillator frequency operates at twice the frequency of the converter because two clock cycles are required for a complete converter period.

During each oscillator cycle the timing capacitor, C_T, must be charged and discharged. Determining the required discharge time to achieve zero voltage switching (ZVS) is the critical design goal in selecting the timing components. The discharge time sets the deadtime between the two outputs, and is the same as ZVS transition time. Once the discharge time is determined, the remainder of the period becomes the charge time.

The ZVS transition duration is determined by the transformer's primary leakage inductance, L_{lk}, by the FET Coss, by the transformer's parasitic winding capacitance, and by any other parasitic elements on the node. The parameters may be determined by measurement, calculation, estimate, or by some combination of these methods.

$$t_{zvs} \approx \frac{\pi\sqrt{L_{lk} \bullet (2C_{oss} + C_{xfrmr})}}{2} \quad s \qquad \text{(EQ. 12)}$$

Device output capacitance, Coss, is non-linear with applied voltage. To find the equivalent discrete capacitance, Cfet, a charge model is used. Using a known current source, the time required to charge the MOSFET drain to the desired operating voltage is determined and the equivalent capacitance is calculated.

$$Cfet = \frac{Ichg \bullet t}{V} \quad F \qquad \text{(EQ. 13)}$$

Once the estimated transition time is determined, it must be verified directly in the application. The transformer leakage inductance was measured at 125nH and the combined capacitance was estimated at 2000pF. Calculations indicate a transition period of ~25ns. Verification of the performance yielded a value of T_D closer to 45ns.

The remainder of the switching half-period is the charge time, T_C, and can be found from

$$T_C = \frac{1}{2 \bullet F_{Sw}} - T_D = \frac{1}{2 \bullet 235 \bullet 10^3} - 45 \bullet 10^{-9} = 2.08 \quad \mu s \qquad \text{(EQ. 14)}$$

where F_{Sw} is the converter switching frequency.

Using Figure 3, the capacitor value appropriate to the desired oscillator operating frequency of 470kHz can be selected. A C_T value of 100pF, 150pF, or 220pF is appropriate for this frequency. A value of 150pF was selected.

To obtain the proper value for R_{TD}, EQ. 3 is used. Since there is a 10ns propagation delay in the oscillator circuit, it must be included in the calculation. The value of R_{TD} selected is 10kΩ.

Output Filter Design

The output filter inductor and capacitor selection is simple and straightforward. Under steady state operating conditions the voltage across the inductor is very small due to the large duty cycle. Voltage is applied across the inductor only during the switch transition time, about 45ns in this application. Ignoring the voltage drop across the SR FETs, the voltage across the inductor during the on time with V_{IN} = 48V is

$$V_L = V_S - V_{OUT} = \frac{V_{IN} \bullet N_S \bullet (1 - D)}{2N_P} \approx 250 \quad mV \qquad \text{(EQ. 15)}$$

where

V_L is the inductor voltage

V_S is the voltage across the secondary winding

V_{OUT} is the output voltage

If we allow a current ramp, ΔI, of 5% of the rated output current, the minimum inductance required is

$$L \geq \frac{V_L \bullet T_{ON}}{\Delta I} = \frac{0.25 \bullet 2.08}{0.5} = 1.04 \quad \mu H \qquad \text{(EQ. 16)}$$

An inductor value of 1.5μH, rated for 18A was selected.

With a maximum input voltage of 53V, the maximum output voltage is about 13V. The closest higher voltage rated capacitor is 16V. Under steady state operating conditions the ripple current in the capacitor is small, so it would seem appropriate to have a low ripple current rated capacitor. However, a high rated ripple current capacitor was selected

based on the nature of the intended load, multiple buck regulators. To minimize the output impedance of the filter, a SANYO OSCON 16SH150M capacitor in parallel with a 22µF ceramic capacitor were selected.

Current Limit Threshold

The current limit threshold is fixed at 0.6V nominal, which is the reference to the overcurrent protection comparator. The current level that corresponds to the overcurrent threshold must be chosen to allow for the dynamic behavior of an open loop converter. In particular, the low inductor ripple current under steady state operation increases significantly as the duty cycle decreases.

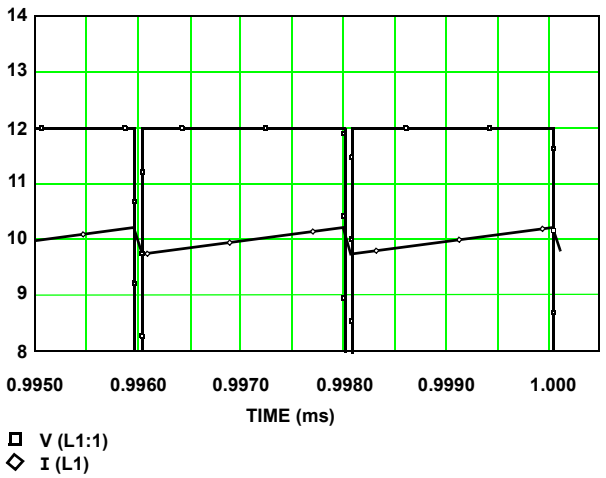


FIGURE 8. STEADY STATE SECONDARY WINDING VOLTAGE AND INDUCTOR CURRENT

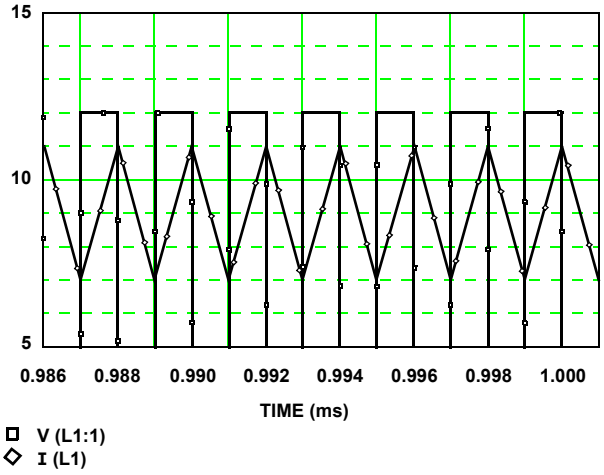


FIGURE 9. SECONDARY WINDING VOLTAGE AND INDUCTOR CURRENT DURING CURRENT LIMIT OPERATION

Figures 8 and 9 show the behavior of the inductor ripple under steady state and overcurrent conditions. In this example, the peak current limit is set at 11A. The peak current limit causes the duty cycle to decrease resulting in a reduction of the average current through the inductor. The implication is that the converter can not supply the same output current in current limit that it can supply under steady state conditions. The peak current limit setpoint must take this behavior into consideration. A 5.11Ω current sense resistor was selected for the rectified secondary of current transformer T2 for the ISL6744Eval 1, corresponding to a peak current limit setpoint of about 11A.

Performance

The major performance criteria for the converter are efficiency, and to a lesser extent, load regulation. Efficiency, load regulation and line regulation performance are demonstrated in the following Figures.

As expected, the output voltage varies considerably with line and load when compared to an equivalent converter with a closed loop feedback. However, for applications where tight regulation is not required, such as those applications that use downstream DC/DC converters, this design approach is viable.

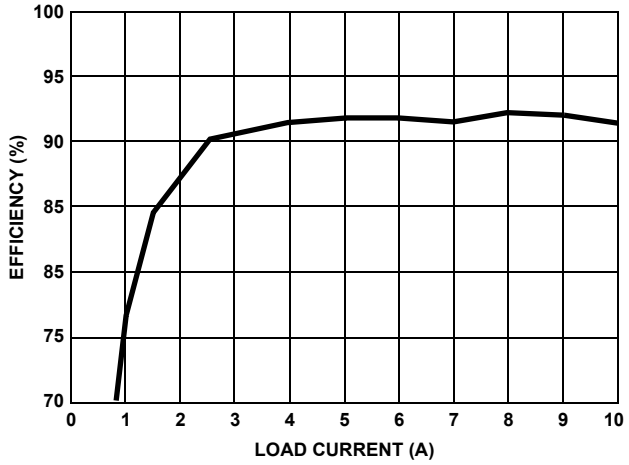


FIGURE 10. EFFICIENCY vs LOAD V_{IN} = 48V

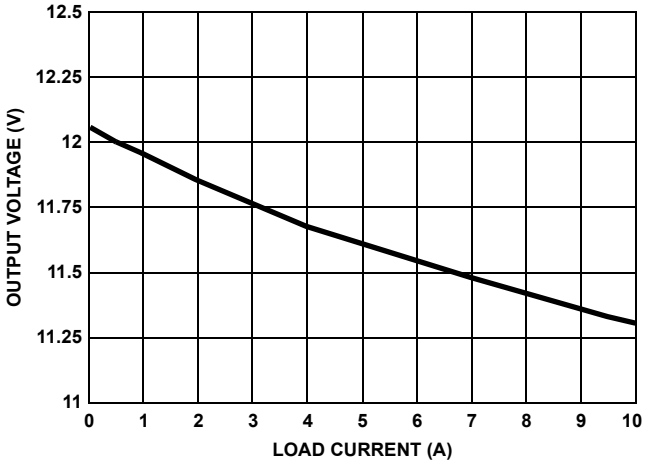


FIGURE 11. LOAD REGULATION AT V_{IN} = 48V

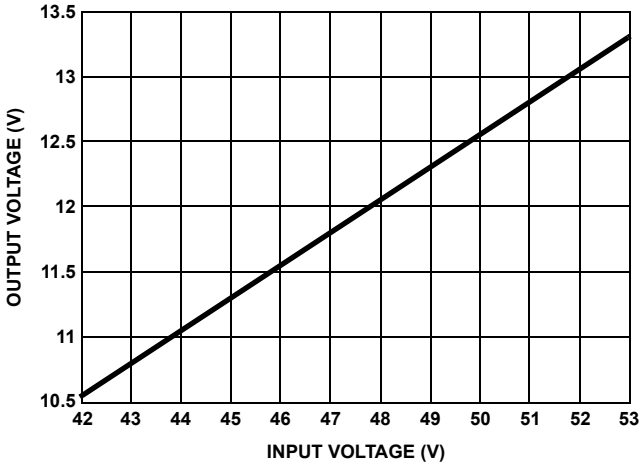


FIGURE 12. LINE REGULATION AT I_{OUT} = 1A

Waveforms

Typical waveforms can be found in the following Figures. Figure 13 shows the output voltage ripple and noise at a 5A.

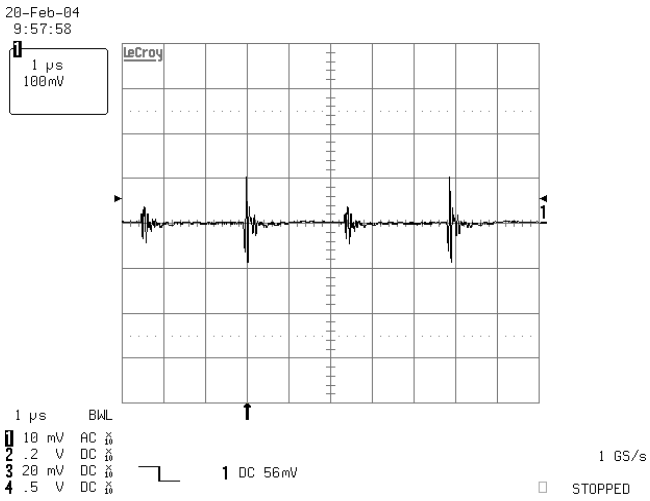


FIGURE 13. OUTPUT RIPPLE AND NOISE - 20MHz BW

Figures 14 and 15 show the voltage waveforms at the switching node shared by the upper FET source and the lower FET drain. In particular, Figure 15 shows near ZVS operation at 5A of load when the upper FET is turning off and the lower FET is turning on. ZVS operation occurs completely, implying that all the energy stored in the node capacitance has been recovered. Figure 16 shows the switching transition between outputs, OUTA and OUTB during steady state operation. The deadtime duration of 46.9ns is clearly shown.

A 2.7V zener is added between the Vdd pins of ISL6700 and ISL6744, in order to ensure that the PWM turns on only after the driver has turned on, thereby ensuring the soft-start function. Figure 17 shows the soft-start operation.

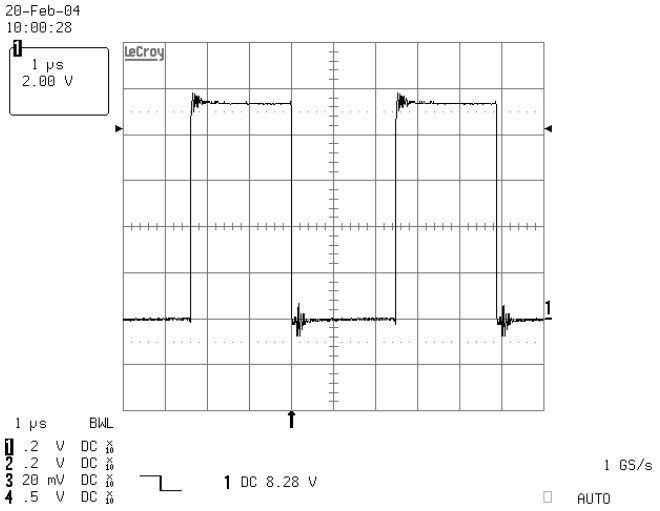


FIGURE 14. FET DRAIN-SOURCE VOLTAGE

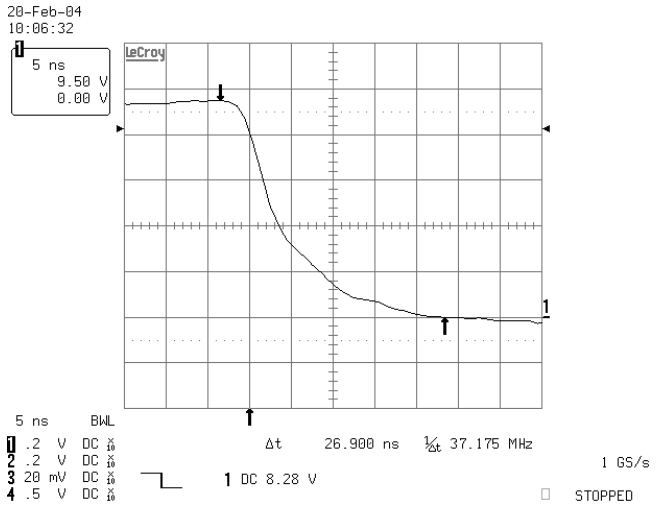


FIGURE 15. FET D-S VOLTAGE NEAR-ZVS TRANSITION

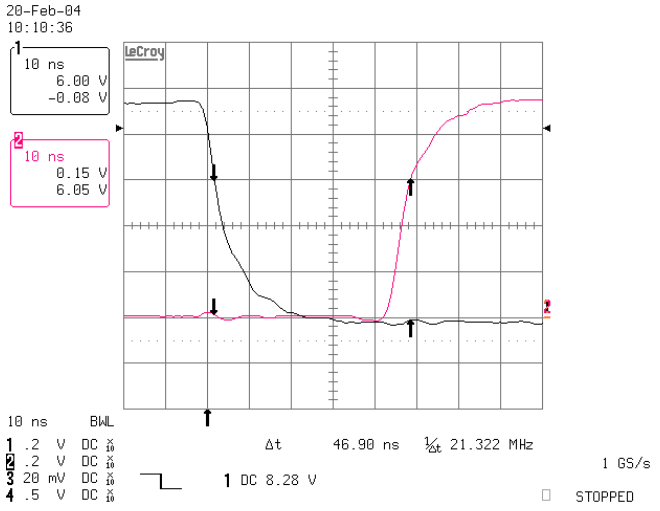


FIGURE 16. OUTA - OUTB TRANSITION

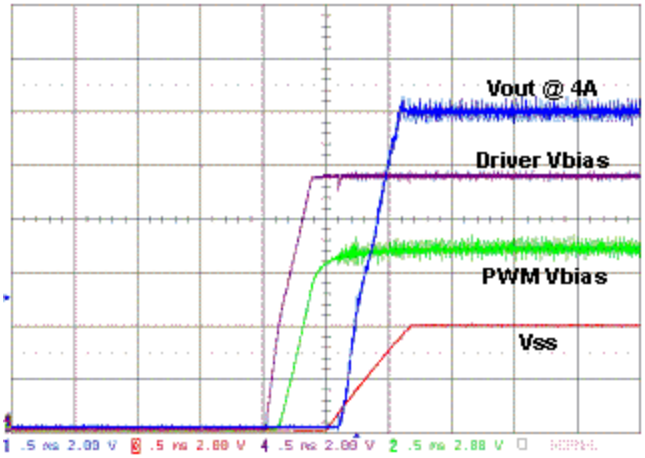


FIGURE 17. OUTPUT SOFT-START

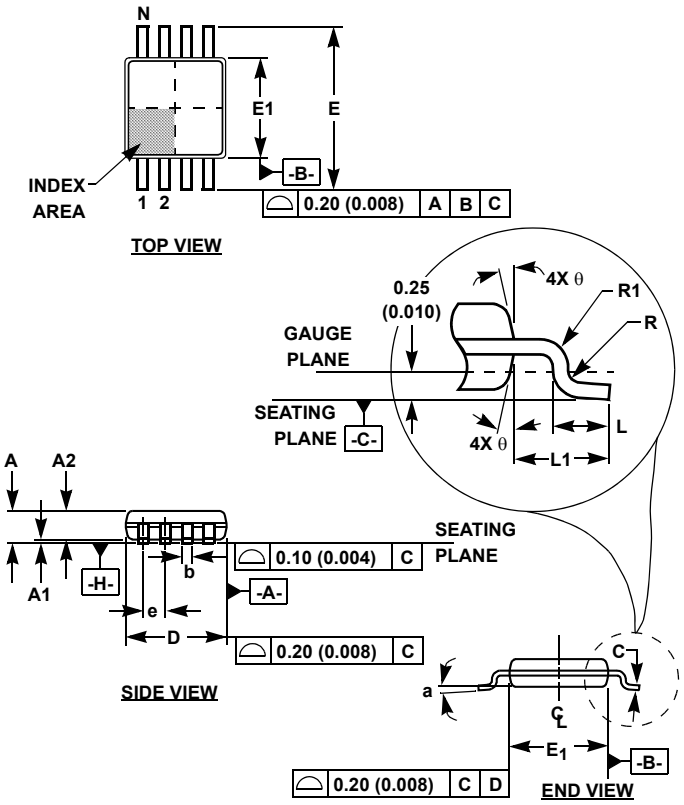
Component List

REFERENCE DESIGNATOR	VALUE	DESCRIPTION
C1	1.0µF	Capacitor, 1812, X7R, 100V, 20%
C2, C3	3.3µF	Capacitor, 1812, X5R, 50V, 20%
C4	1.0µF	Capacitor, 0805, X5R, 16V, 10%
C5	0.1µF	Capacitor, 0603, X7R, 16V, 10%
C6, C15	4.7µF	Capacitor, 0805, X5R, 10V, 20%
C7	Open	Capacitor, 0603, Open or Optional Discrete Stray Capacitance
C8	22µF	Capacitor, 1812, X5R, 16V, 20%
C9	150µF	Capacitor, Radial, Sanyo 16SH150M
C10, C11, C12, C13, C14	1000pF	Capacitor, 0603, X7R, 50V, 10%
C16	150pF	Capacitor, 0603, COG, 16V, 5%
C18	0.01µF	Capacitor, 0603, X7R, 16V, 10%
CR1, CR2		Diode, Schottky, BAT54S, 30V
CR3		Diode, Schottky, BAT54, 30V
CR4		Diode, Schottky, SMA, 100V, 2.1A
D1		Zener, 10V,Zetex BZX84C10ZXCT-ND
D2		Zener, 2.7V, BZX84C2V7
L1	190nH	Pulse, P2004T
L2	1.5µH	Bitech, HM73-301R5
L3	Short	Jumper or Optional Discrete Leakage Inductance
P1, P2, P3, P4		Keystone, 1514-2
Q5	NPN	Transistor, ON MJD31C
QL, QH		FET, Fairchild FDS3672, 100V

Component List (Continued)

REFERENCE DESIGNATOR	VALUE	DESCRIPTION
QR1, QR2, QR3, QR4		FET, Fairchild FDS5670, 60V
R1	3.3	Resistor, 2512, 1%
R2	3.01K	Resistor, 2512, 1%
R5	5.11	Resistor, 0603, 1%
R6	205	Resistor, 0603, 1%
R7	75.0K	Resistor, 0805, 1%
R8, R9	20.0	Resistor, 0805, 1%
R10	18	Resistor, 2512, 1%
R11	100	Resistor, 0603, 1%
R12	10.0K	Resistor, 0603, 1%
T1	Custom	Midcom 31718
T2	Custom	Midcom 31719R
TP1, TP2, TP4, TP5, TP6	5002	Keystone
SP1		Tektronix Scope Jack, 131-4353-00
U1		Intersil ISL6744AU, MSOP8
U4		Intersil ISL6700IB, SOIC

Mini Small Outline Plastic Packages (MSOP)



M8.118 (JEDEC MO-187AA)

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

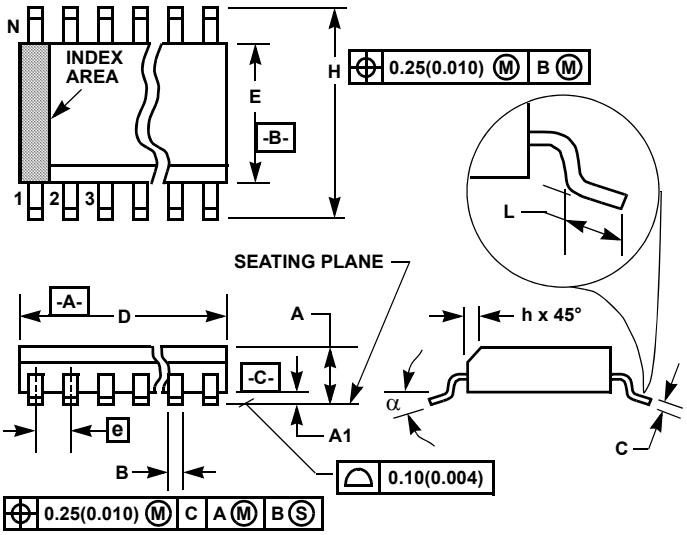
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.010	0.014	0.25	0.36	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.026 BSC		0.65 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	8		8		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
0	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

Rev. 2 01/03

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Rev. 1 6/05

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