



## SN74LVC2G157 Single 2-Line to 1-Line Data Selector Multiplexer

### 1 Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 6 ns at 3.3 V
- Low Power Consumption, 10- $\mu$ A Maximum  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Can Be Used as a Down Translator to Translate Inputs From a Maximum of 5.5 V Down to the  $V_{CC}$  Level
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- Barcode Scanner
- Cable Solutions
- E-Books
- Embedded PC
- Field Transmitter: Temperature or Pressure Sensors
- Fingerprint Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning
- Network-Attached Storage (NAS)
- Server Motherboard and PSU
- Software Defined Radio (SDR)
- TV: High Definition (HDTV), LCD, and Digital
- Video Communications Systems
- Wireless Data Access Cards, Headsets, Keyboards, Mice, and LAN Cards

### 3 Description

This single 2-line to 1-line data selector multiplexer is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC2G157 device features a common strobe ( $\bar{G}$ ) input. When the strobe is high, Y is low and  $\bar{Y}$  is high. When the strobe is low, a single bit is selected from one of two sources and is routed to the outputs. The device provides true and complementary data.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

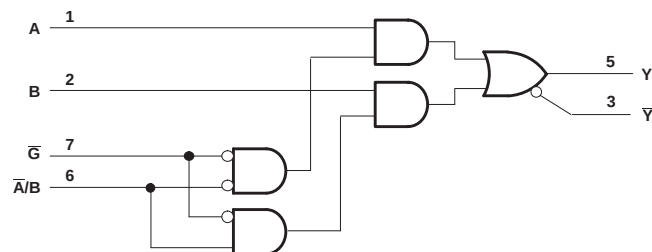
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### Device Information<sup>(1)</sup>

| PART NUMBER     | PACKAGE   | BODY SIZE (NOM)   |
|-----------------|-----------|-------------------|
| SN74LVC2G157DCT | SSOP (8)  | 2.95 mm × 2.80 mm |
| SN74LVC2G157DCU | VSSOP (8) | 2.30 mm × 2.00 mm |
| SN74LVC2G157YZP | DSBGA (8) | 1.91 mm × 0.91 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram (Positive Logic)



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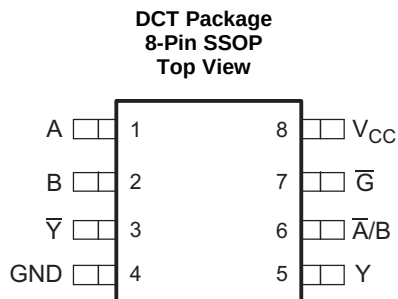
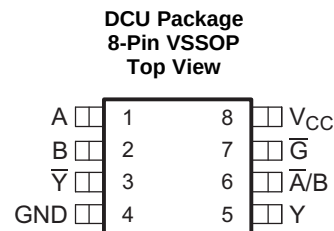
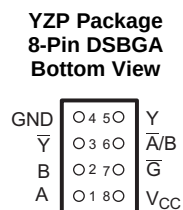
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision L (January 2014) to Revision M</b>                   | <b>Page</b> |
|-------------------------------------------------------------------------------|-------------|
| • Added <i>ESD Ratings</i> table .....                                        | <b>4</b>    |
| • Added <i>Thermal Information</i> table .....                                | <b>5</b>    |
| • Added <i>Typical Characteristics</i> .....                                  | <b>6</b>    |
| • Added <i>Mechanical, Packaging, and Orderable Information</i> section ..... | <b>12</b>   |

| <b>Changes from Revision K (January 2007) to Revision L</b> | <b>Page</b> |
|-------------------------------------------------------------|-------------|
| • Updated document to new TI data sheet format .....        | <b>1</b>    |
| • Removed <i>Ordering Information</i> table .....           | <b>1</b>    |
| • Updated <i>Features</i> .....                             | <b>1</b>    |
| • Added <i>Device Information</i> table .....               | <b>1</b>    |

## 5 Pin Configuration and Functions



See mechanical drawings for dimensions

### Pin Functions

| PIN              |                |       | I/O | DESCRIPTION         |
|------------------|----------------|-------|-----|---------------------|
| NAME             | SSOP,<br>VSSOP | DSBGA |     |                     |
| A                | 1              | 1     | I   | Data Input          |
| $\overline{A/B}$ | 6              | 6     | I   | Input Selector      |
| B                | 2              | 2     | I   | Data Input          |
| $\overline{G}$   | 7              | 7     | I   | Common Strobe Input |
| GND              | 4              | 4     | —   | Ground              |
| $V_{CC}$         | 8              | 8     | —   | Power               |
| Y                | 5              | 5     | O   | Output              |
| $\overline{Y}$   | 3              | 3     | O   | Inverted Output     |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                                                       |                    | MIN  | MAX                   | UNIT |
|------------------|---------------------------------------------------------------------------------------|--------------------|------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage                                                                        |                    | −0.5 | 6.5                   | V    |
| V <sub>I</sub>   | Input voltage <sup>(2)</sup>                                                          |                    | −0.5 | 6.5                   | V    |
| V <sub>O</sub>   | Voltage applied to any output in the high-impedance or power-off state <sup>(2)</sup> |                    | −0.5 | 6.5                   | V    |
| V <sub>O</sub>   | Voltage applied to any output in the high or low state <sup>(2)(3)</sup>              |                    | −0.5 | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>  | Input clamp current                                                                   | V <sub>I</sub> < 0 | −50  |                       | mA   |
| I <sub>OK</sub>  | Output clamp current                                                                  | V <sub>O</sub> < 0 | −50  |                       | mA   |
| I <sub>O</sub>   | Continuous output current                                                             |                    | ±50  |                       | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND                                     |                    | ±100 |                       | mA   |
| T <sub>stg</sub> | Storage temperature                                                                   |                    | −65  | 150                   | °C   |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.

### 6.2 ESD Ratings

|                    |                         | VALUE                                                                          | UNIT |
|--------------------|-------------------------|--------------------------------------------------------------------------------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | 2000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | 1000 |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

See <sup>(1)</sup>.

|                 |                           |                                    | MIN                    | MAX                    | UNIT |
|-----------------|---------------------------|------------------------------------|------------------------|------------------------|------|
| V <sub>CC</sub> | Supply voltage            | Operating                          | 1.65                   | 5.5                    | V    |
|                 |                           | Data retention only                | 1.5                    |                        |      |
| V <sub>IH</sub> | High-level input voltage  | V <sub>CC</sub> = 1.65 V to 1.95 V | 0.65 × V <sub>CC</sub> |                        | V    |
|                 |                           | V <sub>CC</sub> = 2.3 V to 2.7 V   | 1.7                    |                        |      |
|                 |                           | V <sub>CC</sub> = 3 V to 3.6 V     | 2                      |                        |      |
|                 |                           | V <sub>CC</sub> = 4.5 V to 5.5 V   | 0.7 × V <sub>CC</sub>  |                        |      |
| V <sub>IL</sub> | Low-level input voltage   | V <sub>CC</sub> = 1.65 V to 1.95 V |                        | 0.35 × V <sub>CC</sub> | V    |
|                 |                           | V <sub>CC</sub> = 2.3 V to 2.7 V   |                        | 0.7                    |      |
|                 |                           | V <sub>CC</sub> = 3 V to 3.6 V     |                        | 0.8                    |      |
|                 |                           | V <sub>CC</sub> = 4.5 V to 5.5 V   |                        | 0.3 × V <sub>CC</sub>  |      |
| V <sub>I</sub>  | Input voltage             |                                    | 0                      | 5.5                    | V    |
| V <sub>O</sub>  | Output voltage            |                                    | 0                      | V <sub>CC</sub>        | V    |
| I <sub>OH</sub> | High-level output current | V <sub>CC</sub> = 1.65 V           |                        | −4                     | mA   |
|                 |                           | V <sub>CC</sub> = 2.3 V            |                        | −8                     |      |
|                 |                           | V <sub>CC</sub> = 3 V              |                        | −16                    |      |
|                 |                           | V <sub>CC</sub> = 4.5 V            |                        | −24                    |      |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

## Recommended Operating Conditions (continued)

See <sup>(1)</sup>.

|                                                        |                                                                          | MIN | MAX | UNIT |
|--------------------------------------------------------|--------------------------------------------------------------------------|-----|-----|------|
| $I_{OL}$ Low-level output current                      | $V_{CC} = 1.65\text{ V}$                                                 |     | 4   | mA   |
|                                                        | $V_{CC} = 2.3\text{ V}$                                                  |     | 8   |      |
|                                                        | $V_{CC} = 3\text{ V}$                                                    |     | 16  |      |
|                                                        |                                                                          |     | 24  |      |
|                                                        | $V_{CC} = 4.5\text{ V}$                                                  |     | 32  |      |
| $\Delta t/\Delta v$ Input transition rise or fall rate | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}, 2.5\text{ V} \pm 0.2\text{ V}$ |     | 20  | ns/V |
|                                                        | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$                                 |     | 10  |      |
|                                                        | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$                                   |     | 5   |      |
| $T_A$ Operating free-air temperature                   |                                                                          | –40 | 85  | °C   |

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup>                          | SN74LVC2G157 |             |             | UNIT |
|--------------------------------------------------------|--------------|-------------|-------------|------|
|                                                        | DCT (SSOP)   | DCU (VSSOP) | YZP (DSBGA) |      |
|                                                        | 8 PINS       | 8 PINS      | 8 PINS      |      |
| $R_{\theta JA}$ Junction-to-ambient thermal resistance | 220          | 227         | 102         | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                     | TEST CONDITIONS                                                        | $V_{CC}$        | MIN            | TYP <sup>(1)</sup> | MAX      | UNIT          |
|-------------------------------|------------------------------------------------------------------------|-----------------|----------------|--------------------|----------|---------------|
| $V_{OH}$                      | $I_{OH} = -100\text{ }\mu\text{A}$                                     | 1.65 V to 5.5 V | $V_{CC} - 0.1$ |                    |          | V             |
|                               | $I_{OH} = -4\text{ mA}$                                                | 1.65 V          | 1.2            |                    |          |               |
|                               | $I_{OH} = -8\text{ mA}$                                                | 2.3 V           | 1.9            |                    |          |               |
|                               | $I_{OH} = -16\text{ mA}$                                               | 3 V             | 2.4            |                    |          |               |
|                               | $I_{OH} = -24\text{ mA}$                                               |                 | 2.3            |                    |          |               |
|                               | $I_{OH} = -32\text{ mA}$                                               | 4.5 V           | 3.8            |                    |          |               |
| $V_{OL}$                      | $I_{OL} = 100\text{ }\mu\text{A}$                                      | 1.65 V to 5.5 V |                |                    | 0.1      | V             |
|                               | $I_{OL} = 4\text{ mA}$                                                 | 1.65 V          |                |                    | 0.45     |               |
|                               | $I_{OL} = 8\text{ mA}$                                                 | 2.3 V           |                |                    | 0.3      |               |
|                               | $I_{OL} = 16\text{ mA}$                                                | 3 V             |                |                    | 0.4      |               |
|                               | $I_{OL} = 24\text{ mA}$                                                |                 |                |                    | 0.55     |               |
|                               | $I_{OL} = 32\text{ mA}$                                                | 4.5 V           |                |                    | 0.55     |               |
| $I_i$ A, B, or control inputs | $V_i = 5.5\text{ V}$ or GND                                            | 0 to 5.5 V      |                |                    | $\pm 5$  | $\mu\text{A}$ |
| $I_{off}$                     | $V_i$ or $V_o = 5.5\text{ V}$                                          | 0               |                |                    | $\pm 10$ | $\mu\text{A}$ |
| $I_{CC}$                      | $V_i = 5.5\text{ V}$ or GND, $I_o = 0$                                 | 1.65 V to 5.5 V |                |                    | 10       | $\mu\text{A}$ |
| $\Delta I_{CC}$               | One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND | 3 V to 5.5 V    |                |                    | 500      | $\mu\text{A}$ |
| $C_i$                         | $V_i = V_{CC}$ or GND                                                  | 3.3 V           |                |                    | 5        | pF            |

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## 6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ |     | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ |     | UNIT |
|-----------|-----------------|----------------|-------------------------------------------|-----|------------------------------------------|-----|------------------------------------------|-----|----------------------------------------|-----|------|
|           |                 |                | MIN                                       | MAX | MIN                                      | MAX | MIN                                      | MAX | MIN                                    | MAX |      |
| $t_{pd}$  | A or B          | Y or $\bar{Y}$ | 4.4                                       | 14  | 2.1                                      | 8   | 2                                        | 6   | 1.4                                    | 4   | ns   |
|           | $\bar{A}/B$     |                | 4.9                                       | 16  | 2.5                                      | 9   | 2.1                                      | 6   | 1.6                                    | 4   |      |
|           | $\bar{G}$       |                | 4.2                                       | 14  | 2                                        | 8   | 1.6                                      | 6   | 1.3                                    | 4   |      |

## 6.7 Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER |                               | TEST CONDITIONS     | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | $V_{CC} = 5\text{ V}$ | UNIT |
|-----------|-------------------------------|---------------------|-------------------------|-------------------------|-------------------------|-----------------------|------|
|           |                               |                     | TYP                     | TYP                     | TYP                     | TYP                   |      |
| $C_{pd}$  | Power dissipation capacitance | $f = 10\text{ MHz}$ | 35                      | 35                      | 37                      | 40                    | pF   |

## 6.8 Typical Characteristics

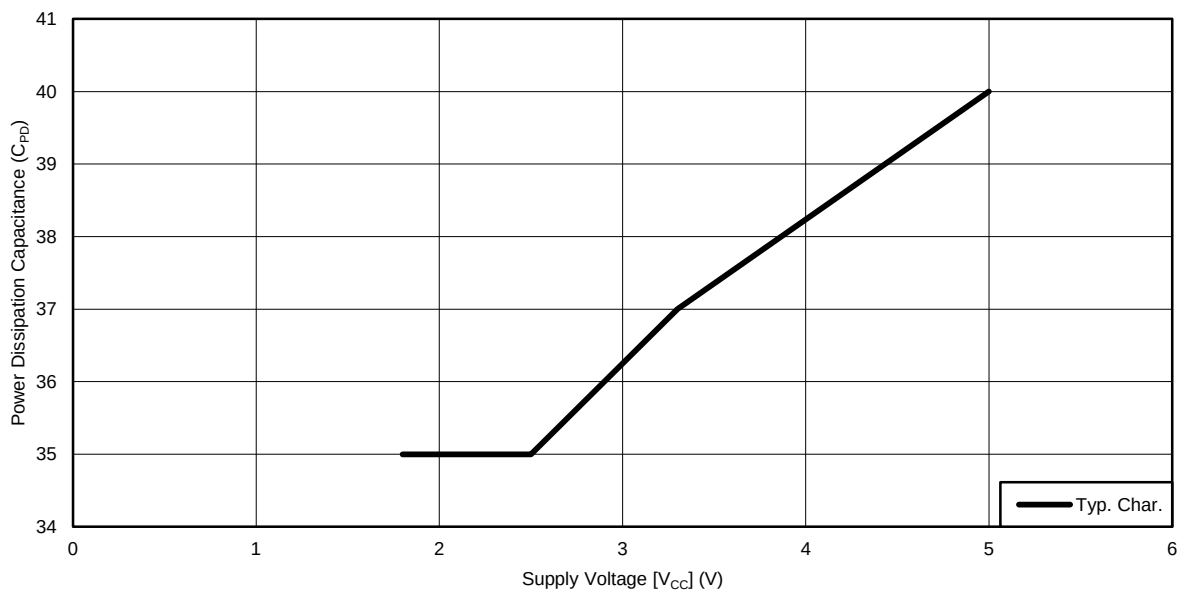
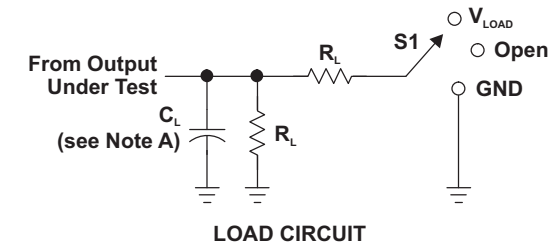


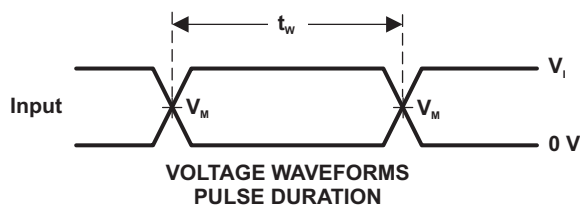
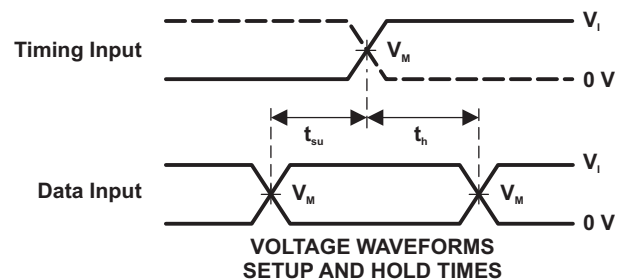
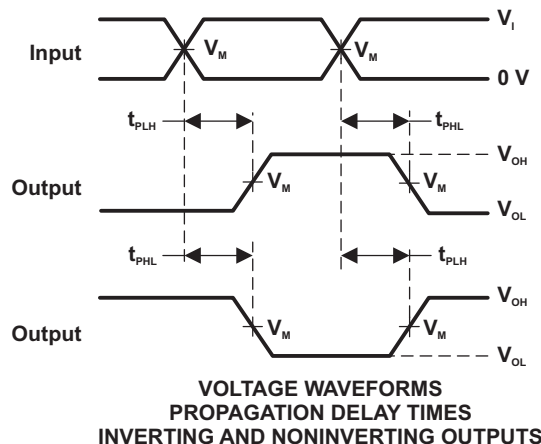
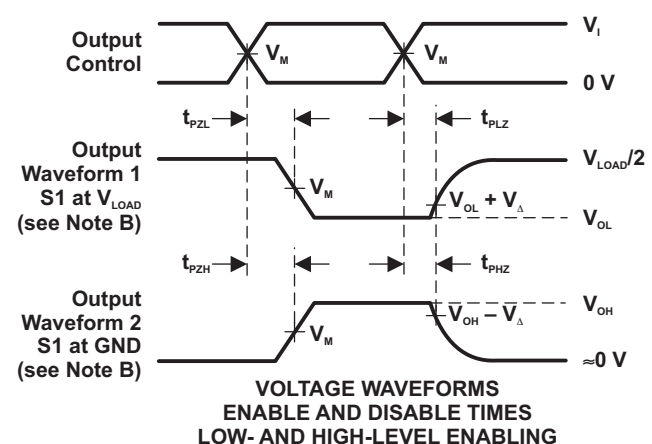
Figure 1. Voltage vs Capacitance

## 7 Parameter Measurement Information



| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_i/t_f$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 3 V      | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $5\text{ V} \pm 0.5\text{ V}$    | $V_{CC}$ | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 $\Omega$ | 0.3 V        |



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_o = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

## 8 Detailed Description

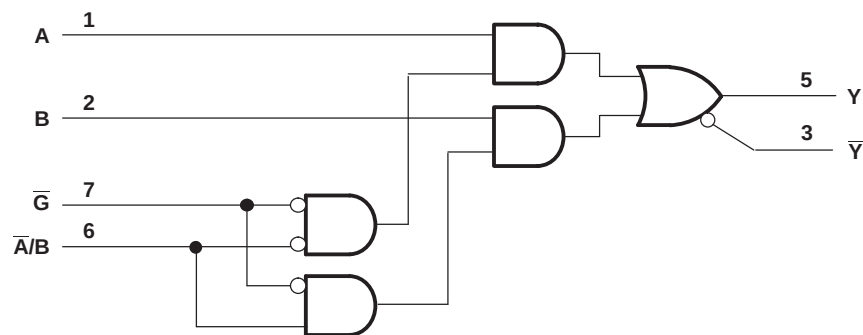
### 8.1 Overview

This single 2-line to 1-line data selector multiplexer is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC2G157 device features a common strobe ( $\overline{G}$ ) input. When the strobe is high, Y is low and  $\overline{Y}$  is high. When the strobe is low, a single bit is selected from one of two sources and is routed to the outputs. The device provides true and complementary data.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The SN74LVC2G157 device has a wide operating  $V_{CC}$  range of 1.65 V to 5.5 V, which allows it to be used in a broad range of systems. The 5.5 V I/Os allow down translation and also allow voltages at the inputs when  $V_{CC} = 0$ .

### 8.4 Device Functional Modes

Table 1 lists the functional modes for SN74LVC2G157.

**Table 1. Function Table**

| INPUTS         |                  |   |   | OUTPUTS |                |
|----------------|------------------|---|---|---------|----------------|
| $\overline{G}$ | $\overline{A/B}$ | A | B | Y       | $\overline{Y}$ |
| H              | X                | X | X | L       | H              |
| L              | L                | L | X | L       | H              |
| L              | L                | H | X | H       | L              |
| L              | H                | X | L | L       | H              |
| L              | H                | X | H | H       | L              |

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The LVC family is TI's premier solution to the industry's high-drive needs in logic devices. The LVC family ensures a symmetric drive of 24 mA across the range  $3.3\text{ V} < V_{CC} < 5.5\text{ V}$ . The SN74LVC2G157 device also maintains excellent response time. The increased drive produces faster edges and improved response performance.

### 9.2 Typical Application

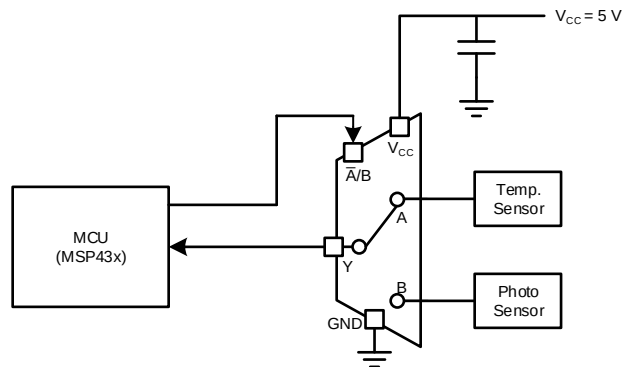


**Figure 3. Multiplexer Controlled by Processor**

#### 9.2.1 Design Requirements

The SN74LVC2G157 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

The SN74LVC2G157 allows switching control of analog and digital signals with a digital control signal. All input signals should remain as close to either 0 V or  $V_{CC}$  for optimal operation.

#### 9.2.2 Detailed Design Procedure

1. Recommended input conditions:
  - For rise time and fall time specifications, see  $\Delta t/\Delta v$  in the table.
  - For specified high and low levels, see  $V_{IH}$  and  $V_{IL}$  in the table.
  - Inputs and outputs are overvoltage tolerant and can therefore go as high as 5.5 V at any valid  $V_{CC}$ .
2. Recommended output conditions:
  - Load currents should not exceed  $\pm 50\text{ mA}$ .
3. Frequency selection criterion:
  - The effects of frequency upon the output current should be studied in Figure 5.
  - Added trace resistance and capacitance can reduce maximum frequency capability; follow the layout practices listed in the [Layout](#) section.

## Typical Application (continued)

### 9.2.3 Application Curve

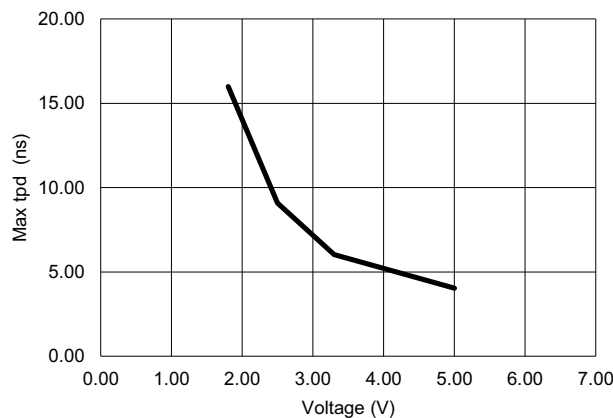


**Figure 4. Max tpd vs Voltage of LVC Family**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the table.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu$ F bypass capacitor is recommended. If multiple pins are labeled  $V_{CC}$ , then a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor is recommended for each  $V_{CC}$  because the  $V_{CC}$  pins are tied together internally. For devices with dual supply pins operating at different voltages, for example  $V_{CC}$  and  $V_{DD}$ , a 0.1- $\mu$ F bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 5](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

## 11.2 Layout Example

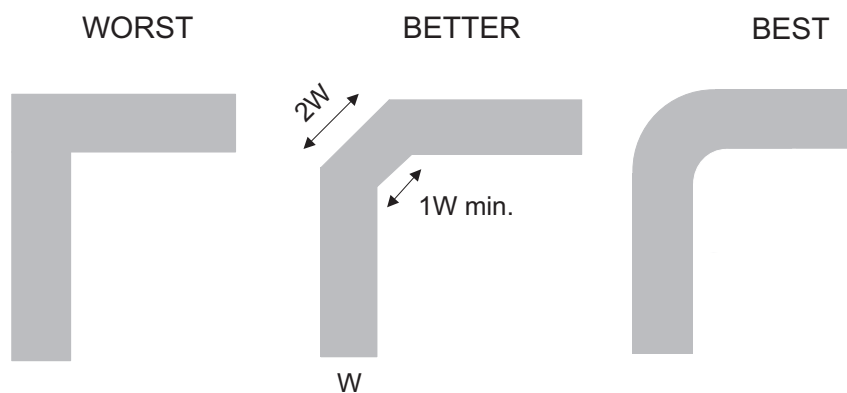


Figure 5. Trace Example

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)
- *Selecting the Right Texas Instruments Signal Switch*, [SZZA030](#)

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

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### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

## PACKAGING INFORMATION

| Orderable Device   | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|--------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| 74LVC2G157DCTRE4   | ACTIVE        | SM8          | DCT                | 8    | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C57<br>(R, Z)           | <a href="#">Samples</a> |
| 74LVC2G157DCURG4   | ACTIVE        | VSSOP        | DCU                | 8    | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C57R                    | <a href="#">Samples</a> |
| 74LVC2G157DCUTG4   | ACTIVE        | VSSOP        | DCU                | 8    | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C57R                    | <a href="#">Samples</a> |
| SN74LVC2G157DCT3   | ACTIVE        | SM8          | DCT                | 8    | 3000           | Pb-Free<br>(RoHS)          | CU SNBI                 | Level-1-260C-UNLIM   | -40 to 85    | C57<br>Z                | <a href="#">Samples</a> |
| SN74LVC2G157DCTR   | ACTIVE        | SM8          | DCT                | 8    | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C57<br>(R, Z)           | <a href="#">Samples</a> |
| SN74LVC2G157DCTRG4 | ACTIVE        | SM8          | DCT                | 8    | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | C57<br>(R, Z)           | <a href="#">Samples</a> |
| SN74LVC2G157DCU3   | ACTIVE        | VSSOP        | DCU                | 8    | 3000           | Pb-Free<br>(RoHS)          | CU SNBI                 | Level-1-260C-UNLIM   | -40 to 85    | 57<br>CZ                | <a href="#">Samples</a> |
| SN74LVC2G157DCUR   | ACTIVE        | VSSOP        | DCU                | 8    | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU   CU SN       | Level-1-260C-UNLIM   | -40 to 85    | (C57Q, C57R)            | <a href="#">Samples</a> |
| SN74LVC2G157DCUT   | ACTIVE        | VSSOP        | DCU                | 8    | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU   CU SN       | Level-1-260C-UNLIM   | -40 to 85    | (C57Q, C57R)            | <a href="#">Samples</a> |
| SN74LVC2G157YZPR   | ACTIVE        | DSBGA        | YZP                | 8    | 3000           | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 85    | (C37, C3N)              | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

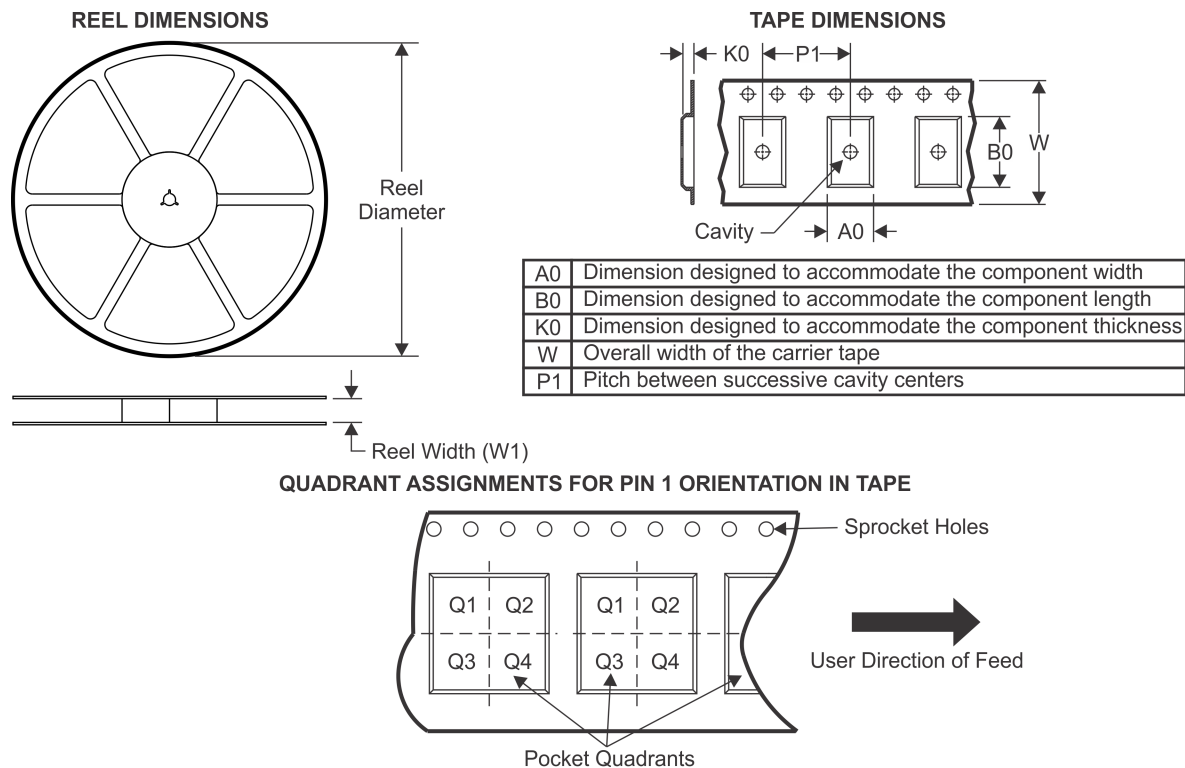
<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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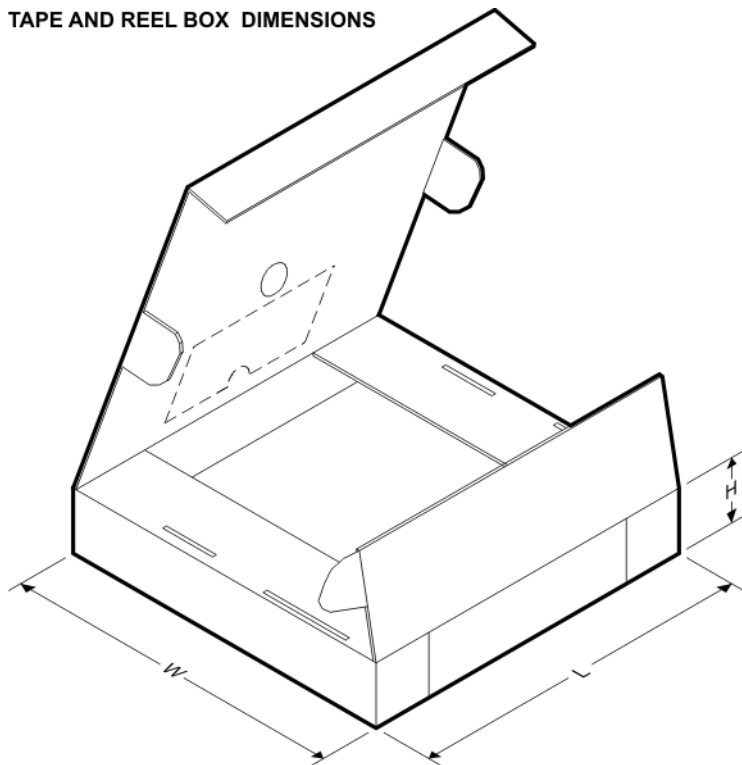
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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74LVC2G157DCURG4 | VSSOP        | DCU             | 8    | 3000 | 180.0              | 8.4                | 2.25    | 3.35    | 1.05    | 4.0     | 8.0    | Q3            |
| 74LVC2G157DCUTG4 | VSSOP        | DCU             | 8    | 250  | 180.0              | 8.4                | 2.25    | 3.35    | 1.05    | 4.0     | 8.0    | Q3            |
| SN74LVC2G157DCT3 | SM8          | DCT             | 8    | 3000 | 180.0              | 13.0               | 3.35    | 4.5     | 1.55    | 4.0     | 12.0   | Q3            |
| SN74LVC2G157DCTR | SM8          | DCT             | 8    | 3000 | 180.0              | 13.0               | 3.35    | 4.5     | 1.55    | 4.0     | 12.0   | Q3            |
| SN74LVC2G157DCUR | VSSOP        | DCU             | 8    | 3000 | 180.0              | 8.4                | 2.25    | 3.35    | 1.05    | 4.0     | 8.0    | Q3            |
| SN74LVC2G157DCUR | VSSOP        | DCU             | 8    | 3000 | 178.0              | 9.5                | 2.25    | 3.35    | 1.05    | 4.0     | 8.0    | Q3            |
| SN74LVC2G157DCUT | VSSOP        | DCU             | 8    | 250  | 178.0              | 9.5                | 2.25    | 3.35    | 1.05    | 4.0     | 8.0    | Q3            |
| SN74LVC2G157YZPR | DSBGA        | YZP             | 8    | 3000 | 178.0              | 9.2                | 1.02    | 2.02    | 0.63    | 4.0     | 8.0    | Q1            |

## TAPE AND REEL BOX DIMENSIONS

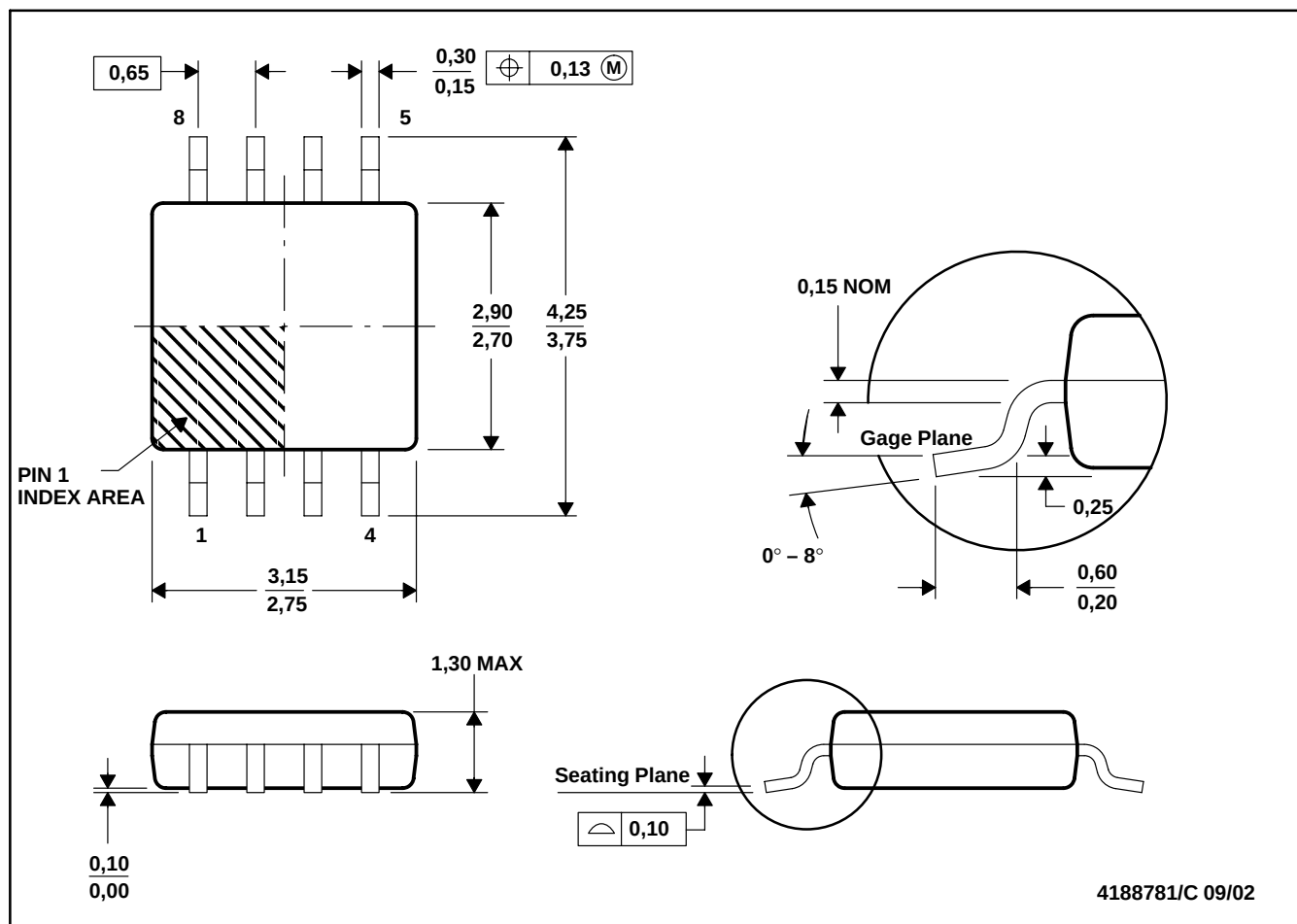


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74LVC2G157DCURG4 | VSSOP        | DCU             | 8    | 3000 | 202.0       | 201.0      | 28.0        |
| 74LVC2G157DCUTG4 | VSSOP        | DCU             | 8    | 250  | 202.0       | 201.0      | 28.0        |
| SN74LVC2G157DCT3 | SM8          | DCT             | 8    | 3000 | 182.0       | 182.0      | 20.0        |
| SN74LVC2G157DCTR | SM8          | DCT             | 8    | 3000 | 182.0       | 182.0      | 20.0        |
| SN74LVC2G157DCUR | VSSOP        | DCU             | 8    | 3000 | 202.0       | 201.0      | 28.0        |
| SN74LVC2G157DCUR | VSSOP        | DCU             | 8    | 3000 | 202.0       | 201.0      | 28.0        |
| SN74LVC2G157DCUT | VSSOP        | DCU             | 8    | 250  | 202.0       | 201.0      | 28.0        |
| SN74LVC2G157YZPR | DSBGA        | YZP             | 8    | 3000 | 220.0       | 220.0      | 35.0        |

## DCT (R-PDSO-G8)

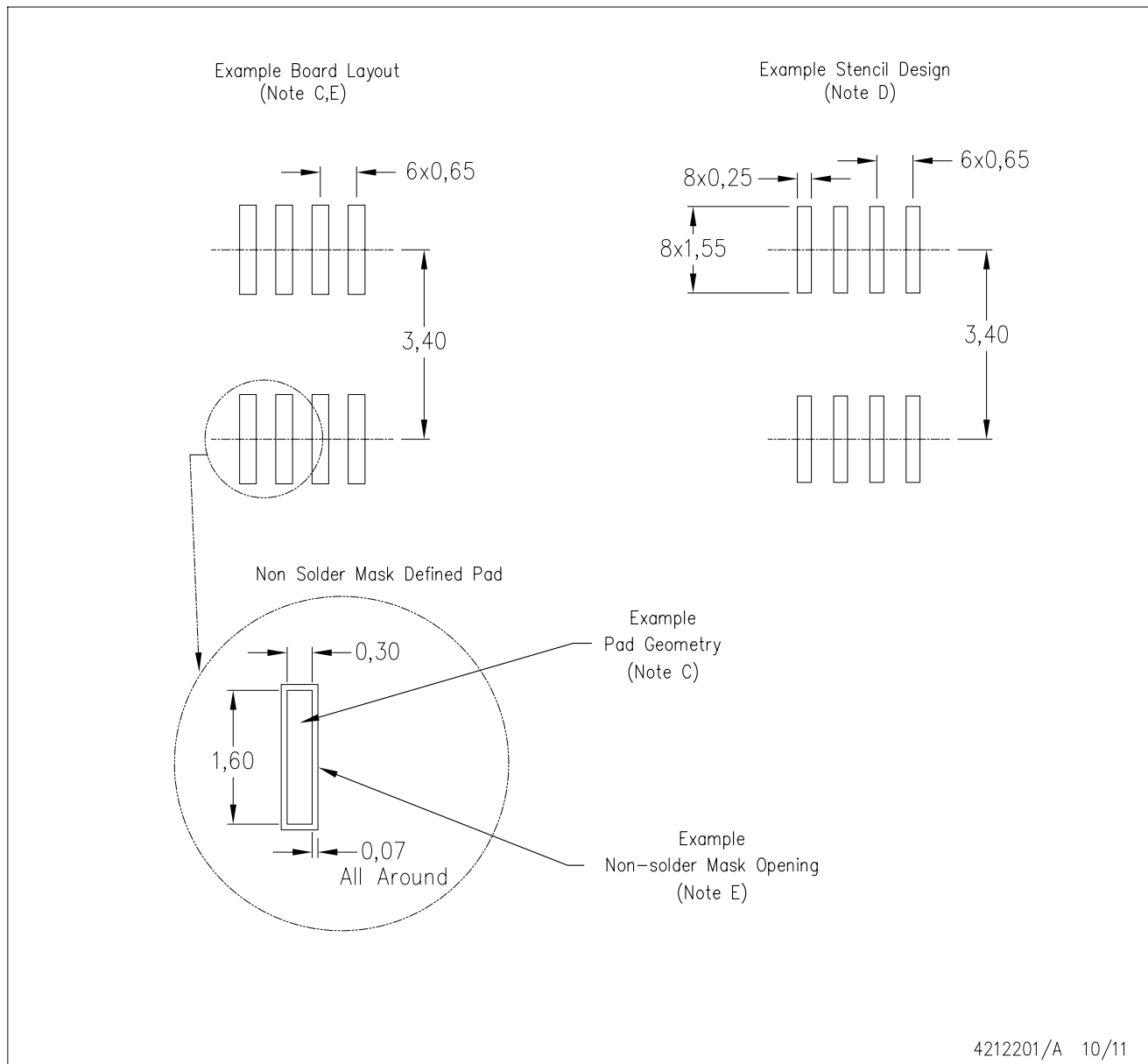
## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - Falls within JEDEC MO-187 variation DA.

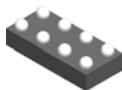
DCT (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

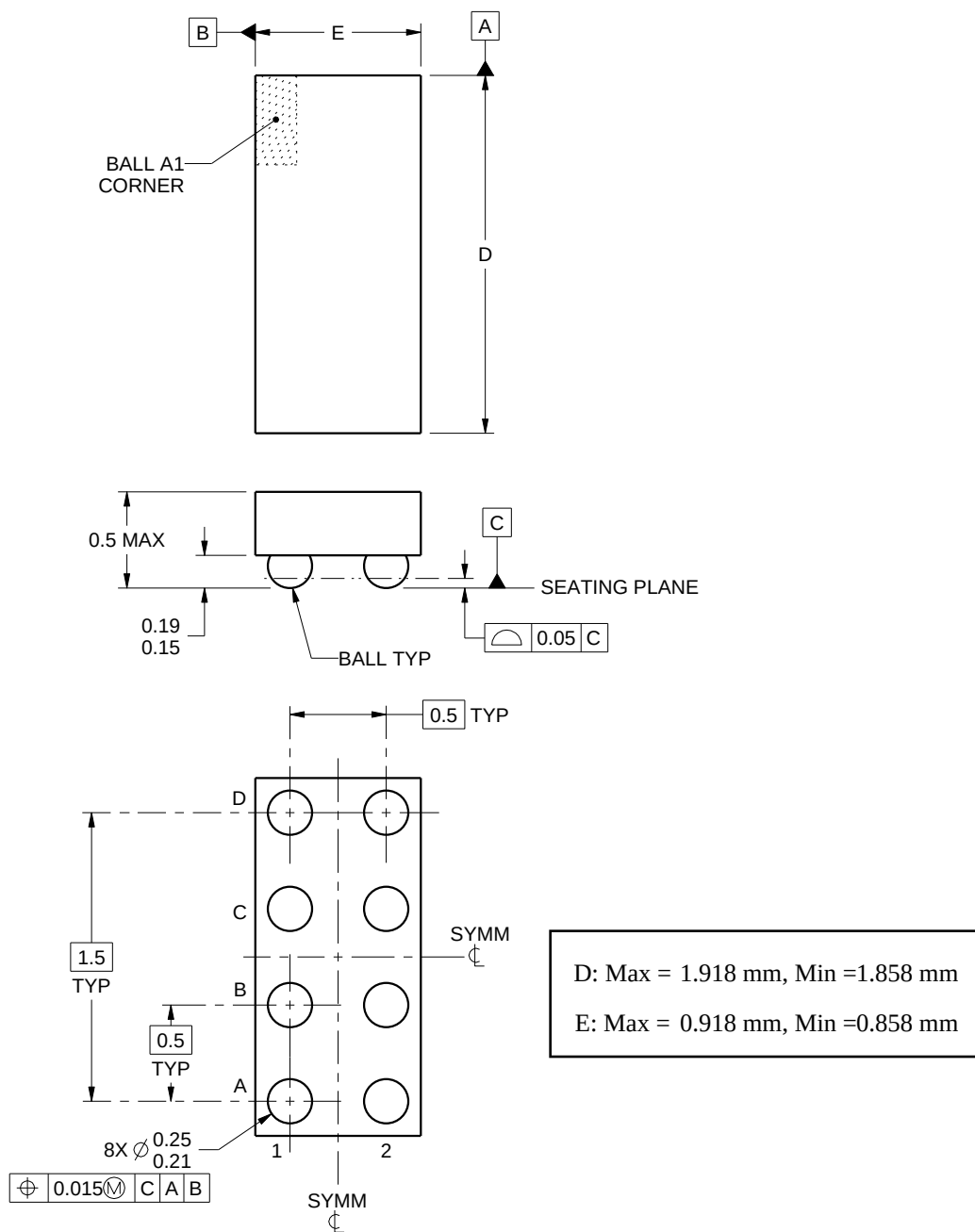
YZP0008



# PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223082/A 07/2016

## NOTES:

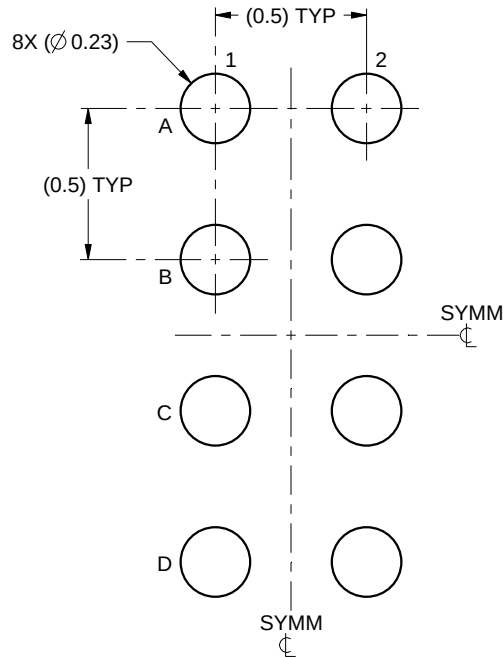
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

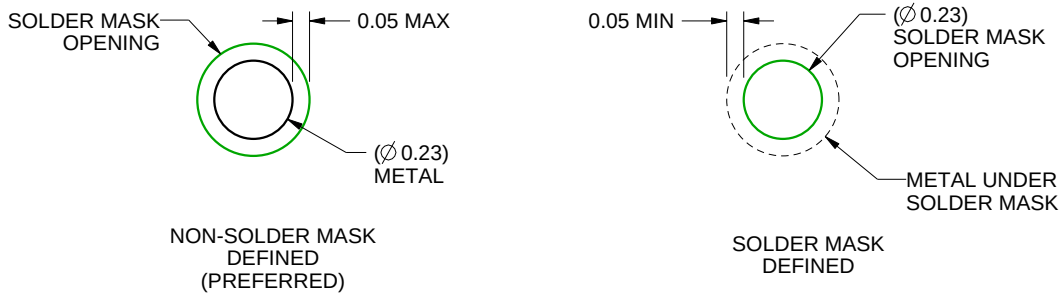
YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X

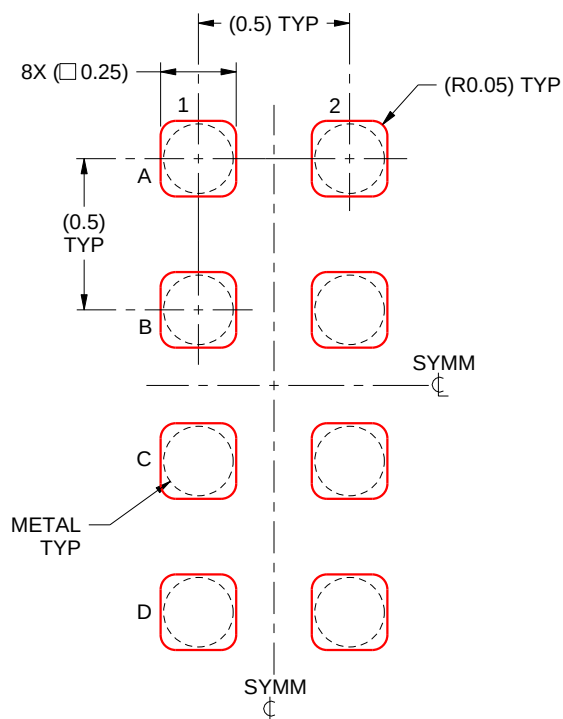


SOLDER MASK DETAILS  
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).



SOLDER PASTE EXAMPLE  
 BASED ON 0.1 mm THICK STENCIL  
 SCALE:40X

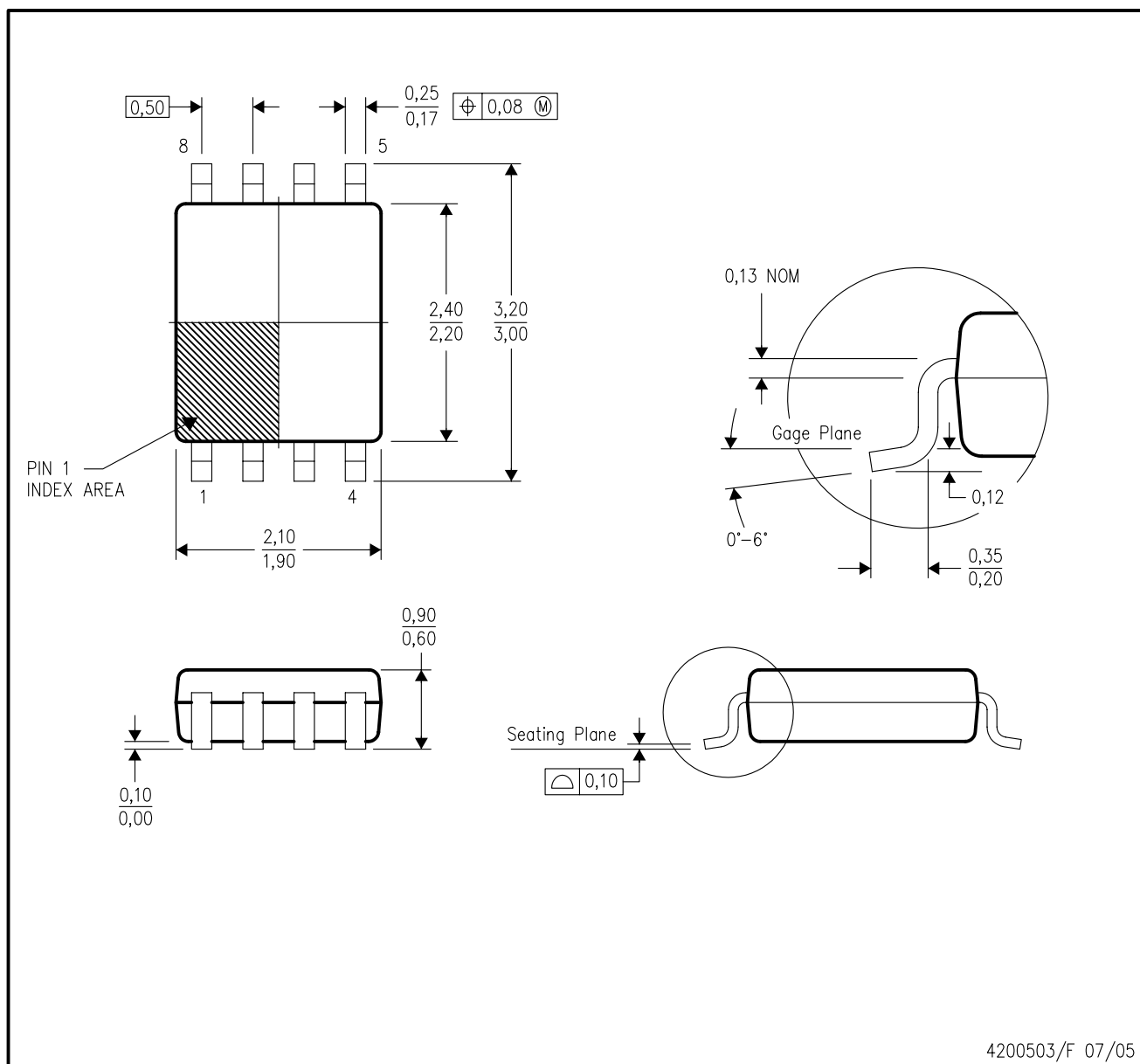
4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)

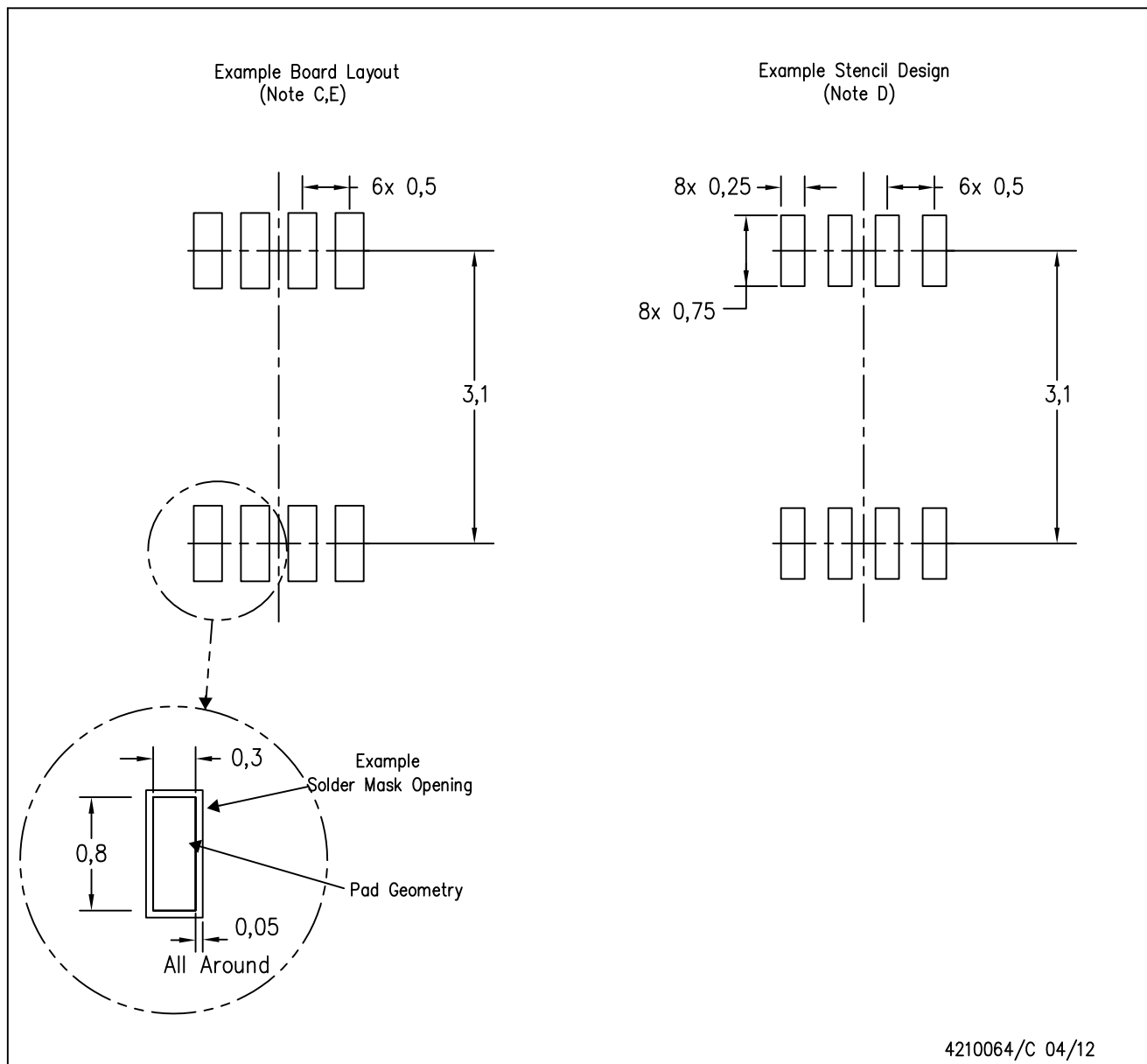


## NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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