# MIXED SIGNAL MICROCONTROLLER

## FEATURES

- Embedded Microcontroller
  - 16-Bit RISC Architecture up to 24-MHz Clock
  - Wide Supply Voltage Range (2 V to 3.6 V)
  - -40°C to 85°C Operation
- Optimized Ultra-Low Power Modes

| Mode | Consumption (Typical) |
|---|---|
| Active Mode | 81.4 µA/MHz |
| Standby (LPM3 With VLO) | 6.3 µA |
| Real-Time Clock (LPM3.5 With Crystal) | 1.5 µA |
| Shutdown (LPM4.5) | 0.32 µA |

- Ultra-Low Power Ferroelectric RAM
  - Up to 16KB Nonvolatile Memory
  - Ultra-Low Power Writes
  - Fast Write at 125 ns per Word (16KB in 1 ms)
  - Built in Error Coding and Correction (ECC) and Memory Protection Unit (MPU)
  - Universal Memory = Program + Data + Storage
  - $10^{15}$ Write Cycle Endurance
  - Radiation Resistant and Nonmagnetic
- Intelligent Digital Peripherals
  - 32-Bit Hardware Multiplier (MPY)
  - Three-Channel Internal DMA
  - Real-Time Clock With Calendar and Alarm Functions
  - Five 16-Bit Timers With up to Three Capture/Compare
  - 16-Bit Cyclic Redundancy Checker (CRC)
- High-Performance Analog
  - 16-Channel Analog Comparator With Voltage Reference and Programmable Hysteresis
  - 14-Channel 10-Bit Analog-to-Digital Converter (ADC) With Internal Reference and Sample-and-Hold
    - 200 ksps at 100-µA Consumption
- Enhanced Serial Communication
  - eUSCI_A0 and eUSCI_A1 Support:
    - UART With Automatic Baud-Rate Detection
    - IrDA Encode and Decode
    - SPI at Rates up to 10 Mbps
  - eUSCI_B0 Supports:
    - $I^2C$ With Multi-Slave Addressing
    - SPI at Rates up to 10 Mbps
  - Hardware UART or I2C Bootstrap Loader (BSL)
- Power Management System
  - Fully Integrated LDO
  - Supply Voltage Supervisor for Core and Supply Voltages With Reset Capability
  - Always-On Zero-Power Brownout Detection
  - Serial On-Board Programming With No External Voltage Needed
- Flexible Clock System
  - Fixed-Frequency DCO With Six Selectable Factory-Trimmed Frequencies (Device Dependent)
  - Low-Power Low-Frequency Internal Clock Source (VLO)
  - 32-kHz Crystals (LFXT)
  - High-Frequency Crystals (HFXT)
- Development Tools and Software
  - Free Professional Development Environments (IAR, CCS, GCC)
  - Low-Cost Full-Featured Kit (MSP-EXP430FR5739)
  - Full Development Kit (MSP-FET430U40A)
  - Target Board (MSP-TS430RHA40A)
- Family Members
  - 20 Different Variants and 5 Available Packages Summarized in Table 1 and Table 2
  - For Complete Module Descriptions, See the *MSP430FR57xx Family User's Guide* (SLAU272)

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**CAUTION** These products use FRAM nonvolatile memory technology. FRAM retention is sensitive to extreme temperatures, such as those experienced during reflow or hand soldering. See Absolute Maximum Ratings for more information.

**CAUTION** System-level ESD protection must be applied in compliance with the device-level ESD specification to prevent electrical overstress or disturb of data or code memory. See the application report *MSP430™ System-Level ESD Considerations* (SLAA530) for more information.

## DESCRIPTION

The Texas Instruments MSP430FR57xx family of ultralow-power microcontrollers consists of multiple devices featuring embedded FRAM nonvolatile memory, ultralow power 16-bit MSP430 CPU, and different peripherals targeted for various applications. The architecture, FRAM, and peripherals, combined with seven low-power modes, are optimized to achieve extended battery life in portable and wireless sensing applications. FRAM is a new nonvolatile memory that combines the speed, flexibility, and endurance of SRAM with the stability and reliability of flash, all at lower total power consumption. Peripherals include 10-bit A/D converter, 16-channel comparator with voltage reference generation and hysteresis capabilities, three enhanced serial channels capable of $I^2C$, SPI, or UART protocols, internal DMA, hardware multiplier, real-time clock, five 16-bit timers, and more. The family members that are available are summarized in Table 1.

**Table 1. Family Members**

| Device | FRAM (KB) | SRAM (KB) | System Clock (MHz) | ADC10_B | Comp_D | Timer_A(1) | Timer_B(2) | eUSCI | | I/O | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Channel A: UART, IrDA, SPI | Channel B: SPI, $I^2C$ | | |
| MSP430FR5739 | 16 | 1 | 24 | 12 ext, 2 int ch. | 16 ch. | 3, 3 | 3, 3, 3 | 2 | 1 | 32 | RHA |
| | | | | | | | | | | 30 | DA |
| MSP430FR5738 | 16 | 1 | 24 | 6 ext, 2 int ch. | 10 ch. | 3, 3 | 3 | 1 | 1 | 17 | RGE |
| | | | | 8 ext, 2 int ch. | 12 ch. | | | | | 21 | PW |
| | | | | 5 ext, 2 int ch. | 9 ch. | | | | | 16 | YFF(3) |
| MSP430FR5737 | 16 | 1 | 24 | | 16 ch. | 3, 3 | 3, 3, 3 | 2 | 1 | 32 | RHA |
| | | | | | | | | | | 30 | DA |
| MSP430FR5736 | 16 | 1 | 24 | | 10 ch. | 3, 3 | 3 | 1 | 1 | 17 | RGE |
| | | | | | 12 ch. | | | | | 21 | PW |
| | | | | | 9 ch. | | | | | 16 | YFF(3) |
| MSP430FR5735 | 8 | 1 | 24 | 12 ext, 2 int ch. | 16 ch. | 3, 3 | 3, 3, 3 | 2 | 1 | 32 | RHA |
| | | | | | | | | | | 30 | DA |
| MSP430FR5734 | 8 | 1 | 24 | 6 ext, 2 int ch. | 10 ch. | 3, 3 | 3 | 1 | 1 | 17 | RGE |
| | | | | 8 ext, 2 int ch. | 12 ch. | | | | | 21 | PW |
| MSP430FR5733 | 8 | 1 | 24 | | 16 ch. | 3, 3 | 3, 3, 3 | 2 | 1 | 32 | RHA |
| | | | | | | | | | | 30 | DA |
| MSP430FR5732 | 8 | 1 | 24 | | 10 ch. | 3, 3 | 3 | 1 | 1 | 17 | RGE |
| | | | | | 12 ch. | | | | | 21 | PW |
| MSP430FR5731 | 4 | 1 | 24 | 12 ext, 2 int ch. | 16 ch. | 3, 3 | 3, 3, 3 | 2 | 1 | 32 | RHA |
| | | | | | | | | | | 30 | DA |

(1) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.
(2) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.
(3) Product Preview


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**Table 1. Family Members (continued)**

| Device | FRAM (KB) | SRAM (KB) | System Clock (MHz) | ADC10_B | Comp_D | Timer_A[1] | Timer_B[2] | eUSCI | | I/O | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Channel A: UART, IrDA, SPI | Channel B: SPI, $I^2C$ | | |
| MSP430FR5730 | 4 | 1 | 24 | 6 ext, 2 int ch. | 10 ch. | 3, 3 | 3 | 1 | 1 | 17 | RGE |
| | | | | 8 ext, 2 int ch. | 12 ch. | | | | | 21 | PW |
| | | | | 5 ext, 2 int ch. | 9 ch. | | | | | 16 | YFF[3] |
| MSP430FR5729 | 16 | 1 | 8 | 12 ext, 2 int ch. | 16 ch. | 3, 3 | 3, 3, 3 | 2 | 1 | 32 | RHA |
| | | | | | | | | | | 30 | DA |
| MSP430FR5728 | 16 | 1 | 8 | 6 ext, 2 int ch. | 10 ch. | 3, 3 | 3 | 1 | 1 | 17 | RGE |
| | | | | 8 ext, 2 int ch. | 12 ch. | | | | | 21 | PW |
| MSP430FR5727 | 16 | 1 | 8 | | 16 ch. | 3, 3 | 3, 3, 3 | 2 | 1 | 32 | RHA |
| | | | | | | | | | | 30 | DA |
| MSP430FR5726 | 16 | 1 | 8 | | 10 ch. | 3, 3 | 3 | 1 | 1 | 17 | RGE |
| | | | | | 12 ch. | | | | | 21 | PW |
| MSP430FR5725 | 8 | 1 | 8 | 12 ext, 2 int ch. | 16 ch. | 3, 3 | 3, 3, 3 | 2 | 1 | 32 | RHA |
| | | | | | | | | | | 30 | DA |
| MSP430FR5724 | 8 | 1 | 8 | 6 ext, 2 int ch. | 10 ch. | 3, 3 | 3 | 1 | 1 | 17 | RGE |
| | | | | 8 ext, 2 int ch. | 12 ch. | | | | | 21 | PW |
| MSP430FR5723 | 8 | 1 | 8 | | 16 ch. | 3, 3 | 3, 3, 3 | 2 | 1 | 32 | RHA |
| | | | | | | | | | | 30 | DA |
| MSP430FR5722 | 8 | 1 | 8 | | 10 ch. | 3, 3 | 3 | 1 | 1 | 17 | RGE |
| | | | | | 12 ch. | | | | | 21 | PW |
| MSP430FR5721 | 4 | 1 | 8 | 12 ext, 2 int ch. | 16 ch. | 3, 3 | 3, 3, 3 | 2 | 1 | 32 | RHA |
| | | | | | | | | | | 30 | DA |
| MSP430FR5720 | 4 | 1 | 8 | 6 ext, 2 int ch. | 10 ch. | 3, 3 | 3 | 1 | 1 | 17 | RGE |
| | | | | 8 ext, 2 int ch. | 12 ch. | | | | | 21 | PW |

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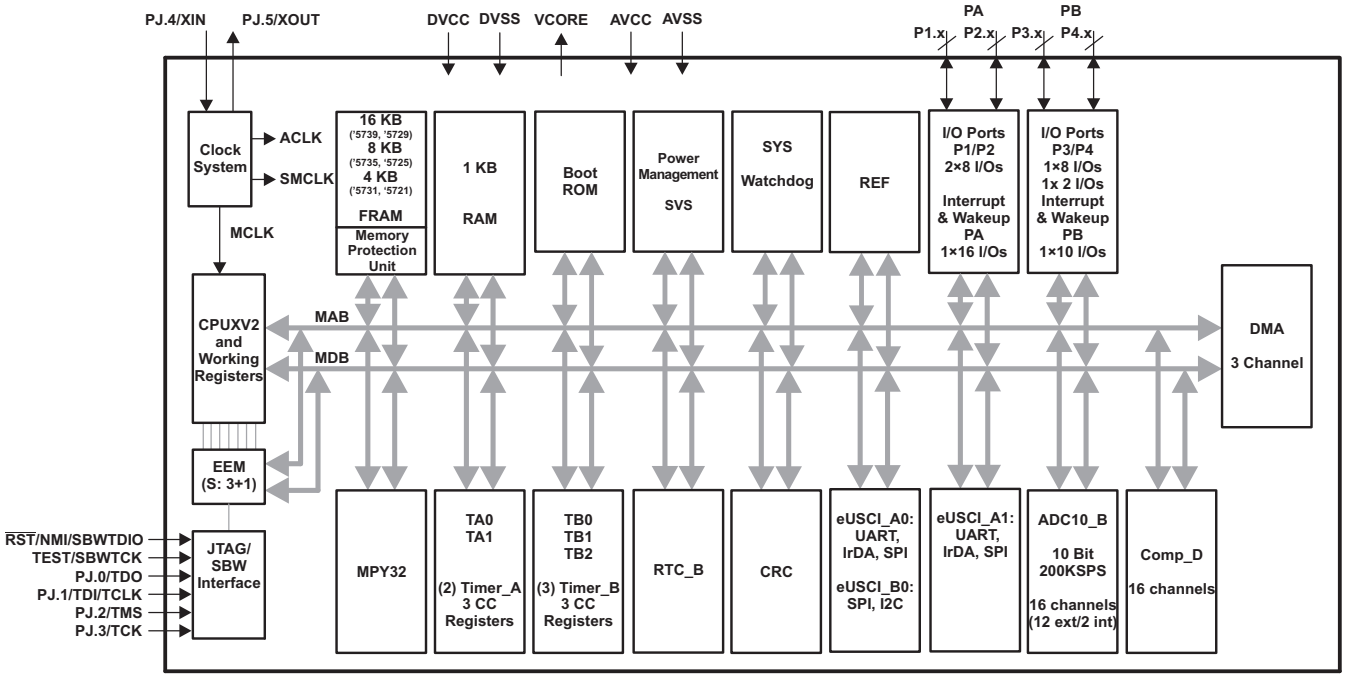
## Table 2. Ordering Information(1)

| $T_A$ | PACKAGED DEVICES(2) | | | | |
|---|---|---|---|---|---|
| | PLASTIC 40-PIN VQFN (RHA) | PLASTIC 24-PIN VQFN (RGE) | PLASTIC 38-PIN TSSOP (DA) | PLASTIC 28-PIN TSSOP (PW) | PLASTIC 25-BALL DSBGA (YFF)(3) |
| –40°C to 85°C | MSP430FR5721IRHA | MSP430FR5720IRGE | MSP430FR5721IDA | MSP430FR5720IPW | MSP430FR5730IYFF(3) |
| | MSP430FR5723IRHA | MSP430FR5722IRGE | MSP430FR5723IDA | MSP430FR5722IPW | MSP430FR5736IYFF(3) |
| | MSP430FR5725IRHA | MSP430FR5724IRGE | MSP430FR5725IDA | MSP430FR5724IPW | MSP430FR5738IYFF(3) |
| | MSP430FR5727IRHA | MSP430FR5726IRGE | MSP430FR5727IDA | MSP430FR5726IPW | |
| | MSP430FR5729IRHA | MSP430FR5728IRGE | MSP430FR5729IDA | MSP430FR5728IPW | |
| | MSP430FR5731IRHA | MSP430FR5730IRGE | MSP430FR5731IDA | MSP430FR5730IPW | |
| | MSP430FR5733IRHA | MSP430FR5732IRGE | MSP430FR5733IDA | MSP430FR5732IPW | |
| | MSP430FR5735IRHA | MSP430FR5734IRGE | MSP430FR5735IDA | MSP430FR5734IPW | |
| | MSP430FR5737IRHA | MSP430FR5736IRGE | MSP430FR5737IDA | MSP430FR5736IPW | |
| | MSP430FR5739IRHA | MSP430FR5738IRGE | MSP430FR5739IDA | MSP430FR5738IPW | |

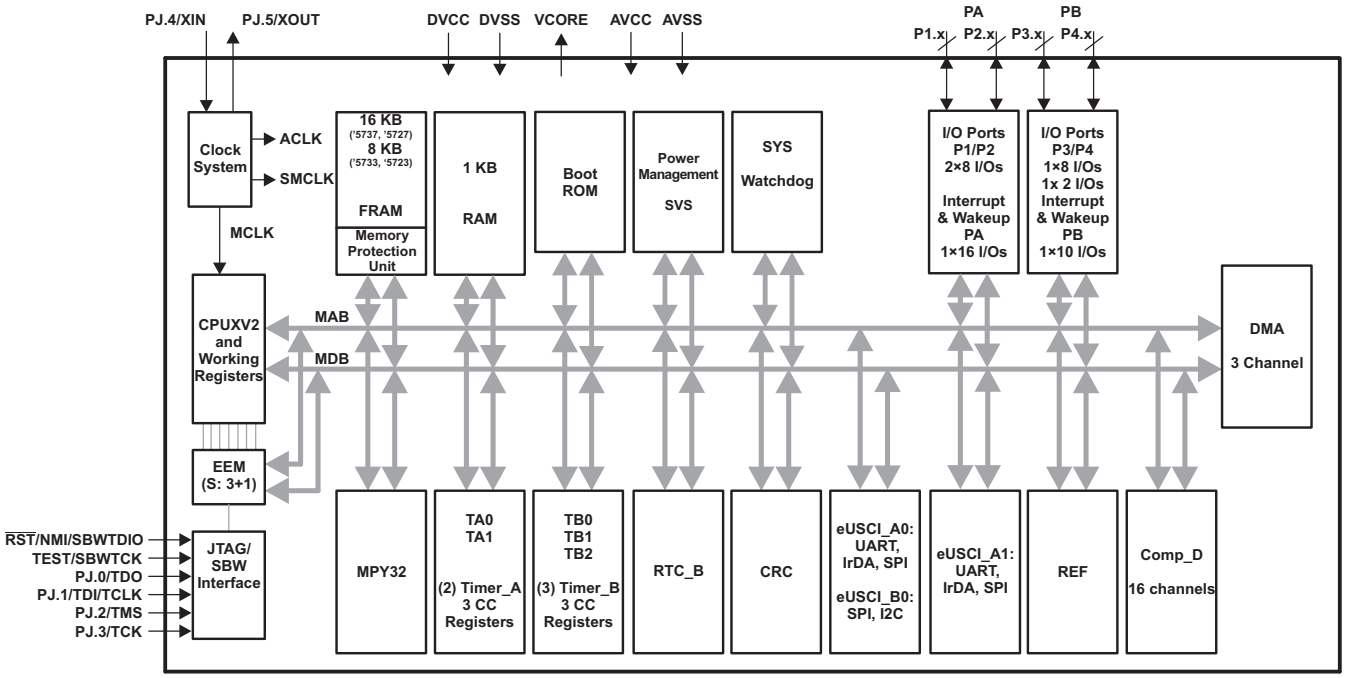
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.
(3) Product Preview


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## Functional Block Diagram – MSP430FR5721IRHA, MSP430FR5725IRHA, MSP430FR5729IRHA, MSP430FR5731IRHA, MSP430FR5735IRHA, MSP430FR5739IRHA



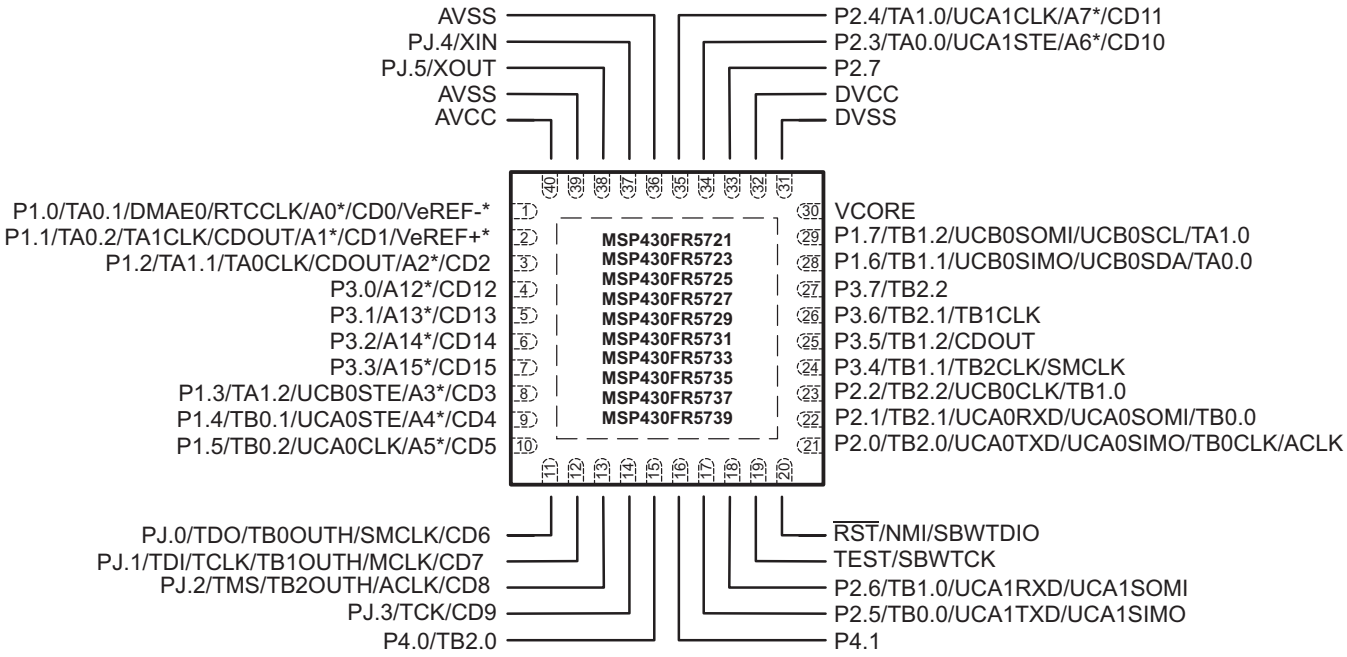

## Functional Block Diagram – MSP430FR5723IRHA, MSP430FR5727IRHA, MSP430FR5733IRHA, MSP430FR5737IRHA




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## Pin Designation – MSP430FR5721IRHA, MSP430FR5723IRHA, MSP430FR5725IRHA, MSP430FR5727IRHA, MSP430FR5729IRHA, MSP430FR5731IRHA, MSP430FR5733IRHA, MSP430FR5735IRHA, MSP430FR5737IRHA, MSP430FR5739IRHA

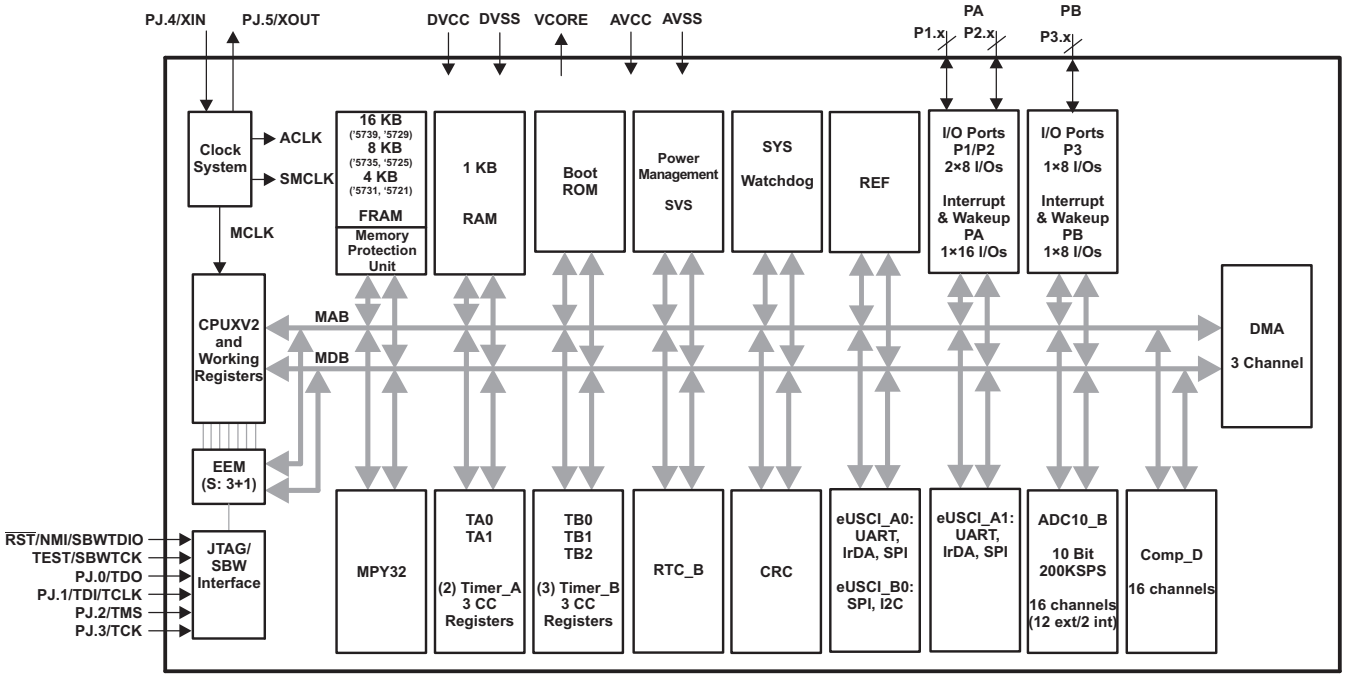
**RHA PACKAGE**
**(TOP VIEW)**



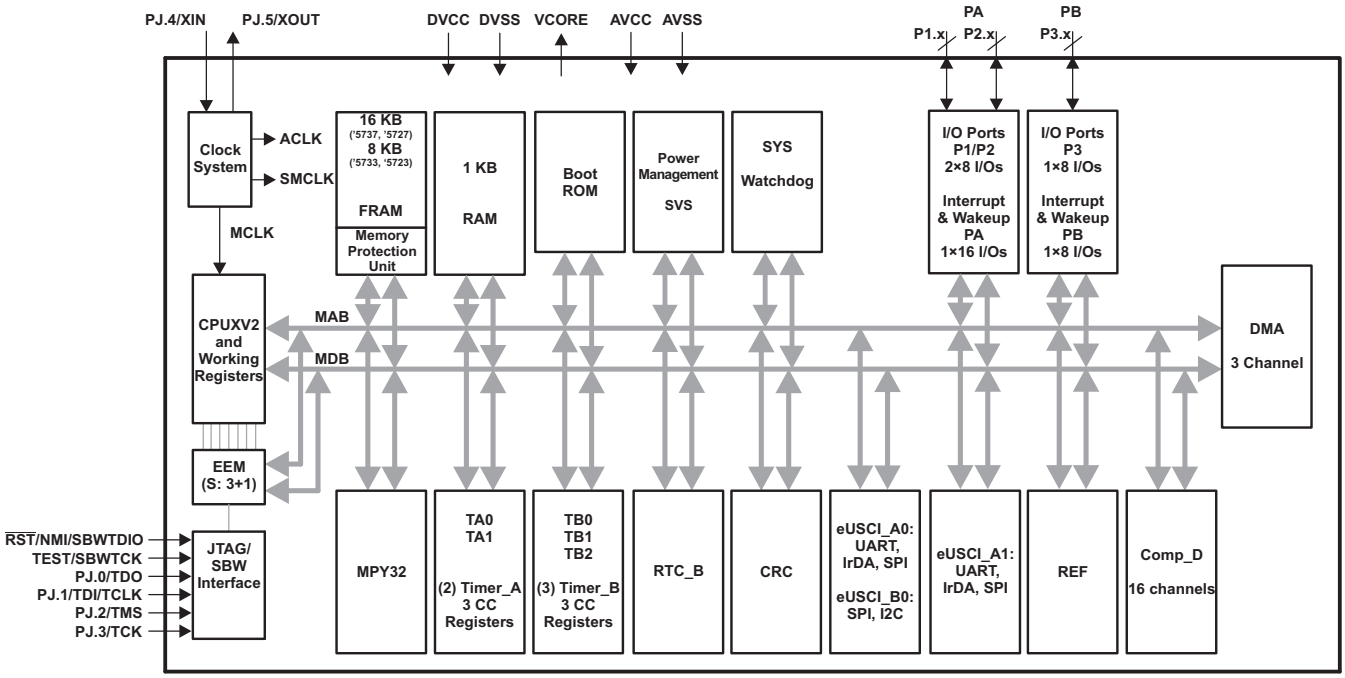

* Not available on MSP430FR5737, MSP430FR5733, MSP430FR5727, MSP430FR5723
Note: Power Pad connection to $V_{SS}$ recommended.


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## Functional Block Diagram – MSP430FR5721IDA, MSP430FR5725IDA, MSP430FR5729IDA, MSP430FR5731IDA, MSP430FR5735IDA, MSP430FR5739IDA



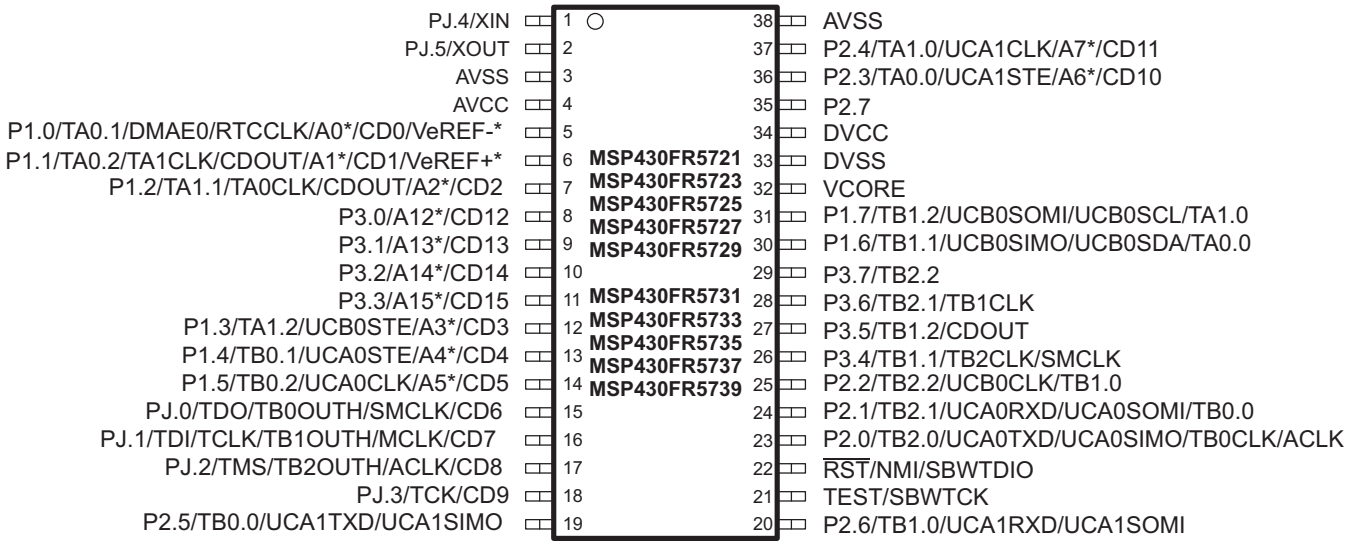

## Functional Block Diagram – MSP430FR5723IDA, MSP430FR5727IDA, MSP430FR5733IDA, MSP430FR5737IDA




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## Pin Designation – MSP430FR5721IDA, MSP430FR5723IDA, MSP430FR5725IDA, MSP430FR5727IDA, MSP430FR5729IDA, MSP430FR5731IDA, MSP430FR5733IDA, MSP430FR5735IDA, MSP430FR5737IDA, MSP430FR5739IDA

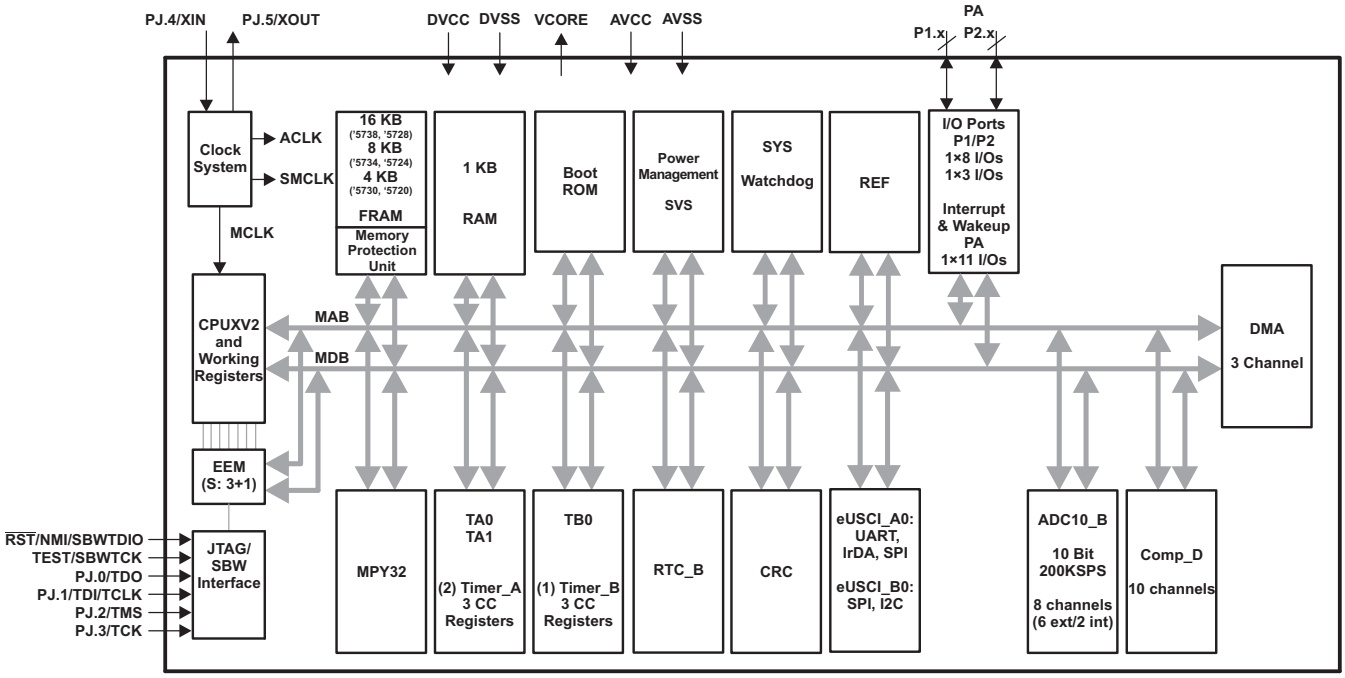
**DA PACKAGE**
**(TOP VIEW)**



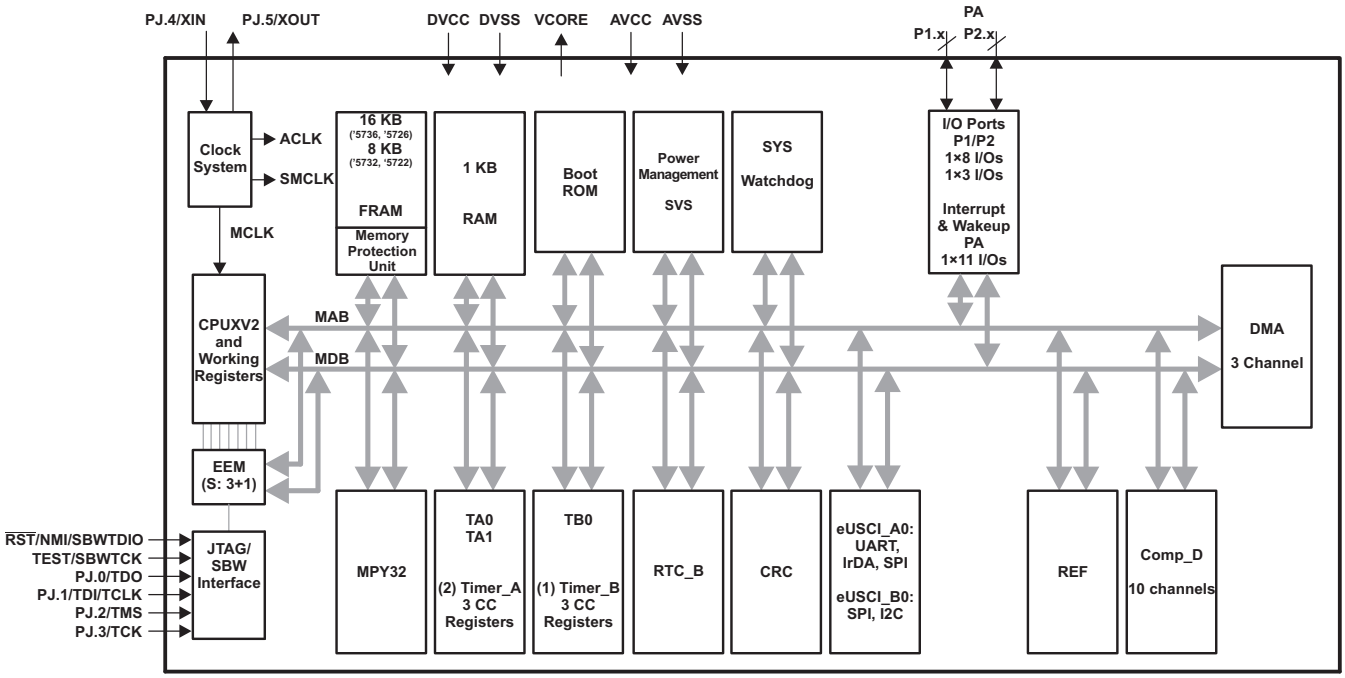

* Not available on MSP430FR5737, MSP430FR5733, MSP430FR5727, MSP430FR5723


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## Functional Block Diagram – MSP430FR5720IRGE, MSP430FR5724IRGE, MSP430FR5728IRGE, MSP430FR5730IRGE, MSP430FR5734IRGE, MSP430FR5738IRGE

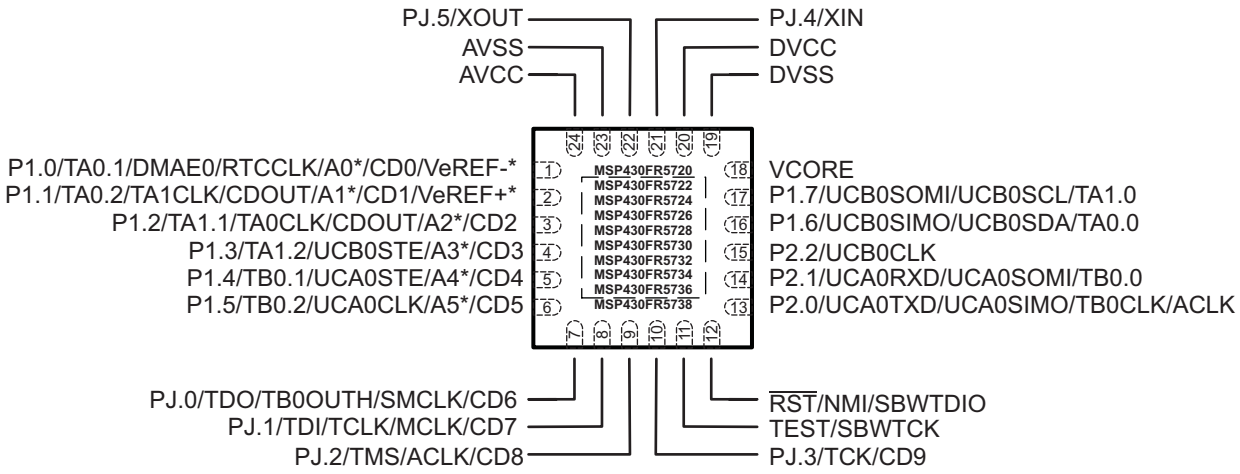



## Functional Block Diagram – MSP430FR5722IRGE, MSP430FR5726IRGE, MSP430FR5732IRGE, MSP430FR5736IRGE



## Pin Designation – MSP430FR5720IRGE, MSP430FR5722IRGE, MSP430FR5724IRGE, MSP430FR5726IRGE, MSP430FR5728IRGE, MSP430FR5730IRGE, MSP430FR5732IRGE, MSP430FR5734IRGE, MSP430FR5736IRGE, MSP430FR5738IRGE

**RGE PACKAGE**
**(TOP VIEW)**

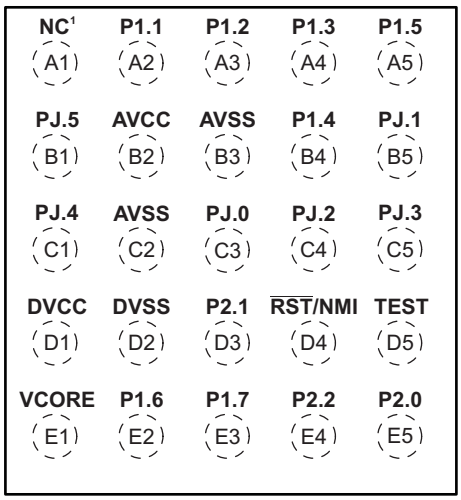



* Not available on MSP430FR5736, MSP430FR5732, MSP430FR5726, MSP430FR5722
Note: Power Pad connection to $V_{SS}$ recommended.


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## Pin Designation – MSP430FR5730IYFF, MSP430FR5736IYFF, MSP430FR5738IYFF

YFF PACKAGE
(TOP VIEW)




[1] NC (no connect). This ball must be attached but remain floating (no electrical connection). P1.0 must be initialized properly to avoid the floating input of the device.

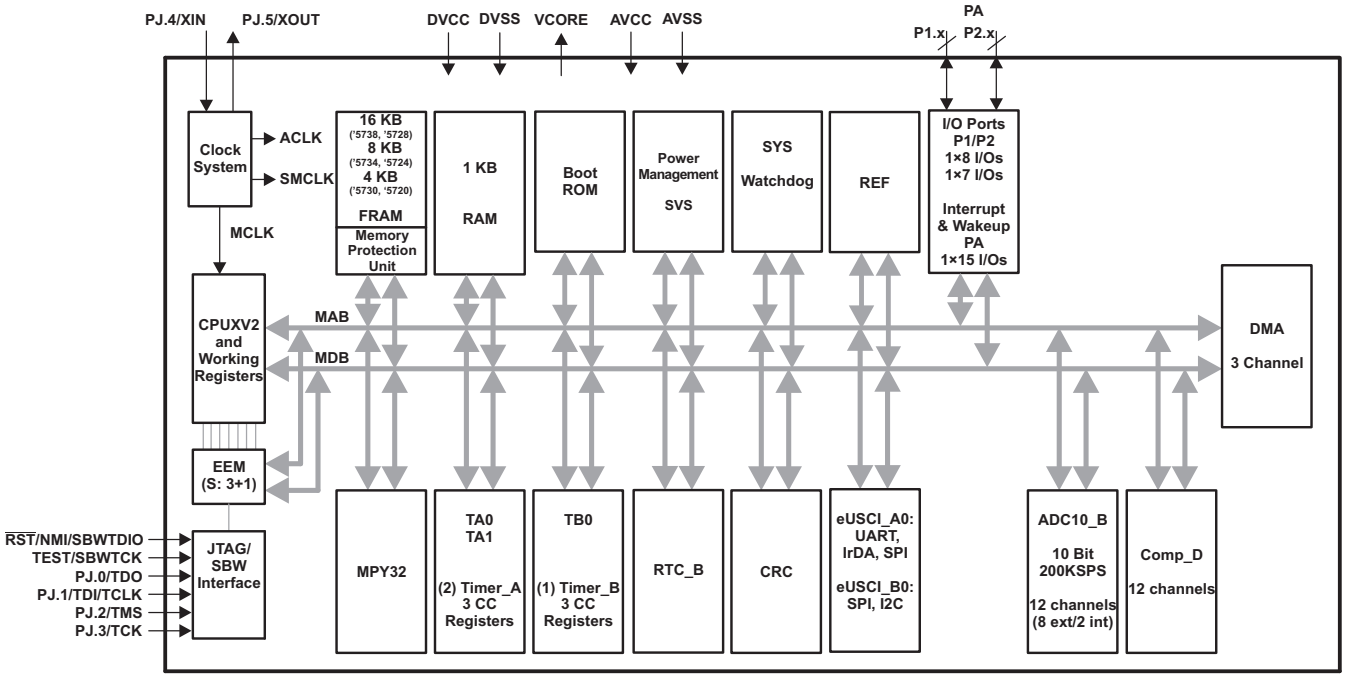
**Package Dimensions:** The package dimensions for the YFF package are shown in Table 3. See the package drawing at the end of this data sheet for more details.

**Table 3. YFF Package Dimensions**

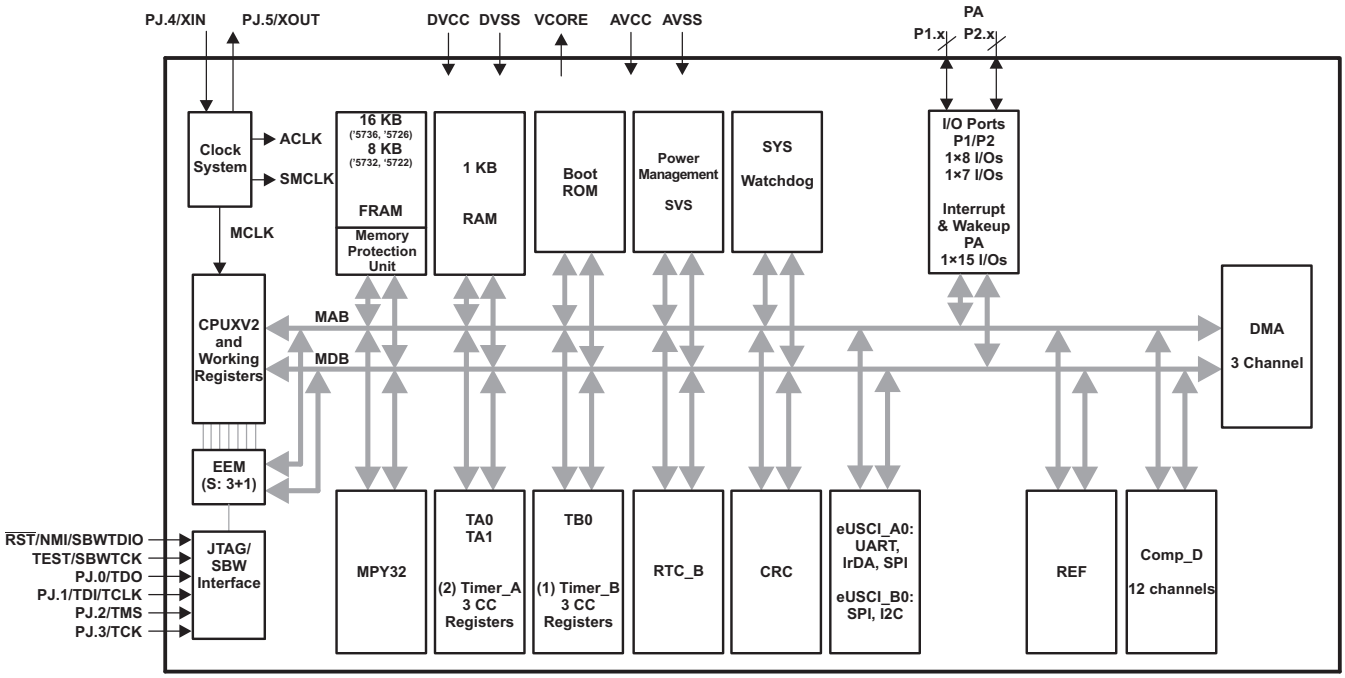
| PACKAGED DEVICES | D | E |
|---|---|---|
| MSP430FR5738IYFF | 2.04 ± 0.03 | 2.24 ± 0.03 |
| MSP430FR5736IYFF | | |
| MSP430FR5730IYFF | | |

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## Functional Block Diagram – MSP430FR5720IPW, MSP430FR5724IPW, MSP430FR5728IPW, MSP430FR5730IPW, MSP430FR5734IPW, MSP430FR5738IPW




## Functional Block Diagram – MSP430FR5722IPW, MSP430FR5726IPW, MSP430FR5732IPW, MSP430FR5736IPW

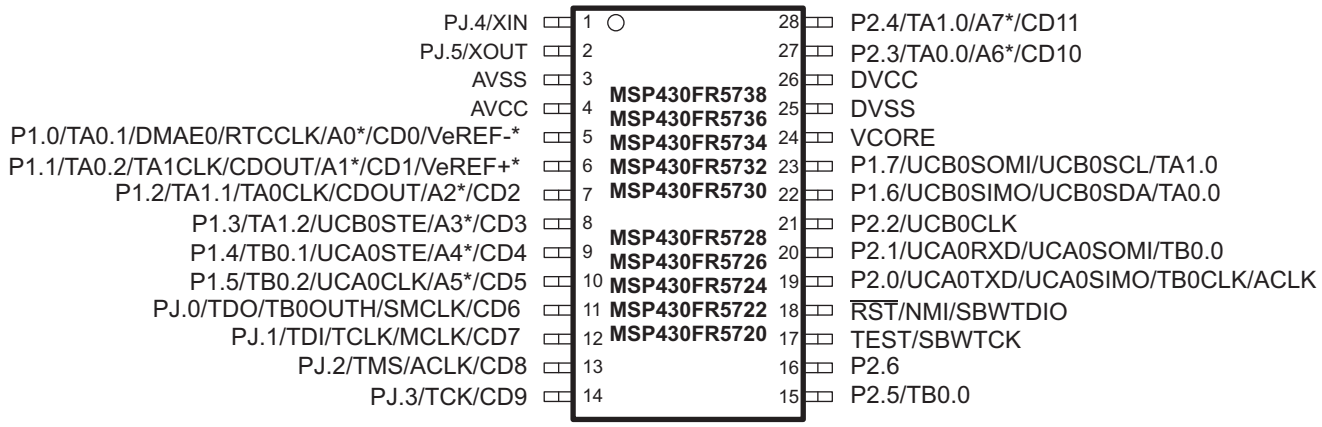




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## Pin Designation – MSP430FR5720IPW, MSP430FR5722IPW, MSP430FR5724IPW, MSP430FR5726IPW, MSP430FR5728IPW, MSP430FR5730IPW, MSP430FR5732IPW, MSP430FR5734IPW, MSP430FR5736IPW, MSP430FR5738IPW

**PW PACKAGE**
**(TOP VIEW)**




* Not available on MSP430FR5736, MSP430FR5732, MSP430FR5726, MSP430FR5722

## Table 4. Terminal Functions

| TERMINAL | | | | | | I/O (1) | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| NAME | NO. | | | | | | |
| | RHA | RGE | DA | PW | YFF | | |
| P1.0/TA0.1/DMAE0/ RTCCLK/A0/CD0/VeREF- | 1 | 1 | 5 | 5 | (2) | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TA0 CCR1 capture: CCI1A input, compare: Out1<br>External DMA trigger<br>RTC clock calibration output<br>Analog input A0 – ADC (not available on devices without ADC)<br>Comparator_D input CD0<br>External applied reference voltage (not available on devices without ADC) |
| P1.1/TA0.2/TA1CLK/ CDOUT/A1/CD1/VeREF+ | 2 | 2 | 6 | 6 | A2 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TA0 CCR2 capture: CCI2A input, compare: Out2<br>TA1 input clock<br>Comparator_D output<br>Analog input A1 – ADC (not available on devices without ADC)<br>Comparator_D input CD1<br>Input for an external reference voltage to the ADC (not available on devices without ADC) |
| P1.2/TA1.1/TA0CLK/ CDOUT/A2/CD2 | 3 | 3 | 7 | 7 | A3 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TA1 CCR1 capture: CCI1A input, compare: Out1<br>TA0 input clock<br>Comparator_D output<br>Analog input A2 – ADC (not available on devices without ADC)<br>Comparator_D input CD2 |
| P3.0/A12/CD12 | 4 | N/A | 8 | N/A | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE)<br>Analog input A12 – ADC (not available on devices without ADC or package options PW, RGE)<br>Comparator_D input CD12 (not available on package options PW, RGE) |
| P3.1/A13/CD13 | 5 | N/A | 9 | N/A | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE)<br>Analog input A13 – ADC (not available on devices without ADC or package options PW, RGE)<br>Comparator_D input CD13 (not available on package options PW, RGE) |
| P3.2/A14/CD14 | 6 | N/A | 10 | N/A | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE)<br>Analog input A14 – ADC (not available on devices without ADC or package options PW, RGE)<br>Comparator_D input CD14 (not available on package options PW, RGE) |
| P3.3/A15/CD15 | 7 | N/A | 11 | N/A | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE)<br>Analog input A15 – ADC (not available on devices without ADC or package options PW, RGE)<br>Comparator_D input CD15 (not available on package options PW, RGE) |

(1) I = input, O = output, N/A = not available
(2) The functions associated with P1.0 are implemented but not available on the device pinout. To avoid floating inputs, this digital I/O should be properly configured. The pullup/down resistors of P1.0 should be enabled.


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**Table 4. Terminal Functions (continued)**

| TERMINAL | | | | | | I/O (1) | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| NAME | NO. | | | | | | |
| | RHA | RGE | DA | PW | YFF | | |
| P1.3/TA1.2/UCB0STE/ A3/CD3 | 8 | 4 | 12 | 8 | A4 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TA1 CCR2 capture: CCI2A input, compare: Out2<br>Slave transmit enable – eUSCI_B0 SPI mode<br>Analog input A3 – ADC (not available on devices without ADC)<br>Comparator_D input CD3 |
| P1.4/TB0.1/UCA0STE/ A4/CD4 | 9 | 5 | 13 | 9 | B4 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB0 CCR1 capture: CCI1A input, compare: Out1<br>Slave transmit enable – eUSCI_A0 SPI mode<br>Analog input A4 – ADC (not available on devices without ADC)<br>Comparator_D input CD4 |
| P1.5/TB0.2/UCA0CLK/ A5/CD5 | 10 | 6 | 14 | 10 | A5 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB0 CCR2 capture: CCI2A input, compare: Out2<br>Clock signal input – eUSCI_B0 SPI slave mode, Clock signal output – eUSCI_B0 SPI master mode<br>Analog input A5 – ADC (not available on devices without ADC)<br>Comparator_D input CD5 |
| PJ.0/TDO/TB0OUTH/ SMCLK/CD6 (3) | 11 | 7 | 15 | 11 | C3 | I/O | General-purpose digital I/O<br>Test data output port<br>Switch all PWM outputs high impedance input – TB0<br>SMCLK output<br>Comparator_D input CD6 |
| PJ.1/TDI/TCLK/TB1OUTH/ MCLK/CD7 (3) | 12 | 8 | 16 | 12 | B5 | I/O | General-purpose digital I/O<br>Test data input or test clock input<br>Switch all PWM outputs high impedance input – TB1 (not available on devices without TB1)<br>MCLK output<br>Comparator_D input CD7 |
| PJ.2/TMS/TB2OUTH/ ACLK/CD8 (3) | 13 | 9 | 17 | 13 | C4 | I/O | General-purpose digital I/O<br>Test mode select<br>Switch all PWM outputs high impedance input – TB2 (not available on devices without TB2)<br>ACLK output<br>Comparator_D input CD8 |
| PJ.3/TCK/CD9 (3) | 14 | 10 | 18 | 14 | C5 | I/O | General-purpose digital I/O<br>Test clock<br>Comparator_D input CD9 |
| P4.0/TB2.0 | 15 | N/A | N/A | N/A | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE)<br>TB2 CCR0 capture: CCI0B input, compare: Out0 (not available on devices without TB2 or package options DA, PW, RGE) |
| P4.1 | 16 | N/A | N/A | N/A | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options DA, PW, RGE) |

(3) See JTAG Operation for use with JTAG function.

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**Table 4. Terminal Functions (continued)**

| TERMINAL | | | | | | I/O (1) | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| NAME | NO. | | | | | | |
| | RHA | RGE | DA | PW | YFF | | |
| P2.5/TB0.0/UCA1TXD/ UCA1SIMO | 17 | N/A | 19 | 15 | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB0 CCR0 capture: CCI0A input, compare: Out0<br>Transmit data – eUSCI_A1 UART mode, Slave in, master out – eUSCI_A1 SPI mode (not available on devices without UCSI_A1) |
| P2.6/TB1.0/UCA1RXD/ UCA1SOMI | 18 | N/A | 20 | 16 | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB1 CCR0 capture: CCI0A input, compare: Out0 (not available on devices without TB1)<br>Receive data – eUSCI_A1 UART mode, Slave out, master in – eUSCI_A1 SPI mode (not available on devices without UCSI_A1) |
| TEST/SBWTCK (3) (4) | 19 | 11 | 21 | 17 | D5 | I | Test mode pin – enable JTAG pins<br>Spy-Bi-Wire input clock |
| $\overline{\text{RST}}$/NMI/SBWTDIO (3) (4) | 20 | 12 | 22 | 18 | D4 | I/O | Reset input active low<br>Non-maskable interrupt input<br>Spy-Bi-Wire data input/output |
| P2.0/TB2.0/UCA0TXD/ UCA0SIMO/TB0CLK/ACLK (4) | 21 | 13 | 23 | 19 | E5 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB2 CCR0 capture: CCI0A input, compare: Out0 (not available on devices without TB2)<br>Transmit data – eUSCI_A0 UART mode, Slave in, master out – eUSCI_A0 SPI mode<br>TB0 clock input<br>ACLK output |
| P2.1/TB2.1/UCA0RXD/ UCA0SOMI/TB0.0 (5) | 22 | 14 | 24 | 20 | D3 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB2 CCR1 capture: CCI1A input, compare: Out1 (not available on devices without TB2)<br>Receive data – eUSCI_A0 UART mode, Slave out, master in – eUSCI_A0 SPI mode<br>TB0 CCR0 capture: CCI0A input, compare: Out0 |
| P2.2/TB2.2/UCB0CLK/ TB1.0 | 23 | 15 | 25 | 21 | E4 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB2 CCR2 capture: CCI2A input, compare: Out2 (not available on devices without TB2)<br>Clock signal input – eUSCI_B0 SPI slave mode, Clock signal output – eUSCI_B0 SPI master mode<br>TB1 CCR0 capture: CCI0A input, compare: Out0 (not available on devices without TB1) |
| P3.4/TB1.1/TB2CLK/ SMCLK | 24 | N/A | 26 | N/A | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE)<br>TB1 CCR1 capture: CCI1B input, compare: Out1 (not available on devices without TB1)<br>TB2 clock input (not available on devices without TB2 or package options PW, RGE)<br>SMCLK output (not available on package options PW, RGE) |

(4) See Bootstrap Loader (BSL) and JTAG Operation for use with BSL and JTAG functions.
(5) See Bootstrap Loader (BSL) and JTAG Operation for use with BSL and JTAG functions.


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**Table 4. Terminal Functions (continued)**

| TERMINAL | | | | | | I/O (1) | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| NAME | NO. | | | | | | |
| | RHA | RGE | DA | PW | YFF | | |
| P3.5/TB1.2/CDOUT | 25 | N/A | 27 | N/A | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE)<br>TB1 CCR2 capture: CCI2B input, compare: Out2 (not available on devices without TB1)<br>Comparator_D output (not available on package options PW, RGE) |
| P3.6/TB2.1/TB1CLK | 26 | N/A | 28 | N/A | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE)<br>TB2 CCR1 capture: CCI1B input, compare: Out1 (not available on devices without TB2)<br>TB1 clock input (not available on devices without TB1 or package options PW, RGE) |
| P3.7/TB2.2 | 27 | N/A | 29 | N/A | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE)<br>TB2 CCR2 capture: CCI2B input, compare: Out2 (not available on devices without TB2 or package options PW, RGE) |
| P1.6/TB1.1/UCB0SIMO/ UCB0SDA/TA0.0 | 28 | 16 | 30 | 22 | E2 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB1 CCR1 capture: CCI1A input, compare: Out1 (not available on devices without TB1)<br>Slave in, master out – eUSCI_B0 SPI mode<br>I2C data – eUSCI_B0 I2C mode<br>TA0 CCR0 capture: CCI0A input, compare: Out0 |
| P1.7/TB1.2/UCB0SOMI/ UCB0SCL/TA1.0 | 29 | 17 | 31 | 23 | E3 | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5<br>TB1 CCR2 capture: CCI2A input, compare: Out2 (not available on devices without TB1)<br>Slave out, master in – eUSCI_B0 SPI mode<br>I2C clock – eUSCI_B0 I2C mode<br>TA1 CCR0 capture: CCI0A input, compare: Out0 |
| VCORE (6) | 30 | 18 | 32 | 24 | E1 | | Regulated core power supply (internal use only, no external current loading) |
| DVSS | 31 | 19 | 33 | 25 | D2 | | Digital ground supply |
| DVCC | 32 | 20 | 34 | 26 | D1 | | Digital power supply |
| P2.7 | 33 | N/A | 35 | N/A | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options PW, RGE) |
| P2.3/TA0.0/UCA1STE/ A6/CD10 | 34 | N/A | 36 | 27 | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options RGE)<br>TA0 CCR0 capture: CCI0B input, compare: Out0 (not available on package options RGE)<br>Slave transmit enable – eUSCI_A1 SPI mode (not available on devices without eUSCI_A1)<br>Analog input A6 – ADC (not available on devices without ADC)<br>Comparator_D input CD10 (not available on package options RGE) |
| P2.4/TA1.0/UCA1CLK/ A7/CD11 | 35 | N/A | 37 | 28 | N/A | I/O | General-purpose digital I/O with port interrupt and wake up from LPMx.5 (not available on package options RGE)<br>TA1 CCR0 capture: CCI0B input, compare: Out0 (not available on package options RGE)<br>Clock signal input – eUSCI_A1 SPI slave mode, Clock signal output – eUSCI_A1 SPI master mode (not available on devices without eUSCI_A1)<br>Analog input A7 – ADC (not available on devices without ADC)<br>Comparator_D input CD11 (not available on package options RGE) |

(6) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, $C_{VCORE}$.

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**Table 4. Terminal Functions (continued)**

| TERMINAL | | | | | | I/O (1) | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| NAME | NO. | | | | | | |
| | RHA | RGE | DA | PW | YFF | | |
| AVSS | 36 | N/A | 38 | N/A | B3 | | Analog ground supply |
| PJ.4/XIN | 37 | 21 | 1 | 1 | C1 | I/O | General-purpose digital I/O<br>Input terminal for crystal oscillator XT1 |
| PJ.5/XOUT | 38 | 22 | 2 | 2 | B1 | I/O | General-purpose digital I/O<br>Output terminal of crystal oscillator XT1 |
| AVSS | 39 | 23 | 3 | 3 | C2 | | Analog ground supply |
| AVCC | 40 | 24 | 4 | 4 | B2 | | Analog power supply |
| QFN Pad | Pad | Pad | N/A | N/A | N/A | | QFN package pad. Connection to VSS recommended. |


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# SHORT-FORM DESCRIPTION

## CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

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## Operating Modes

The MSP430 has one active mode and seven software-selectable low-power modes of operation. An interrupt event can wake up the device from low-power modes LPM0 through LPM4, service the request, and restore back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

The following eight operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK active, MCLK disabled, SMCLK optionally active
  - Complete data retention
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK active, MCLK disabled, SMCLK optionally active
  - DCO disabled
  - Complete data retention
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - ACLK active, MCLK disabled, SMCLK optionally active
  - DCO disabled
  - Complete data retention
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - ACLK active, MCLK and SMCLK disabled
  - DCO disabled
  - Complete data retention
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK, MCLK, SMCLK disabled
  - Complete data retention
- Low-power mode 3.5 (LPM3.5)
  - RTC operation
  - Internal regulator disabled
  - No data retention
  - I/O pad state retention
  - Wake up from $\overline{\text{RST}}$, general-purpose I/O, RTC events
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator disabled
  - No data retention
  - I/O pad state retention
  - Wake up from $\overline{\text{RST}}$ and general-purpose I/O


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## Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

**Table 5. Interrupt Sources, Flags, and Vectors**

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| **System Reset**<br>Power-Up, Brownout, Supply Supervisors<br>External Reset $\overline{RST}$<br>Watchdog Timeout (Watchdog mode)<br>WDT, FRCTL MPU, CS, PMM Password Violation<br>FRAM double bit error detection<br>MPU segment violation<br>Software POR, BOR | SVSLIFG, SVSHIFG<br>PMMRSTIFG<br>WDTIFG<br>WDTPW, FRCTLPW, MPUPW, CSPW, PMMPW<br>DBDIFG<br>MPUSEGIIFG, MPUSEG1IFG, MPUSEG2IFG, MPUSEG3IFG<br>PMMPORIFG, PMMBORIFG<br>(SYSRSTIV) (1) (2) | Reset | 0FFFEh | 63, highest |
| **System NMI**<br>Vacant Memory Access<br>JTAG Mailbox<br>FRAM access time error<br>Access violation<br>FRAM single, double bit error detection | VMAIFG<br>JMBNIFG, JMBOUTIFG<br>ACCTIMIFG<br>ACCVIFG<br>SBDIFG, DBDIFG<br>(SYSSNIV) (1) | (Non)maskable | 0FFFCh | 62 |
| **User NMI**<br>External NMI<br>Oscillator Fault | NMIIFG, OFIFG<br>(SYSUNIV) (1) (2) | (Non)maskable | 0FFFAh | 61 |
| Comparator_D | Comparator_D interrupt flags<br>(CBIV) (1) (3) | Maskable | 0FFF8h | 60 |
| TB0 | TB0CCR0 CCIFG0 (3) | Maskable | 0FFF6h | 59 |
| TB0 | TB0CCR1 CCIFG1 to TB0CCR2 CCIFG2, TB0IFG<br>(TB0IV) (1) (3) | Maskable | 0FFF4h | 58 |
| Watchdog Timer (Interval Timer Mode) | WDTIFG | Maskable | 0FFF2h | 57 |
| eUSCI_A0 Receive and Transmit | UCA0RXIFG, UCA0TXIFG (SPI mode)<br>UCA0STTIFG, UCA0TXCPTIFG, UCA0RXIFG, UXA0TXIFG (UART mode)<br>(UCA0IV) (1) (3) | Maskable | 0FFF0h | 56 |
| eUSCI_B0 Receive and Transmit | UCB0STTIFG, UCB0TXCPTIFG, UCB0RXIFG, UCB0TXIFG (SPI mode)<br>UCB0ALIFG, UCB0NACKIFG, UCB0STTIFG, UCB0STPIFG, UCB0RXIFG0, UCB0TXIFG0, UCB0RXIFG1, UCB0TXIFG1, UCB0RXIFG2, UCB0TXIFG2, UCB0RXIFG3, UCB0TXIFG3, UCB0CNTIFG, UCB0BIT9IFG (I2C mode)<br>(UCB0IV) (1) (3) | Maskable | 0FFEEh | 55 |
| ADC10_B | ADC10OVIFG, ADC10TOVIFG, ADC10HIIFG, ADC10LOIFG<br>ADC10INIFG, ADC10IFG0<br>(ADC10IV) (1) (3) (4) | Maskable | 0FFECh | 54 |
| TA0 | TA0CCR0 CCIFG0 (3) | Maskable | 0FFEAh | 53 |
| TA0 | TA0CCR1 CCIFG1 to TA0CCR2 CCIFG2, TA0IFG<br>(TA0IV) (1) (3) | Maskable | 0FFE8h | 52 |

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
(3) Interrupt flags are located in the module.
(4) Only on devices with ADC, otherwise reserved.

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**Table 5. Interrupt Sources, Flags, and Vectors (continued)**

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| eUSCI_A1 Receive and Transmit | UCA1RXIFG, UCA1TXIFG (SPI mode) UCA1STTIFG, UCA1TXCPTIFG, UCA1RXIFG, UXA1TXIFG (UART mode) (UCA1IV) (1) (3) | Maskable | 0FFE6h | 51 |
| DMA | DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) (1) (3) | Maskable | 0FFE4h | 50 |
| TA1 | TA1CCR0 CCIFG0 (3) | Maskable | 0FFE2h | 49 |
| TA1 | TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV) (1) (3) | Maskable | 0FFE0h | 48 |
| I/O Port P1 | P1IFG.0 to P1IFG.7 (P1IV) (1) (3) | Maskable | 0FFDEh | 47 |
| TB1 | TB1CCR0 CCIFG0 (3) | Maskable | 0FFDCh | 46 |
| TB1 | TB1CCR1 CCIFG1 to TB1CCR2 CCIFG2, TB1IFG (TB1IV) (1) (3) | Maskable | 0FFDAh | 45 |
| I/O Port P2 | P2IFG.0 to P2IFG.7 (P2IV) (1) (3) | Maskable | 0FFD8h | 44 |
| TB2 | TB2CCR0 CCIFG0 (3) | Maskable | 0FFD6h | 43 |
| TB2 | TB2CCR1 CCIFG1 to TB2CCR2 CCIFG2, TB2IFG (TB2IV) (1) (3) | Maskable | 0FFD4h | 42 |
| I/O Port P3 | P3IFG.0 to P3IFG.7 (P3IV) (5) (6) | Maskable | 0FFD2h | 41 |
| I/O Port P4 | P4IFG.0 to P4IFG.2 (P4IV) (5) (6) | Maskable | 0FFD0h | 40 |
| RTC_B | RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV) (5) (6) | Maskable | 0FFCEh | 39 |
| Reserved | Reserved (7) | | 0FFCCh<br>⋮<br>0FF80h | 38<br>⋮<br>0, lowest |

(5) Multiple source flags
(6) Interrupt flags are located in the module.
(7) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.


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## Memory Organization

**Table 6. Memory Organization (1) (2)**

| | | MSP430FR5726<br>MSP430FR5727<br>MSP430FR5728<br>MSP430FR5729<br>MSP430FR5736<br>MSP430FR5737<br>MSP430FR5738<br>MSP430FR5739 | MSP430FR5722<br>MSP430FR5723<br>MSP430FR5724<br>MSP430FR5725<br>MSP430FR5732<br>MSP430FR5733<br>MSP430FR5734<br>MSP430FR5735 | MSP430FR5720<br>MSP430FR5721<br>MSP430FR5730<br>MSP430FR5731 |
|---|---|---|---|---|
| Memory (FRAM)<br>Main: interrupt vectors<br>Main: code memory | Total Size | 15.5 KB<br>00FFFFh–00FF80h<br>00FF7Fh–00C200h | 8.0 KB<br>00FFFFh–00FF80h<br>00FF7Fh–00E000h | 4 KB<br>00FFFFh–00FF80h<br>00FF7Fh–00F000h |
| RAM | | 1 KB<br>001FFFh–001C00h | 1 KB<br>001FFFh–001C00h | 1 KB<br>001FFFh–001C00h |
| Device Descriptor Info (TLV) (FRAM) | | 128 B<br>001A7Fh–001A00h | 128 B<br>001A7Fh–001A00h | 128 B<br>001A7Fh–001A00h |
| Information memory (FRAM) | N/A | 0019FFh–001980h<br>Address space mirrored to Info A | 0019FFh–001980h<br>Address space mirrored to Info A | 0019FFh–001980h<br>Address space mirrored to Info A |
| | N/A | 00197Fh–001900h<br>Address space mirrored to Info B | 00197Fh–001900h<br>Address space mirrored to Info B | 00197Fh–001900h<br>Address space mirrored to Info B |
| | Info A | 128 B<br>0018FFh–001880h | 128 B<br>0018FFh–001880h | 128 B<br>0018FFh–001880h |
| | Info B | 128 B<br>00187Fh–001800h | 128 B<br>00187Fh–001800h | 128 B<br>00187Fh–001800h |
| Bootstrap loader (BSL) memory (ROM) | BSL 3 | 512 B<br>0017FFh–001600h | 512 B<br>0017FFh–001600h | 512 B<br>0017FFh–001600h |
| | BSL 2 | 512 B<br>0015FFh–001400h | 512 B<br>0015FFh–001400h | 512 B<br>0015FFh–001400h |
| | BSL 1 | 512 B<br>0013FFh–001200h | 512 B<br>0013FFh–001200h | 512 B<br>0013FFh–001200h |
| | BSL 0 | 512 B<br>0011FFh–001000h | 512 B<br>0011FFh–001000h | 512 B<br>0011FFh–001000h |
| Peripherals | Size | 4 KB<br>000FFFh–0h | 4 KB<br>000FFFh–0h | 4 KB<br>000FFFh–0h |

(1) N/A = Not available
(2) All address space not listed in this table is considered vacant memory.

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## Bootstrap Loader (BSL)

The BSL enables users to program the FRAM or RAM using a UART serial interface. Access to the device memory by the BSL is protected by an user-defined password. Use of the BSL requires four pins as shown in Table 7. BSL entry requires a specific entry sequence on the RST/NMI/SBWTDIO and TEST/SBWTCK pins. For complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader User's Guide* (SLAU319).

**Table 7. BSL Pin Requirements and Functions**

| DEVICE SIGNAL | BSL FUNCTION |
|---|---|
| RST/NMI/SBWTDIO | Entry sequence signal |
| TEST/SBWTCK | Entry sequence signal |
| P2.0 | Data transmit |
| P2.1 | Data receive |
| VCC | Power supply |
| VSS | Ground supply |

## JTAG Operation

### JTAG Standard Interface

The MSP430 family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the RST/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are shown in Table 8. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

**Table 8. JTAG Pin Requirements and Functions**

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|---|---|---|
| PJ.3/TCK | IN | JTAG clock input |
| PJ.2/TMS | IN | JTAG state control |
| PJ.1/TDI/TCLK | IN | JTAG data input, TCLK input |
| PJ.0/TDO | OUT | JTAG data output |
| TEST/SBWTCK | IN | Enable JTAG pins |
| RST/NMI/SBWTDIO | IN | External reset |
| VCC | | Power supply |
| VSS | | Ground supply |

### Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. The Spy-Bi-Wire interface pin requirements are shown in Table 9. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

**Table 9. Spy-Bi-Wire Pin Requirements and Functions**

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|---|---|---|
| TEST/SBWTCK | IN | Spy-Bi-Wire clock input |
| RST/NMI/SBWTDIO | IN, OUT | Spy-Bi-Wire data input and output |
| VCC | | Power supply |
| VSS | | Ground supply |


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## FRAM

The FRAM can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. Features of the FRAM include:

- Low-power ultrafast write nonvolatile memory
- Byte and word access capability
- Programmable and automated wait state generation
- Error Correction Coding (ECC) with single bit detection and correction, double bit detection

## Memory Protection Unit (MPU)

The FRAM can be protected from inadvertent CPU execution or write access by the MPU. Features of the MPU include:

- Main memory partitioning programmable up to three segments
- Each segment's (main and information memory) access rights can be individually selected
- Access violation flags with interrupt capability for easy servicing of access violations

## Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430FR57xx Family User's Guide* (SLAU272).

### Digital I/O

There are up to four 8-bit I/O ports implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for all ports.
- Read/write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.

### Oscillator and Clock System (CS)

The clock system includes support for a 32-kHz watch crystal oscillator XT1 (LF mode), an internal very-low-power low-frequency oscillator (VLO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator XT1 (HF mode). The clock system module is designed to meet the requirements of both low system cost and low power consumption. A fail-safe mechanism exists for all crystal sources. The clock system module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (XT1 LF mode), a high-frequency crystal (XT1 HF mode), the internal VLO, or the internal DCO.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by the same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by the same sources made available to ACLK.

### Power Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS circuitry detects if the supply voltage drops below a user-selectable safe level. SVS circuitry is available on the primary and core supplies.

### Hardware Multiplier (MPY)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

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### Real-Time Clock (RTC_B)

The RTC_B module contains an integrated real-time clock (RTC) (calendar mode). Calendar mode integrates an internal calendar which compensates for months with fewer than 31 days and includes leap year correction. The RTC_B also supports flexible alarm functions and offset-calibration hardware. RTC operation is available in LPM3.5 mode to minimize power consumption.

### Watchdog Timer (WDT_A)

The primary function of the watchdog timer (WDT_A) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

### System Module (SYS)

The SYS module handles many of the system functions within the device. These include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootstrap loader entry mechanisms, and configuration management (device descriptors). It also includes a data exchange mechanism using JTAG called a JTAG mailbox that can be used in the application.


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**Table 10. System Module Interrupt Vector Registers**

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT | VALUE | PRIORITY |
|---|---|---|---|---|
| **SYSRSTIV, System Reset** | 019Eh | No interrupt pending | 00h | |
| | | Brownout (BOR) | 02h | Highest |
| | | RSTIFG $\overline{\text{RST}}$/NMI (BOR) | 04h | |
| | | PMMSWBOR software BOR (BOR) | 06h | |
| | | LPMx.5 wake up (BOR) | 08h | |
| | | Security violation (BOR) | 0Ah | |
| | | SVSLIFG SVSL event (BOR) | 0Ch | |
| | | SVSHIFG SVSH event (BOR) | 0Eh | |
| | | Reserved | 10h | |
| | | Reserved | 12h | |
| | | PMMSWPOR software POR (POR) | 14h | |
| | | WDTIFG watchdog timeout (PUC) | 16h | |
| | | WDTPW password violation (PUC) | 18h | |
| | | FRCTLPW password violation (PUC) | 1Ah | |
| | | DBDIFG FRAM double bit error (PUC) | 1Ch | |
| | | Peripheral area fetch (PUC) | 1Eh | |
| | | PMMPW PMM password violation (PUC) | 20h | |
| | | MPUPW MPU password violation (PUC) | 22h | |
| | | CSPW CS password violation (PUC) | 24h | |
| | | MPUSEGIIFG information memory segment violation (PUC) | 26h | |
| | | MPUSEG1IFG segment 1 memory violation (PUC) | 28h | |
| | | MPUSEG2IFG segment 2 memory violation (PUC) | 2Ah | |
| | | MPUSEG3IFG segment 3 memory violation (PUC) | 2Ch | |
| | | Reserved | 2Eh | |
| | | Reserved | 30h to 3Eh | Lowest |
| **SYSSNIV, System NMI** | 019Ch | No interrupt pending | 00h | |
| | | DBDIFG FRAM double bit error | 02h | Highest |
| | | ACCTIMIFG access time error | 04h | |
| | | ACCVIFG access violation | 0Eh | |
| | | VMAIFG Vacant memory access | 10h | |
| | | JMBINIFG JTAG mailbox input | 12h | |
| | | JMBOUTIFG JTAG mailbox output | 14h | |
| | | SBDIFG FRAM single bit error | 16h | |
| | | Reserved | 18h to 1Eh | Lowest |
| **SYSUNIV, User NMI** | 019Ah | No interrupt pending | 00h | |
| | | NMIFG NMI pin | 02h | Highest |
| | | OFIFG oscillator fault | 04h | |
| | | Reserved | 06h | |
| | | Reserved | 08h | |
| | | Reserved | 0Ah to 1Eh | Lowest |

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### DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10_B conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

**Table 11. DMA Trigger Assignments (1)**

| TRIGGER | CHANNEL 0 | CHANNEL 1 | CHANNEL 2 |
|---|---|---|---|
| 0 | DMAREQ | DMAREQ | DMAREQ |
| 1 | TA0CCR0 CCIFG | TA0CCR0 CCIFG | TA0CCR0 CCIFG |
| 2 | TA0CCR2 CCIFG | TA0CCR2 CCIFG | TA0CCR2 CCIFG |
| 3 | TA1CCR0 CCIFG | TA1CCR0 CCIFG | TA1CCR0 CCIFG |
| 4 | TA1CCR2 CCIFG | TA1CCR2 CCIFG | TA1CCR2 CCIFG |
| 5 | Reserved | Reserved | Reserved |
| 6 | Reserved | Reserved | Reserved |
| 7 | TB0CCR0 CCIFG | TB0CCR0 CCIFG | TB0CCR0 CCIFG |
| 8 | TB0CCR2 CCIFG | TB0CCR2 CCIFG | TB0CCR2 CCIFG |
| 9 | TB1CCR0 CCIFG (2) | TB1CCR0 CCIFG (2) | TB1CCR0 CCIFG (2) |
| 10 | TB1CCR2 CCIFG (2) | TB1CCR2 CCIFG (2) | TB1CCR2 CCIFG (2) |
| 11 | TB2CCR0 CCIFG (3) | TB2CCR0 CCIFG (3) | TB2CCR0 CCIFG (3) |
| 12 | TB2CCR2 CCIFG (3) | TB2CCR2 CCIFG (3) | TB2CCR2 CCIFG (3) |
| 13 | Reserved | Reserved | Reserved |
| 14 | UCA0RXIFG | UCA0RXIFG | UCA0RXIFG |
| 15 | UCA0TXIFG | UCA0TXIFG | UCA0TXIFG |
| 16 | UCA1RXIFG (4) | UCA1RXIFG (4) | UCA1RXIFG (4) |
| 17 | UCA1TXIFG (4) | UCA1TXIFG (4) | UCA1TXIFG (4) |
| 18 | UCB0RXIFG0 | UCB0RXIFG0 | UCB0RXIFG0 |
| 19 | UCB0TXIFG0 | UCB0TXIFG0 | UCB0TXIFG0 |
| 20 | UCB0RXIFG1 | UCB0RXIFG1 | UCB0RXIFG1 |
| 21 | UCB0TXIFG1 | UCB0TXIFG1 | UCB0TXIFG1 |
| 22 | UCB0RXIFG2 | UCB0RXIFG2 | UCB0RXIFG2 |
| 23 | UCB0TXIFG2 | UCB0TXIFG2 | UCB0TXIFG2 |
| 24 | UCB0RXIFG3 | UCB0RXIFG3 | UCB0RXIFG3 |
| 25 | UCB0TXIFG3 | UCB0TXIFG3 | UCB0TXIFG3 |
| 26 | ADC10IFGx (5) | ADC10IFGx (5) | ADC10IFGx (5) |
| 27 | Reserved | Reserved | Reserved |
| 28 | Reserved | Reserved | Reserved |
| 29 | MPY ready | MPY ready | MPY ready |
| 30 | DMA2IFG | DMA0IFG | DMA1IFG |
| 31 | DMAE0 (6) | DMAE0 (6) | DMAE0 (6) |

(1) If a reserved trigger source is selected, no trigger is generated.
(2) Only on devices with TB1, otherwise reserved
(3) Only on devices with TB2, otherwise reserved
(4) Only on devices with eUSCI_A1, otherwise reserved
(5) Only on devices with ADC, otherwise reserved
(6) This function is not available on YFF package types.


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### Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI modules are used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and $I^2C$, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each eUSCI module contains two portions, A and B.

The eUSCI_An module provides support for SPI (3 pin or 4 pin), UART, enhanced UART, or IrDA.

The eUSCI_Bn module provides support for SPI (3 pin or 4 pin) or I2C.

The MSP430FR572x and MSP430FR573x series include one or two eUSCI_An modules (eUSCI_A0, eUSCI_A1) and one eUSCI_Bn module (eUSCI_B).

### TA0, TA1

TA0 and TA1 are 16-bit timers/counters (Timer_A type) with three capture/compare registers each. Each can support multiple capture/compares, PWM outputs, and interval timing. Each has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 12. TA0 Signal Connections**

| INPUT PIN NUMBER | | | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RHA | RGE, YFF | DA | PW | | | | | | RHA | RGE, YFF | DA | PW |
| 3-P1.2 | 3-P1.2, A3-P1.2 | 7-P1.2 | 7-P1.2 | TA0CLK | TACLK | Timer | N/A | N/A | | | | |
| | | | | ACLK (internal) | ACLK | | | | | | | |
| | | | | SMCLK (internal) | SMCLK | | | | | | | |
| 3-P1.2 | 3-P1.2, A3-P1.2 | 7-P1.2 | 7-P1.2 | TA0CLK | $\overline{\text{TACLK}}$ | | | | | | | |
| 28-P1.6 | 16-P1.6, E2-P1.6 | 30-P1.6 | 22-P1.6 | TA0.0 | CCI0A | CCR0 | TA0 | TA0.0 | 28-P1.6 | 16-P1.6 , E2-P1.6 | 30-P1.6 | 22-P1.6 |
| 34-P2.3 | N/A | 36-P2.3 | 27-P2.3 | TA0.0 | CCI0B | | | | 34-P2.3 | N/A | 36-P2.3 | 27-P2.3 |
| | | | | $DV_{SS}$ | GND | | | | | | | |
| | | | | $DV_{CC}$ | $V_{CC}$ | | | | | | | |
| 1-P1.0 | 1-P1.0, N/A | 5-P1.0 | 5-P1.0 | TA0.1 | CCI1A | CCR1 | TA1 | TA0.1 | 1-P1.0 | 1-P1.0 , N/A | 5-P1.0 | 5-P1.0 |
| | | | | CDOUT (internal) | CCI1B | | | | ADC10 (internal) (1) ADC10SHSx = {1} | ADC10 (internal) (1) ADC10SHSx = {1} | ADC10 (internal) (1) ADC10SHSx = {1} | ADC10 (internal) (1) ADC10SHSx = {1} |
| | | | | $DV_{SS}$ | GND | | | | | | | |
| | | | | $DV_{CC}$ | $V_{CC}$ | | | | | | | |
| 2-P1.1 | 2-P1.1, A2-P1.1 | 6-P1.1 | 6-P1.1 | TA0.2 | CCI2A | CCR2 | TA2 | TA0.2 | 2-P1.1 | 2-P1.1, A2-P1.1 | 6-P1.1 | 6-P1.1 |
| | | | | ACLK (internal) | CCI2B | | | | | | | |
| | | | | $DV_{SS}$ | GND | | | | | | | |
| | | | | $DV_{CC}$ | $V_{CC}$ | | | | | | | |

(1) Only on devices with ADC

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## Table 13. TA1 Signal Connections

| INPUT PIN NUMBER | | | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RHA | RGE, YFF | DA | PW | | | | | | RHA | RGE, YFF | DA | PW |
| 2-P1.1 | 2-P1.1, A2-P1.1 | 6-P1.1 | 6-P1.1 | TA1CLK | TACLK | Timer | N/A | N/A | | | | |
| | | | | ACLK (internal) | ACLK | | | | | | | |
| | | | | SMCLK (internal) | SMCLK | | | | | | | |
| 2-P1.1 | 2-P1.1, A2-P1.1 | 6-P1.1 | 6-P1.1 | TA1CLK | $\overline{\text{TACLK}}$ | | | | | | | |
| 29-P1.7 | 17-P1.7, E3-P1.7 | 31-P1.7 | 23-P1.7 | TA1.0 | CCI0A | CCR0 | TA0 | TA1.0 | 29-P1.7 | 17-P1.7, E3-P1.7 | 31-P1.7 | 23-P1.7 |
| 35-P2.4 | N/A | 37-P2.4 | 28-P2.4 | TA1.0 | CCI0B | | | | 35-P2.4 | N/A | 37-P2.4 | 28-P2.4 |
| | | | | $DV_{SS}$ | GND | | | | | | | |
| | | | | $DV_{CC}$ | $V_{CC}$ | | | | | | | |
| 3-P1.2 | 3-P1.2, N/A | 7-P1.2 | 7-P1.2 | TA1.1 | CCI1A | CCR1 | TA1 | TA1.1 | 3-P1.2 | 3-P1.2, N/A | 7-P1.2 | 7-P1.2 |
| | | | | CDOUT (internal) | CCI1B | | | | | | | |
| | | | | $DV_{SS}$ | GND | | | | | | | |
| | | | | $DV_{CC}$ | $V_{CC}$ | | | | | | | |
| 8-P1.3 | 4-P1.3, A4-P1.3 | 12-P1.3 | 8-P1.3 | TA1.2 | CCI2A | CCR2 | TA2 | TA1.2 | 8-P1.3 | 4-P1.3, A4-P1.3 | 12-P1.3 | 8-P1.3 |
| | | | | ACLK (internal) | CCI2B | | | | | | | |
| | | | | $DV_{SS}$ | GND | | | | | | | |
| | | | | $DV_{CC}$ | $V_{CC}$ | | | | | | | |


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### TB0, TB1, TB2

TB0, TB1, and TB2 are 16-bit timers/counters (Timer_B type) with three capture/compare registers each. Each can support multiple capture/compares, PWM outputs, and interval timing. Each has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 14. TB0 Signal Connections**

| INPUT PIN NUMBER | | | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RHA | RGE, YFF | DA | PW | | | | | | RHA | RGE, YFF | DA | PW |
| 21-P2.0 | 13-P2.0, E5-P2.0 | 23-P2.0 | 19-P2.0 | TB0CLK | TBCLK | Timer | N/A | N/A | | | | |
| | | | | ACLK (internal) | ACLK | | | | | | | |
| | | | | SMCLK (internal) | SMCLK | | | | | | | |
| 21-P2.0 | 13-P2.0, E5-P2.0 | 23-P2.0 | 19-P2.0 | TB0CLK | $\overline{\text{TBCLK}}$ | | | | | | | |
| 22-P2.1 | 14-P2.1, D3-P2.1 | 24-P2.1 | 20-P2.1 | TB0.0 | CCI0A | CCR0 | TB0 | TB0.0 | 22-P2.1 | 14-P2.1, D3-P2.1 | 24-P2.1 | 20-P2.1 |
| 17-P2.5 | N/A | 19-P2.5 | 15-P2.5 | TB0.0 | CCI0B | | | | 17-P2.5 | N/A | 19-P2.5 | 15-P2.5 |
| | | | | $DV_{SS}$ | GND | | | | ADC10 (internal) (1) ADC10SHSx = {2} | ADC10 (internal) (1) ADC10SHSx = {2} | ADC10 (internal) (1) ADC10SHSx = {2} | ADC10 (internal) (1) ADC10SHSx = {2} |
| | | | | $DV_{CC}$ | $V_{CC}$ | | | | | | | |
| 9-P1.4 | 5-P1.4, B4-P1.4 | 13-P1.4 | 9-P1.4 | TB0.1 | CCI1A | CCR1 | TB1 | TB0.1 | 9-P1.4 | 5-P1.4, B4-P1.4 | 13-P1.4 | 9-P1.4 |
| | | | | CDOUT (internal) | CCI1B | | | | ADC10 (internal) (1) ADC10SHSx = {3} | ADC10 (internal) (1) ADC10SHSx = {3} | ADC10 (internal) (1) ADC10SHSx = {3} | ADC10 (internal) (1) ADC10SHSx = {3} |
| | | | | $DV_{SS}$ | GND | | | | | | | |
| | | | | $DV_{CC}$ | $V_{CC}$ | | | | | | | |
| 10-P1.5 | 6-P1.5, A5-P1.5 | 14-P1.5 | 19-P1.5 | TB0.2 | CCI2A | CCR2 | TB2 | TB0.2 | 10-P1.5 | 6-P1.5, A5-P1.5 | 14-P1.5 | 19-P1.5 |
| | | | | ACLK (internal) | CCI2B | | | | | | | |
| | | | | $DV_{SS}$ | GND | | | | | | | |
| | | | | $DV_{CC}$ | $V_{CC}$ | | | | | | | |

(1) Only on devices with ADC

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## Table 15. TB1 Signal Connections (1)

| INPUT PIN NUMBER | | | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RHA | RGE, YFF | DA | PW | | | | | | RHA | RGE, YFF | DA | PW |
| 26-P3.6 | N/A ($DV_{SS}$), N/A ($DV_{SS}$) | 28-P3.6 | N/A ($DV_{SS}$) | TB1CLK | TBCLK | Timer | N/A | N/A | | | | |
| | | | | ACLK (internal) | ACLK | | | | | | | |
| | | | | SMCLK (internal) | SMCLK | | | | | | | |
| 26-P3.6 | N/A ($DV_{SS}$), N/A ($DV_{SS}$) | 28-P3.6 | N/A ($DV_{SS}$) | TB1CLK | $\overline{TBCLK}$ | | | | | | | |
| 23-P2.2 | N/A ($DV_{SS}$), N/A ($DV_{SS}$) | 25-P2.2 | N/A ($DV_{SS}$) | TB1.0 | CCI0A | CCR0 | TB0 | TB1.0 | 23-P2.2 | N/A | 25-P2.2 | N/A |
| 18-P2.6 | N/A ($DV_{SS}$), N/A ($DV_{SS}$) | 20-P2.6 | N/A ($DV_{SS}$) | TB1.0 | CCI0B | | | | 18-P2.6 | N/A | 20-P2.6 | N/A |
| | | | | $DV_{SS}$ | GND | | | | | | | |
| | | | | $DV_{CC}$ | $V_{CC}$ | | | | | | | |
| 28-P1.6 | N/A ($DV_{SS}$), N/A ($DV_{SS}$) | 30-P1.6 | N/A ($DV_{SS}$) | TB1.1 | CCI1A | CCR1 | TB1 | TB1.1 | 28-P1.6 | N/A | 30-P1.6 | N/A |
| 24-P3.4 | N/A ($DV_{SS}$), N/A ($DV_{SS}$) | 26-P3.4 | N/A ($DV_{SS}$) | TB1.1 | CCI1B | | | | 24-P3.4 | N/A | 26-P3.4 | N/A |
| | | | | $DV_{SS}$ | GND | | | | | | | |
| | | | | $DV_{CC}$ | $V_{CC}$ | | | | | | | |
| 29-P1.7 | N/A ($DV_{SS}$), N/A ($DV_{SS}$) | 31-P1.7 | N/A ($DV_{SS}$) | TB1.2 | CCI2A | CCR2 | TB2 | TB1.2 | 29-P1.7 | N/A | 31-P1.7 | N/A |
| 25-P3.5 | N/A ($DV_{SS}$), N/A ($DV_{SS}$) | 27-P3.5 | N/A ($DV_{SS}$) | TB1.2 | CCI2B | | | | 25-P3.5 | N/A | 27-P3.5 | N/A |
| | | | | $DV_{SS}$ | GND | | | | | | | |
| | | | | $DV_{CC}$ | $V_{CC}$ | | | | | | | |

(1) TB1 is not present on all device types.

## Table 16. TB2 Signal Connections (1)

| INPUT PIN NUMBER | | | | DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RHA | RGE, YFF | DA | PW | | | | | | RHA | RGE, YFF | DA | PW |
| 24-P3.4 | N/A ($DV_{SS}$), N/A ($DV_{SS}$) | 26-P3.4 | N/A ($DV_{SS}$) | TB2CLK | TBCLK | Timer | N/A | N/A | | | | |
| | | | | ACLK (internal) | ACLK | | | | | | | |
| | | | | SMCLK (internal) | SMCLK | | | | | | | |
| 24-P3.4 | N/A ($DV_{SS}$), N/A ($DV_{SS}$) | 26-P3.4 | N/A ($DV_{SS}$) | TB2CLK | $\overline{TBCLK}$ | | | | | | | |
| 21-P2.0 | N/A ($DV_{SS}$), N/A ($DV_{SS}$) | 23-P2.0 | N/A ($DV_{SS}$) | TB2.0 | CCI0A | CCR0 | TB0 | TB2.0 | 21-P2.0 | N/A | 23-P2.0 | N/A |
| 15-P4.0 | N/A ($DV_{SS}$), N/A ($DV_{SS}$) | N/A ($DV_{SS}$) | N/A ($DV_{SS}$) | TB2.0 | CCI0B | | | | 15-P4.0 | N/A | 36-P4.0 | N/A |
| | | | | $DV_{SS}$ | GND | | | | | | | |
| | | | | $DV_{CC}$ | $V_{CC}$ | | | | | | | |
| 22-P2.1 | N/A ($DV_{SS}$), N/A ($DV_{SS}$) | 24-P2.1 | N/A ($DV_{SS}$) | TB2.1 | CCI1A | CCR1 | TB1 | TB2.1 | 22-P2.1 | N/A | 24-P2.1 | N/A |
| 26-P3.6 | N/A ($DV_{SS}$), N/A ($DV_{SS}$) | 28-P3.6 | N/A ($DV_{SS}$) | TB2.1 | CCI1B | | | | 26-P3.6 | N/A | 28-P3.6 | N/A |
| | | | | $DV_{SS}$ | GND | | | | | | | |
| | | | | $DV_{CC}$ | $V_{CC}$ | | | | | | | |
| 23-P2.2 | N/A ($DV_{SS}$), N/A ($DV_{SS}$) | 25-P2.2 | N/A ($DV_{SS}$) | TB2.2 | CCI2A | CCR2 | TB2 | TB2.2 | 23-P2.2 | N/A | 25-P2.2 | N/A |
| 27-P3.7 | N/A ($DV_{SS}$), N/A ($DV_{SS}$) | 29-P3.7 | N/A ($DV_{SS}$) | TB2.2 | CCI2B | | | | 27-P3.7 | N/A | 29-P3.7 | N/A |
| | | | | $DV_{SS}$ | GND | | | | | | | |
| | | | | $DV_{CC}$ | $V_{CC}$ | | | | | | | |

(1) TB2 is not present on all device types.


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### ADC10_B

The ADC10_B module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and a conversion result buffer. A window comparator with a lower limit and an upper limit allows CPU-independent result monitoring with three window comparator interrupt flags.

### Comparator_D

The primary function of the Comparator_D module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

### CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

### Shared Reference (REF)

The reference module (REF) is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device.

### Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The S version of the EEM implemented on all devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

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## Peripheral File Map

**Table 17. Peripherals**

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE |
|---|---|---|
| Special Functions (see Table 18) | 0100h | 000h-01Fh |
| PMM (see Table 19) | 0120h | 000h-010h |
| FRAM Control (see Table 20) | 0140h | 000h-00Fh |
| CRC16 (see Table 21) | 0150h | 000h-007h |
| Watchdog (see Table 22) | 015Ch | 000h-001h |
| CS (see Table 23) | 0160h | 000h-00Fh |
| SYS (see Table 24) | 0180h | 000h-01Fh |
| Shared Reference (see Table 25) | 01B0h | 000h-001h |
| Port P1/P2 (see Table 26) | 0200h | 000h-01Fh |
| Port P3/P4 (see Table 27) | 0220h | 000h-01Fh |
| Port PJ (see Table 28) | 0320h | 000h-01Fh |
| TA0 (see Table 29) | 0340h | 000h-02Fh |
| TA1 (see Table 30) | 0380h | 000h-02Fh |
| TB0 (see Table 31) | 03C0h | 000h-02Fh |
| TB1 (see Table 32) | 0400h | 000h-02Fh |
| TB2 (see Table 33) | 0440h | 000h-02Fh |
| Real-Time Clock (RTC_B) (see Table 34) | 04A0h | 000h-01Fh |
| 32-Bit Hardware Multiplier (see Table 35) | 04C0h | 000h-02Fh |
| DMA General Control (see Table 36) | 0500h | 000h-00Fh |
| DMA Channel 0 (see Table 36) | 0510h | 000h-00Ah |
| DMA Channel 1 (see Table 36) | 0520h | 000h-00Ah |
| DMA Channel 2 (see Table 36) | 0530h | 000h-00Ah |
| MPU Control (see Table 37) | 05A0h | 000h-00Fh |
| eUSCI_A0 (see Table 38) | 05C0h | 000h-01Fh |
| eUSCI_A1 (see Table 39) | 05E0h | 000h-01Fh |
| eUSCI_B0 (see Table 40) | 0640h | 000h-02Fh |
| ADC10_B (see Table 41) | 0700h | 000h-03Fh |
| Comparator_D (see Table 42) | 08C0h | 000h-00Fh |


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**Table 18. Special Function Registers (Base Address: 0100h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

**Table 19. PMM Registers (Base Address: 0120h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| PMM Control 0 | PMMCTL0 | 00h |
| PMM interrupt flags | PMMIFG | 0Ah |
| PM5 Control 0 | PM5CTL0 | 10h |

**Table 20. FRAM Control Registers (Base Address: 0140h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| FRAM control 0 | FRCTLCTL0 | 00h |
| General control 0 | GCCTL0 | 04h |
| General control 1 | GCCTL1 | 06h |

**Table 21. CRC16 Registers (Base Address: 0150h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| CRC data input | CRC16DI | 00h |
| CRC data input reverse byte | CRCDIRB | 02h |
| CRC initialization and result | CRCINIRES | 04h |
| CRC result reverse byte | CRCRESR | 06h |

**Table 22. Watchdog Registers (Base Address: 015Ch)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Watchdog timer control | WDTCTL | 00h |

**Table 23. CS Registers (Base Address: 0160h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| CS control 0 | CSCTL0 | 00h |
| CS control 1 | CSCTL1 | 02h |
| CS control 2 | CSCTL2 | 04h |
| CS control 3 | CSCTL3 | 06h |
| CS control 4 | CSCTL4 | 08h |
| CS control 5 | CSCTL5 | 0Ah |
| CS control 6 | CSCTL6 | 0Ch |

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**Table 24. SYS Registers (Base Address: 0180h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| System control | SYSCTL | 00h |
| JTAG mailbox control | SYSJMBC | 06h |
| JTAG mailbox input 0 | SYSJMBI0 | 08h |
| JTAG mailbox input 1 | SYSJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYSJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYSJMBO1 | 0Eh |
| Bus Error vector generator | SYSBERRIV | 18h |
| User NMI vector generator | SYSUNIV | 1Ah |
| System NMI vector generator | SYSSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |

**Table 25. Shared Reference Registers (Base Address: 01B0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Shared reference control | REFCTL | 00h |

**Table 26. Port P1/P2 Registers (Base Address: 0200h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 pullup/pulldown enable | P1REN | 06h |
| Port P1 selection 0 | P1SEL0 | 0Ah |
| Port P1 selection 1 | P1SEL1 | 0Ch |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 complement selection | P1SELC | 16h |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 pullup/pulldown enable | P2REN | 07h |
| Port P2 selection 0 | P2SEL0 | 0Bh |
| Port P2 selection 1 | P2SEL1 | 0Dh |
| Port P2 complement selection | P2SELC | 17h |
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |


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**Table 27. Port P3/P4 Registers (Base Address: 0220h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P3 input | P3IN | 00h |
| Port P3 output | P3OUT | 02h |
| Port P3 direction | P3DIR | 04h |
| Port P3 pullup/pulldown enable | P3REN | 06h |
| Port P3 selection 0 | P3SEL0 | 0Ah |
| Port P3 selection 1 | P3SEL1 | 0Ch |
| Port P3 interrupt vector word | P3IV | 0Eh |
| Port P3 complement selection | P3SELC | 16h |
| Port P3 interrupt edge select | P3IES | 18h |
| Port P3 interrupt enable | P3IE | 1Ah |
| Port P3 interrupt flag | P3IFG | 1Ch |
| Port P4 input | P4IN | 01h |
| Port P4 output | P4OUT | 03h |
| Port P4 direction | P4DIR | 05h |
| Port P4 pullup/pulldown enable | P4REN | 07h |
| Port P4 selection 0 | P4SEL0 | 0Bh |
| Port P4 selection 1 | P4SEL1 | 0Dh |
| Port P4 complement selection | P4SELC | 17h |
| Port P4 interrupt vector word | P4IV | 1Eh |
| Port P4 interrupt edge select | P4IES | 19h |
| Port P4 interrupt enable | P4IE | 1Bh |
| Port P4 interrupt flag | P4IFG | 1Dh |

**Table 28. Port J Registers (Base Address: 0320h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port PJ input | PJIN | 00h |
| Port PJ output | PJOUT | 02h |
| Port PJ direction | PJDIR | 04h |
| Port PJ pullup/pulldown enable | PJREN | 06h |
| Port PJ selection 0 | PJSEL0 | 0Ah |
| Port PJ selection 1 | PJSEL1 | 0Ch |
| Port PJ complement selection | PJSELC | 16h |

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**Table 29. TA0 Registers (Base Address: 0340h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA0 control | TA0CTL | 00h |
| Capture/compare control 0 | TA0CCTL0 | 02h |
| Capture/compare control 1 | TA0CCTL1 | 04h |
| Capture/compare control 2 | TA0CCTL2 | 06h |
| TA0 counter register | TA0R | 10h |
| Capture/compare register 0 | TA0CCR0 | 12h |
| Capture/compare register 1 | TA0CCR1 | 14h |
| Capture/compare register 2 | TA0CCR2 | 16h |
| TA0 expansion register 0 | TA0EX0 | 20h |
| TA0 interrupt vector | TA0IV | 2Eh |

**Table 30. TA1 Registers (Base Address: 0380h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA1 control | TA1CTL | 00h |
| Capture/compare control 0 | TA1CCTL0 | 02h |
| Capture/compare control 1 | TA1CCTL1 | 04h |
| Capture/compare control 2 | TA1CCTL2 | 06h |
| TA1 counter register | TA1R | 10h |
| Capture/compare register 0 | TA1CCR0 | 12h |
| Capture/compare register 1 | TA1CCR1 | 14h |
| Capture/compare register 2 | TA1CCR2 | 16h |
| TA1 expansion register 0 | TA1EX0 | 20h |
| TA1 interrupt vector | TA1IV | 2Eh |

**Table 31. TB0 Registers (Base Address: 03C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TB0 control | TB0CTL | 00h |
| Capture/compare control 0 | TB0CCTL0 | 02h |
| Capture/compare control 1 | TB0CCTL1 | 04h |
| Capture/compare control 2 | TB0CCTL2 | 06h |
| TB0 register | TB0R | 10h |
| Capture/compare register 0 | TB0CCR0 | 12h |
| Capture/compare register 1 | TB0CCR1 | 14h |
| Capture/compare register 2 | TB0CCR2 | 16h |
| TB0 expansion register 0 | TB0EX0 | 20h |
| TB0 interrupt vector | TB0IV | 2Eh |


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**Table 32. TB1 Registers (Base Address: 0400h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TB1 control | TB1CTL | 00h |
| Capture/compare control 0 | TB1CCTL0 | 02h |
| Capture/compare control 1 | TB1CCTL1 | 04h |
| Capture/compare control 2 | TB1CCTL2 | 06h |
| TB1 register | TB1R | 10h |
| Capture/compare register 0 | TB1CCR0 | 12h |
| Capture/compare register 1 | TB1CCR1 | 14h |
| Capture/compare register 2 | TB1CCR2 | 16h |
| TB1 expansion register 0 | TB1EX0 | 20h |
| TB1 interrupt vector | TB1IV | 2Eh |

**Table 33. TB2 Registers (Base Address: 0440h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TB2 control | TB2CTL | 00h |
| Capture/compare control 0 | TB2CCTL0 | 02h |
| Capture/compare control 1 | TB2CCTL1 | 04h |
| Capture/compare control 2 | TB2CCTL2 | 06h |
| TB2 register | TB2R | 10h |
| Capture/compare register 0 | TB2CCR0 | 12h |
| Capture/compare register 1 | TB2CCR1 | 14h |
| Capture/compare register 2 | TB2CCR2 | 16h |
| TB2 expansion register 0 | TB2EX0 | 20h |
| TB2 interrupt vector | TB2IV | 2Eh |

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**Table 34. Real-Time Clock Registers (Base Address: 04A0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| RTC control 0 | RTCCTL0 | 00h |
| RTC control 1 | RTCCTL1 | 01h |
| RTC control 2 | RTCCTL2 | 02h |
| RTC control 3 | RTCCTL3 | 03h |
| RTC prescaler 0 control | RTCPS0CTL | 08h |
| RTC prescaler 1 control | RTCPS1CTL | 0Ah |
| RTC prescaler 0 | RTCPS0 | 0Ch |
| RTC prescaler 1 | RTCPS1 | 0Dh |
| RTC interrupt vector word | RTCIV | 0Eh |
| RTC seconds, RTC counter register 1 | RTCSEC, RTCNT1 | 10h |
| RTC minutes, RTC counter register 2 | RTCMIN, RTCNT2 | 11h |
| RTC hours, RTC counter register 3 | RTCHOUR, RTCNT3 | 12h |
| RTC day of week, RTC counter register 4 | RTCDOW, RTCNT4 | 13h |
| RTC days | RTCDAY | 14h |
| RTC month | RTCMON | 15h |
| RTC year low | RTCYEARL | 16h |
| RTC year high | RTCYEARH | 17h |
| RTC alarm minutes | RTCAMIN | 18h |
| RTC alarm hours | RTCAHOUR | 19h |
| RTC alarm day of week | RTCADOW | 1Ah |
| RTC alarm days | RTCADAY | 1Bh |
| Binary-to-BCD conversion register | BIN2BCD | 1Ch |
| BCD-to-binary conversion register | BCD2BIN | 1Eh |


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**Table 35. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| 16-bit operand 1 – multiply | MPY | 00h |
| 16-bit operand 1 – signed multiply | MPYS | 02h |
| 16-bit operand 1 – multiply accumulate | MAC | 04h |
| 16-bit operand 1 – signed multiply accumulate | MACS | 06h |
| 16-bit operand 2 | OP2 | 08h |
| 16 × 16 result low word | RESLO | 0Ah |
| 16 × 16 result high word | RESHI | 0Ch |
| 16 × 16 sum extension register | SUMEXT | 0Eh |
| 32-bit operand 1 – multiply low word | MPY32L | 10h |
| 32-bit operand 1 – multiply high word | MPY32H | 12h |
| 32-bit operand 1 – signed multiply low word | MPYS32L | 14h |
| 32-bit operand 1 – signed multiply high word | MPYS32H | 16h |
| 32-bit operand 1 – multiply accumulate low word | MAC32L | 18h |
| 32-bit operand 1 – multiply accumulate high word | MAC32H | 1Ah |
| 32-bit operand 1 – signed multiply accumulate low word | MACS32L | 1Ch |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H | 1Eh |
| 32-bit operand 2 – low word | OP2L | 20h |
| 32-bit operand 2 – high word | OP2H | 22h |
| 32 × 32 result 0 – least significant word | RES0 | 24h |
| 32 × 32 result 1 | RES1 | 26h |
| 32 × 32 result 2 | RES2 | 28h |
| 32 × 32 result 3 – most significant word | RES3 | 2Ah |
| MPY32 control register 0 | MPY32CTL0 | 2Ch |

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**Table 36. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| DMA channel 0 control | DMA0CTL | 00h |
| DMA channel 0 source address low | DMA0SAL | 02h |
| DMA channel 0 source address high | DMA0SAH | 04h |
| DMA channel 0 destination address low | DMA0DAL | 06h |
| DMA channel 0 destination address high | DMA0DAH | 08h |
| DMA channel 0 transfer size | DMA0SZ | 0Ah |
| DMA channel 1 control | DMA1CTL | 00h |
| DMA channel 1 source address low | DMA1SAL | 02h |
| DMA channel 1 source address high | DMA1SAH | 04h |
| DMA channel 1 destination address low | DMA1DAL | 06h |
| DMA channel 1 destination address high | DMA1DAH | 08h |
| DMA channel 1 transfer size | DMA1SZ | 0Ah |
| DMA channel 2 control | DMA2CTL | 00h |
| DMA channel 2 source address low | DMA2SAL | 02h |
| DMA channel 2 source address high | DMA2SAH | 04h |
| DMA channel 2 destination address low | DMA2DAL | 06h |
| DMA channel 2 destination address high | DMA2DAH | 08h |
| DMA channel 2 transfer size | DMA2SZ | 0Ah |
| DMA module control 0 | DMACTL0 | 00h |
| DMA module control 1 | DMACTL1 | 02h |
| DMA module control 2 | DMACTL2 | 04h |
| DMA module control 3 | DMACTL3 | 06h |
| DMA module control 4 | DMACTL4 | 08h |
| DMA interrupt vector | DMAIV | 0Ah |

**Table 37. MPU Control Registers (Base Address: 05A0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| MPU control 0 | MPUCTL0 | 00h |
| MPU control 1 | MPUCTL1 | 02h |
| MPU Segmentation Register | MPUSEG | 04h |
| MPU access management | MPUSAM | 06h |


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**Table 38. eUSCI_A0 Registers (Base Address: 05C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| eUSCI_A control word 0 | UCA0CTLW0 | 00h |
| eUSCI _A control word 1 | UCA0CTLW1 | 03h |
| eUSCI_A baud rate 0 | UCA0BR0 | 06h |
| eUSCI_A baud rate 1 | UCA0BR1 | 07h |
| eUSCI_A modulation control | UCA0MCTLW | 08h |
| eUSCI_A status | UCA0STAT | 0Ah |
| eUSCI_A receive buffer | UCA0RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA0TXBUF | 0Eh |
| eUSCI_A LIN control | UCA0ABCTL | 10h |
| eUSCI_A IrDA transmit control | UCA0IRTCTL | 12h |
| eUSCI_A IrDA receive control | UCA0IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA0IE | 1Ah |
| eUSCI_A interrupt flags | UCA0IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA0IV | 1Eh |

**Table 39. eUSCI_A1 Registers (Base Address: 05E0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| eUSCI_A control word 0 | UCA1CTLW0 | 00h |
| eUSCI _A control word 1 | UCA1CTLW1 | 03h |
| eUSCI_A baud rate 0 | UCA1BR0 | 06h |
| eUSCI_A baud rate 1 | UCA1BR1 | 07h |
| eUSCI_A modulation control | UCA1MCTLW | 08h |
| eUSCI_A status | UCA1STAT | 0Ah |
| eUSCI_A receive buffer | UCA1RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA1TXBUF | 0Eh |
| eUSCI_A LIN control | UCA1ABCTL | 10h |
| eUSCI_A IrDA transmit control | UCA1IRTCTL | 12h |
| eUSCI_A IrDA receive control | UCA1IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA1IE | 1Ah |
| eUSCI_A interrupt flags | UCA1IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA1IV | 1Eh |

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**Table 40. eUSCI_B0 Registers (Base Address: 0640h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| eUSCI_B control word 0 | UCB0CTLW0 | 00h |
| eUSCI_B control word 1 | UCB0CTLW1 | 02h |
| eUSCI_B bit rate 0 | UCB0BR0 | 06h |
| eUSCI_B bit rate 1 | UCB0BR1 | 07h |
| eUSCI_B status word | UCB0STATW | 08h |
| eUSCI_B byte counter threshold | UCB0TBCNT | 0Ah |
| eUSCI_B receive buffer | UCB0RXBUF | 0Ch |
| eUSCI_B transmit buffer | UCB0TXBUF | 0Eh |
| eUSCI_B I2C own address 0 | UCB0I2COA0 | 14h |
| eUSCI_B I2C own address 1 | UCB0I2COA1 | 16h |
| eUSCI_B I2C own address 2 | UCB0I2COA2 | 18h |
| eUSCI_B I2C own address 3 | UCB0I2COA3 | 1Ah |
| eUSCI_B received address | UCB0ADDRX | 1Ch |
| eUSCI_B address mask | UCB0ADDMASK | 1Eh |
| eUSCI I2C slave address | UCB0I2CSA | 20h |
| eUSCI interrupt enable | UCB0IE | 2Ah |
| eUSCI interrupt flags | UCB0IFG | 2Ch |
| eUSCI interrupt vector word | UCB0IV | 2Eh |

**Table 41. ADC10_B Registers (Base Address: 0700h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| ADC10_B Control register 0 | ADC10CTL0 | 00h |
| ADC10_B Control register 1 | ADC10CTL1 | 02h |
| ADC10_B Control register 2 | ADC10CTL2 | 04h |
| ADC10_B Window Comparator Low Threshold | ADC10LO | 06h |
| ADC10_B Window Comparator High Threshold | ADC10HI | 08h |
| ADC10_B Memory Control Register 0 | ADC10MCTL0 | 0Ah |
| ADC10_B Conversion Memory Register | ADC10MEM0 | 12h |
| ADC10_B Interrupt Enable | ADC10IE | 1Ah |
| ADC10_B Interrupt Flags | ADC10IGH | 1Ch |
| ADC10_B Interrupt Vector Word | ADC10IV | 1Eh |

**Table 42. Comparator_D Registers (Base Address: 08C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Comparator_D control register 0 | CDCTL0 | 00h |
| Comparator_D control register 1 | CDCTL1 | 02h |
| Comparator_D control register 2 | CDCTL2 | 04h |
| Comparator_D control register 3 | CDCTL3 | 06h |
| Comparator_D interrupt register | CDINT | 0Ch |
| Comparator_D interrupt vector word | CDIV | 0Eh |


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## Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted)

| | |
|---|---|
| Voltage applied at $V_{CC}$ to $V_{SS}$ | –0.3 V to 4.1 V |
| Voltage applied to any pin (excluding VCORE) (2) | –0.3 V to $V_{CC}$ + 0.3 V |
| Diode current at any device pin | ±2 mA |
| Storage temperature range, $T_{stg}$ (3) (4) (5) | -55°C to 125°C |
| Maximum junction temperature, $T_J$ | 95°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to $V_{SS}$. $V_{CORE}$ is for internal device use only. No external DC loading or voltage should be applied.
(3) Data retention on FRAM memory cannot be ensured when exceeding the specified maximum storage temperature, $T_{stg}$.
(4) For soldering during board manufacturing, it is required to follow the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.
(5) Programming of devices with user application code should only be performed after reflow or hand soldering. Factory programmed information, such as calibration values, are designed to withstand the temperatures reached in the current JEDEC J-STD-020 specification.

## Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage during program execution and FRAM programming (AVCC = DVCC) (1) | | 2.0 | | 3.6 | V |
| $V_{SS}$ | Supply voltage (AVSS = DVSS) | | | 0 | | V |
| $T_A$ | Operating free-air temperature | I version | -40 | | 85 | °C |
| $T_J$ | Operating junction temperature | I version | -40 | | 85 | °C |
| $C_{VCORE}$ | Required capacitor at VCORE | | | 470 | | nF |
| $C_{VCC}/C_{VCORE}$ | Capacitor ratio of VCC to VCORE | | 10 | | | |
| $f_{SYSTEM}$ | Processor frequency (maximum MCLK frequency) (2) | No FRAM wait states (3), 2 V ≤ $V_{CC}$ ≤ 3.6 V | 0 | | 8.0 | MHz |
| | | With FRAM wait states (3), NACCESS = {2}, NPRECHG = {1}, 2 V ≤ $V_{CC}$ ≤ 3.6 V | 0 | | 24.0 | |

(1) It is recommended to power AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.
(2) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
(3) When using manual wait state control, see the *MSP430FR57xx Family User's Guide* (SLAU272) for recommended settings for common system frequencies.

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## Electrical Characteristics

### Active Mode Supply Current Into $V_{CC}$ Excluding External Current

over recommended operating free-air temperature (unless otherwise noted) (1) (2) (3)

| PARAMETER | EXECUTION MEMORY | $V_{CC}$ | Frequency ($f_{MCLK}$ = $f_{SMCLK}$) (4) | | | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1 MHz | | 4 MHz | | 8 MHz | | 16 MHz (5) | | 20 MHz (5) | | 24 MHz (5) | | |
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM,\ FRAM_UNI}$ (6) | FRAM | 3 V | 0.27 | | 0.58 | | 1.0 | | 1.53 | | 1.9 | | 2.2 | | mA |
| $I_{AM,0\%}$ (7) | FRAM 0% cache hit ratio | 3 V | 0.42 | 0.73 | 1.2 | 1.6 | 2.2 | 2.8 | 2.3 | 2.9 | 2.8 | 3.6 | 3.45 | 4.3 | mA |
| $I_{AM,50\%}$ (7) (8) | FRAM 50% cache hit ratio | 3 V | 0.31 | | 0.73 | | 1.3 | | 1.75 | | 2.1 | | 2.5 | | |
| $I_{AM,66\%}$ (7) (8) | FRAM 66% cache hit ratio | 3 V | 0.27 | | 0.58 | | 1.0 | | 1.55 | | 1.9 | | 2.2 | | |
| $I_{AM,75\%}$ (7) (8) | FRAM 75% cache hit ratio | 3 V | 0.25 | | 0.5 | | 0.82 | | 1.3 | | 1.6 | | 1.8 | | |
| $I_{AM,100\%}$ (7) (8) | FRAM 100% cache hit ratio | 3 V | 0.2 | 0.43 | 0.3 | 0.55 | 0.42 | 0.8 | 0.73 | 1.15 | 0.88 | 1.3 | 1.0 | 1.5 | |
| $I_{AM,\ RAM}$ (8) (9) | RAM | 3 V | 0.2 | 0.4 | 0.35 | 0.55 | 0.55 | 0.75 | 1.0 | 1.25 | 1.20 | 1.45 | 1.45 | 1.75 | mA |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.
(3) Characterized with program executing typical data processing.
(4) At MCLK frequencies above 8 MHz, the FRAM requires wait states. When wait states are required, the effective MCLK frequency, $f_{MCLK,eff}$, decreases. The effective MCLK frequency is also dependent on the cache hit ratio. SMCLK is not affected by the number of wait states or the cache hit ratio. The following equation can be used to compute $f_{MCLK,eff}$:
$f_{MCLK,eff,MHZ} = f_{MCLK,MHZ} \times 1 / [\#\ of\ wait\ states \times ((1 - cache\ hit\ ratio\ percent/100)) + 1]$
(5) MSP430FR573x series only
(6) Program and data reside entirely in FRAM. No wait states enabled. DCORSEL = 0, DCOFSELx = 3 ($f_{DCO}$ = 8 MHz). MCLK = SMCLK.
(7) Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 25% ratio implies one of every four accesses is from cache, the remaining are FRAM accesses.
For 1, 4, and 8 MHz, DCORSEL = 0, DCOFSELx = 3 ($f_{DCO}$ = 8 MHz). MCLK = SMCLK. No wait states enabled.
For 16 MHz, DCORSEL = 1, DCOFSELx = 0 ($f_{DCO}$ = 16 MHz).MCLK = SMCLK. One wait state enabled.
For 20 MHz, DCORSEL = 1, DCOFSELx = 2 ($f_{DCO}$ = 20 MHz).MCLK = SMCLK. Three wait states enabled.
For 24 MHz, DCORSEL = 1, DCOFSELx = 3 ($f_{DCO}$ = 24 MHz).MCLK = SMCLK. Three wait states enabled.
(8) See Figure 1 for typical curves. Each characteristic equation shown in the graph is computed using the least squares method for best linear fit using the typical data shown in Active Mode Supply Current Into $V_{CC}$ Excluding External Current.
$f_{ACLK}$ = 32786 Hz, $f_{MCLK}$ = $f_{SMCLK}$ at specified frequency. No peripherals active.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF= SMCLKOFF = 0.
(9) All execution is from RAM.
For 1, 4, and 8 MHz, DCORSEL = 0, DCOFSELx = 3 ($f_{DCO}$ = 8 MHz). MCLK = SMCLK.
For 16 MHz, DCORSEL = 1, DCOFSELx = 0 ($f_{DCO}$ = 16 MHz). MCLK = SMCLK.
For 20 MHz, DCORSEL = 1, DCOFSELx = 2 ($f_{DCO}$ = 20 MHz). MCLK = SMCLK.
For 24 MHz, DCORSEL = 1, DCOFSELx = 3 ($f_{DCO}$ = 24 MHz). MCLK = SMCLK.


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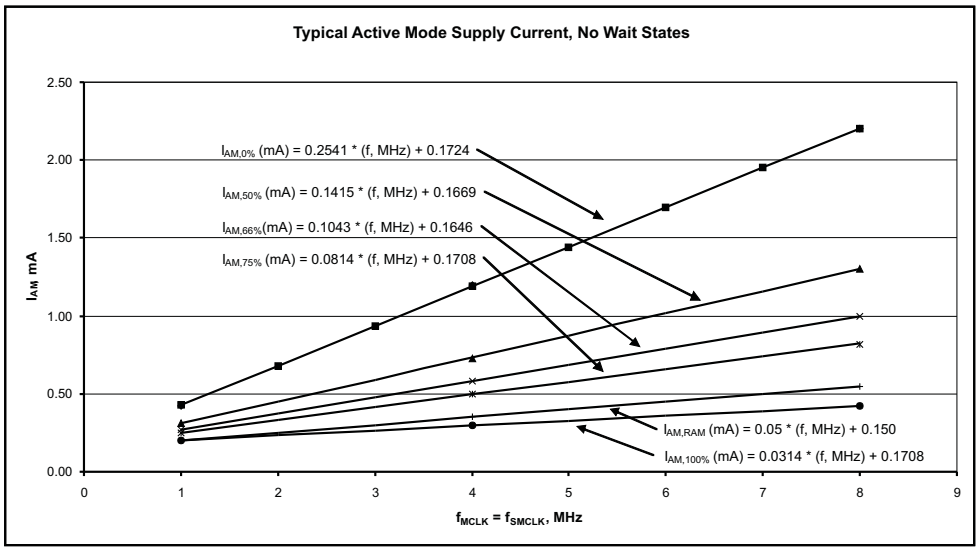



**Figure 1. Typical Active Mode Supply Currents, No Wait States**

## Low-Power Mode Supply Currents (Into $V_{CC}$) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1) (2)

| PARAMETER | | $V_{CC}$ | -40°C | | 25°C | | 60°C | | 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0,1MHz}$ | Low-power mode 0 (3) (4) | 2 V, 3 V | 166 | | 175 | | 190 | | 225 | | µA |
| $I_{LPM0,8MHz}$ | Low-power mode 0 (5) (4) | 2 V, 3 V | 170 | | 177 | 244 | 195 | | 225 | 360 | µA |
| $I_{LPM0,24MHz}$ | Low-power mode 0 (6) (4) | 2 V, 3 V | 274 | | 285 | 340 | 315 | | 340 | 455 | µA |
| $I_{LPM2}$ | Low-power mode 2 (7) (8) | 2 V, 3 V | 56 | | 61 | 80 | 75 | | 110 | 210 | µA |
| $I_{LPM3,XT1LF}$ | Low-power mode 3, crystal mode (9) (8) | 2 V, 3 V | 3.4 | | 6.4 | 15 | 18 | | 48 | 150 | µA |
| $I_{LPM3,VLO}$ | Low-power mode 3, VLO mode (10) (8) | 2 V, 3 V | 3.3 | | 6.3 | 15 | 18 | | 48 | 150 | µA |
| $I_{LPM4}$ | Low-power mode 4 (11) (8) | 2 V, 3 V | 2.9 | | 5.9 | 15 | 18 | | 48 | 150 | µA |
| $I_{LPM3.5}$ | Low-power mode 3.5 (12) | 2 V, 3 V | 1.3 | | 1.5 | 2.2 | 1.9 | | 2.8 | 5.0 | µA |
| $I_{LPM4.5}$ | Low-power mode 4.5 (13) | 2 V, 3 V | 0.3 | | 0.32 | 0.66 | 0.38 | | 0.57 | 2.55 | µA |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.
(3) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ = 1 MHz. DCORSEL = 0, DCOFSELx = 3 ($f_{DCO}$ = 8 MHz)
(4) Current for brownout, high-side supervisor ($SVS_H$) and low-side supervisor ($SVS_L$) included.
(5) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ = 8 MHz. DCORSEL = 0, DCOFSELx = 3 ($f_{DCO}$ = 8 MHz)
(6) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ = 24 MHz. DCORSEL = 1, DCOFSELx = 3 ($f_{DCO}$ = 24 MHz)
(7) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ = $f_{DCO}$ = 0 MHz, DCORSEL = 0, DCOFSELx = 3, DCO bias generator enabled.
(8) Current for brownout, high-side supervisor ($SVS_H$) included. Low-side supervisor disabled ($SVS_L$).
(9) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = $f_{SMCLK}$ = $f_{DCO}$ = 0 MHz
(10) Current for watchdog timer and RTC clocked by ACLK included. ACLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK}$ = $f_{VLO}$, $f_{MCLK}$ = $f_{SMCLK}$ = $f_{DCO}$ = 0 MHz
(11) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), $f_{DCO}$ = $f_{ACLK}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz
(12) Internal regulator disabled. No data retention. RTC active. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM3.5), $f_{DCO}$ = $f_{ACLK}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz
(13) Internal regulator disabled. No data retention. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5), $f_{DCO}$ = $f_{ACLK}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz


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## Schmitt-Trigger Inputs – General Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5, $\overline{RST}$/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | | 2 V | 0.80 | | 1.40 | V |
| | | | 3 V | 1.50 | | 2.10 | |
| $V_{IT-}$ | Negative-going input threshold voltage | | 2 V | 0.45 | | 1.10 | V |
| | | | 3 V | 0.75 | | 1.65 | |
| $V_{hys}$ | Input voltage hysteresis ($V_{IT+} - V_{IT-}$) | | 2 V | 0.25 | | 0.8 | V |
| | | | 3 V | 0.30 | | 1.0 | |
| $R_{Pull}$ | Pullup or pulldown resistor | For pullup: $V_{IN} = V_{SS}$<br>For pulldown: $V_{IN} = V_{CC}$ | | 20 | 35 | 50 | kΩ |
| $C_I$ | Input capacitance | $V_{IN} = V_{SS}$ or $V_{CC}$ | | | 5 | | pF |

## Inputs – Ports P1 and P2 (1) (P1.0 to P1.7, P2.0 to P2.7)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(int)}$ | External interrupt timing (2) | External trigger pulse duration to set interrupt flag | 2 V, 3 V | 20 | | ns |

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

## Leakage Current – General Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5, $\overline{RST}$/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{lkg(Px.x)}$ | High-impedance leakage current | (1) (2) | 2 V, 3 V | -50 | 50 | nA |

(1) The leakage current is measured with $V_{SS}$ or $V_{CC}$ applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

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## Outputs – General Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{(OHmax)}$ = –1 mA (1) | 2 V | $V_{CC}$ – 0.25 | $V_{CC}$ | V |
| | | $I_{(OHmax)}$ = –3 mA (2) | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –2 mA (1) | 3 V | $V_{CC}$ – 0.25 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –6 mA (2) | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| $V_{OL}$ | Low-level output voltage | $I_{(OLmax)}$ = 1 mA (1) | 2 V | $V_{SS}$ | $V_{SS}$ + 0.25 | V |
| | | $I_{(OLmax)}$ = 3 mA (2) | | $V_{SS}$ | $V_{SS}$ + 0.60 | |
| | | $I_{(OLmax)}$ = 2 mA (1) | 3 V | $V_{SS}$ | $V_{SS}$ + 0.25 | |
| | | $I_{(OLmax)}$ = 6 mA (2) | | $V_{SS}$ | $V_{SS}$ + 0.60 | |

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

## Output Frequency – General Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{Px.y}$ | Port output frequency (with load) | Px.y (1) (2) | 2 V | | 16 | MHz |
| | | | 3 V | | 24 | |
| $f_{Port_CLK}$ | Clock output frequency | ACLK, SMCLK, or MCLK at configured output port, $C_L$ = 20 pF, no DC loading (2) | 2 V | | 16 | MHz |
| | | | 3 V | | 24 | |

(1) A resistive divider with 2 × 1.6 kΩ between $V_{CC}$ and $V_{SS}$ is used as load. The output is connected to the center tap of the divider. $C_L$ = 20 pF is connected from the output to $V_{SS}$.
(2) The output voltage reaches at least 10% and 90% $V_{CC}$ at the specified toggle frequency.


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## Typical Characteristics – Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

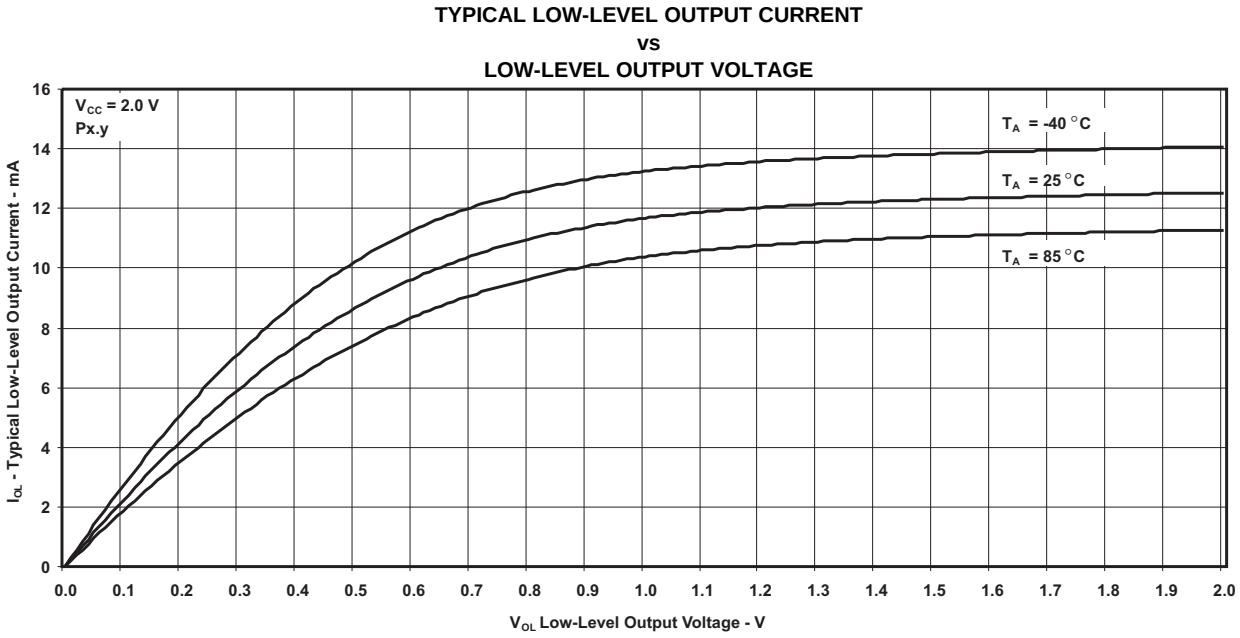



**Figure 2.**

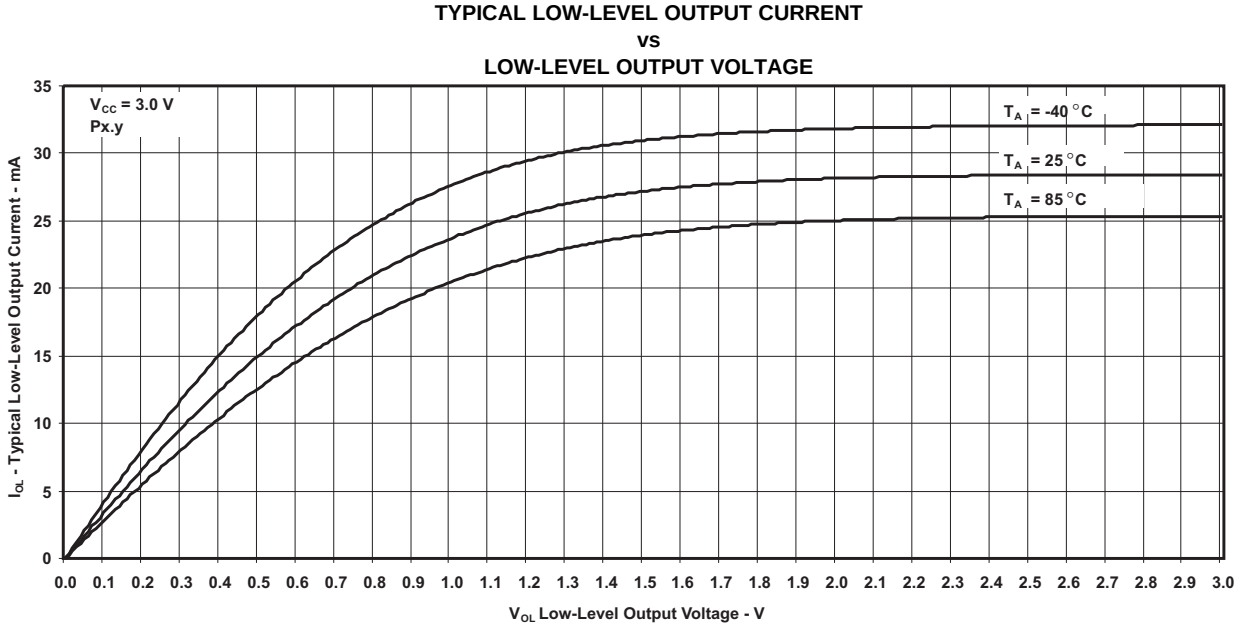



**Figure 3.**

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## Typical Characteristics – Outputs (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

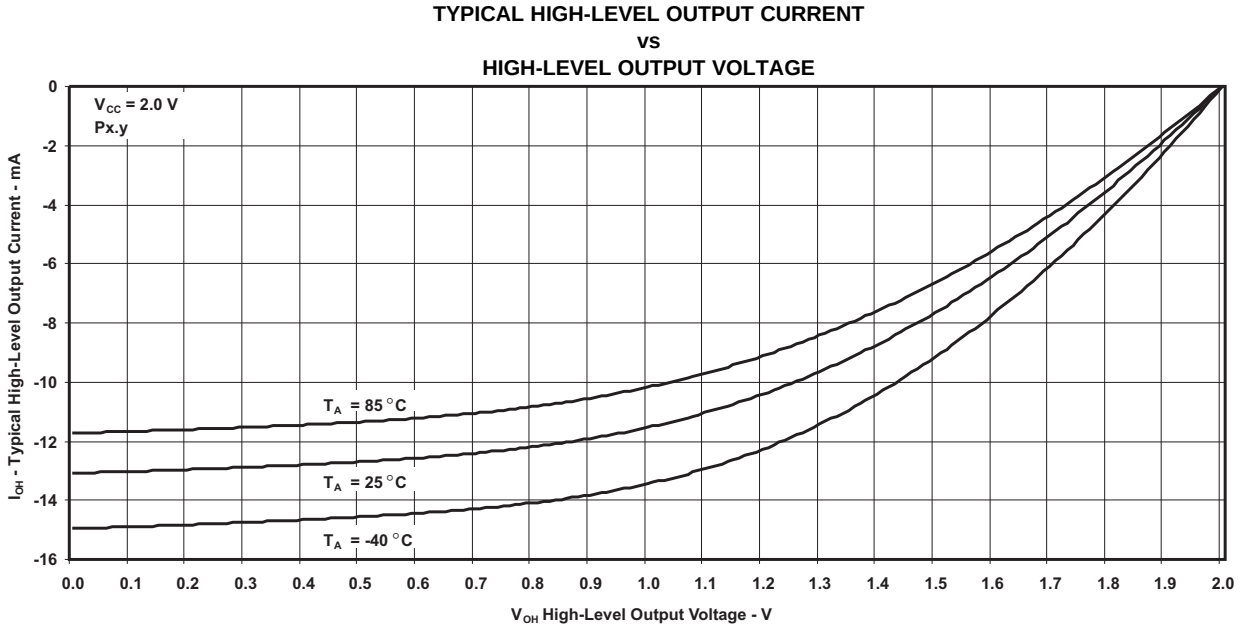



**Figure 4.**

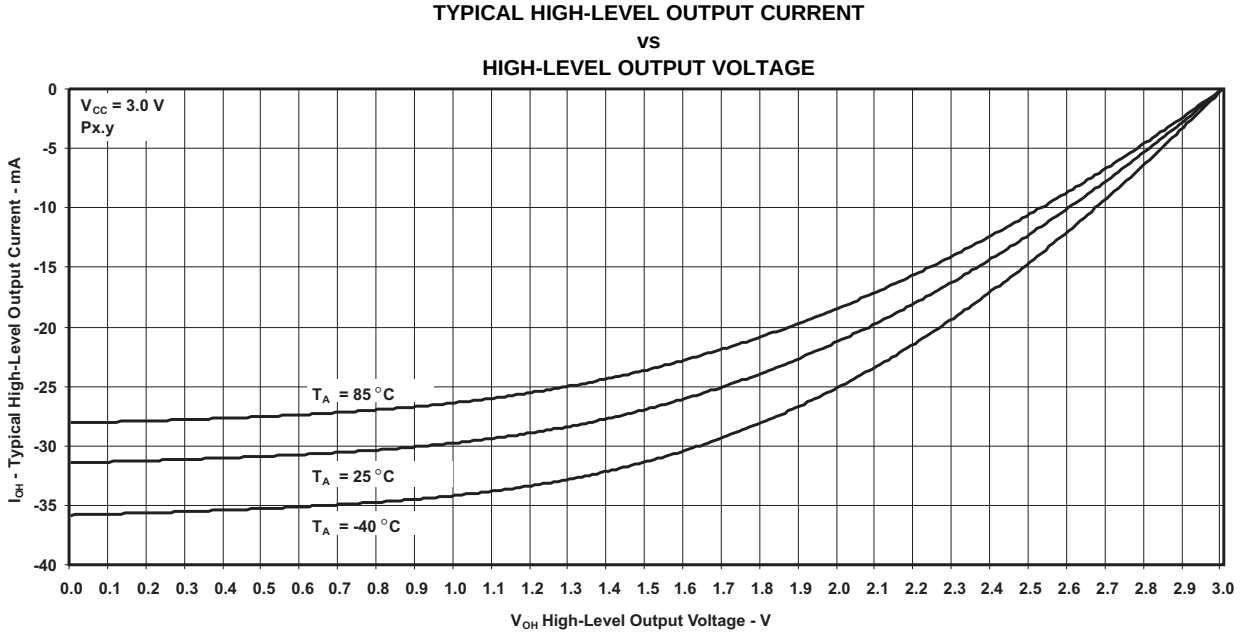



**Figure 5.**


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## Crystal Oscillator, XT1, Low-Frequency (LF) Mode (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $\Delta I_{VCC.LF}$ | Additional current consumption XT1 LF mode from lowest drive setting | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {1}, $C_{L,eff}$ = 9 pF, $T_A$ = 25°C, | 3 V | | 60 | | nA |
| | | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {2}, $T_A$ = 25°C, $C_{L,eff}$ = 9 pF | 3 V | | 90 | | |
| | | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {3}, $T_A$ = 25°C, $C_{L,eff}$ = 12 pF | 3 V | | 140 | | |
| $f_{XT1,LF0}$ | XT1 oscillator crystal frequency, LF mode | XTS = 0, XT1BYPASS = 0 | | | 32768 | | Hz |
| $f_{XT1,LF,SW}$ | XT1 oscillator logic-level square-wave input frequency, LF mode | XTS = 0, XT1BYPASS = 1 (2) (3) | | 10 | 32.768 | 50 | kHz |
| $OA_{LF}$ | Oscillation allowance for LF crystals (4) | XTS = 0, XT1BYPASS = 0, XT1DRIVE = {0}, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF | | | 210 | | kΩ |
| | | XTS = 0, XT1BYPASS = 0, XT1DRIVE = {3}, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF | | | 300 | | |
| | Duty cycle, LF mode | XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz | | 30 | | 70 | % |
| $f_{Fault,LF}$ | Oscillator fault frequency, LF mode (5) | XTS = 0 (6) | | 10 | | 10000 | Hz |
| $t_{START,LF}$ | Startup time, LF mode (7) | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {0}, $T_A$ = 25°C, $C_{L,eff}$ = 6 pF | 3 V | | 1000 | | ms |
| | | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE = {3}, $T_A$ = 25°C, $C_{L,eff}$ = 12 pF | | | 1000 | | |
| $C_{L,eff}$ | Integrated effective load capacitance, LF mode (8) (9) | XTS = 0 | | | 1 | | pF |

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
  (a) Keep the trace between the device and the crystal as short as possible.
  (b) Design a good ground plane around the oscillator pins.
  (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
  (f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.

(2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
  (a) For XT1DRIVE = {0}, $C_{L,eff} \le 6$ pF.
  (b) For XT1DRIVE = {1}, 6 pF $\le C_{L,eff} \le$ 9 pF.
  (c) For XT1DRIVE = {2}, 6 pF $\le C_{L,eff} \le$ 10 pF.
  (d) For XT1DRIVE = {3}, 6 pF $\le C_{L,eff} \le$ 12 pF.

(5) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(6) Measured with logic-level input frequency but also applies to operation with crystals.

(7) Includes startup counter of 4096 clock cycles.

(8) Requires external capacitors at both terminals.

(9) Values are specified by crystal manufacturers. Include parasitic bond and package capacitance (approximately 2 pF per pin). Recommended values supported are 6 pF, 9 pF, and 12 pF. Maximum shunt capacitance of 1.6 pF.

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## Crystal Oscillator, XT1, High-Frequency (HF) Mode (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{VCC,HF}$ | XT1 oscillator crystal current HF mode | $f_{OSC}$ = 4 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {0}, $T_A$ = 25°C, $C_{L,eff}$ = 16 pF | 3 V | | 175 | | µA |
| | | $f_{OSC}$ = 8 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {1}, $T_A$ = 25°C, $C_{L,eff}$ = 16 pF | | | 300 | | |
| | | $f_{OSC}$ = 16 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {2}, $T_A$ = 25°C, $C_{L,eff}$ = 16 pF | | | 350 | | |
| | | $f_{OSC}$ = 24 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVE = {3}, $T_A$ = 25°C, $C_{L,eff}$ = 16 pF | | | 550 | | |
| $f_{XT1,HF0}$ | XT1 oscillator crystal frequency, HF mode 0 | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {0} (2) | | 4 | | 6 | MHz |
| $f_{XT1,HF1}$ | XT1 oscillator crystal frequency, HF mode 1 | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {1} (3) | | 6 | | 10 | MHz |
| $f_{XT1,HF2}$ | XT1 oscillator crystal frequency, HF mode 2 | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {2} (3) | | 10 | | 16 | MHz |
| $f_{XT1,HF3}$ | XT1 oscillator crystal frequency, HF mode 3 | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {3} (3) | | 16 | | 24 | MHz |
| $f_{XT1,HF,SW}$ | XT1 oscillator logic-level square-wave input frequency, HF mode | XTS = 1, XT1BYPASS = 1 (4) (3) | | 1 | | 24 | MHz |
| $OA_{HF}$ | Oscillation allowance for HF crystals (5) | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {0}, $f_{XT1,HF}$ = 4 MHz, $C_{L,eff}$ = 16 pF | | | 450 | | Ω |
| | | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {1}, $f_{XT1,HF}$ = 8 MHz, $C_{L,eff}$ = 16 pF | | | 320 | | |
| | | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {2}, $f_{XT1,HF}$ = 16 MHz, $C_{L,eff}$ = 16 pF | | | 200 | | |
| | | XTS = 1, XT1BYPASS = 0, XT1DRIVE = {3}, $f_{XT1,HF}$ = 24 MHz, $C_{L,eff}$ = 16 pF | | | 200 | | |
| $t_{START,HF}$ | Startup time, HF mode (6) | $f_{OSC}$ = 4 MHz, XTS = 1, XT2BYPASS = 0, XT2DRIVE = {0}, $T_A$ = 25°C, $C_{L,eff}$ = 16 pF | 3 V | | 8 | | ms |
| | | $f_{OSC}$ = 24 MHz, XTS = 1, XT2BYPASS = 0, XT2DRIVE = {3}, $T_A$ = 25°C, $C_{L,eff}$ = 16 pF | | | 2 | | |

(1) To improve EMI on the XT1 oscillator the following guidelines should be observed.
(a) Keep the traces between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
(2) Maximum frequency of operation of the entire device cannot be exceeded.
(3) Maximum frequency of operation of the entire device cannot be exceeded.
(4) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
(6) Includes startup counter of 4096 clock cycles.


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## Crystal Oscillator, XT1, High-Frequency (HF) Mode (1) (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{L,eff}$ | Integrated effective load capacitance (7) (8) | XTS = 1 | | | 1 | | pF |
| | Duty cycle, HF mode | XTS = 1, Measured at ACLK, $f_{XT1,HF2}$ = 24 MHz | | 40 | 50 | 60 | % |
| $f_{Fault,HF}$ | Oscillator fault frequency, HF mode (9) | XTS = 1 (10) | | 145 | | 900 | kHz |

(7) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(8) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. Recommended values supported are 14 pF, 16 pF, and 18 pF. Maximum shunt capacitance of 7 pF.
(9) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
(10) Measured with logic-level input frequency but also applies to operation with crystals.

## Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{VLO}$ | VLO frequency | Measured at ACLK | 2 V to 3.6 V | 5 | 8.3 | 13 | kHz |
| $df_{VLO}/d_T$ | VLO frequency temperature drift | Measured at ACLK (1) | 2 V to 3.6 V | | 0.5 | | %/°C |
| $df_{VLO}/dV_{CC}$ | VLO frequency supply voltage drift | Measured at ACLK (2) | 2 V to 3.6 V | | 4 | | %/V |
| $f_{VLO,DC}$ | Duty cycle | Measured at ACLK | 2 V to 3.6 V | 40 | 50 | 60 | % |

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(2.0 to 3.6 V) – MIN(2.0 to 3.6 V)) / MIN(2.0 to 3.6 V) / (3.6 V – 2 V)

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## DCO Frequencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$, $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{DCO,LO}$ | DCO frequency low, trimmed | Measured at ACLK, DCORSEL = 0 | 2 V to 3.6 V -40°C to 85°C | | 5.37 | ±3.5% | MHz |
| | | | 2 V to 3.6 V 0°C to 50°C | | 5.37 | ±2.0% | |
| | | Measured at ACLK, DCORSEL = 1 (1) | 2 V to 3.6 V -40°C to 85°C | | 16.2 | ±3.5% | MHz |
| | | | 2 V to 3.6 V 0°C to 50°C | | 16.2 | ±2.0% | |
| $f_{DCO,MID}$ | DCO frequency mid, trimmed | Measured at ACLK, DCORSEL = 0 | 2 V to 3.6 V -40°C to 85°C | | 6.67 | ±3.5% | MHz |
| | | | 2 V to 3.6 V 0°C to 50°C | | 6.67 | ±2.0% | |
| | | Measured at ACLK, DCORSEL = 1 (1) | 2 V to 3.6 V -40°C to 85°C | | 20 | ±3.5% | MHz |
| | | | 2 V to 3.6 V 0°C to 50°C | | 20 | ±2.0% | |
| $f_{DCO,HI}$ | DCO frequency high, trimmed | Measured at ACLK, DCORSEL = 0 | 2 V to 3.6 V -40°C to 85°C | | 8 | ±3.5% | MHz |
| | | | 2 V to 3.6 V 0°C to 50°C | | 8 | ±2.0% | |
| | | Measured at ACLK, DCORSEL = 1 (1) | 2 V to 3.6 V -40°C to 85°C | | 23.8 | ±3.5% | MHz |
| | | | 2 V to 3.6 V 0°C to 50°C | | 23.8 | ±2.0% | |
| $f_{DCO,DC}$ | Duty cycle | Measured at ACLK, divide by 1, No external divide, all DCO settings | 2 V to 3.6 V -40°C to 85°C | 40 | 50 | 60 | % |

(1) MSP40FR573x devices only

## MODOSC

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{MODOSC}$ | Current consumption | Enabled | 2 V to 3.6 V | | 44 | 80 | µA |
| $f_{MODOSC}$ | MODOSC frequency | | 2 V to 3.6 V | 4.5 | 5.0 | 5.5 | MHz |
| $f_{MODOSC,DC}$ | Duty cycle | Measured at ACLK, divide by 1 | 2 V to 3.6 V | 40 | 50 | 60 | % |


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## PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CORE}$(AM) | Core voltage, active mode | 2 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.5 | | V |
| $V_{CORE}$(LPM) | Core voltage, low-current mode | 2 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.5 | | V |

## PMM, SVS, BOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{SVSH,AM}$ | $SVS_H$ current consumption, active mode | $V_{CC}$ = 3.6 V | | 5 | | µA |
| $I_{SVSH,LPM}$ | $SVS_H$ current consumption, low power modes | $V_{CC}$ = 3.6 V | | 0.8 | 1.5 | µA |
| $V_{SVSH-}$ | $SVS_H$ on voltage level, falling supply voltage | | 1.83 | 1.88 | 1.93 | V |
| $V_{SVSH+}$ | $SVS_H$ off voltage level, rising supply voltage | | 1.88 | 1.93 | 1.98 | V |
| $t_{PD,SVSH,\ AM}$ | $SVS_H$ propagation delay, active mode | $dV_{CC}/dt$ = 10 mV/µs | | 10 | | µs |
| $t_{PD,SVSH,\ LPM}$ | $SVS_H$ propagation delay, low power modes | $dV_{CC}/dt$ = 1 mV/µs | | 30 | | µs |
| $I_{SVSL}$ | $SVS_L$ current consumption | | | 0.3 | 0.5 | µA |

## Wake-Up from Low Power Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{WAKE-UP\ LPM0}$ | Wake-up time from LPM0 to active mode (1) | | 2 V, 3 V -40°C to 85°C | | 0.58 | 1 | µs |
| $t_{WAKE-UP\ LPM12}$ | Wake-up time from LPM1, LPM2 to active mode (1) | | 2 V, 3 V -40°C to 85°C | | 12 | 25 | µs |
| $t_{WAKE-UP\ LPM34}$ | Wake-up time from LPM3 or LPM4 to active mode (1) | | 2 V, 3 V -40°C to 85°C | | 78 | 120 | µs |
| $t_{WAKE-UP\ LPMx.5}$ | Wake-up time from LPM3.5 or LPM4.5 to active mode (1) | | 2 V, 3 V 0°C to 85°C | | 310 | 575 | µs |
| | | | 2 V, 3 V -40°C to 85°C | | 310 | 1100 | µs |
| $t_{WAKE-UP\ RESET}$ | Wake-up time from $\overline{RST}$ to active mode (2) | $V_{CC}$ stable | 2 V, 3 V -40°C to 85°C | | 170 | 210 | µs |
| $t_{WAKE-UP\ BOR}$ | Wake-up time from BOR or power-up to active mode | $dV_{CC}/dt$ = 2400 V/s | 2 V, 3 V -40°C to 85°C | | 1.6 | | ms |

(1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.
(2) The wake-up time is measured from the rising edge of the $\overline{RST}$ signal until the first instruction of the user program is executed.

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## Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{TA}$ | Timer_A input clock frequency | Internal: SMCLK, ACLK<br>External: TACLK<br>Duty cycle = 50% ± 10% | 2 V, 3 V | | | 8 | MHz |
| | | | | | | 24 (1) | |
| $t_{TA,cap}$ | Timer_A capture timing | All capture inputs, Minimum pulse duration required for capture | 2 V, 3 V | 20 | | | ns |

(1) MSP430FR573x devices only

## Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{TB}$ | Timer_B input clock frequency | Internal: SMCLK, ACLK<br>External: TBCLK<br>Duty cycle = 50% ± 10% | 2 V, 3 V | | | 8 | MHz |
| | | | | | | 24 (1) | |
| $t_{TB,cap}$ | Timer_B capture timing | All capture inputs, Minimum pulse duration required for capture | 2 V, 3 V | 20 | | | ns |

(1) MSP430FR573x devices only

## eUSCI (UART Mode) Recommended Operating Conditions

| PARAMETER | | CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK, ACLK<br>External: UCLK<br>Duty cycle = 50% ± 10% | | | | $f_{SYSTEM}$ | MHz |
| $f_{BITCLK}$ | BITCLK clock frequency (equals baud rate in MBaud) | | | | | 5 | MHz |

## eUSCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_t$ | UART receive deglitch time (1) | UCGLITx = 0 | 2 V, 3 V | 5 | 15 | 20 | ns |
| | | UCGLITx = 1 | | 20 | 45 | 60 | |
| | | UCGLITx = 2 | | 35 | 80 | 120 | |
| | | UCGLITx = 3 | | 50 | 110 | 180 | |

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.


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## eUSCI (SPI Master Mode) Recommended Operating Conditions

| PARAMETER | | CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK, ACLK<br>Duty cycle = 50% ± 10% | | | | $f_{SYSTEM}$ | MHz |

## eUSCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time, STE active to clock | UCSTEM = 0,<br>UCMODEx = 01 or 10 | 2 V, 3 V | 1 | | | UCxCLK cycles |
| | | UCSTEM = 1,<br>UCMODEx = 01 or 10 | 2 V, 3 V | 1 | | | |
| $t_{STE,LAG}$ | STE lag time, Last clock to STE inactive | UCSTEM = 0,<br>UCMODEx = 01 or 10 | 2 V, 3 V | 1 | | | UCxCLK cycles |
| | | UCSTEM = 1,<br>UCMODEx = 01 or 10 | 2 V, 3 V | 1 | | | |
| $t_{STE,ACC}$ | STE access time, STE active to SIMO data out | UCSTEM = 0,<br>UCMODEx = 01 or 10 | 2 V, 3 V | | | 55 | ns |
| | | UCSTEM = 1,<br>UCMODEx = 01 or 10 | 2 V, 3 V | | | 35 | |
| $t_{STE,DIS}$ | STE disable time, STE inactive to SIMO high impedance | UCSTEM = 0,<br>UCMODEx = 01 or 10 | 2 V, 3 V | | | 40 | ns |
| | | UCSTEM = 1,<br>UCMODEx = 01 or 10 | 2 V, 3 V | | | 30 | |
| $t_{SU,MI}$ | SOMI input data setup time | | 2 V | 35 | | | ns |
| | | | 3 V | 35 | | | |
| $t_{HD,MI}$ | SOMI input data hold time | | 2 V | 0 | | | ns |
| | | | 3 V | 0 | | | |
| $t_{VALID,MO}$ | SIMO output data valid time (2) | UCLK edge to SIMO valid,<br>$C_L$ = 20 pF | 2 V | | | 30 | ns |
| | | | 3 V | | | 30 | |
| $t_{HD,MO}$ | SIMO output data hold time (3) | $C_L$ = 20 pF | 2 V | 0 | | | ns |
| | | | 3 V | 0 | | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ see the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 6 and Figure 7.

(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 6 and Figure 7.

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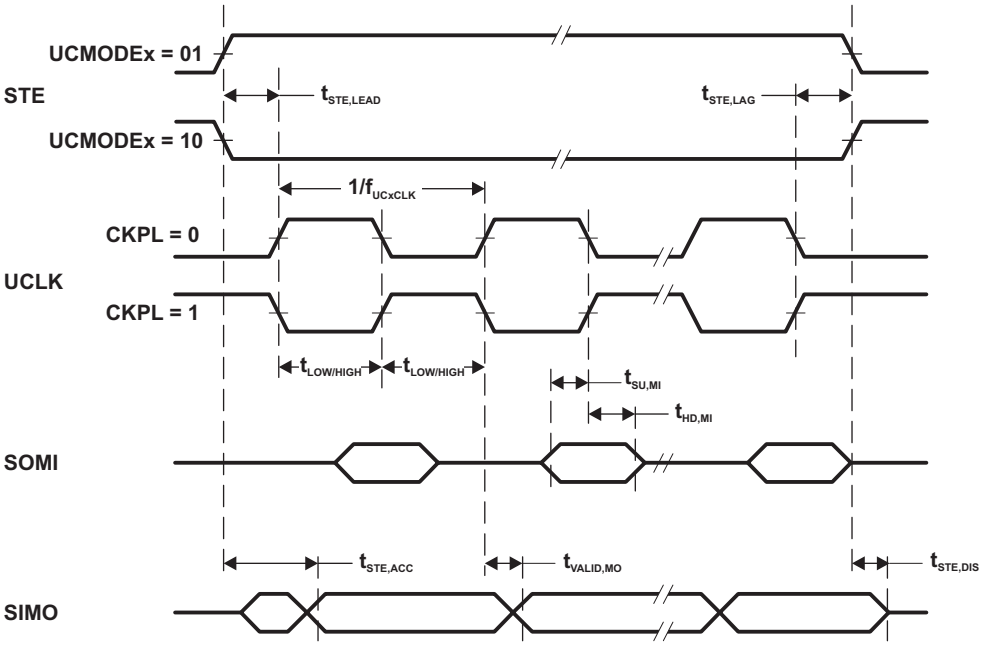



**Figure 6. SPI Master Mode, CKPH = 0**

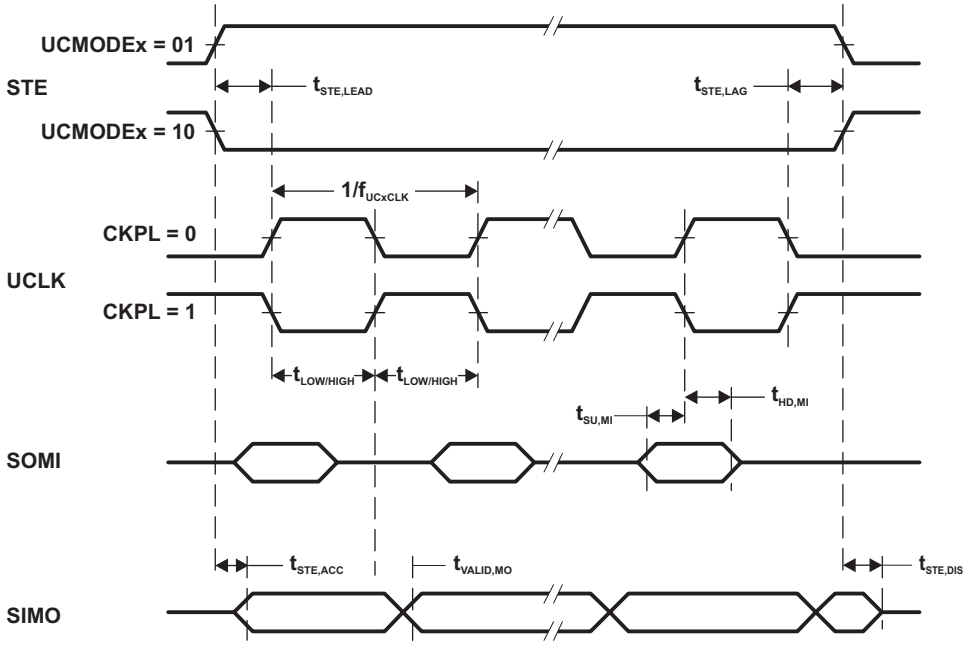



**Figure 7. SPI Master Mode, CKPH = 1**


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## eUSCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time, STE active to clock | | 2 V | 7 | | | ns |
| | | | 3 V | 7 | | | |
| $t_{STE,LAG}$ | STE lag time, Last clock to STE inactive | | 2 V | 0 | | | ns |
| | | | 3 V | 0 | | | |
| $t_{STE,ACC}$ | STE access time, STE active to SOMI data out | | 2 V | | | 65 | ns |
| | | | 3 V | | | 40 | |
| $t_{STE,DIS}$ | STE disable time, STE inactive to SOMI high impedance | | 2 V | | | 40 | ns |
| | | | 3 V | | | 35 | |
| $t_{SU,SI}$ | SIMO input data setup time | | 2 V | 2 | | | ns |
| | | | 3 V | 2 | | | |
| $t_{HD,SI}$ | SIMO input data hold time | | 2 V | 5 | | | ns |
| | | | 3 V | 5 | | | |
| $t_{VALID,SO}$ | SOMI output data valid time (2) | UCLK edge to SOMI valid, $C_L$ = 20 pF | 2 V | | | 30 | ns |
| | | | 3 V | | | 30 | |
| $t_{HD,SO}$ | SOMI output data hold time (3) | $C_L$ = 20 pF | 2 V | 4 | | | ns |
| | | | 3 V | 4 | | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$.
For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ see the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 8 and Figure 9.

(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 8 and Figure 9.

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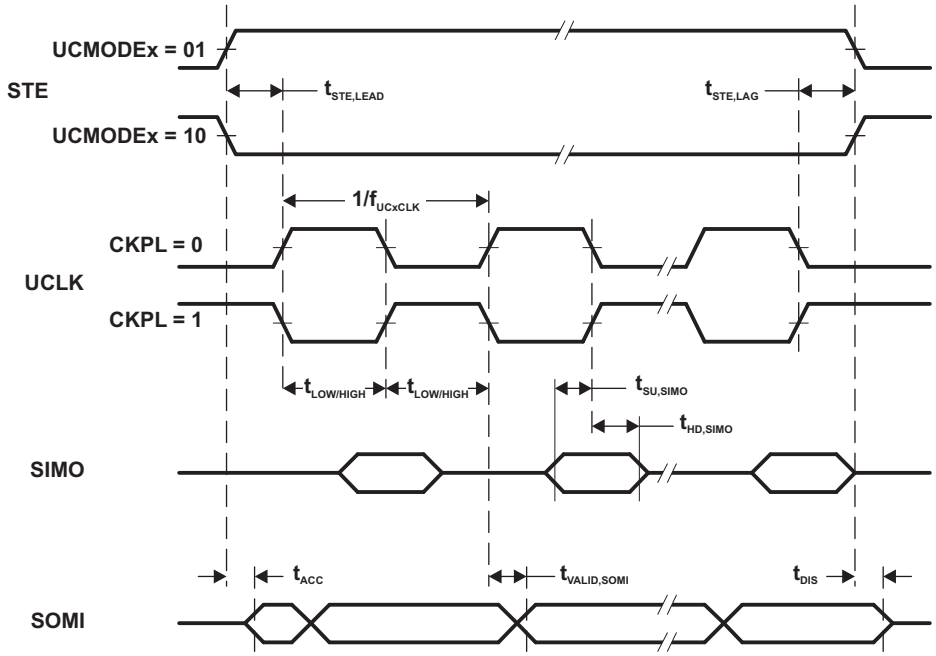



**Figure 8. SPI Slave Mode, CKPH = 0**

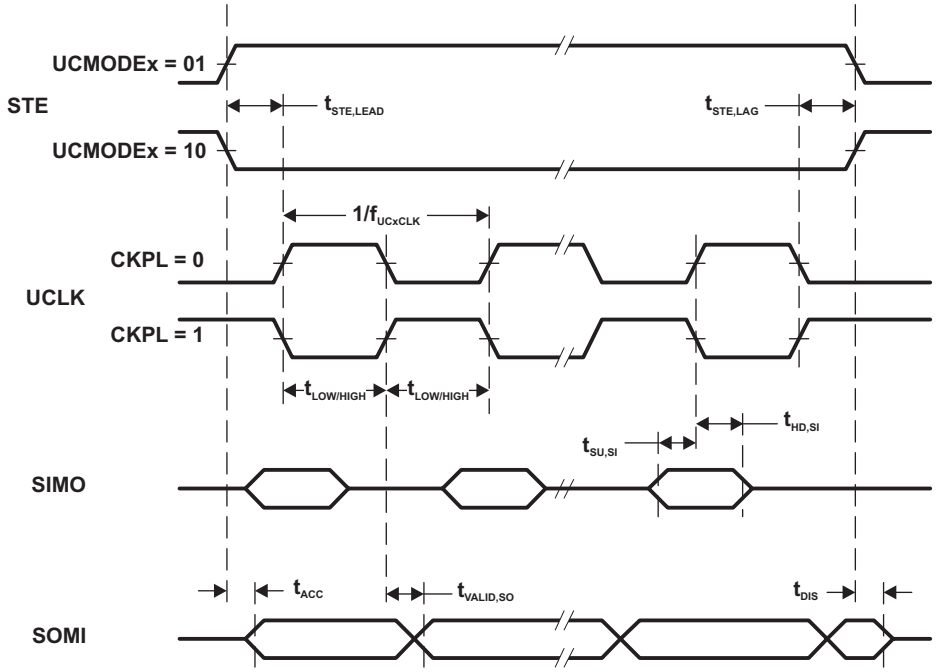



**Figure 9. SPI Slave Mode, CKPH = 1**


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## eUSCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 10)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK, ACLK<br>External: UCLK<br>Duty cycle = 50% ± 10% | | | | $f_{SYSTEM}$ | MHz |
| $f_{SCL}$ | SCL clock frequency | | 2 V, 3 V | 0 | | 400 | kHz |
| $t_{HD,STA}$ | Hold time (repeated) START | $f_{SCL}$ = 100 kHz | 2 V, 3 V | 4.0 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 0.6 | | | |
| $t_{SU,STA}$ | Setup time for a repeated START | $f_{SCL}$ = 100 kHz | 2 V, 3 V | 4.7 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 0.6 | | | |
| $t_{HD,DAT}$ | Data hold time | | 2 V, 3 V | 0 | | | ns |
| $t_{SU,DAT}$ | Data setup time | | 2 V, 3 V | 250 | | | ns |
| $t_{SU,STO}$ | Setup time for STOP | $f_{SCL}$ = 100 kHz | 2 V, 3 V | 4.0 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 0.6 | | | |
| $t_{SP}$ | Pulse duration of spikes suppressed by input filter | UCGLITx = 0 | 2 V, 3 V | 50 | | 600 | ns |
| | | UCGLITx = 1 | | 25 | | 300 | ns |
| | | UCGLITx = 2 | | 12.5 | | 150 | ns |
| | | UCGLITx = 3 | | 6.25 | | 75 | ns |
| $t_{TIMEOUT}$ | Clock low timeout | UCCLTOx = 1 | 2 V, 3 V | | 27 | | ms |
| | | UCCLTOx = 2 | | | 30 | | ms |
| | | UCCLTOx = 3 | | | 33 | | ms |

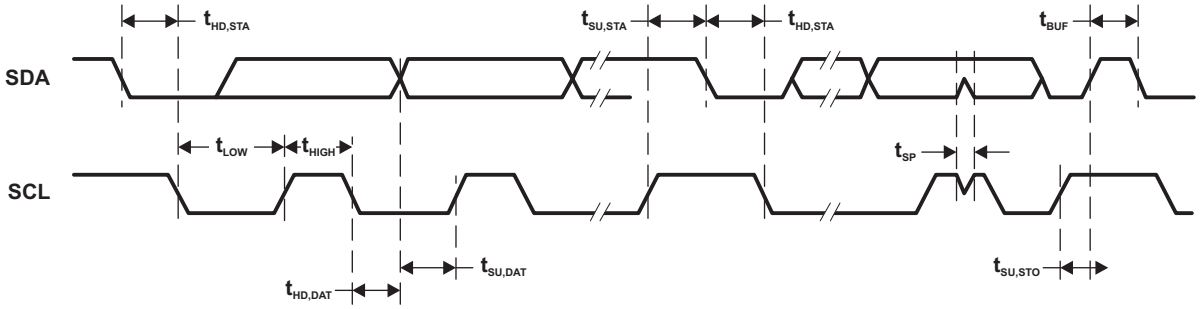



**Figure 10. I2C Mode Timing**

## 10-Bit ADC, Power Supply and Input Range Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | $AV_{CC}$ and $DV_{CC}$ are connected together, $AV_{SS}$ and $DV_{SS}$ are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V | | 2.0 | | 3.6 | V |
| $V_{(Ax)}$ | Analog input voltage range | All ADC10 pins | | 0 | | $AV_{CC}$ | V |
| $I_{ADC10_A}$ | Operating supply current into $AV_{CC}$ terminal, reference current not included | $f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0 | 2 V | | 90 | 140 | µA |
| | | | 3 V | | 100 | 160 | |
| $C_I$ | Input capacitance | Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad | 2.2 V | | 6 | 8 | pF |
| $R_I$ | Input MUX ON resistance | $AV_{CC} \geq 2$ V, 0 V ≤ $V_{Ax}$ ≤ $AV_{CC}$ | | | | 36 | kΩ |

## 10-Bit ADC, Timing Parameters

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{ADC10CLK}$ | | For specified performance of ADC10 linearity parameters | 2 V to 3.6 V | 0.45 | 5 | 5.5 | MHz |
| $f_{ADC10OSC}$ | Internal ADC10 oscillator (MODOSC) | ADC10DIV = 0, $f_{ADC10CLK} = f_{ADC10OSC}$ | 2 V to 3.6 V | 4.5 | 4.5 | 5.5 | MHz |
| $t_{CONVERT}$ | Conversion time | REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode, $f_{ADC10OSC}$ = 4.5 MHz to 5.5 MHz | 2 V to 3.6 V | 2.18 | | 2.67 | µs |
| | | External $f_{ADC10CLK}$ from ACLK, MCLK, or SMCLK, ADC10SSEL ≠ 0 | 2 V to 3.6 V | | (1) | | |
| $t_{ADC10ON}$ | Turn on settling time of the ADC | The error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB, Reference and input signal already settled | | | | 100 | ns |
| $t_{Sample}$ | Sampling time | $R_S$ = 1000 Ω, $R_I$ = 36000 Ω, $C_I$ = 3.5 pF, Approximately eight Tau (τ) are required to get an error of less than ±0.5 LSB | 2 V | 1.5 | | | µs |
| | | | 3 V | 2.0 | | | |

(1) 12 × ADC10DIV × $1/f_{ADC10CLK}$

## 10-Bit ADC, Linearity Parameters

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $E_I$ | Integral linearity error | 1.4 V ≤ ($V_{eREF+}$ – $V_{REF-}$/$V_{eREF-}$)min ≤ 1.6 V | 2 V to 3.6 V | -1.4 | | 1.4 | LSB |
| | | 1.6 V < ($V_{eREF+}$ – $V_{REF-}$/$V_{eREF-}$)min ≤ $V_{AVCC}$ | | -1.1 | | 1.1 | |
| $E_D$ | Differential linearity error | ($V_{eREF+}$ – $V_{REF-}$/$V_{eREF-}$)min ≤ ($V_{eREF+}$ – $V_{REF-}$/$V_{eREF-}$) | 2 V to 3.6 V | -1 | | 1 | LSB |
| $E_O$ | Offset error | ($V_{eREF+}$ – $V_{REF-}$/$V_{eREF-}$)min ≤ ($V_{eREF+}$ – $V_{REF-}$/$V_{eREF-}$) | 2 V to 3.6 V | -6.5 | | 6.5 | mV |
| $E_G$ | Gain error, external reference | ($V_{eREF+}$ – $V_{REF-}$/$V_{eREF-}$)min ≤ ($V_{eREF+}$ – $V_{REF-}$/$V_{eREF-}$) | 2 V to 3.6 V | -1.2 | | 1.2 | LSB |
| | Gain error, internal reference (1) | | | -4 | | 4 | % |
| $E_T$ | Total unadjusted error, external reference | ($V_{eREF+}$ – $V_{REF-}$/$V_{eREF-}$)min ≤ ($V_{eREF+}$ – $V_{REF-}$/$V_{eREF-}$) | 2 V to 3.6 V | -2 | | 2 | LSB |
| | Total unadjusted error, internal reference (1) | | | -4 | | 4 | % |

(1) Error is dominated by the internal reference.


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## REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{eREF+}$ | Positive external reference voltage input | $V_{eREF+} > V_{eREF-}$ (2) | | 1.4 | | $AV_{CC}$ | V |
| $V_{eREF-}$ | Negative external reference voltage input | $V_{eREF+} > V_{eREF-}$ (3) | | 0 | | 1.2 | V |
| ($V_{eREF+} – V_{REF-}/V_{eREF-}$) | Differential external reference voltage input | $V_{eREF+} > V_{eREF-}$ (4) | | 1.4 | | $AV_{CC}$ | V |
| $I_{VeREF+}$, $I_{VeREF-}$ | Static input current | 1.4 V ≤ $V_{eREF+}$ ≤ $V_{AVCC}$, $V_{eREF-}$ = 0 V, $f_{ADC10CLK}$ = 5 MHz, ADC10SHTx = 1h, Conversion rate 200 ksps | 2.2 V, 3 V | -6 | | 6 | µA |
| | | 1.4 V ≤ $V_{eREF+}$ ≤ $V_{AVCC}$, $V_{eREF-}$ = 0 V, $f_{ADC10CLK}$ = 5 MHz, ADC10SHTx = 8h, Conversion rate 20 ksps | 2.2 V, 3 V | -1 | | 1 | µA |
| $C_{VREF+}$, $C_{VREF-}$ | Capacitance at VREF+ or VREF- terminal (5) | | | 10 | | | µF |

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, $C_i$, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
(5) Two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_B. Also see the *MSP430FR57xx Family User's Guide* (SLAU272).

## REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REF+}$ | Positive built-in reference voltage output | REFVSEL = {2} for 2.5 V, REFON = 1 | 3 V | 2.4 | 2.5 | 2.6 | V |
| | | REFVSEL = {1} for 2 V, REFON = 1 | 3 V | 1.92 | 2.0 | 2.08 | |
| | | REFVSEL = {0} for 1.5 V, REFON = 1 | 3 V | 1.44 | 1.5 | 1.56 | |
| $AV_{CC(min)}$ | $AV_{CC}$ minimum voltage, Positive built-in reference active | REFVSEL = {0} for 1.5 V | | 2.0 | | | V |
| | | REFVSEL = {1} for 2 V | | 2.2 | | | |
| | | REFVSEL = {2} for 2.5 V | | 2.7 | | | |
| $I_{REF+}$ | Operating supply current into AVCC terminal (1) | $f_{ADC10CLK}$ = 5 MHz, REFON = 1, REFBURST = 0 | 3 V | | 33 | 45 | µA |
| $T_{REF+}$ | Temperature coefficient of built-in reference | REFVSEL = {0, 1, 2}, REFON = 1 | | | ±35 | | ppm/°C |
| PSRR_DC | Power supply rejection ratio (DC) | $AV_{CC}$ = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, $T_A$ = 25°C, REFON = 1, REFVSEL = {0} for 1.5 V | | | 1600 | | µV/V |
| | | $AV_{CC}$ = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, $T_A$ = 25°C, REFON = 1, REFVSEL = {1} for 2 V | | | 1900 | | |
| | | $AV_{CC}$ = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, $T_A$ = 25°C, REFON = 1, REFVSEL = {2} for 2.5 V | | | 3600 | | |
| $t_{SETTLE}$ | Settling time of reference voltage (2) | $AV_{CC}$ = $AV_{CC\ (min)}$ - $AV_{CC(max)}$, REFVSEL = {0, 1, 2}, REFON = 0 → 1 | | | 30 | | µs |

(1) The internal reference current is supplied by terminal AVCC. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.
(2) The condition is that the error in a conversion started after $t_{REFON}$ is less than ±0.5 LSB.

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## REF, Temperature Sensor and Built-In $V_{MID}$

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{SENSOR}$ | See (1) | ADC10ON = 1, INCH = 0Ah, $T_A$ = 0°C | 2 V, 3 V | | 790 | | mV |
| $TC_{SENSOR}$ | | ADC10ON = 1, INCH = 0Ah | 2 V, 3 V | | 2.55 | | mV/°C |
| $t_{SENSOR(sample)}$ | Sample time required if channel 10 is selected (2) | ADC10ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB | 2 V | 30 | | | µs |
| | | | 3 V | 30 | | | |
| $V_{MID}$ | $AV_{CC}$ divider at channel 11 | ADC10ON = 1, INCH = 0Bh, $V_{MID}$ is ~0.5 × $V_{AVCC}$ | 2 V | 0.97 | 1.0 | 1.03 | V |
| | | | 3 V | 1.46 | 1.5 | 1.54 | |
| $t_{VMID(sample)}$ | Sample time required if channel 11 is selected (3) | ADC10ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB | 2 V, 3 V | 1000 | | | ns |

(1) The temperature sensor offset can vary significantly. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor.
(2) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(3) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

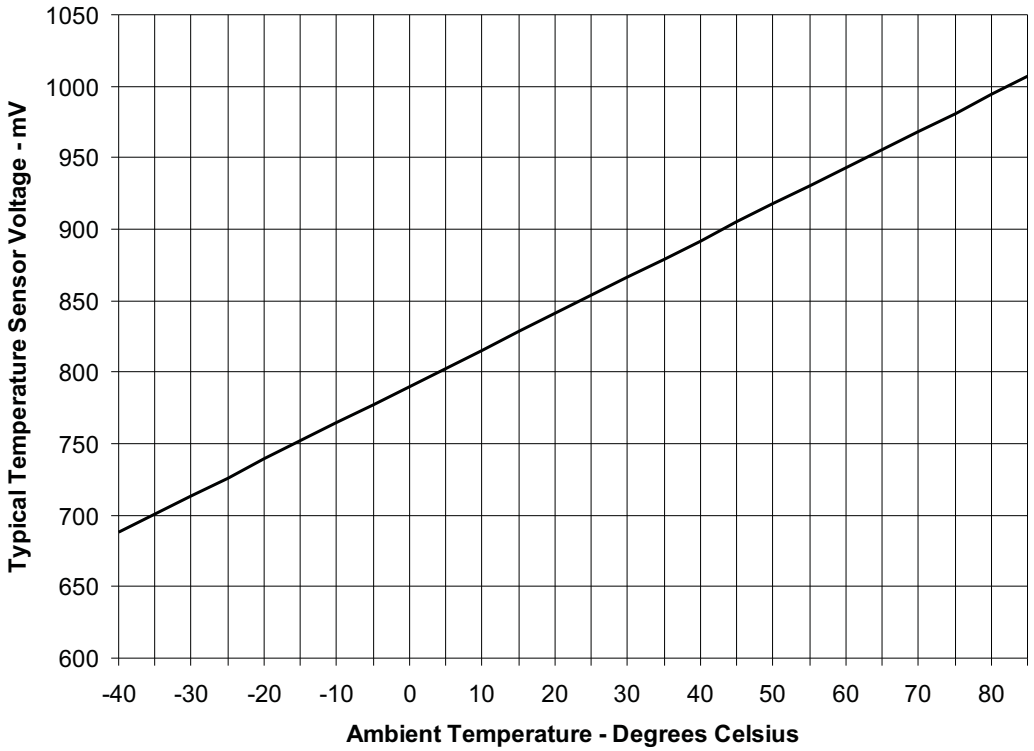



**Figure 11. Typical Temperature Sensor Voltage**


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## Comparator_D

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$ | Propagation delay, AVCC = 2 V to 3.6 V | Overdrive = 10 mV, VIN- = (VIN+ – 400 mV) to (VIN+ + 10 mV) | 50 | 100 | 200 | ns |
| | | Overdrive = 100 mV, VIN- = (VIN+ – 400 mV) to (VIN+ + 100 mV) | | 80 | | ns |
| | | Overdrive = 250 mV, (VIN+ – 400 mV) to (VIN+ + 250 mV) | | 50 | | ns |
| $t_{filter}$ | Filter timer added to the propagation delay of the comparator | CDF = 1, CDFDLY = 00 | 0.3 | 0.5 | 0.9 | µs |
| | | CDF = 1, CDFDLY = 01 | 0.5 | 0.9 | 1.5 | µs |
| | | CDF = 1, CDFDLY = 10 | 0.9 | 1.6 | 2.8 | µs |
| | | CDF = 1, CDFDLY = 11 | 1.6 | 3.0 | 5.5 | µs |
| $V_{offset}$ | Input offset | AVCC = 2 V to 3.6 V | -20 | | 20 | mV |
| $V_{ic}$ | Common mode input range | AVCC = 2 V to 3.6 V | 0 | | AVCC - 1 | V |
| $I_{comp(AVCC)}$ | Comparator only | CDON = 1, AVCC = 2 V to 3.6 V | | 29 | 34 | µA |
| $I_{ref(AVCC)}$ | Reference buffer and R-ladder | CDREFLx = 01, AVCC = 2 V to 3.6 V | | 20 | 24 | µA |
| $t_{enable,comp}$ | Comparator enable time | CDON = 0 to CDON = 1, AVCC = 2 V to 3.6 V | | 1.1 | 2.0 | µs |
| $t_{enable,rladder}$ | Resistor ladder enable time | CDON = 0 to CDON = 1, AVCC = 2 V to 3.6 V | | 1.1 | 2.0 | µs |
| $V_{CB_REF}$ | Reference voltage for a tap | VIN = voltage input to the R-ladder, n = 0 to 31 | VIN × (n + 0.5) / 32 | VIN × (n + 1) / 32 | VIN × (n + 1.5) / 32 | V |

## FRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $DV_{CC(WRITE)}$ | Write supply voltage | | 2.0 | | 3.6 | V |
| $t_{WRITE}$ | Word or byte write time | | | | 120 | ns |
| $t_{ACCESS}$ | Read access time (1) | | | | 60 | ns |
| $t_{PRECHARGE}$ | Precharge time (1) | | | | 60 | ns |
| $t_{CYCLE}$ | Cycle time, read or write operation (1) | | 120 | | | ns |
| | Read and write endurance | | $10^{15}$ | | | cycles |
| $t_{Retention}$ | Data retention duration | $T_J$ = 25°C | 100 | | | years |
| | | $T_J$ = 70°C | 40 | | | |
| | | $T_J$ = 85°C | 10 | | | |

(1) When using manual wait state control, see the *MSP430FR57xx Family User's Guide* (SLAU272) for recommended settings for common system frequencies.

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## JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SBW}$ | Spy-Bi-Wire input frequency | 2 V, 3 V | 0 | | 20 | MHz |
| $t_{SBW,Low}$ | Spy-Bi-Wire low clock pulse duration | 2 V, 3 V | 0.025 | | 15 | µs |
| $t_{SBW,\ En}$ | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1) | 2 V, 3 V | | | 1 | µs |
| $t_{SBW,Rst}$ | Spy-Bi-Wire return to normal operation time | | 19 | | 35 | µs |
| $f_{TCK}$ | TCK input frequency, 4-wire JTAG (2) | 2 V | 0 | | 5 | MHz |
| | | 3 V | 0 | | 10 | MHz |
| $R_{internal}$ | Internal pulldown resistance on TEST | 2 V, 3 V | 20 | 35 | 50 | kΩ |

(1) Tools accessing the Spy-Bi-Wire interface must wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) $f_{TCK}$ may be restricted to meet the timing requirements of the module selected.


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## INPUT/OUTPUT SCHEMATICS

### Port P1, P1.0 to P1.2, Input/Output With Schmitt Trigger

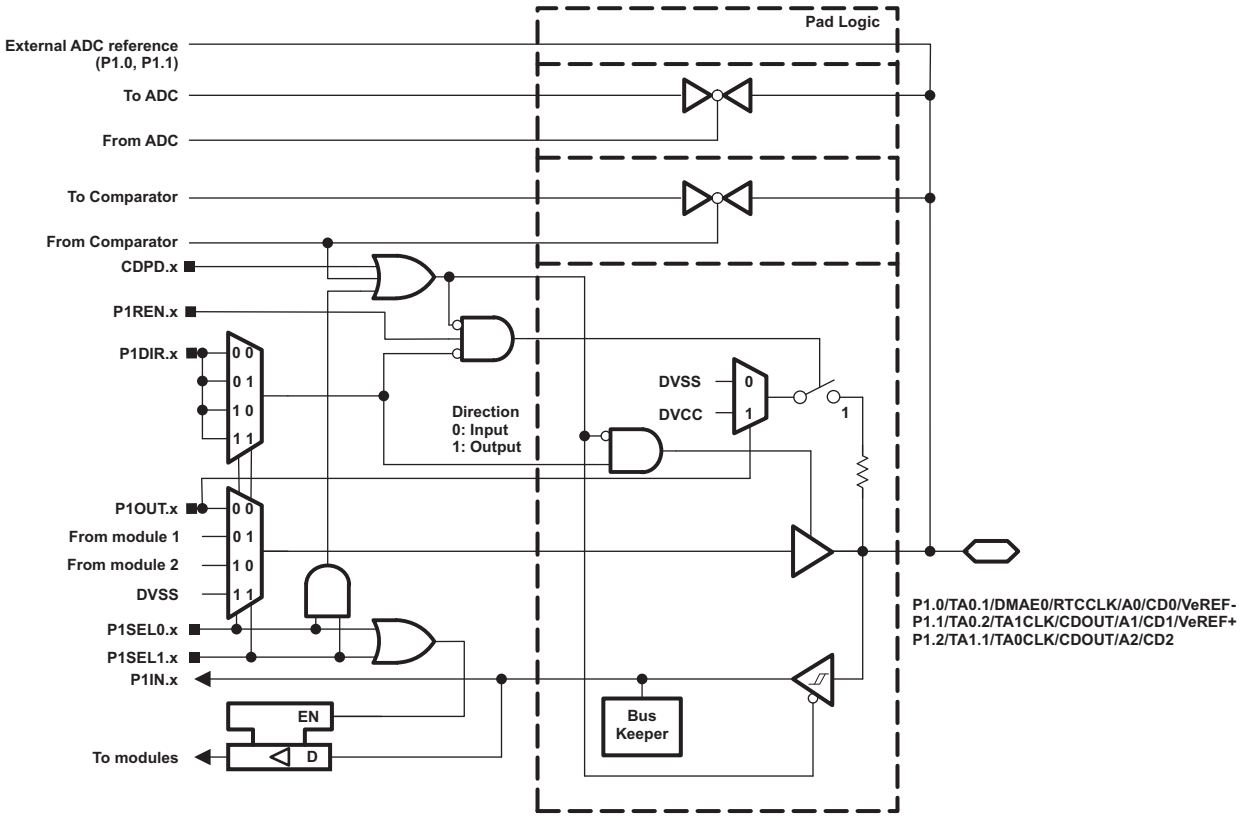


**Table 43. Port P1 (P1.0 to P1.2) Pin Functions**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x |
| P1.0/TA0.1/DMAE0/RTCCLK/A0/CD0/VeREF- (1) | 0 | P1.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA0.CCI1A | 0 | 0 | 1 |
| | | TA0.1 | 1 | | |
| | | DMAE0 | 0 | 1 | 0 |
| | | RTCCLK | 1 | | |
| | | A0 (2) (3)<br>CD0 (2) (4)<br>VeREF- (2) (3) | X | 1 | 1 |
| P1.1/TA0.2/TA1CLK/CDOUT/A1/CD1/VeREF+ | 1 | P1.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA0.CCI2A | 0 | 0 | 1 |
| | | TA0.2 | 1 | | |
| | | TA1CLK | 0 | 1 | 0 |
| | | CDOUT | 1 | | |
| | | A1 (2) (3)<br>CD1 (2) (4)<br>VeREF+ (2) (3) | X | 1 | 1 |
| P1.2/TA1.1/TA0CLK/CDOUT/A2/CD2 | 2 | P1.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA1.CCI1A | 0 | 0 | 1 |
| | | TA1.1 | 1 | | |
| | | TA0CLK | 0 | 1 | 0 |
| | | CDOUT | 1 | | |
| | | A2 (2) (3)<br>CD2 (2) (4) | X | 1 | 1 |

(1) This pin is tied to AVSS for YFF package types. All functions are therefore tied to ground at the pin.
(2) Setting P1SEL1.x and P1SEL0.x disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Not available on all devices and package types.
(4) Setting the CDPD.x bit of the comparator disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CDx input pin to the comparator multiplexer with the CDx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CDPD.x bit.


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## Port P1, P1.3 to P1.5, Input/Output With Schmitt Trigger

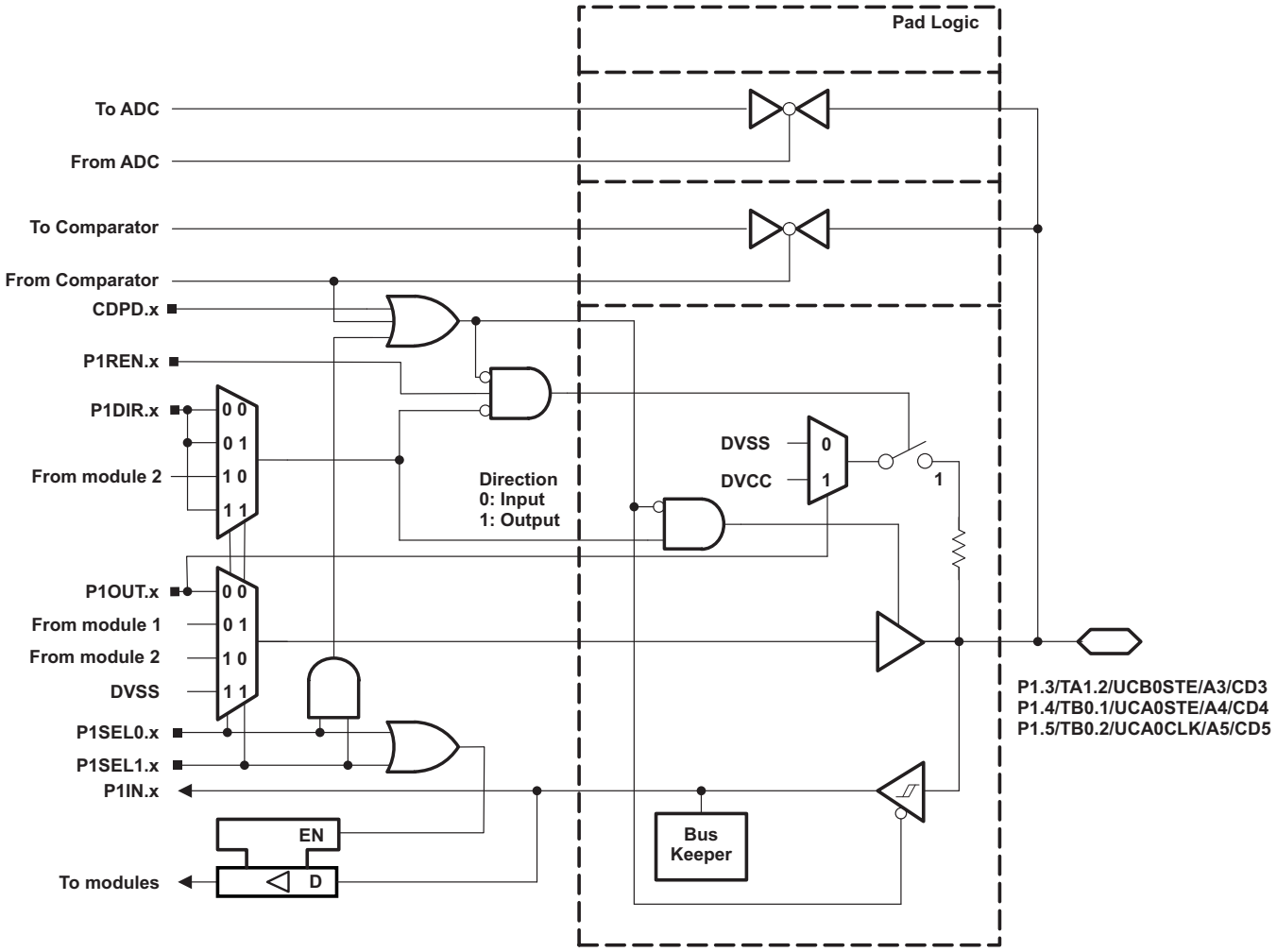


**Table 44. Port P1 (P1.3 to P1.5) Pin Functions**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x |
| P1.3/TA1.2/UCB0STE/A3/CD3 | 3 | P1.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA1.CCI2A | 0 | 0 | 1 |
| | | TA1.2 | 1 | | |
| | | UCB0STE | X (1) | 1 | 0 |
| | | A3 (2) (3)<br>CD3 (2) (4) | X | 1 | 1 |
| P1.4/TB0.1/UCA0STE/A4/CD4 | 4 | P1.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB0.CCI1A | 0 | 0 | 1 |
| | | TB0.1 | 1 | | |
| | | UCA0STE | X (5) | 1 | 0 |
| | | A4 (2) (3)<br>CD4 (2) (4) | X | 1 | 1 |
| P1.5/TB0.2/UCA0CLK/A5/CD5 | 5 | P1.5(I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB0.CCI2A | 0 | 0 | 1 |
| | | TB0.2 | 1 | | |
| | | UCA0CLK | X (5) | 1 | 0 |
| | | A5 (2) (3)<br>CD5 (2) (4) | X | 1 | 1 |

(1) Direction controlled by eUSCI_B0 module.
(2) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Not available on all devices and package types.
(4) Setting the CDPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CDx input pin to the comparator multiplexer with the CDx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CDPD.x bit
(5) Direction controlled by eUSCI_A0 module.


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## Port P1, P1.6 to P1.7, Input/Output With Schmitt Trigger

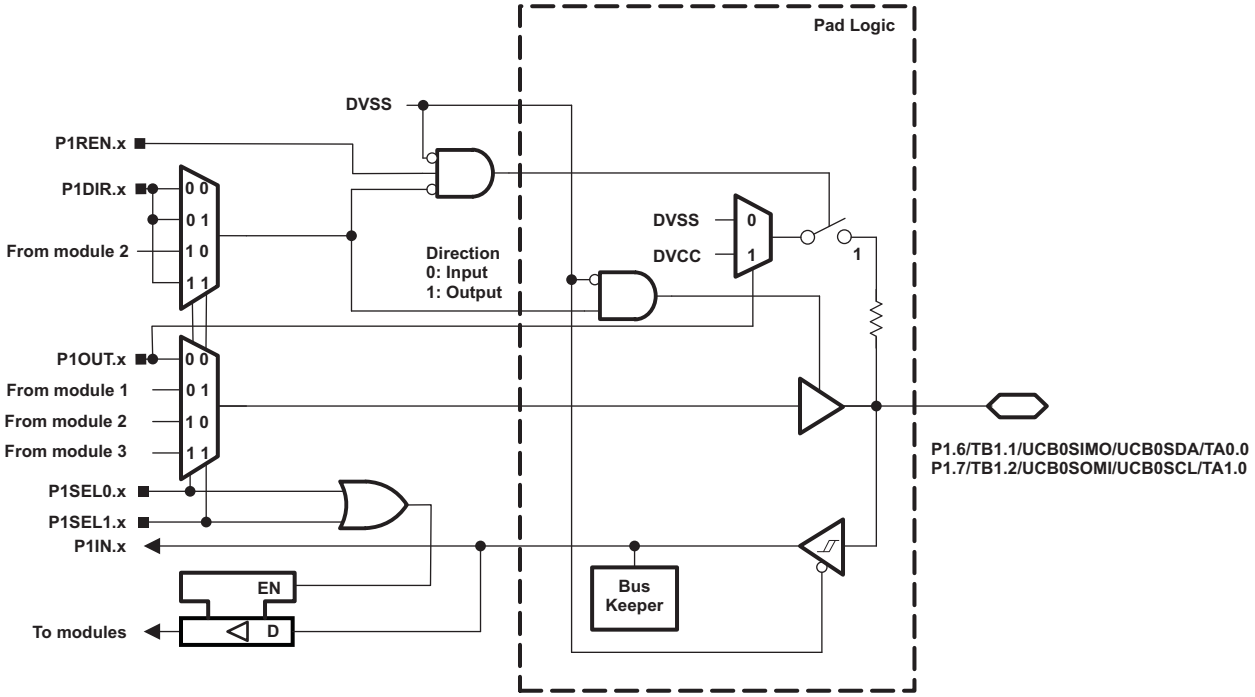



**Table 45. Port P1 (P1.6 to P1.7) Pin Functions**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x |
| P1.6/TB1.1/UCB0SIMO/UCB0SDA/TA0.0 | 6 | P1.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB1.CCI1A (1) | 0 | 0 | 1 |
| | | TB1.1 (1) | 1 | | |
| | | UCB0SIMO/UCB0SDA | X (2) | 1 | 0 |
| | | TA0.CCI0A | 0 | 1 | 1 |
| | | TA0.0 | 1 | | |
| P1.7/TB1.2/UCB0SOMI/UCB0SCL/TA1.0 | 7 | P1.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB1.CCI2A (1) | 0 | 0 | 1 |
| | | TB1.2 (1) | 1 | | |
| | | UCB0SOMI/UCB0SCL | X (3) | 1 | 0 |
| | | TA1.CCI0A | 0 | 1 | 1 |
| | | TA1.0 | 1 | | |

(1) Not available on all devices and package types.
(2) Direction controlled by eUSCI_B0 module.
(3) Direction controlled by eUSCI_A0 module.

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## Port P2, P2.0 to P2.2, Input/Output With Schmitt Trigger

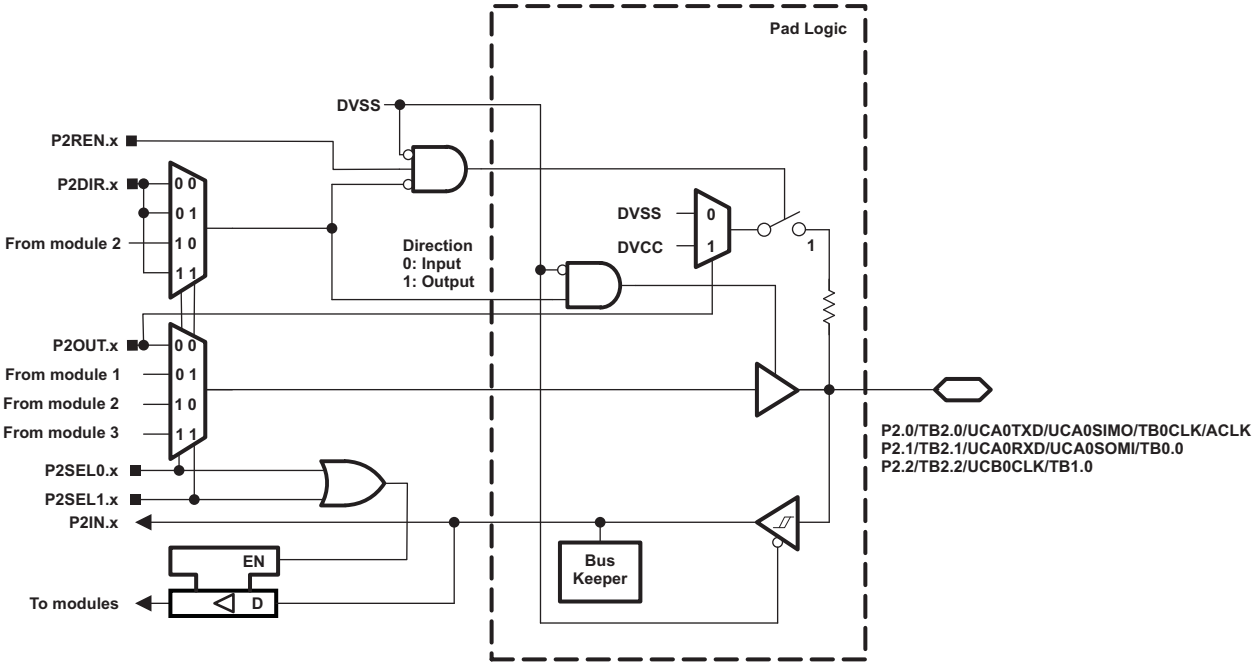



**Table 46. Port P2 (P2.0 to P2.2) Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL1.x | P2SEL0.x |
| P2.0/TB2.0/UCA0TXD/UCA0SIMO/TB0CLK/ACLK | 0 | P2.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB2.CCI0A (1) | 0 | 0 | 1 |
| | | TB2.0 (1) | 1 | | |
| | | UCA0TXD/UCA0SIMO | X (2) | 1 | 0 |
| | | TB0CLK | 0 | 1 | 1 |
| | | ACLK | 1 | | |
| P2.1/TB2.1/UCA0RXD/UCA0SOMI/TB0.0 | 1 | P2.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB2.CCI1A (1) | 0 | 0 | 1 |
| | | TB2.1 (1) | 1 | | |
| | | UCA0RXD/UCA0SOMI | X (2) | 1 | 0 |
| | | TB0.CCI0A | 0 | 1 | 1 |
| | | TB0.0 | 1 | | |
| P2.2/TB2.2/UCB0CLK/TB1.0 | 2 | P2.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TB2.CCI2A (1) | 0 | 0 | 1 |
| | | TB2.2 (1) | 1 | | |
| | | UCB0CLK | X (3) | 1 | 0 |
| | | TB1.CCI0A (1) | 0 | 1 | 1 |
| | | TB1.0 (1) | 1 | | |

(1) Not available on all devices and package types.
(2) Direction controlled by eUSCI_A0 module.
(3) Direction controlled by eUSCI_B0 module.


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## Port P2, P2.3 to P2.4, Input/Output With Schmitt Trigger

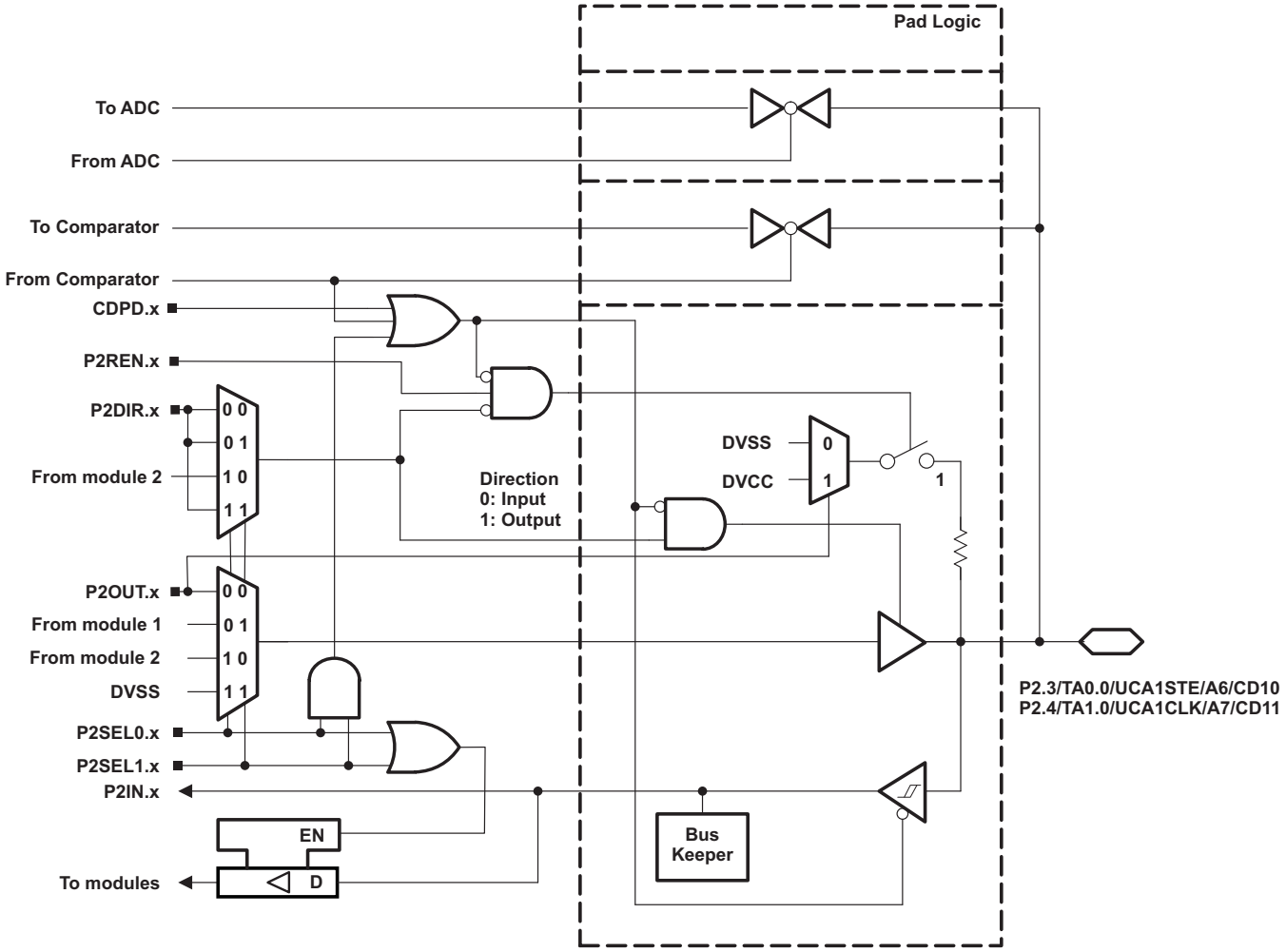


**Table 47. Port P2 (P2.3 to P2.4) Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL1.x | P2SEL0.x |
| P2.3/TA0.0/UCA1STE/A6/CD10 | 3 | P2.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA0.CCI0B | 0 | 0 | 1 |
| | | TA0.0 | 1 | | |
| | | UCA1STE | X (1) | 1 | 0 |
| | | A6 (2) (3)<br>CD10 (2) (4) | X | 1 | 1 |
| P2.4/TA1.0/UCA1CLK/A7/CD11 | 4 | P2.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA1.CCI0B | 0 | 0 | 1 |
| | | TA1.0 | 1 | | |
| | | UCA1CLK | X (1) | 1 | 0 |
| | | A7 (2) (3)<br>CD11 (2) (4) | X | 1 | 1 |

(1) Direction controlled by eUSCI_A1 module.
(2) Setting P2SEL1.x and P2SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Not available on all devices and package types.
(4) Setting the CDPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CDx input pin to the comparator multiplexer with the CDx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CDPD.x bit.


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## Port P2, P2.5 to P2.6, Input/Output With Schmitt Trigger

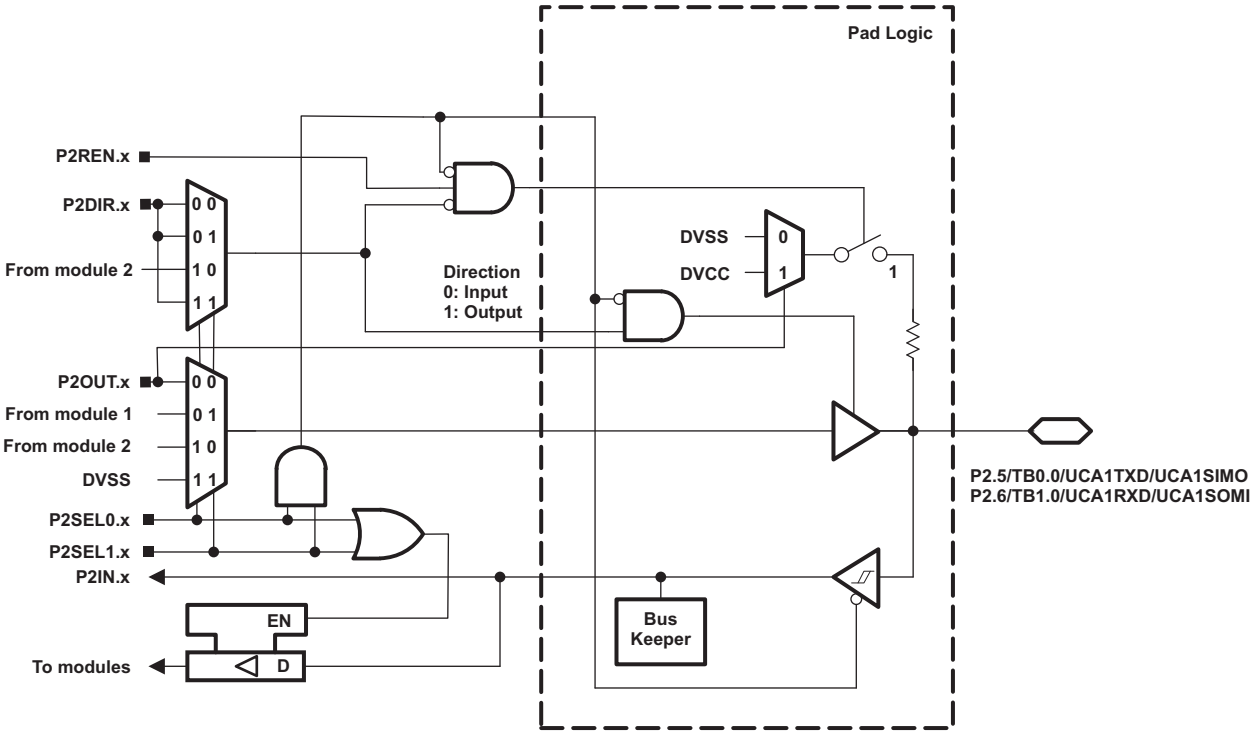



**Table 48. Port P2 (P2.5 to P2.6) Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL1.x | P2SEL0.x |
| P2.5/TB0.0/UCA1TXD/UCA1SIMO | 5 | P2.5(I/O) (1) | I: 0; O: 1 | 0 | 0 |
| | | TB0.CCI0B (1) | 0 | 0 | 1 |
| | | TB0.0 (1) | 1 | | |
| | | UCA1TXD/UCA1SIMO (1) | X (2) | 1 | 0 |
| P2.6/TB1.0/UCA1RXD/UCA1SOMI | 6 | P2.6(I/O) (1) | I: 0; O: 1 | 0 | 0 |
| | | TB1.CCI0B (1) | 0 | 0 | 1 |
| | | TB1.0 (1) | 1 | | |
| | | UCA1RXD/UCA1SOMI (1) | X (2) | 1 | 0 |

(1) Not available on all devices and package types.
(2) Direction controlled by eUSCI_A1 module.

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## Port P2, P2.7, Input/Output With Schmitt Trigger

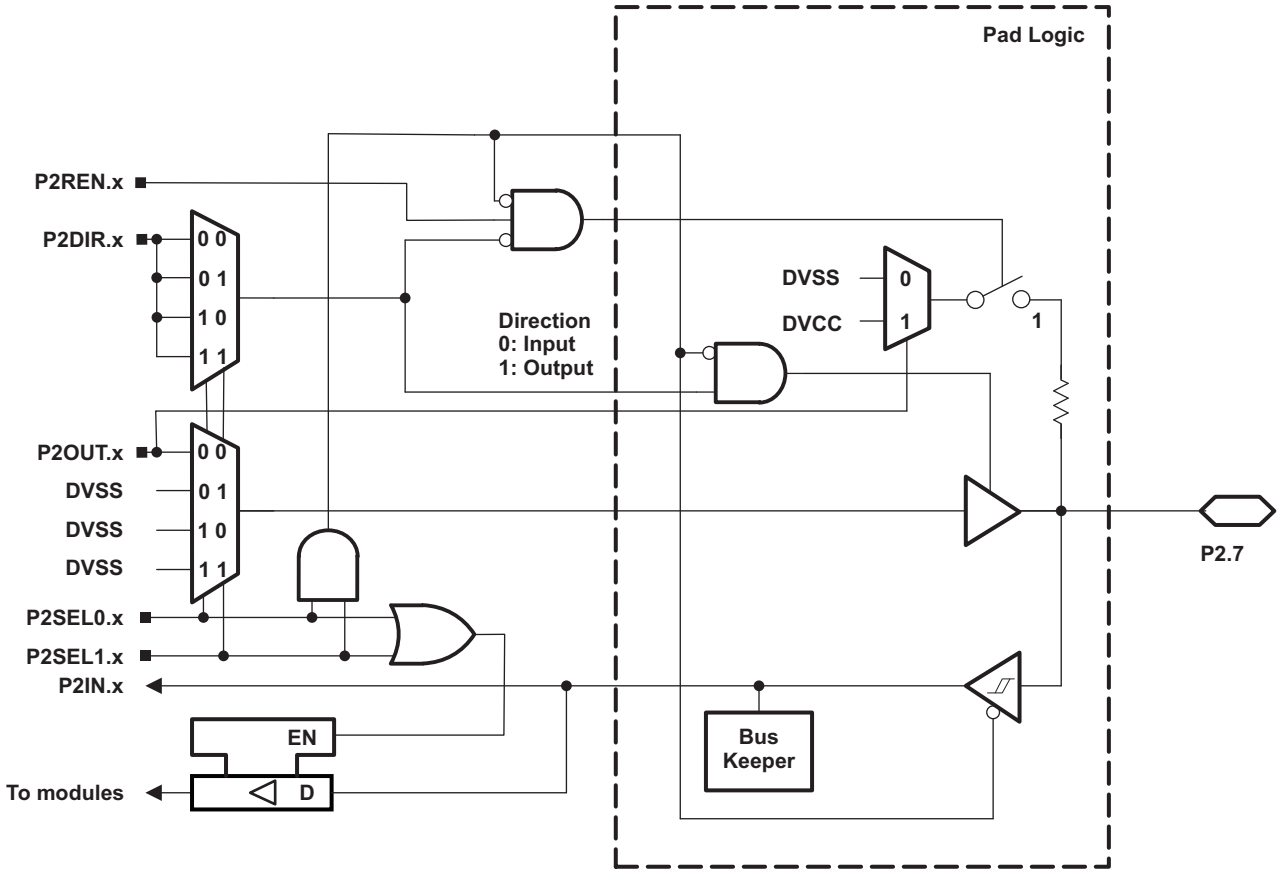



**Table 49. Port P2 (P2.7) Pin Functions**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL1.x | P2SEL0.x |
| P2.7 | 7 | P2.7(I/O) (1) | I: 0; O: 1 | 0 | 0 |

(1) Not available on all devices and package types.


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## Port P3, P3.0 to P3.3, Input/Output With Schmitt Trigger

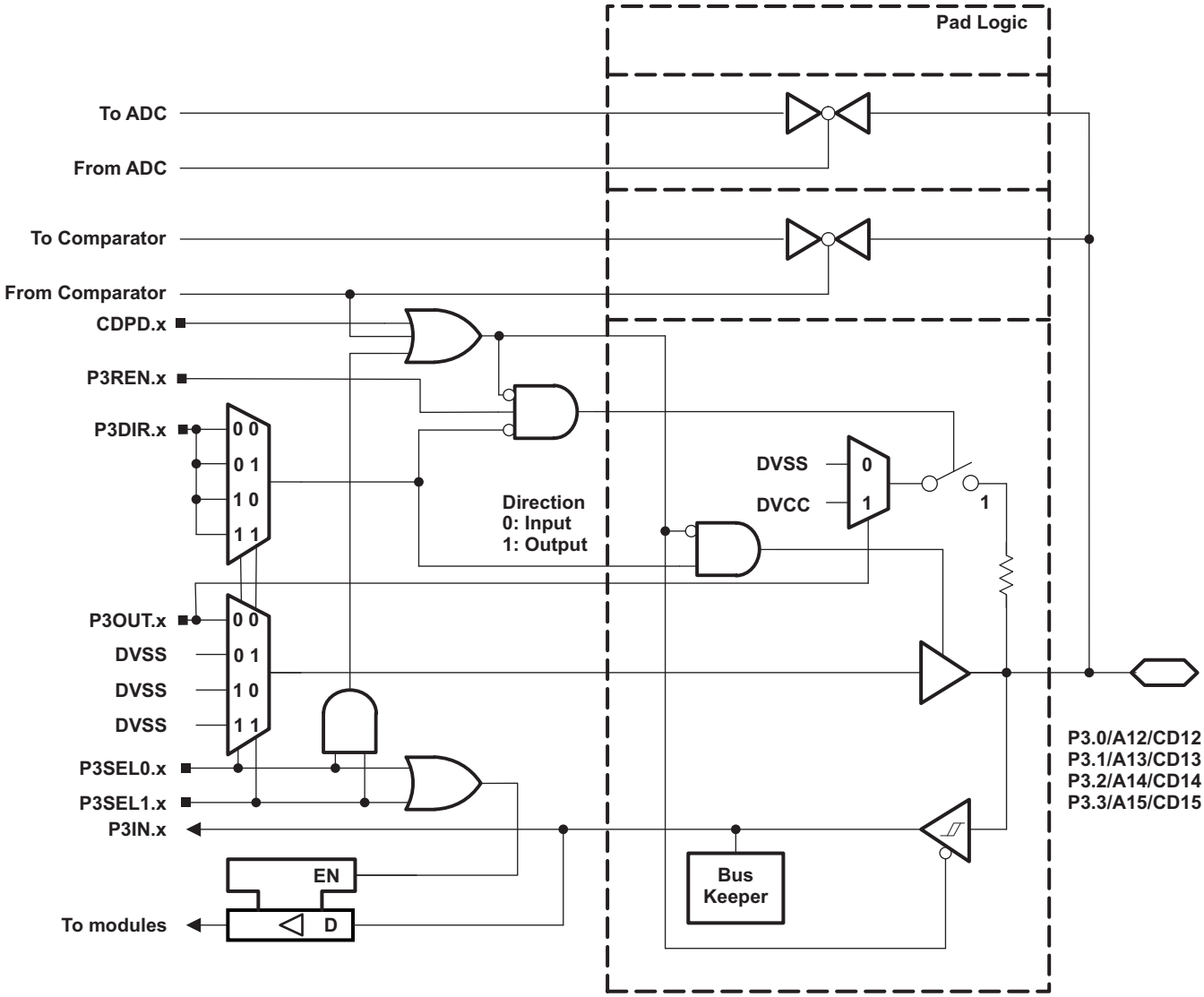


**Table 50. Port P3 (P3.0 to P3.3) Pin Functions**

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL1.x | P3SEL0.x |
| P3.0/A12/CD12 | 0 | P3.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A12 (1) (2)<br>CD12 (1) (3) | X | 1 | 1 |
| P3.1/A13/CD13 | 1 | P3.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A13 (1) (2)<br>CD13 (1) (3) | X | 1 | 1 |
| P3.2/A14/CD14 | 2 | P3.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A14 (1) (2)<br>CD14 (1) (3) | X | 1 | 1 |
| P3.3/A15/CD15 | 3 | P3.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | A15 (1) (2)<br>CD15 (1) (3) | X | 1 | 1 |

(1) Setting P1SEL1.x and P1SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(2) Not available on all devices and package types.
(3) Setting the CDPD.x bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CDx input pin to the comparator multiplexer with the CDx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CDPD.x bit.


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## Port P3, P3.4 to P3.6, Input/Output With Schmitt Trigger

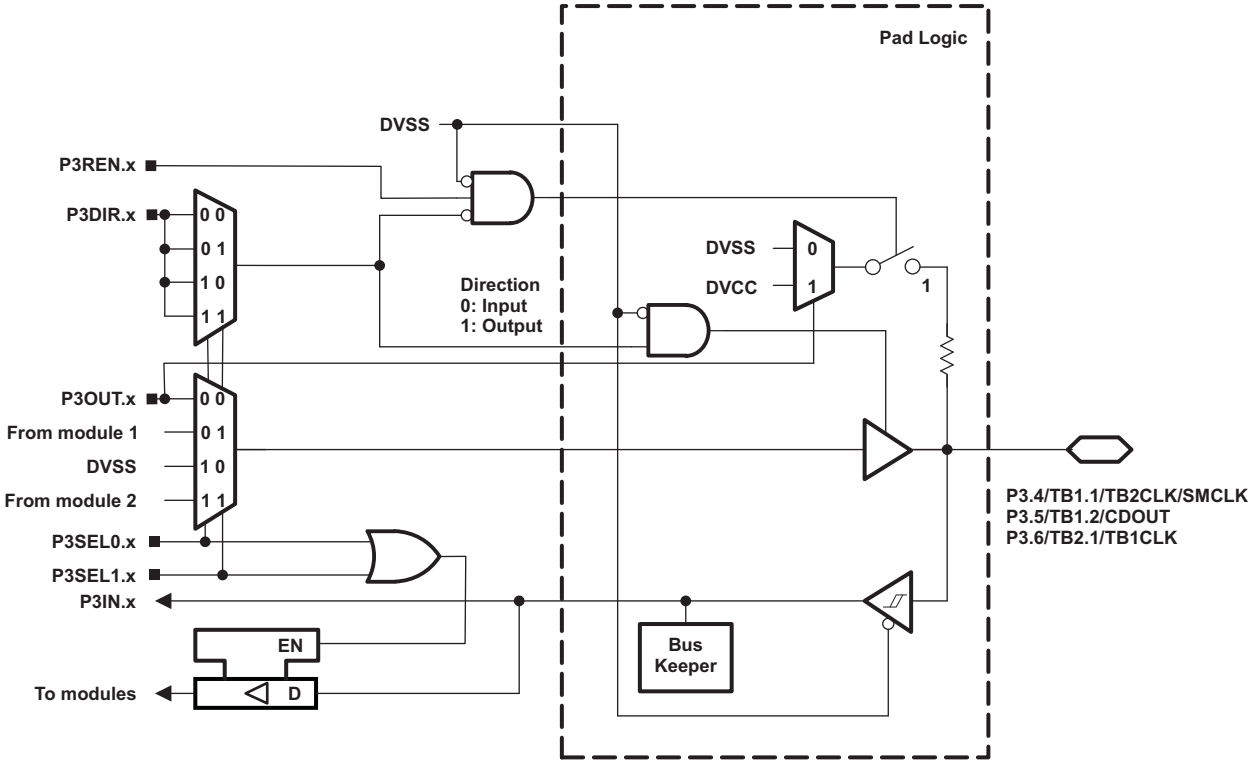



**Table 51. Port P3 (P3.4 to P3.6) Pin Functions**

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL1.x | P3SEL0.x |
| P3.4/TB1.1/TB2CLK/SMCLK | 4 | P3.4 (I/O) (1) | I: 0; O: 1 | 0 | 0 |
| | | TB1.CCI1B (1) | 0 | 0 | 1 |
| | | TB1.1 (1) | 1 | | |
| | | TB2CLK (1) | 0 | 1 | 1 |
| | | SMCLK (1) | 1 | | |
| P3.5/TB1.2/CDOUT | 5 | P3.5 (I/O) (1) | I: 0; O: 1 | 0 | 0 |
| | | TB1.CCI2B (1) | 0 | 0 | 1 |
| | | TB1.2 (1) | 1 | | |
| | | CDOUT (1) | 1 | 1 | 1 |
| P3.6/TB2.1/TB1CLK | 6 | P3.6 (I/O) (1) | I: 0; O: 1 | 0 | 0 |
| | | TB2.CCI1B (1) | 0 | 0 | 1 |
| | | TB2.1 (1) | 1 | | |
| | | TB1CLK (1) | 0 | 1 | 1 |

(1) Not available on all devices and package types.

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## Port P3, P3.7, Input/Output With Schmitt Trigger

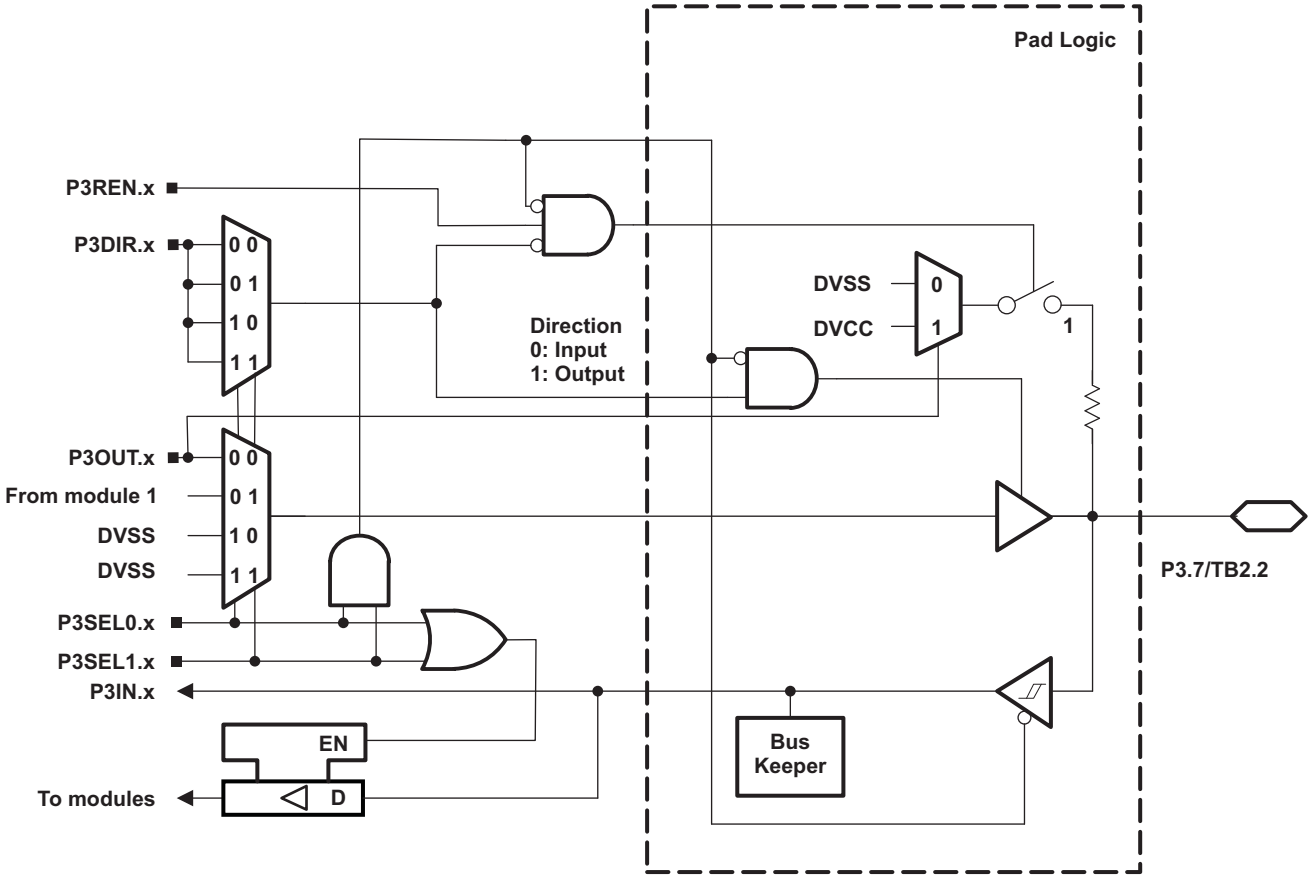



**Table 52. Port P3 (P3.7) Pin Functions**

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL1.x | P3SEL0.x |
| P3.7/TB2.2 | 7 | P3.7 (I/O) (1) | I: 0; O: 1 | 0 | 0 |
| | | TB2.CCI2B (1) | 0 | 0 | 1 |
| | | TB2.2 (1) | 1 | | |

(1) Not available on all devices and package types.


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## Port P4, P4.0, Input/Output With Schmitt Trigger

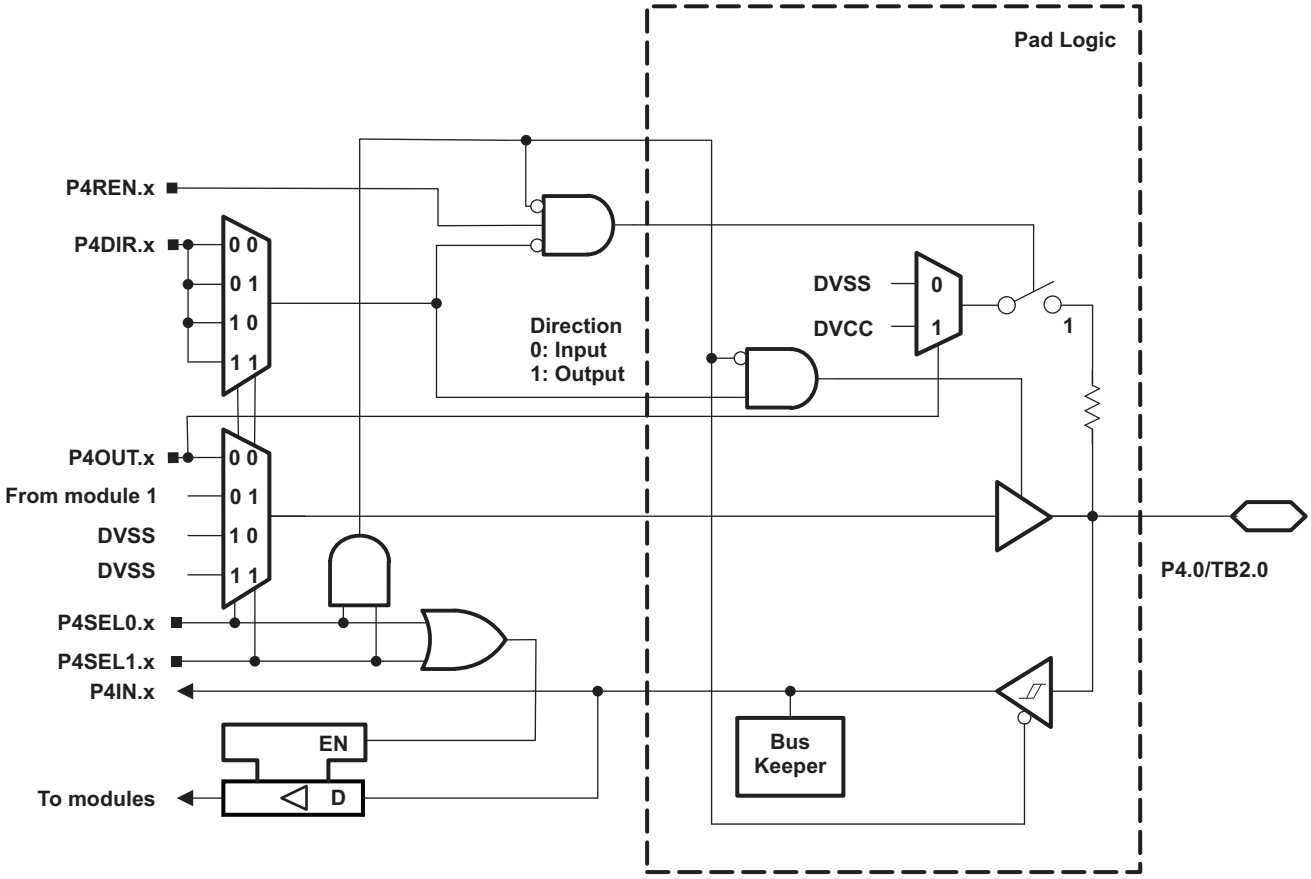



**Table 53. Port P4 (P4.0) Pin Functions**

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P4DIR.x | P4SEL1.x | P4SEL0.x |
| P4.0/TB2.0 | 0 | P4.0 (I/O) (1) | I: 0; O: 1 | 0 | 0 |
| | | TB2.CCI0B (1) | 0 | 0 | 1 |
| | | TB2.0 (1) | 1 | | |

(1) Not available on all devices and package types.

## Port P4, P4.1, Input/Output With Schmitt Trigger

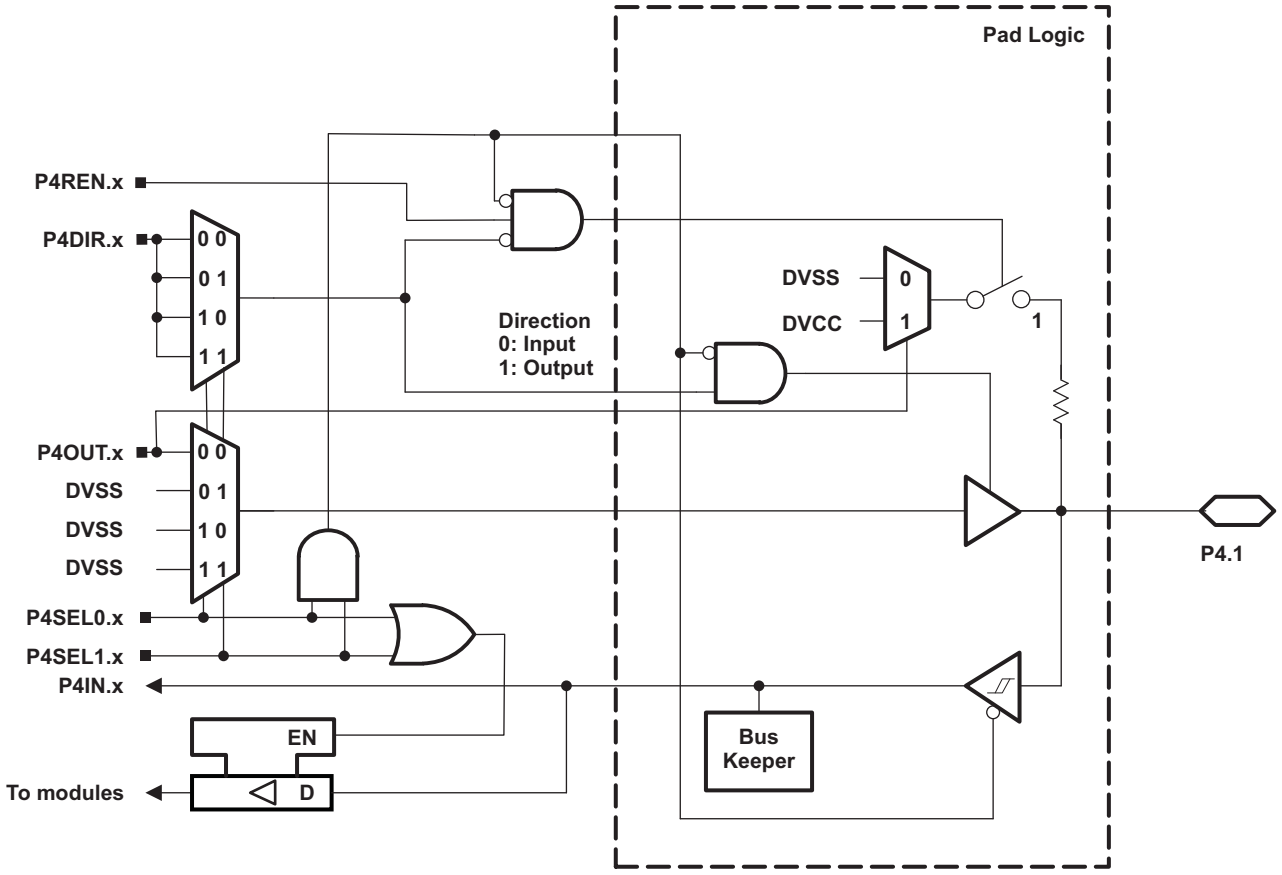



**Table 54. Port P4 (P4.1) Pin Functions**

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS/SIGNALS | | |
|---|---|---|---|---|---|
| | | | P4DIR.x | P4SEL1.x | P4SEL0.x |
| P4.1 | 1 | P4.1 (I/O) (1) | I: 0; O: 1 | 0 | 0 |

(1) Not available on all devices and package types.


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## Port J, J.0 to J.3 JTAG pins TDO, TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

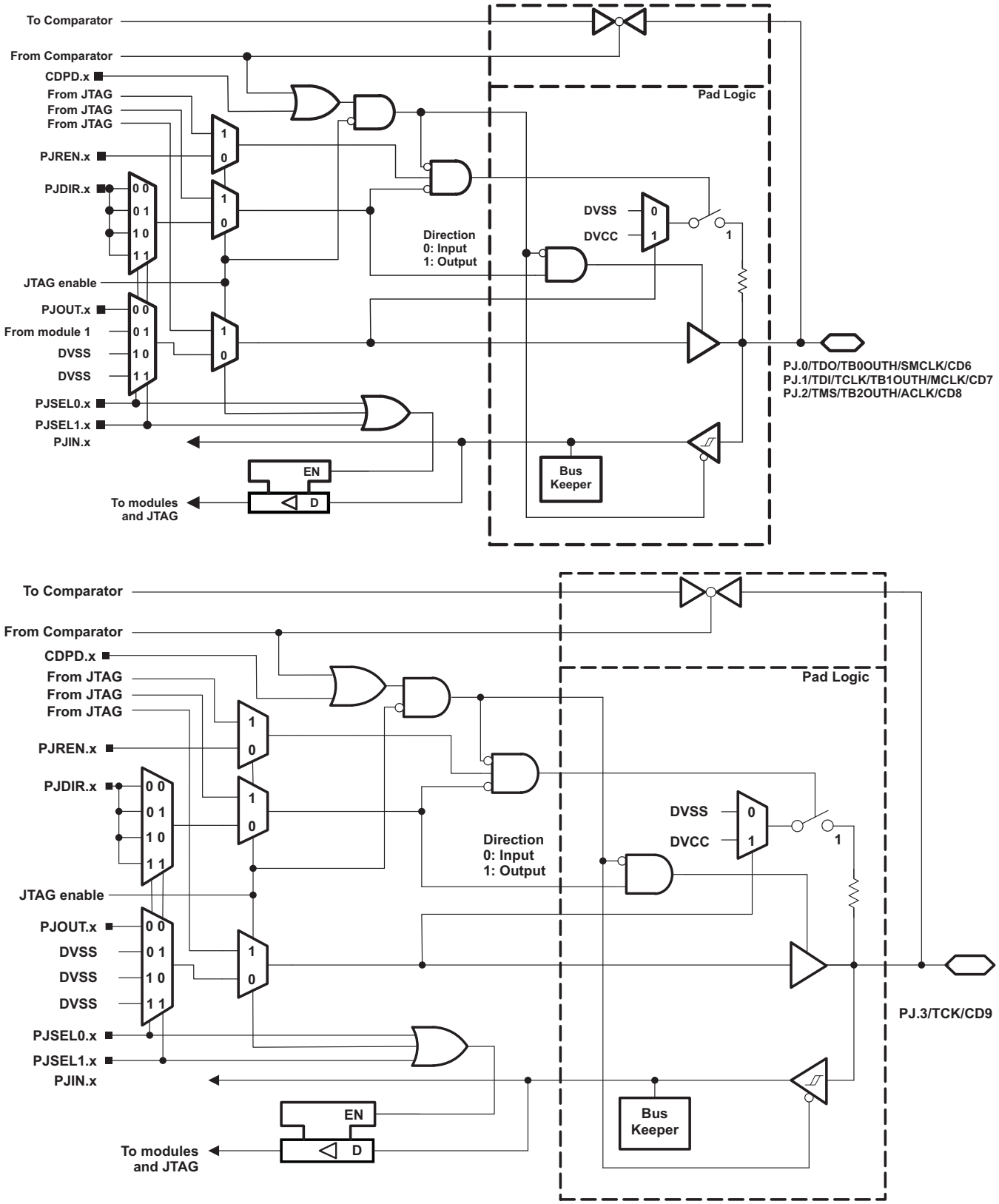


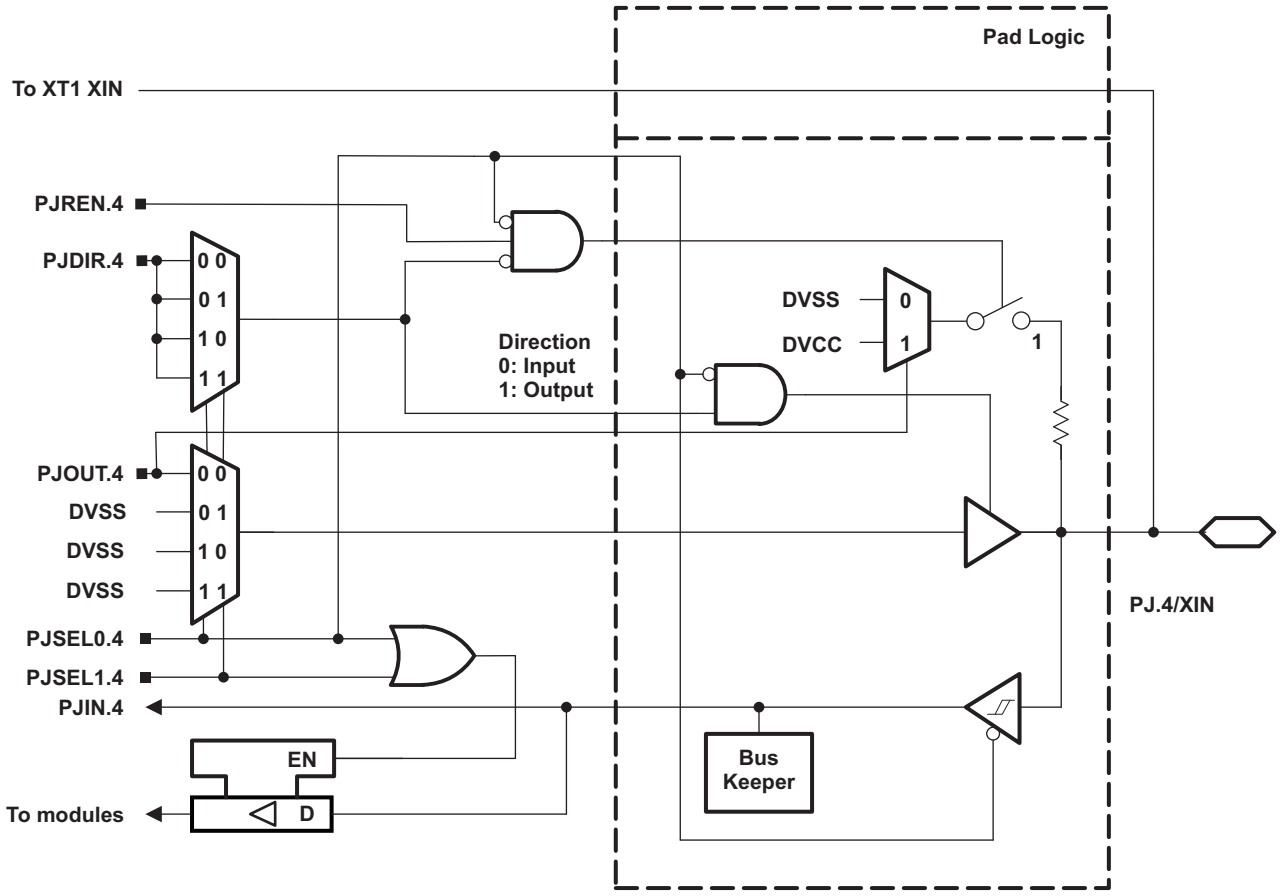
**Table 55. Port PJ (PJ.0 to PJ.3) Pin Functions**

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS/ SIGNALS (1) | | |
|---|---|---|---|---|---|
| | | | PJDIR.x | PJSEL1.x | PJSEL0.x |
| PJ.0/TDO/TB0OUTH/SMCLK/CD6 | 0 | PJ.0 (I/O) (2) | I: 0; O: 1 | 0 | 0 |
| | | TDO (3) | X | X | X |
| | | TB0OUTH | 0 | 0 | 1 |
| | | SMCLK | 1 | | |
| | | CD6 | X | 1 | 1 |
| PJ.1/TDI/TCLK/TB1OUTH/MCLK/CD7 | 1 | PJ.1 (I/O) (2) | I: 0; O: 1 | 0 | 0 |
| | | TDI/TCLK (3) (4) | X | X | X |
| | | TB1OUTH | 0 | 0 | 1 |
| | | MCLK | 1 | | |
| | | CD7 | X | 1 | 1 |
| PJ.2/TMS/TB2OUTH/ACLK/CD8 | 2 | PJ.2 (I/O) (2) | I: 0; O: 1 | 0 | 0 |
| | | TMS (3) (4) | X | X | X |
| | | TB2OUTH | 0 | 0 | 1 |
| | | ACLK | 1 | | |
| | | CD8 | X | 1 | 1 |
| PJ.3/TCK/CD9 | 3 | PJ.3 (I/O) (2) | I: 0; O: 1 | 0 | 0 |
| | | TCK (3) (4) | X | X | X |
| | | CD9 | X | 1 | 1 |

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module. JTAG mode selection is made by the SYS module or by the Spy-Bi-Wire four-wire entry sequence. PJSEL1.x and PJSEL0.x have no effect in these cases.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are do not care.


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## Port PJ, PJ.4 and PJ.5 Input/Output With Schmitt Trigger



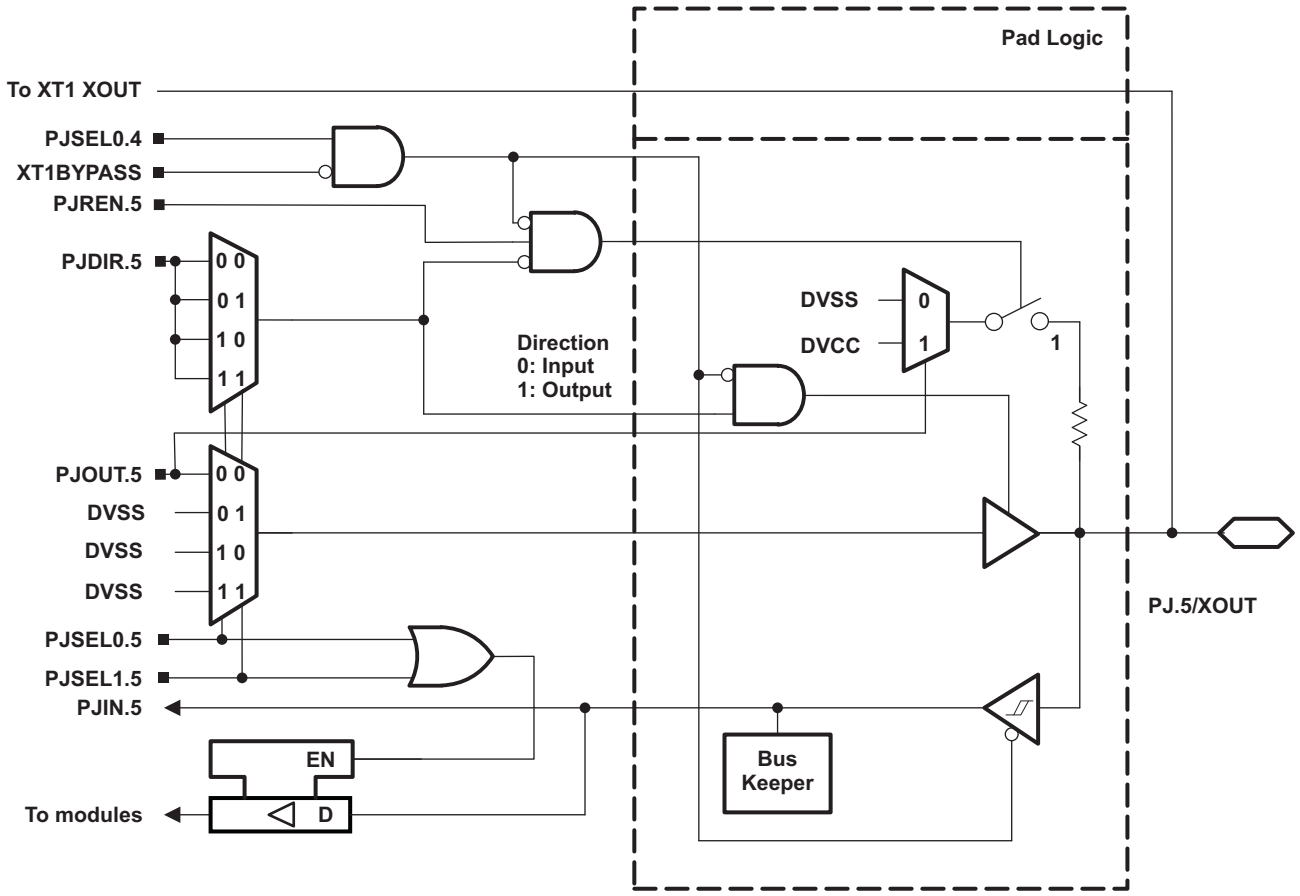



**Table 56. Port PJ (PJ.4 and PJ.5) Pin Functions**

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS/SIGNALS (1) | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | PJDIR.x | PJSEL1.5 | PJSEL0.5 | PJSEL1.4 | PJSEL0.4 | XT1 BYPASS |
| PJ.4/XIN | 4 | PJ.4 (I/O) | I: 0; O: 1 | X | X | 0 | 0 | X |
| | | XIN crystal mode (2) | X | X | X | 0 | 1 | 0 |
| | | XIN bypass mode (2) | X | X | X | 0 | 1 | 1 |
| PJ.5/XOUT | 5 | PJ.5 (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 | X |
| | | XOUT crystal mode (3) | X | X | X | 0 | 1 | 0 |
| | | PJ.5 (I/O) (4) | I: 0; O: 1 | X | X | 0 | 1 | 1 |

(1) X = Don't care
(2) Setting PJSEL1.4 = 0 and PJSEL0.4 = 1 causes the general-purpose I/O to be disabled. When XT1BYPASS = 0, PJ.4 and PJ.5 are configured for crystal operation and PJSEL1.5 and PJSEL0.5 are do not care. When XT1BYPASS = 1, PJ.4 is configured for bypass operation and PJ.5 is configured as general-purpose I/O.
(3) Setting PJSEL1.4 = 0 and PJSEL0.4 = 1 causes the general-purpose I/O to be disabled. When XT1BYPASS = 0, PJ.4 and PJ.5 are configured for crystal operation and PJSEL1.5 and PJSEL0.5 are do not care. When XT1BYPASS = 1, PJ.4 is configured for bypass operation and PJ.5 is configured as general-purpose I/O.
(4) When PJ.4 is configured in bypass mode, PJ.5 is configured as general-purpose I/O.


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## DEVICE DESCRIPTORS (TLV)

The following tables list the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

**Table 57. Device Descriptor Table (1)**

| | Description | Address | FR5739 | FR5738 | FR5737 | FR5736 | FR5735 |
|---|---|---|---|---|---|---|---|
| | | | Value | Value | Value | Value | Value |
| **Info Block** | Info length | 01A00h | 05h | 05h | 05h | 05h | 05h |
| | CRC length | 01A01h | 05h | 05h | 05h | 05h | 05h |
| | CRC value | 01A02h | per unit | per unit | per unit | per unit | per unit |
| | | 01A03h | per unit | per unit | per unit | per unit | per unit |
| | Device ID | 01A04h | 03h | 02h | 01h | 77h | 76h |
| | Device ID | 01A05h | 81h | 81h | 81h | 81h | 81h |
| | Hardware revision | 01A06h | per unit | per unit | per unit | per unit | per unit |
| | Firmware revision | 01A07h | per unit | per unit | per unit | per unit | per unit |
| **Die Record** | Die Record Tag | 01A08h | 08h | 08h | 08h | 08h | 08h |
| | Die Record length | 01A09h | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot/Wafer ID | 01A0Ah | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Bh | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Ch | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Dh | per unit | per unit | per unit | per unit | per unit |
| | Die X position | 01A0Eh | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Fh | per unit | per unit | per unit | per unit | per unit |
| | Die Y position | 01A10h | per unit | per unit | per unit | per unit | per unit |
| | | 01A11h | per unit | per unit | per unit | per unit | per unit |
| | Test results | 01A12h | per unit | per unit | per unit | per unit | per unit |
| | | 01A13h | per unit | per unit | per unit | per unit | per unit |
| **ADC10 Calibration** | ADC10 Calibration Tag | 01A14h | 13h | 13h | 13h | 05h | 13h |
| | ADC10 Calibration length | 01A15h | 10h | 10h | 10h | 10h | 10h |
| | ADC Gain Factor | 01A16h | per unit | per unit | NA | NA | per unit |
| | | 01A17h | per unit | per unit | NA | NA | per unit |
| | ADC Offset | 01A18h | per unit | per unit | NA | NA | per unit |
| | | 01A19h | per unit | per unit | NA | NA | per unit |
| | ADC 1.5-V Reference Temp. Sensor 30°C | 01A1Ah | per unit | per unit | NA | NA | per unit |
| | | 01A1Bh | per unit | per unit | NA | NA | per unit |
| | ADC 1.5-V Reference Temp. Sensor 85°C | 01A1Ch | per unit | per unit | NA | NA | per unit |
| | | 01A1Dh | per unit | per unit | NA | NA | per unit |
| | ADC 2.0-V Reference Temp. Sensor 30°C | 01A1Eh | per unit | per unit | NA | NA | per unit |
| | | 01A1Fh | per unit | per unit | NA | NA | per unit |
| | ADC 2.0-V Reference Temp. Sensor 85°C | 01A20h | per unit | per unit | NA | NA | per unit |
| | | 01A21h | per unit | per unit | NA | NA | per unit |
| | ADC 2.5-V Reference Temp. Sensor 30°C | 01A22h | per unit | per unit | NA | NA | per unit |
| | | 01A23h | per unit | per unit | NA | NA | per unit |

(1) NA = Not applicable

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**Table 57. Device Descriptor Table (1) (continued)**

| | Description | Address | FR5739 | FR5738 | FR5737 | FR5736 | FR5735 |
|---|---|---|---|---|---|---|---|
| | | | Value | Value | Value | Value | Value |
| | ADC 2.5-V Reference Temp. Sensor 85°C | 01A24h | per unit | per unit | NA | NA | per unit |
| | | 01A25h | per unit | per unit | NA | NA | per unit |
| **REF Calibration** | REF Calibration Tag | 01A26h | 12h | 12h | 12h | 12h | 12h |
| | REF Calibration length | 01A27h | 06h | 06h | 06h | 06h | 06h |
| | REF 1.5-V Reference | 01A28h | per unit | per unit | per unit | per unit | per unit |
| | | 01A29h | per unit | per unit | per unit | per unit | per unit |
| | REF 2.0-V Reference | 01A2Ah | per unit | per unit | per unit | per unit | per unit |
| | | 01A2Bh | per unit | per unit | per unit | per unit | per unit |
| | REF 2.5-V Reference | 01A2Ch | per unit | per unit | per unit | per unit | per unit |
| | | 01A2Dh | per unit | per unit | per unit | per unit | per unit |

**Table 58. Device Descriptor Table (1)**

| | Description | Address | FR5734 | FR5733 | FR5732 | FR5731 | FR5730 |
|---|---|---|---|---|---|---|---|
| | | | Value | Value | Value | Value | Value |
| **Info Block** | Info length | 01A00h | 05h | 05h | 05h | 05h | 05h |
| | CRC length | 01A01h | 05h | 05h | 05h | 05h | 05h |
| | CRC value | 01A02h | per unit | per unit | per unit | per unit | per unit |
| | | 01A03h | per unit | per unit | per unit | per unit | per unit |
| | Device ID | 01A04h | 00h | 7Fh | 75h | 7Eh | 7Ch |
| | Device ID | 01A05h | 81h | 80h | 81h | 80h | 80h |
| | Hardware revision | 01A06h | per unit | per unit | per unit | per unit | per unit |
| | Firmware revision | 01A07h | per unit | per unit | per unit | per unit | per unit |
| **Die Record** | Die Record Tag | 01A08h | 08h | 08h | 08h | 08h | 08h |
| | Die Record length | 01A09h | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot/Wafer ID | 01A0Ah | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Bh | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Ch | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Dh | per unit | per unit | per unit | per unit | per unit |
| | Die X position | 01A0Eh | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Fh | per unit | per unit | per unit | per unit | per unit |
| | Die Y position | 01A10h | per unit | per unit | per unit | per unit | per unit |
| | | 01A11h | per unit | per unit | per unit | per unit | per unit |
| | Test results | 01A12h | per unit | per unit | per unit | per unit | per unit |
| | | 01A13h | per unit | per unit | per unit | per unit | per unit |
| **ADC10 Calibration** | ADC10 Calibration Tag | 01A14h | 13h | 13h | 13h | 05h | 13h |
| | ADC10 Calibration length | 01A15h | 10h | 10h | 10h | 10h | 10h |
| | ADC Gain Factor | 01A16h | per unit | NA | NA | per unit | per unit |
| | | 01A17h | per unit | NA | NA | per unit | per unit |
| | ADC Offset | 01A18h | per unit | NA | NA | per unit | per unit |
| | | 01A19h | per unit | NA | NA | per unit | per unit |
| | ADC 1.5-V Reference Temp. Sensor 30°C | 01A1Ah | per unit | NA | NA | per unit | per unit |
| | | 01A1Bh | per unit | NA | NA | per unit | per unit |

(1) NA = Not applicable


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**Table 58. Device Descriptor Table [1] (continued)**

| | Description | Address | FR5734 | FR5733 | FR5732 | FR5731 | FR5730 |
|---|---|---|---|---|---|---|---|
| | | | Value | Value | Value | Value | Value |
| | ADC 1.5-V Reference Temp. Sensor 85°C | 01A1Ch | per unit | NA | NA | per unit | per unit |
| | | 01A1Dh | per unit | NA | NA | per unit | per unit |
| | ADC 2.0-V Reference Temp. Sensor 30°C | 01A1Eh | per unit | NA | NA | per unit | per unit |
| | | 01A1Fh | per unit | NA | NA | per unit | per unit |
| | ADC 2.0-V Reference Temp. Sensor 85°C | 01A20h | per unit | NA | NA | per unit | per unit |
| | | 01A21h | per unit | NA | NA | per unit | per unit |
| | ADC 2.5-V Reference Temp. Sensor 30°C | 01A22h | per unit | NA | NA | per unit | per unit |
| | | 01A23h | per unit | NA | NA | per unit | per unit |
| | ADC 2.5-V Reference Temp. Sensor 85°C | 01A24h | per unit | NA | NA | per unit | per unit |
| | | 01A25h | per unit | NA | NA | per unit | per unit |
| **REF Calibration** | REF Calibration Tag | 01A26h | 12h | 12h | 12h | 12h | 12h |
| | REF Calibration length | 01A27h | 06h | 06h | 06h | 06h | 06h |
| | REF 1.5-V Reference | 01A28h | per unit | per unit | per unit | per unit | per unit |
| | | 01A29h | per unit | per unit | per unit | per unit | per unit |
| | REF 2.0-V Reference | 01A2Ah | per unit | per unit | per unit | per unit | per unit |
| | | 01A2Bh | per unit | per unit | per unit | per unit | per unit |
| | REF 2.5-V Reference | 01A2Ch | per unit | per unit | per unit | per unit | per unit |
| | | 01A2Dh | per unit | per unit | per unit | per unit | per unit |

**Table 59. Device Descriptor Table [1]**

| | Description | Address | FR5729 | FR5728 | FR5727 | FR5726 | FR5725 |
|---|---|---|---|---|---|---|---|
| | | | Value | Value | Value | Value | Value |
| **Info Block** | Info length | 01A00h | 05h | 05h | 05h | 05h | 05h |
| | CRC length | 01A01h | 05h | 05h | 05h | 05h | 05h |
| | CRC value | 01A02h | per unit | per unit | per unit | per unit | per unit |
| | | 01A03h | per unit | per unit | per unit | per unit | per unit |
| | Device ID | 01A04h | 7Bh | 7Ah | 79h | 74h | 78h |
| | Device ID | 01A05h | 80h | 80h | 80h | 81h | 80h |
| | Hardware revision | 01A06h | per unit | per unit | per unit | per unit | per unit |
| | Firmware revision | 01A07h | per unit | per unit | per unit | per unit | per unit |
| **Die Record** | Die Record Tag | 01A08h | 08h | 08h | 08h | 08h | 08h |
| | Die Record length | 01A09h | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot/Wafer ID | 01A0Ah | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Bh | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Ch | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Dh | per unit | per unit | per unit | per unit | per unit |
| | Die X position | 01A0Eh | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Fh | per unit | per unit | per unit | per unit | per unit |
| | Die Y position | 01A10h | per unit | per unit | per unit | per unit | per unit |
| | | 01A11h | per unit | per unit | per unit | per unit | per unit |
| | Test results | 01A12h | per unit | per unit | per unit | per unit | per unit |
| | | 01A13h | per unit | per unit | per unit | per unit | per unit |

(1) NA = Not applicable

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**Table 59. Device Descriptor Table (1) (continued)**

| | Description | Address | FR5729 | FR5728 | FR5727 | FR5726 | FR5725 |
|---|---|---|---|---|---|---|---|
| | | | Value | Value | Value | Value | Value |
| **ADC10 Calibration** | ADC10 Calibration Tag | 01A14h | 13h | 13h | 13h | 05h | 13h |
| | ADC10 Calibration length | 01A15h | 10h | 10h | 10h | 10h | 10h |
| | ADC Gain Factor | 01A16h | per unit | per unit | NA | NA | per unit |
| | | 01A17h | per unit | per unit | NA | NA | per unit |
| | ADC Offset | 01A18h | per unit | per unit | NA | NA | per unit |
| | | 01A19h | per unit | per unit | NA | NA | per unit |
| | ADC 1.5-V Reference Temp. Sensor 30°C | 01A1Ah | per unit | per unit | NA | NA | per unit |
| | | 01A1Bh | per unit | per unit | NA | NA | per unit |
| | ADC 1.5-V Reference Temp. Sensor 85°C | 01A1Ch | per unit | per unit | NA | NA | per unit |
| | | 01A1Dh | per unit | per unit | NA | NA | per unit |
| | ADC 2.0-V Reference Temp. Sensor 30°C | 01A1Eh | per unit | per unit | NA | NA | per unit |
| | | 01A1Fh | per unit | per unit | NA | NA | per unit |
| | ADC 2.0-V Reference Temp. Sensor 85°C | 01A20h | per unit | per unit | NA | NA | per unit |
| | | 01A21h | per unit | per unit | NA | NA | per unit |
| | ADC 2.5-V Reference Temp. Sensor 30°C | 01A22h | per unit | per unit | NA | NA | per unit |
| | | 01A23h | per unit | per unit | NA | NA | per unit |
| | ADC 2.5-V Reference Temp. Sensor 85°C | 01A24h | per unit | per unit | NA | NA | per unit |
| | | 01A25h | per unit | per unit | NA | NA | per unit |
| **REF Calibration** | REF Calibration Tag | 01A26h | 12h | 12h | 12h | 12h | 12h |
| | REF Calibration length | 01A27h | 06h | 06h | 06h | 06h | 06h |
| | REF 1.5-V Reference | 01A28h | per unit | per unit | per unit | per unit | per unit |
| | | 01A29h | per unit | per unit | per unit | per unit | per unit |
| | REF 2.0-V Reference | 01A2Ah | per unit | per unit | per unit | per unit | per unit |
| | | 01A2Bh | per unit | per unit | per unit | per unit | per unit |
| | REF 2.5-V Reference | 01A2Ch | per unit | per unit | per unit | per unit | per unit |
| | | 01A2Dh | per unit | per unit | per unit | per unit | per unit |

**Table 60. Device Descriptor Table (1)**

| | Description | Address | FR5724 | FR5723 | FR5722 | FR5721 | FR5720 |
|---|---|---|---|---|---|---|---|
| | | | Value | Value | Value | Value | Value |
| **Info Block** | Info length | 01A00h | 05h | 05h | 05h | 05h | 05h |
| | CRC length | 01A01h | 05h | 05h | 05h | 05h | 05h |
| | CRC value | 01A02h | per unit | per unit | per unit | per unit | per unit |
| | | 01A03h | per unit | per unit | per unit | per unit | per unit |
| | Device ID | 01A04h | 73h | 72h | 71h | 77h | 70h |
| | Device ID | 01A05h | 81h | 81h | 81h | 80h | 81h |
| | Hardware revision | 01A06h | per unit | per unit | per unit | per unit | per unit |
| | Firmware revision | 01A07h | per unit | per unit | per unit | per unit | per unit |
| **Die Record** | Die Record Tag | 01A08h | 08h | 08h | 08h | 08h | 08h |
| | Die Record length | 01A09h | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |

(1) NA = Not applicable


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**Table 60. Device Descriptor Table [1] (continued)**

| | Description | Address | FR5724 | FR5723 | FR5722 | FR5721 | FR5720 |
|---|---|---|---|---|---|---|---|
| | | | Value | Value | Value | Value | Value |
| | Lot/Wafer ID | 01A0Ah | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Bh | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Ch | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Dh | per unit | per unit | per unit | per unit | per unit |
| | Die X position | 01A0Eh | per unit | per unit | per unit | per unit | per unit |
| | | 01A0Fh | per unit | per unit | per unit | per unit | per unit |
| | Die Y position | 01A10h | per unit | per unit | per unit | per unit | per unit |
| | | 01A11h | per unit | per unit | per unit | per unit | per unit |
| | Test results | 01A12h | per unit | per unit | per unit | per unit | per unit |
| | | 01A13h | per unit | per unit | per unit | per unit | per unit |
| **ADC10 Calibration** | ADC10 Calibration Tag | 01A14h | 13h | 13h | 13h | 05h | 13h |
| | ADC10 Calibration length | 01A15h | 10h | 10h | 10h | 10h | 10h |
| | ADC Gain Factor | 01A16h | per unit | NA | NA | per unit | per unit |
| | | 01A17h | per unit | NA | NA | per unit | per unit |
| | ADC Offset | 01A18h | per unit | NA | NA | per unit | per unit |
| | | 01A19h | per unit | NA | NA | per unit | per unit |
| | ADC 1.5-V Reference Temp. Sensor 30°C | 01A1Ah | per unit | NA | NA | per unit | per unit |
| | | 01A1Bh | per unit | NA | NA | per unit | per unit |
| | ADC 1.5-V Reference Temp. Sensor 85°C | 01A1Ch | per unit | NA | NA | per unit | per unit |
| | | 01A1Dh | per unit | NA | NA | per unit | per unit |
| | ADC 2.0-V Reference Temp. Sensor 30°C | 01A1Eh | per unit | NA | NA | per unit | per unit |
| | | 01A1Fh | per unit | NA | NA | per unit | per unit |
| | ADC 2.0-V Reference Temp. Sensor 85°C | 01A20h | per unit | NA | NA | per unit | per unit |
| | | 01A21h | per unit | NA | NA | per unit | per unit |
| | ADC 2.5-V Reference Temp. Sensor 30°C | 01A22h | per unit | NA | NA | per unit | per unit |
| | | 01A23h | per unit | NA | NA | per unit | per unit |
| | ADC 2.5-V Reference Temp. Sensor 85°C | 01A24h | per unit | NA | NA | per unit | per unit |
| | | 01A25h | per unit | NA | NA | per unit | per unit |
| **REF Calibration** | REF Calibration Tag | 01A26h | 12h | 12h | 12h | 12h | 12h |
| | REF Calibration length | 01A27h | 06h | 06h | 06h | 06h | 06h |
| | REF 1.5-V Reference | 01A28h | per unit | per unit | per unit | per unit | per unit |
| | | 01A29h | per unit | per unit | per unit | per unit | per unit |
| | REF 2.0-V Reference | 01A2Ah | per unit | per unit | per unit | per unit | per unit |
| | | 01A2Bh | per unit | per unit | per unit | per unit | per unit |
| | REF 2.5-V Reference | 01A2Ch | per unit | per unit | per unit | per unit | per unit |
| | | 01A2Dh | per unit | per unit | per unit | per unit | per unit |

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## REVISION HISTORY

| REVISION | COMMENTS |
|---|---|
| SLAS639 | Product Preview release |
| SLAS639A | Updated Product Preview release including preliminary electrical specifications |
| SLAS639B | Changes throughout for updated Product Preview |
| SLAS639C | Production Data release |
| SLAS639D | Changed PW package options from Product Preview to Production Data.<br>Added information for YFF package option throughout as Product Preview.<br>Table 26 and Table 27, Changed offset of PxSELC registers.<br>Table 28, Added PJSELC register.<br>Table 29, Removed registers that do no apply (TA0CCTL3,4 and TA0CCR3,4)<br>Absolute Maximum Ratings, Changed low limit of $T_{stg}$ from -40°C to -55°C.<br>FRAM, Added $t_{Retention}$ MIN values for $T_J$ = 25°C and $T_J$ = 70°C. |


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430FR5720IPWR | PREVIEW | TSSOP | PW | 28 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430FR5720IRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5720IRGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5721IDA | PREVIEW | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5721IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5721IRHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| MSP430FR5721IRHAT | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| MSP430FR5722IPWR | PREVIEW | TSSOP | PW | 28 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430FR5722IRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5722IRGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5723IDA | PREVIEW | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5723IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5723IRHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| MSP430FR5723IRHAT | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| MSP430FR5724IPWR | PREVIEW | TSSOP | PW | 28 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430FR5724IRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5724IRGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430FR5725IDA | PREVIEW | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5725IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5725IRHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| MSP430FR5726IPWR | PREVIEW | TSSOP | PW | 28 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430FR5726IRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5726IRGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5727IDA | PREVIEW | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5727IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5727IRHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| MSP430FR5727IRHAT | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| MSP430FR5728IPWR | PREVIEW | TSSOP | PW | 28 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430FR5728IRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5728IRGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5729IDA | ACTIVE | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5729IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5729IRHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| MSP430FR5730IPW | PREVIEW | TSSOP | PW | 28 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430FR5730IRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430FR5730IRGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5731IDA | PREVIEW | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5731IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5731IRHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| MSP430FR5731IRHAT | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| MSP430FR5732IPWR | PREVIEW | TSSOP | PW | 28 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430FR5732IRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5732IRGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5733IDA | PREVIEW | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5733IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5733IRHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| MSP430FR5733IRHAT | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| MSP430FR5734IPWR | PREVIEW | TSSOP | PW | 28 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430FR5734IRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5734IRGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5735IDA | ACTIVE | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5735IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5735IRHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| MSP430FR5736IPWR | PREVIEW | TSSOP | PW | 28 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430FR5736IRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5736IRGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5737IDA | PREVIEW | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5737IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5737IRHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| MSP430FR5737IRHAT | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| MSP430FR5738IPWR | PREVIEW | TSSOP | PW | 28 | | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| MSP430FR5738IRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5738IRGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5739IDA | ACTIVE | TSSOP | DA | 38 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5739IDAR | ACTIVE | TSSOP | DA | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| MSP430FR5739IRHAR | ACTIVE | VQFN | RHA | 40 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |
| MSP430FR5739IRHAT | ACTIVE | VQFN | RHA | 40 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

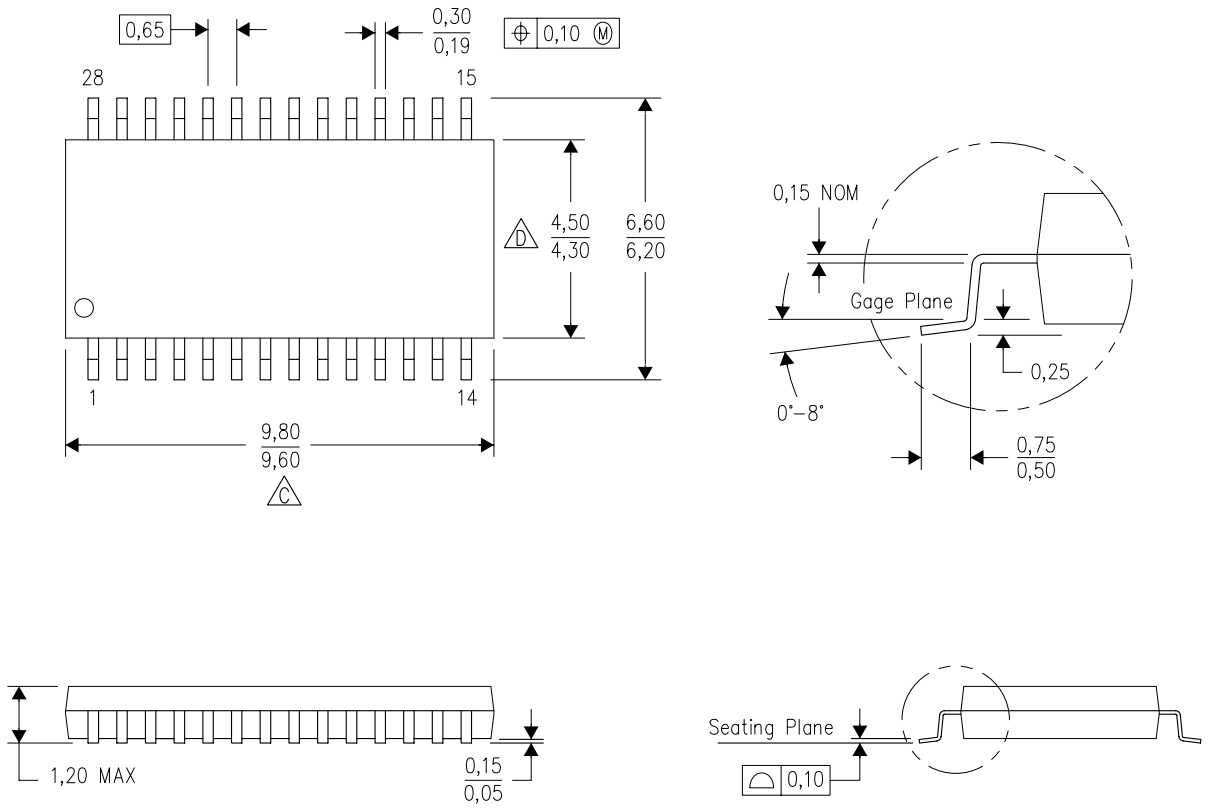
**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

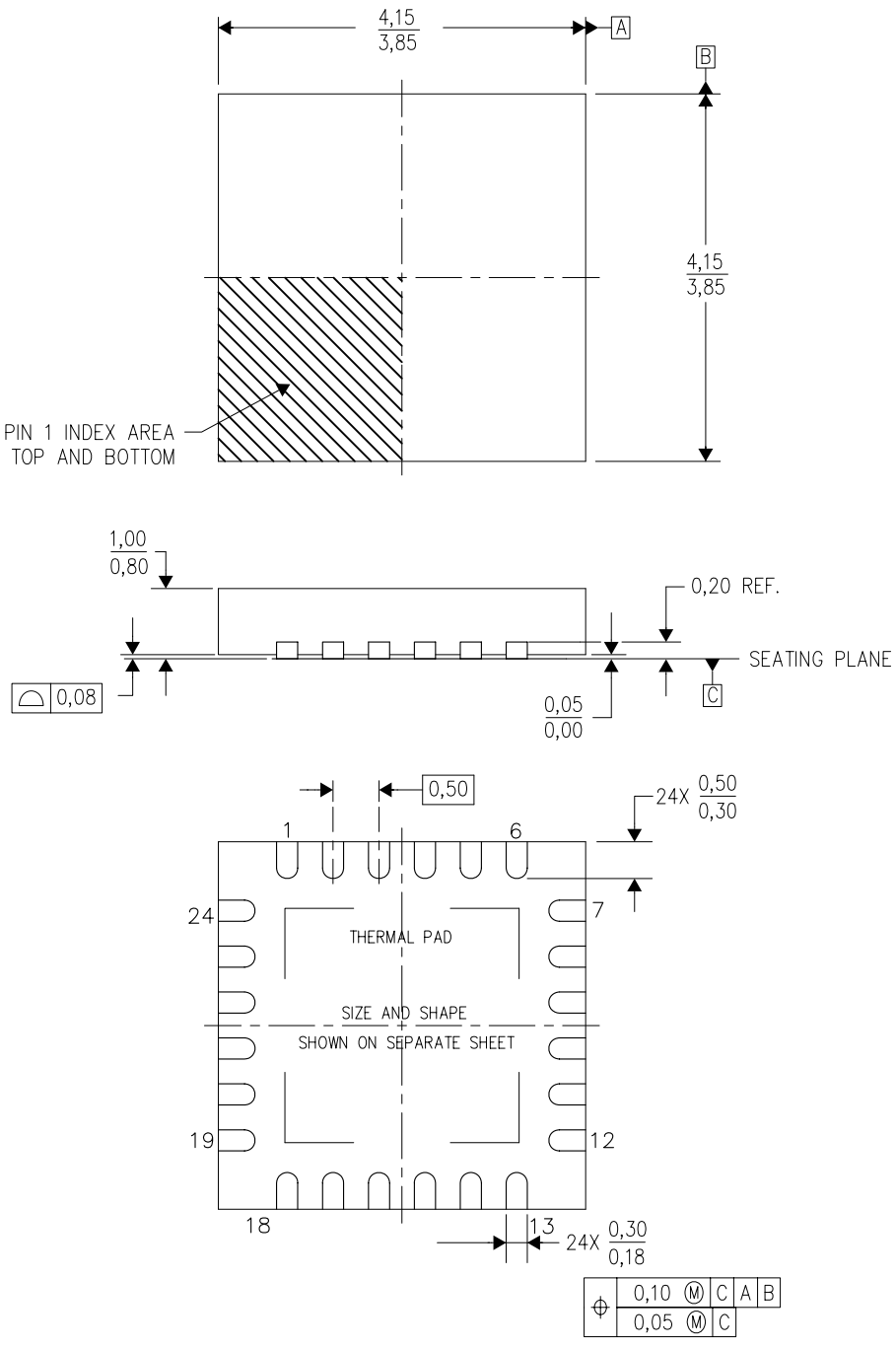
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE




4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

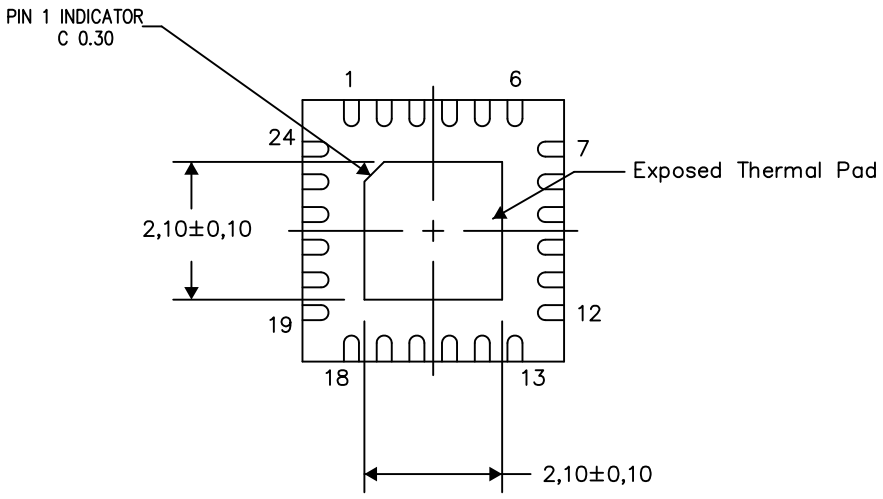
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



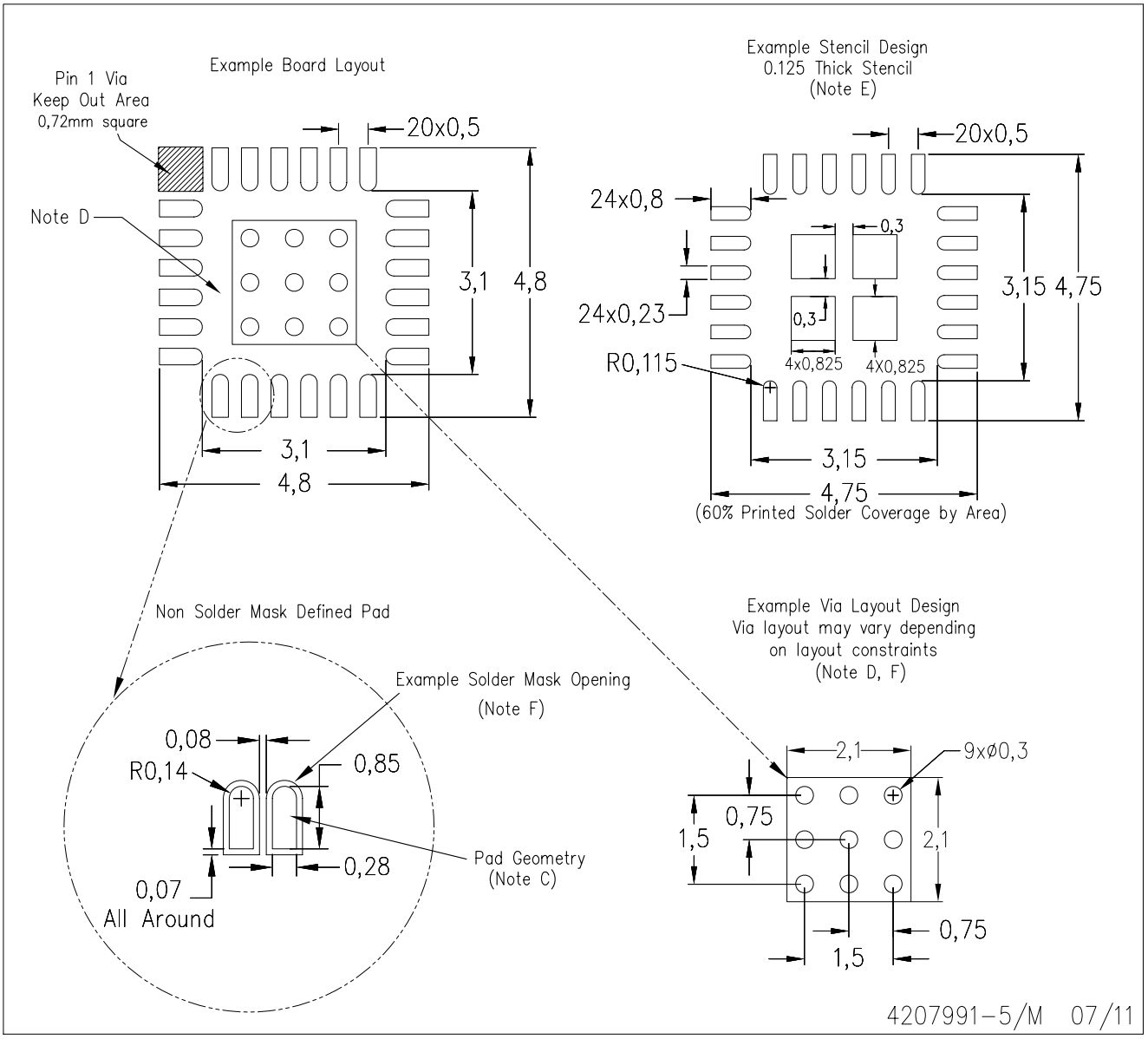

Bottom View

Exposed Thermal Pad Dimensions

4206344–6/AA 04/12

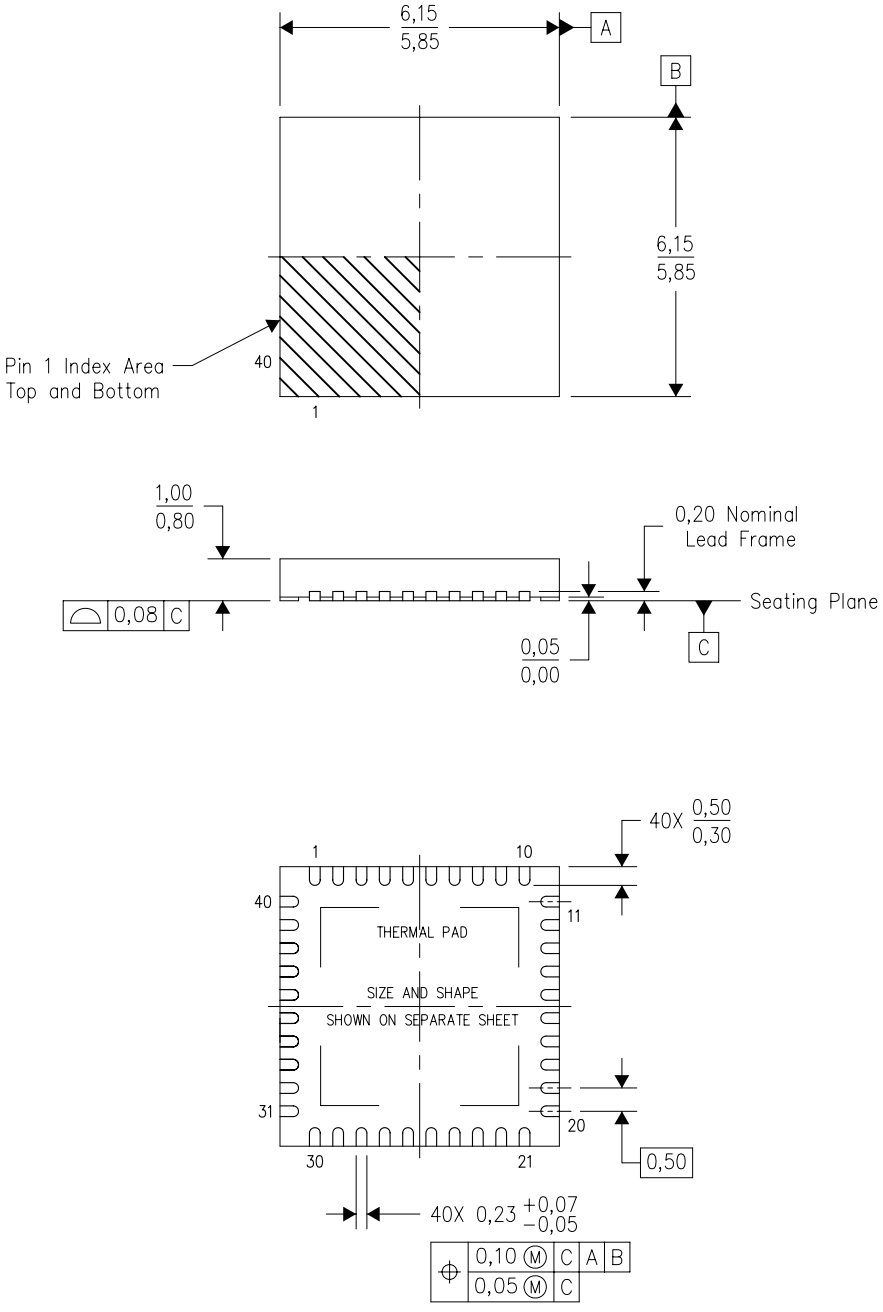
NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD




Bottom View

4204276/E 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220 variation VJJD–2.

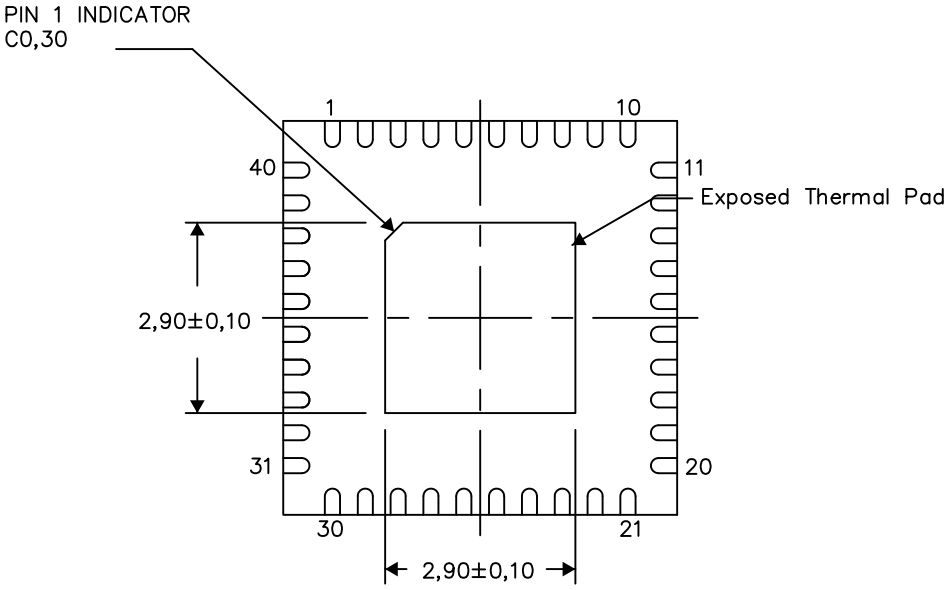
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



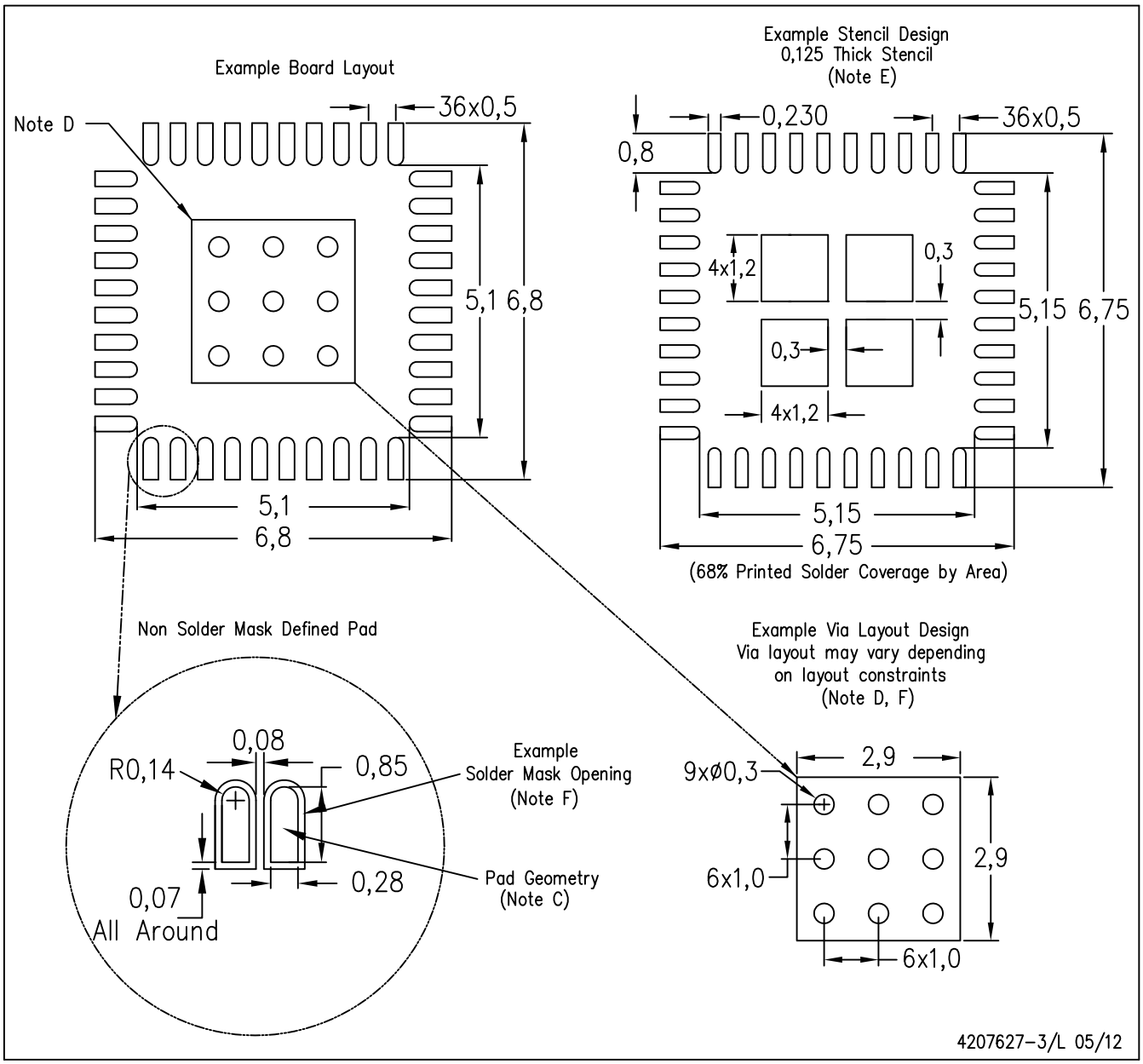

Bottom View

Exposed Thermal Pad Dimensions

4206355–3/Q 05/12

NOTES: A. All linear dimensions are in millimeters

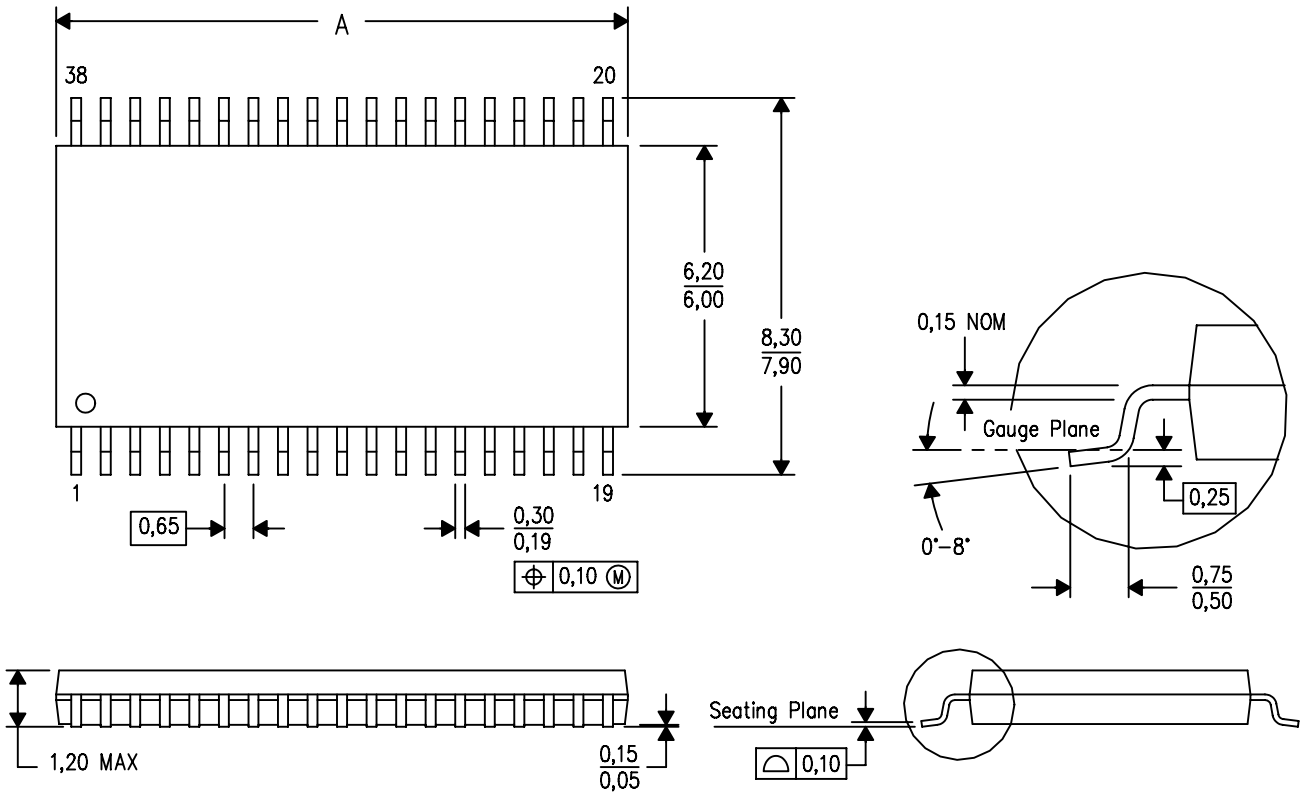
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

DA (R–PDSO–G**) PLASTIC SMALL–OUTLINE PACKAGE

38 PIN SHOWN

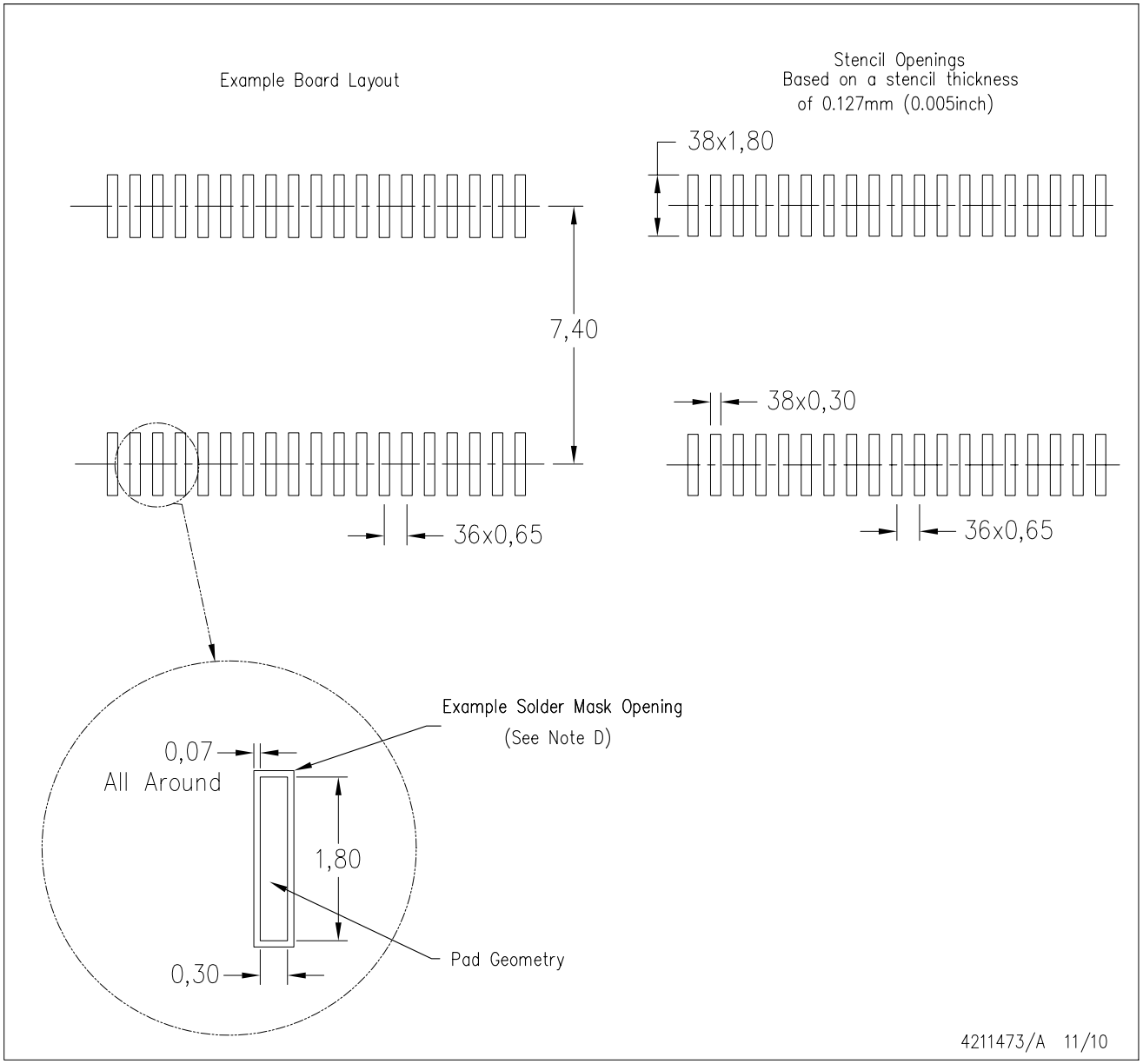



| DIM \ PINS ** | 30 | 32 | 38 |
|---|---|---|---|
| A MAX | 11,10 | 11,10 | 12,60 |
| A MIN | 10,90 | 10,90 | 12,40 |
| △D MO–153 Variation | DB–1 | DC | DD–1 |

4040066/F 01/2009

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
△D Falls within JEDEC MO–153, except 30 pin body length.

DA (R–PDSO–G38) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Contact the board fabrication site for recommended soldermask tolerances.

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