

16-Bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90880 Series

**MB90F882(S)/F883(S)/F883A(S)/F884(S)/F884A(S)
MB90882(S)/883(S)/884(S)/V880(A)-101/-102**

■ DESCRIPTION

The MB90880 series is a general-purpose 16-bit microcontroller, designed by Fujitsu, for process control of devices such as consumer appliances, which require high-speed real-time processing capabilities.

The instruction set of the F²MC-16LX CPU core retains the same AT architecture as the F²MC*¹ family, with further refinements including high-level language instructions, an expanded addressing mode, enhanced multiplier-divider instructions and bit processing. In addition, a 32-bit accumulator is built in to enable long word processing.

As its peripheral resources, the MB90880 series has a 16-bit PPG, multi-function serial interface (software switch over enabled for SIO, UART and I²C*²), 10-bit A/D converter, 16-bit I/O timer, 8/16-bit up-down counter, base timer (software switch over enabled for 16-bit reload timer, PWC timer, PPG timer and PWM timer), DTP / external interrupt and chip select pins.

*1 : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

*2 : Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use, these components in an I²C system provided that the system conforms to the I²C Standard Specification as defined by Philips.

Be sure to refer to the "Check Sheet" for the latest cautions on development.

"Check Sheet" is seen at the following support page

URL : <http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html>

"Check Sheet" lists the minimal requirement items to be checked to prevent problems beforehand in system development.

MB90880 Series

■ FEATURES

- Clock
Minimum instruction execution time : 30.3 ns / 4.125 MHz source oscillation × eight times
(in internal operation : 33 MHz/3.3 V ± 0.3 V)
PLL clock multiplication system
- Maximum memory space
16 Mbytes
- Instruction set optimized for control applications
Supported data types : bit, byte, word and long word
Standard addressing modes : 23 types
Enhanced high-precision calculation realized by 32-bit accumulator
Signed multiplication/division instructions and extended RETI instruction functions
- Instruction set supporting high-level language (C language) and multi-task operations
Introduction of system stack pointer
Symmetrical instruction set and barrel shift instructions
- Improved execution speed
4-byte queue
- Powerful interrupt functions
Eight priority levels programmable; External interrupts : 24
- Data transfer functions (μDMAC)
Up to 16 channels
- Built-in ROM
Flash ROM : 256, 384 and 512 Kbytes; MASK ROM : 256, 384 and 512 Kbytes
- Built-in RAM
Flash RAM : 16, 24 and 30 Kbytes; MASK RAM : 16, 24 and 30 Kbytes
- General-purpose ports
Dual clock product : up to 81 channels; Single clock product : up to 83 channels
- A/D converter
RC successive approximation conversion type : 20 channels (Resolution : 8 or 10 bits)
- Multi-function serial interface
7 channels (software switchable between for SIO, UART and I²C)
- 16-bit PPG
8 channels
- 8/16-bit up-down counter/timer
Event input pins : 6
8-bit up-down counters : 2
8-bit reload/compare registers : 2
- Base timer
4 channels (software switchable between 16-bit reload timer, PWC timer, PPG timer, and PWM timer)
- 16-bit I/O timer
Input capture × 2 channels, output compare × 6 channels, free run timer × 1 channel
- Built-in dual clock generator
- Low power consumption modes
Stop mode, sleep mode, CPU intermittent operation mode, watch timer, time base timer mode
- Package
QFP-100/LQFP-100
- Process
CMOS technology
- Power supply voltage
3V : Single power supply operation

MB90880 Series

■ PRODUCT LINEUP

Item Name		MB90882(S)	MB90883(S)	MB90884(S)	MB90F882(S)	MB90F883 (S) / MB90F883A (S)	MB90F884 (S) / MB90F884A (S)
Class		MASK ROM product			Flash memory product		
ROM size		256 Kbytes	384 Kbytes	512 Kbytes	256 Kbytes	384 Kbytes	512 Kbytes
RAM size		16 Kbytes	24 Kbytes	30 Kbytes	16 Kbytes	24 Kbytes	30 Kbytes
CPU functions		Number of instructions : 351 Instruction bit length : 8 bits, 16 bits Instruction length : 1 to 7 bytes Data bit length : 1 bit, 8 bits, 16 bits Minimum execution time : 30.3 ns (machine clock : 33 MHz) The maximum operating frequency of MB90F883(S) and MB90F884(S) is 25 MHz.					
Ports		General-purpose I/O ports : up to 81 for dual clock model, up to 83 for single clock model General-purpose I/O ports (CMOS output)					
Multi-function serial interface		7 channels (software switchable between SIO, UART & I ² C)					
16-bit PPG timer		8 channels					
8/16-bit up-down counter/timer		Event input pins : 6, 8-bit up-down counters : 2 8-bit reload/compare registers : 2					
16-bit I/O timer	16-bit free run timer	Number of channels : 1 Overflow interrupt					
	Output compare (OCU)	Number of channels : 6 Pin input source : Match signal of compare register					
	Input capture (ICU)	Number of channels : 2 Rewriting register by pin input (rising, falling or both edges)					
DTP/external interrupt circuit		External interrupt pins : 24 channels (edge/level support)					
Base timer		4 channels (software switchable between 16-bit reload timer, PWC timer, PPG timer, and PWM timer) In MB90F883(S) and MB90F884(S), P24/TIO0, P25/TIO1, P26/TIO2, and P27/TIO3 cannot be used as input function.					
Time base timer		18-bit counter Interrupt interval : 1.0 ms, 4.1 ms, 16.4 ms, 131.1 ms (source oscillation : 4 MHz)					
A/D converter		Conversion accuracy : 8 or 10 bits can be switched Single conversion mode (Selected channel converted only once) Scan conversion mode (Multiple successive channels converted) Successive conversion mode (Selected channel converted repeatedly) Stop conversion mode (Selected channel converted and stopped repeatedly)					
Watchdog timer		Reset generation interval : 3.58 ms, 14.33 ms, 57.23ms, 458.75 ms (source oscillation : 4 MHz, minimum value)					

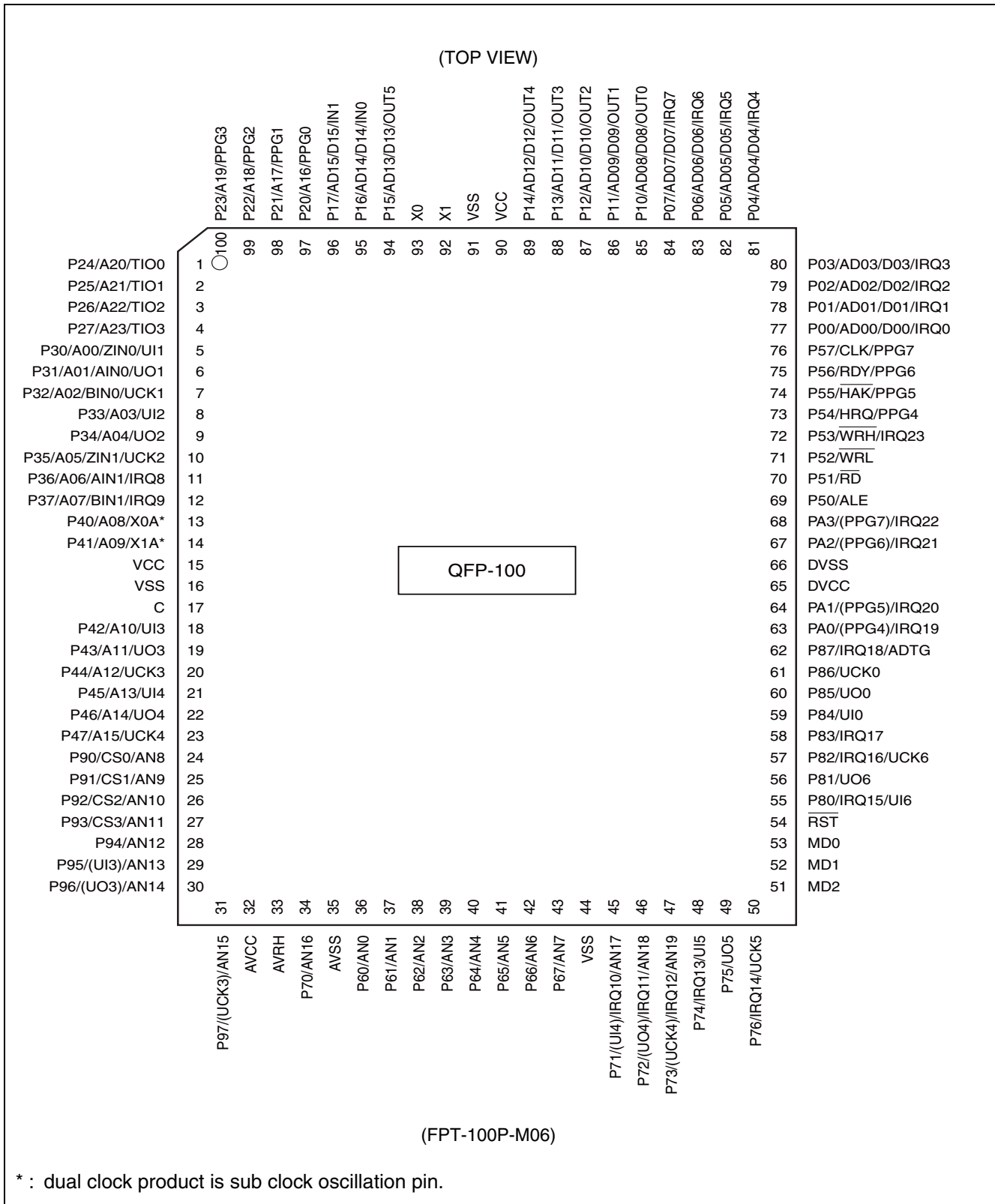
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MB90880 Series

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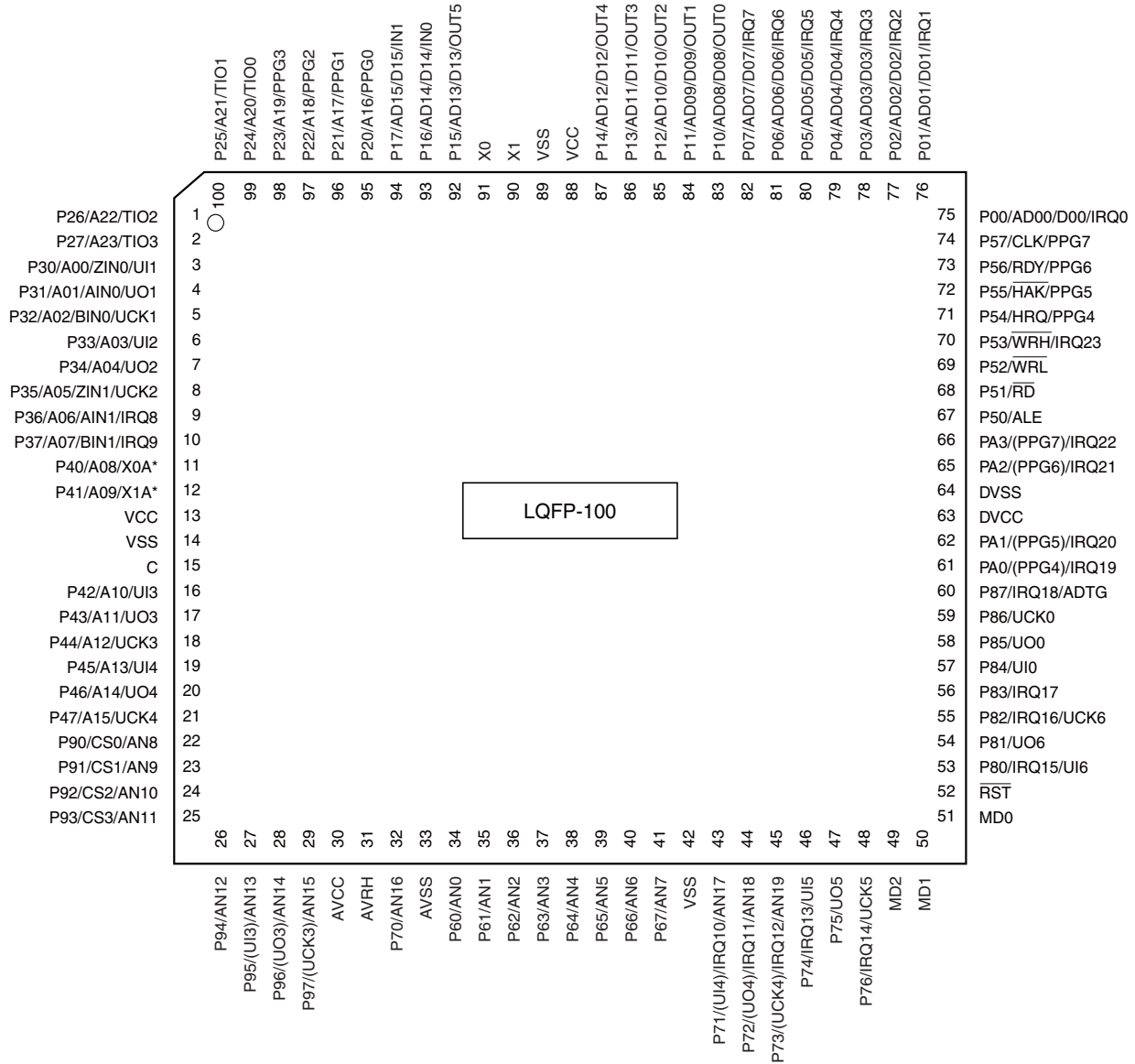
Item Name	MB90882 (S)	MB90883 (S)	MB90884 (S)	MB90F882 (S)	MB90F883 (S) / MB90F883A (S)	MB90F884 (S) / MB90F884A (S)
Low power consumption (standby) modes	Sleep, stop, CPU intermittent operation, watch timer, time base timer					
Flash memory	—			Flash security/ write-protect feature (not available in MB90F883(S), MB90F884(S), MB90F883A(S), and MB90F884A(S))		
Process	CMOS technology					

PIN ASSIGNMENTS



MB90880 Series

(TOP VIEW)



(FPT-100P-M20)

* : dual clock product is sub clock oscillation pin.

■ PIN DESCRIPTIONS

Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
1	3	P26	D	General-purpose I/O port
		A22		In multiplex mode, it serves as higher address output pin (A22) when corresponding bit in external address output control register (HACR) is set to "0".
				In non-multiplex mode, it serves as higher address output pin (A22) when corresponding bit in external address output control register (HACR) is set to "0".
		TIO2		Base timer I/O pin (ch.2)
2	4	P27	D	General-purpose I/O port
		A23		In multiplex mode, it serves as higher address output pin (A23) when corresponding bit in external address output control register (HACR) is set to "0".
				In non-multiplex mode, it serves as higher address output pin (A23) when corresponding bit in external address output control register (HACR) is set to "0".
		TIO3		Base timer I/O pin (ch.3)
3	5	P30	E	General-purpose I/O port
		A00		Serves as an external address pin in non-multiplex mode.
		ZIN0		8/16-bit up-down counter/timer input pin (ch.0)
		UI1		Multi-function serial input pin
4	6	P31	E	General-purpose I/O port
		A01		Serves as an external address pin in non-multiplex mode.
		AIN0		8/16-bit up-down counter/timer input pin (ch.0)
		UO1/ (SDA1)		Multi-function serial output pin
5	7	P32	E	General-purpose I/O port
		A02		Serves as an external address pin in non-multiplex mode.
		BIN0		8/16-bit up-down counter/timer input pin (ch.0)
		UCK1/ (SCL1)		Multi-function serial clock I/O pin
6	8	P33	E	General-purpose I/O port
		A03		Serves as an external address pin in non-multiplex mode.
		UI2		Multi-function serial input pin
7	9	P34	E	General-purpose I/O port
		A04		Serves as an external address pin in non-multiplex mode.
		UO2/ (SDA2)		Multi-function serial output pin

(Continued)

MB90880 Series

Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
8	10	P35	E	General-purpose I/O port
		A05		Serves as an external address pin in non-multiplex mode.
		ZIN1		8/16-bit up-down counter/timer input pin (ch.1)
		UCK2/(SCL2)		Multi-function serial clock I/O pin
9	11	P36	D	General-purpose I/O port
		A06		Serves as an external address pin in non-multiplex mode.
		AIN1		8/16-bit up-down counter/timer input pin (ch.1)
		IRQ8		External interrupt input pin
10	12	P37	D	General-purpose I/O port
		A07		Serves as an external address pin in non-multiplex mode.
		BIN1		8/16-bit up-down counter/timer input pin (ch.1)
		IRQ9		External interrupt input pin
11	13	P40	A/D	General-purpose I/O port
		A08		Serves as an external address pin in non-multiplex mode.
		X0A		32 kHz oscillator connecting pin
12	14	P41	A/D	General-purpose I/O port
		A09		Serves as an external address pin in non-multiplex mode.
		X1A		32 kHz oscillator connecting pin
13	15	VCC	-	Power supply pin
14	16	VSS	-	Power supply pin (GND)
15	17	C	-	Regulator stabilization capacity connecting pin
16	18	P42	E	General-purpose I/O port
		A10		Serves as an external address pin in non-multiplex mode.
		UI3		Multi-function serial input pin
17	19	P43	E	General-purpose I/O port
		A11		Serves as an external address pin in non-multiplex mode.
		UO3/(SDA3)		Multi-function serial output pin
18	20	P44	E	General-purpose I/O port
		A12		Serves as an external address pin in non-multiplex mode.
		UCK3/(SCL3)		Multi-function serial clock I/O pin
19	21	P45	E	General-purpose I/O port
		A13		Serves as an external address pin in non-multiplex mode.
		UI4		Multi-function serial input pin

(Continued)

MB90880 Series

Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
20	22	P46	E	General-purpose I/O port
		A14		Serves as an external address pin in non-multiplex mode.
		UO4/ (SDA4)		Multi-function serial output pin
21	23	P47	E	General-purpose I/O port
		A15		Serves as an external address pin in non-multiplex mode.
		UCK4/ (SCL4)		Multi-function serial clock I/O pin
22	24	P90	H	General-purpose I/O port
		CS0		Chip select 0
		AN8		Analog input pin
23	25	P91	H	General-purpose I/O port
		CS1		Chip select 1
		AN9		Analog input pin
24	26	P92	H	General-purpose I/O port
		CS2		Chip select 2
		AN10		Analog input pin
25	27	P93	H	General-purpose I/O port
		CS3		Chip select 3
		AN11		Analog input pin
26	28	P94	H	General-purpose I/O port
		AN12		Analog input pin
27	29	P95	K	General-purpose I/O port
		AN13		Analog input pin
		(UI3)		Multi-function serial input pin (when set by P9FSR register)
28	30	P96	K	General-purpose I/O port
		AN14		Analog input pin
		(UO3)/ (SDA3)		Multi-function serial output pin (when set by P9FSR register)
29	31	P97	K	General-purpose I/O port
		AN15		Analog input pin
		(UCK3)/ (SCL3)		Multi-function serial clock I/O pin (when set by P9FSR register)
30	32	AVCC	-	A/D converter power supply pin
31	33	AVRH	-	A/D converter external reference power supply pin
32	34	P70	H	General-purpose I/O port
		AN16		Analog input pin

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MB90880 Series

Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
33	35	AVSS	-	A/D converter power supply pin
34	36	P60	H	General-purpose I/O port
		AN0		Analog input pin
35	37	P61	H	General-purpose I/O port
		AN1		Analog input pin
36	38	P62	H	General-purpose I/O port
		AN2		Analog input pin
37	39	P63	H	General-purpose I/O port
		AN3		Analog input pin
38	40	P64	H	General-purpose I/O port
		AN4		Analog input pin
39	41	P65	H	General-purpose I/O port
		AN5		Analog input pin
40	42	P66	H	General-purpose I/O port
		AN6		Analog input pin
41	43	P67	H	General-purpose I/O port
		AN7		Analog input pin
42	44	VSS	-	Power supply pin (GND)
43	45	P71	K	General-purpose I/O port
		IRQ10		External interrupt input pin
		AN17		Analog input pin
		(UI4)		Multi-function serial input pin (when set by P7FSR register)
44	46	P72	K	General-purpose I/O port
		IRQ11		External interrupt input pin
		AN18		Analog input pin
		(UO4)/ (SDA4)		Multi-function serial output pin (when set by P7FSR register)
45	47	P73	K	General-purpose I/O port
		IRQ12		External interrupt input pin
		AN19		Analog input pin
		(UCK4)/ (SCL4)		Multi-function serial clock I/O pin (when set by F7FSR register)
46	48	P74	G	General-purpose I/O port
		IRQ13		External interrupt input pin
		UI5		Multi-function serial input pin

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
47	49	P75	G	General-purpose I/O port
		UO5/ (SDA5)		Multi-function serial output pin
48	50	P76	G	General-purpose I/O port
		IRQ14		External interrupt input pin
		UCK5/ (SCL5)		Multi-function serial clock I/O pin
49	51	MD2	L	Operation mode specification input pin
50	52	MD1	L	Operation mode specification input pin
51	53	MD0	L	Operation mode specification input pin
52	54	$\overline{\text{RST}}$	B	Reset input pin
53	55	P80	G	General-purpose I/O port
		IRQ15		External interrupt input pin
		UI6		Multi-function serial input pin
54	56	P81	G	General-purpose I/O port
		UO6/ (SDA6)		Multi-function serial output pin
55	57	P82	G	General-purpose I/O port
		IRQ16		External interrupt input pin
		UCK6/ (SCL6)		Multi-function serial clock I/O pin
56	58	P83	I	General-purpose I/O port
		IRQ17		External interrupt input pin
57	59	P84	G	General-purpose I/O port
		UI0		Multi-function serial input pin
58	60	P85	G	General-purpose I/O port
		UO0/ (SDA0)		Multi-function serial output pin
59	61	P86	G	General-purpose I/O port
		UCK0/ (SCL0)		Multi-function serial clock I/O pin
60	62	P87	I	General-purpose I/O port
		IRQ18		External interrupt input pin
		ADTG		External trigger input pin, when A/D converter is used.
61	63	PA0	J	General-purpose I/O port
		IRQ19		External interrupt input pin
		(PPG4)		PPG timer output pin (when set by PAFSR register)

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
62	64	PA1	J	General-purpose I/O port
		IRQ20		External interrupt input pin
		(PPG5)		PPG timer output pin (when set by PAFSR register)
63	65	DVCC	-	PA port power supply pin
64	66	DVSS	-	PA port power supply pin (GND)
65	67	PA2	J	General-purpose I/O port
		IRQ21		External interrupt input pin
		(PPG6)		PPG timer output pin (when set by PAFSR register)
66	68	PA3	J	General-purpose I/O port
		IRQ22		External interrupt input pin
		(PPG7)		PPG timer output pin (when set by PAFSR register)
67	69	P50	F	General-purpose I/O port
		ALE		Serves as address latch enable signal (ALE) pin in external bus mode.
68	70	P51	F	General-purpose I/O port
		$\overline{RD}$		Serves as read strobe output ($\overline{RD}$) pin in external bus mode.
69	71	P52	F	General-purpose I/O port
		$\overline{WRL}$		Serves as lower data write strobe output ($\overline{WRL}$) pin in external bus mode, and serves as a general-purpose I/O port when WRE bit in EPCR register is "0".
70	72	P53	F	General-purpose I/O port
		$\overline{WRH}$		Serves as higher data write strobe output ($\overline{WRH}$) pin in external bus mode with 16-bit bus width, and serves as a general-purpose I/O port when WRE bit in EPCR register is "0".
		IRQ23		External interrupt input pin
71	73	P54	F	General-purpose I/O port
		HRQ		Serves as hold request input (HRQ) pin in external bus mode, and serves as a general-purpose I/O port when HDE bit in EPCR register is "0".
		PPG4		PPG timer output pin
72	74	P55	F	General-purpose I/O port
		$\overline{HAK}$		Serves as hold acknowledge output ($\overline{HAK}$) pin in external bus mode, and serves as a general-purpose I/O port when HDE bit in EPCR register is "0".
		PPG5		PPG timer output pin

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
73	75	P56	F	General-purpose I/O port
		RDY		Serves as external ready input (RDY) pin in external bus mode, and serves as a general-purpose I/O port when RYE bit in EPCR register is "0".
		PPG6		PPG timer output pin
74	76	P57	F	General-purpose I/O port
		CLK		Serves as machine cycle clock output (CLK) pin in external bus mode, and serves as a general-purpose I/O port when CKE bit in EPCR register is "0".
		PPG7		PPG timer output pin
75	77	P00	C	General-purpose I/O port
		AD00/ D00		In multiplex mode, it serves as lower external address/data bus I/O pin.
		IRQ0		Serves as lower external data bus output pin in non-multiplex mode. External interrupt input pin
76	78	P01	C	General-purpose I/O port
		AD01/ D01		Serves as an external address/lower data bus I/O pin in multiplex mode.
		IRQ1		Serves as a lower external data bus output pin in non-multiplex mode. External interrupt input pin
77	79	P02	C	General-purpose I/O port
		AD02/ D02		Serves as an external address/lower data bus I/O pin in multiplex mode.
		IRQ2		Serves as a lower external data bus output pin in non-multiplex mode. External interrupt input pin
78	80	P03	C	General-purpose I/O port
		AD03/ D03		Serves as an external address/lower data bus I/O pin in multiplex mode.
		IRQ3		Serves as a lower external data bus output pin in non-multiplex mode. External interrupt input pin
79	81	P04	C	General-purpose I/O port
		AD04/ D04		In multiplex mode, it serves as lower external address/data bus I/O pin.
		IRQ4		Serves as a lower external data bus output pin in non-multiplex mode. External interrupt input pin

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MB90880 Series

Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
80	82	P05	C	General-purpose I/O port
		AD05/D05		In multiplex mode, it serves as lower external address/data bus I/O pin.
				Serves as a lower external data bus output pin in non-multiplex mode.
		IRQ5		External interrupt input pin
81	83	P06	C	General-purpose I/O port
		AD06/D06		In multiplex mode, it serves as lower external address/data bus I/O pin.
				Serves as a lower external data bus output pin in non-multiplex mode.
		IRQ6		External interrupt input pin
82	84	P07	C	General-purpose I/O port
		AD07/D07		In multiplex mode, it serves as lower external address/data bus I/O pin.
				Serves as a lower external data bus output pin in non-multiplex mode.
		IRQ7		External interrupt input pin
83	85	P10	C	General-purpose I/O port
		AD08/D08		In multiplex mode, it serves as higher external address/data bus I/O pin.
				In non-multiplex mode, it serves as higher external data output pin.
		OUT0		Output compare event output pin
84	86	P11	C	General-purpose I/O port
		AD09/D09		In multiplex mode, it serves as higher external address/data bus I/O pin.
				In non-multiplex mode, it serves as higher external data output pin.
		OUT1		Output compare event output pin
85	87	P12	C	General-purpose I/O port
		AD10/D10		In multiplex mode, it serves as higher external address/data bus I/O pin.
				In non-multiplex mode, it serves as higher external data output pin.
		OUT2		Output compare event output pin
86	88	P13	C	General-purpose I/O port
		AD11/D11		In multiplex mode, it serves as higher external address/data bus I/O pin.
				In non-multiplex mode, it serves as higher external data output pin.
		OUT3		Output compare event output pin

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MB90880 Series

Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
87	89	P14	C	General-purpose I/O port
		AD12/D12		In non-multiplex mode, it serves as higher external data output pin.
		OUT4		Output compare event output pin
88	90	VCC	-	Power supply pin
89	91	VSS	-	Power supply pin (GND)
90	92	X1	A	Main oscillator connecting pin
91	93	X0	A	Main oscillator connecting pin
92	94	P15	C	General-purpose I/O port
		AD13/D13		In multiplex mode, it serves as higher external address/data bus I/O pin.
				In non-multiplex mode, it serves as higher external data output pin.
		OUT5		Output compare event output pin
93	95	P16	C	General-purpose I/O port
		AD14/D14		In multiplex mode, it serves as higher external address/data bus I/O pin.
				In non-multiplex mode, it serves as higher external data output pin.
		IN0		Trigger input pin for input capture ch.0
94	96	P17	C	General-purpose I/O port
		AD15/D15		In multiplex mode, it serves as higher external address/data bus I/O pin.
				In non-multiplex mode, it serves as higher external data output pin.
		IN1		Trigger input pin for input capture ch.1
95	97	P20	D	General-purpose I/O port
		A16		In multiplex mode, it serves as higher address output pin (A16) when corresponding bit in external address output control register (HACR) is set to "0".
				In non-multiplex mode, it serves as higher address output pin (A16) when corresponding bit in external address output control register (HACR) is set to "0".
		PPG0		PPG timer output pin
96	98	P21	D	General-purpose I/O port
		A17		In multiplex mode, it serves as higher address output pin (A17) when corresponding bit in external address output control register (HACR) is set to "0".
				In non-multiplex mode, it serves as higher address output pin (A17) when corresponding bit in external address output control register (HACR) is set to "0".
		PPG1		PPG timer output pin

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MB90880 Series

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Pin no.		Pin name	I/O circuit type*3	Function
LQFP *1	QFP *2			
97	99	P22	D	General-purpose I/O port
		A18		In multiplex mode, it serves as higher address output pin (A18) when corresponding bit in external address output control register (HACR) is set to "0".
				In non-multiplex mode, it serves as higher address output pin (A18) when corresponding bit in external address output control register (HACR) is set to "0".
		PPG2		PPG timer output pin
98	100	P23	D	General-purpose I/O port
		A19		In multiplex mode, it serves as higher address output pin (A19) when corresponding bit in external address output control register (HACR) is set to "0".
				In non-multiplex mode, it serves as higher address output pin (A19) when corresponding bit in external address output control register (HACR) is set to "0".
		PPG3		PPG timer output pin
99	1	P24	D	General-purpose I/O port
		A20		In multiplex mode, it serves as higher address output pin (A20) when corresponding bit in external address output control register (HACR) is set to "0".
				In non-multiplex mode, it serves as higher address output pin (A20) when corresponding bit in external address output control register (HACR) is set to "0".
		TIO0		Base timer I/O pin (ch.0)
100	2	P25	D	General-purpose I/O port
		A21		In multiplex mode, it serves as higher address output pin (A21) when corresponding bit in external address output control register (HACR) is set to "0".
				In non-multiplex mode, it serves as higher address output pin (A21) when corresponding bit in external address output control register (HACR) is set to "0".
		TIO1		Base timer I/O pin (ch.1)

*1 : LQFP : FPT-100P-M20

*2 : QFP : FPT-100P-M06

*3 : For the I/O circuit type, refer to "■ I/O CIRCUIT TYPE".

I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	X1, X1A X0, X0A P-ch N-ch Xout Standby control signal	- Oscillation feedback resistance X1, X0 : approx. 1 MΩ X1A, X0A : approx. 10 MΩ - Standby control provided
B	R R Hysteresis input	Hysteresis input with pull-up resistor
C	Pull-up control signal P-ch N-ch R CMOS input Hysteresis input Standby control for input shutdown	- Input pull-up resistor control provided - CMOS level output - Hysteresis input - CMOS input (in external bus mode)
D	P-ch N-ch R Hysteresis input Standby control for input shutdown	- CMOS level output - Hysteresis input
E	P-ch N-ch R Hysteresis input I²C level hysteresis input Standby control for input shutdown	- CMOS level output - Hysteresis input - I²C level hysteresis input

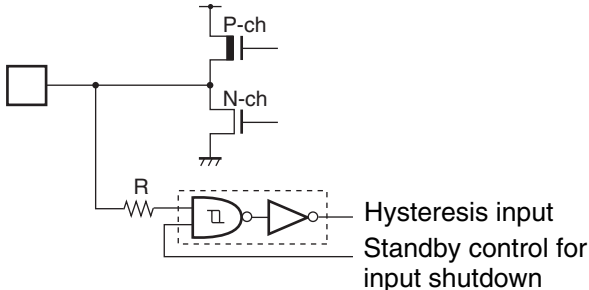
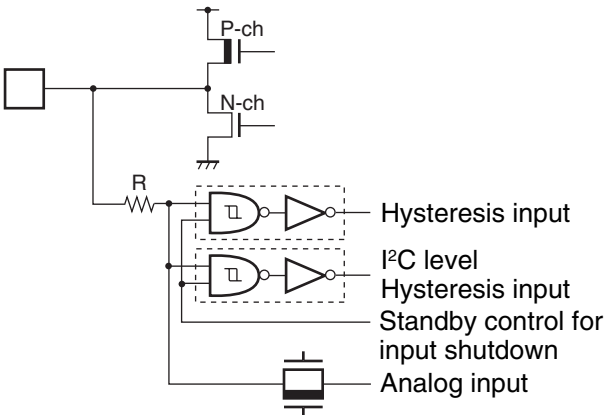
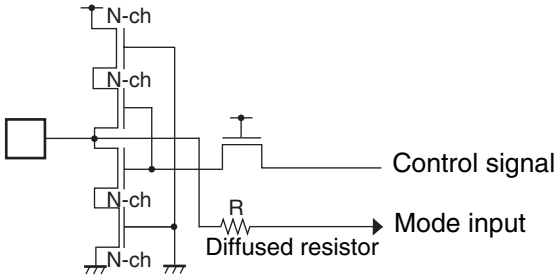
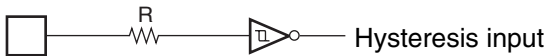
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MB90880 Series

Type	Circuit	Remarks
F	CMOS input Hysteresis input Standby control for input shutdown	• CMOS level output • Hysteresis input • CMOS input (in external bus mode)
G	Open-drain control signal Hysteresis input I²C level hysteresis input Standby control for input shutdown	• CMOS level output (Open-drain control provided) • 5V tolerant • Hysteresis input • I²C level hysteresis input
H	Hysteresis input Standby control for input shutdown Analog input	• CMOS level output • Hysteresis input • Analog input
I	Open-drain control signal Hysteresis input Standby control for input shutdown	• CMOS level output (Open-drain control provided) • 5V tolerant • Hysteresis input

(Continued)

(Continued)

Type	Circuit	Remarks
J		• CMOS/level output (high-current type) • Hysteresis input
K		• CMOS level output • Hysteresis input • Analog input • I²C level hysteresis input
L	Flash memory product 	Flash memory product • CMOS level input • High-voltage control for flash test provided
	MASK ROM product 	MASK ROM product Hysteresis input

■ HANDLING DEVICES

1. Maximum rated voltages for the prevention of latch-up

Be cautious not to exceed the absolute maximum rating.

CMOS ICs may cause latch-up, when a voltage higher than V_{CC} or lower than V_{SS} is applied to input or output pins other than medium-to-high resistant pins, or when a voltage exceeding the rating is applied between V_{CC} and V_{SS} pins.

If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Take the utmost care not to let it occur.

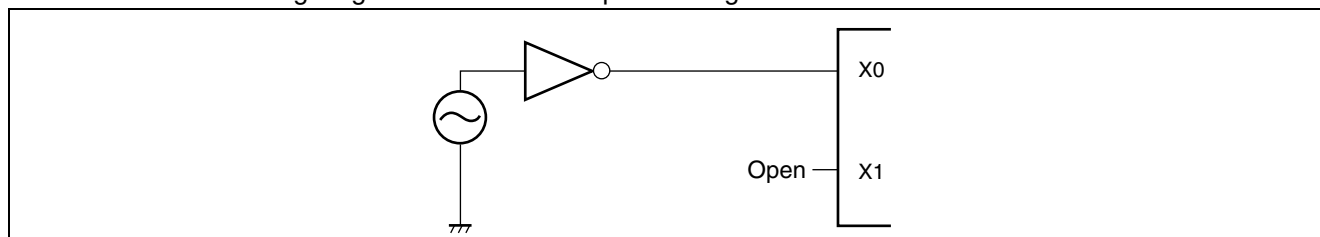
Likewise, care must be taken not to allow the analog power supply (AV_{CC} , $AVRH$) and analog input to exceed the digital power supply (V_{CC}) when turning on or off any analog system.

2. Handling unused pins

Leaving unused input pins open may cause a malfunction or latch-up which leads to fatal damage to the device. Therefore, they must be pulled up or down through at least $2\text{ k}\Omega$ resistance. Also, any unused I/O pin should be left open in the output state, or set to the input state and handled in the same way as an unused input pin.

3. Notes on using external clock

Even when an external clock is being used, oscillation stabilization wait time is required for a power-on reset or release from sub clock mode or stop mode. Note that 25 MHz is the upper limit on the external clock that can be used. The following diagram shows an example of using an external clock.



4. Handling power supply pins (V_{CC}/V_{SS})

When multiple V_{CC} and V_{SS} pins supply pins are used, all the power supply pins must be connected to external power and ground lines due to the device design, to reduce latch-up and unwanted radiation, prevent abnormal operation of strobe signals caused by the rise in the ground level and to conform to the total output current rating. Make sure to connect the V_{CC} and V_{SS} pins of this device via lowest impedance to power lines. It is recommended that a bypass capacitor of around $0.1\text{ }\mu\text{F}$ be placed between the V_{CC} and V_{SS} pins near the device.

5. Crystal oscillator circuit

Noises around X0/X1 or X0A/X1A pins may cause abnormal operations. It is strongly recommended to provide bypass capacitors via shortest distance from X0/X1, X0A/X1A pins, crystal oscillator (or ceramic oscillator) and ground lines and also not to allow the lines of the oscillation circuit to cross the lines of other circuits. This will ensure stable operations of the printed circuit boards. Please ask each crystal maker to evaluate the oscillational characteristics of the crystal and this device.

6. Notes on PLL clock mode operation

If an oscillator comes off or clock input stops during PLL clock mode operation, this microcontroller may continue its operation using a free-running frequency from a self-excited oscillation circuit within PLL. This is not a guaranteed operation.

7. Power-on and power-off sequence of A/D converter and analog input

Turn on the A/D converters (AV_{CC} , $AVRH$) and analog inputs ($AN0$ to $AN19$) after turning on the digital power supply (V_{CC}) .

During power-off, turn off the digital power supply (V_{CC}) after turning off the A/D converters and analog inputs ($AN0$ to $AN19$) .

In this case, make sure that $AVRH$ does not exceed AV_{CC} during the power-on/power-off procedure.

Also make sure that the input voltage does not exceed AV_{CC} when a pin which is also used as an analog input is used as an input port.

8. Handling power supply pins on A/D converter-mounted models

Make sure to achieve " $AV_{CC} = AVRH = V_{CC}$ " and " $AV_{SS} = V_{SS}$ " in connecting the circuits, even when not using the A/D converter function.

9. Note on power-up

To prevent the internal regulator from malfunctioning, maintain the voltage rise time at $50\ \mu s$ (between 0.2V and 2.7V) or more during power-up.

10. Stabilization of power supply

Even when the V_{CC} power supply voltage is within the specified operating range, it may still cause the device to malfunction, if the power supply changes rapidly. For stabilization reference, it is recommended to control the supply voltage so that V_{CC} ripple variations (P-P values) at commercial frequencies (50/60 Hz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

11. Writing to Flash memory

For serial writing to Flash memory, always make sure that the operating voltage V_{CC} is between 3.13V and 3.6V.

For normal writing to Flash memory, always make sure that the operating voltage V_{CC} is between 3.0V and 3.6V.

12. P90/CS0 pins

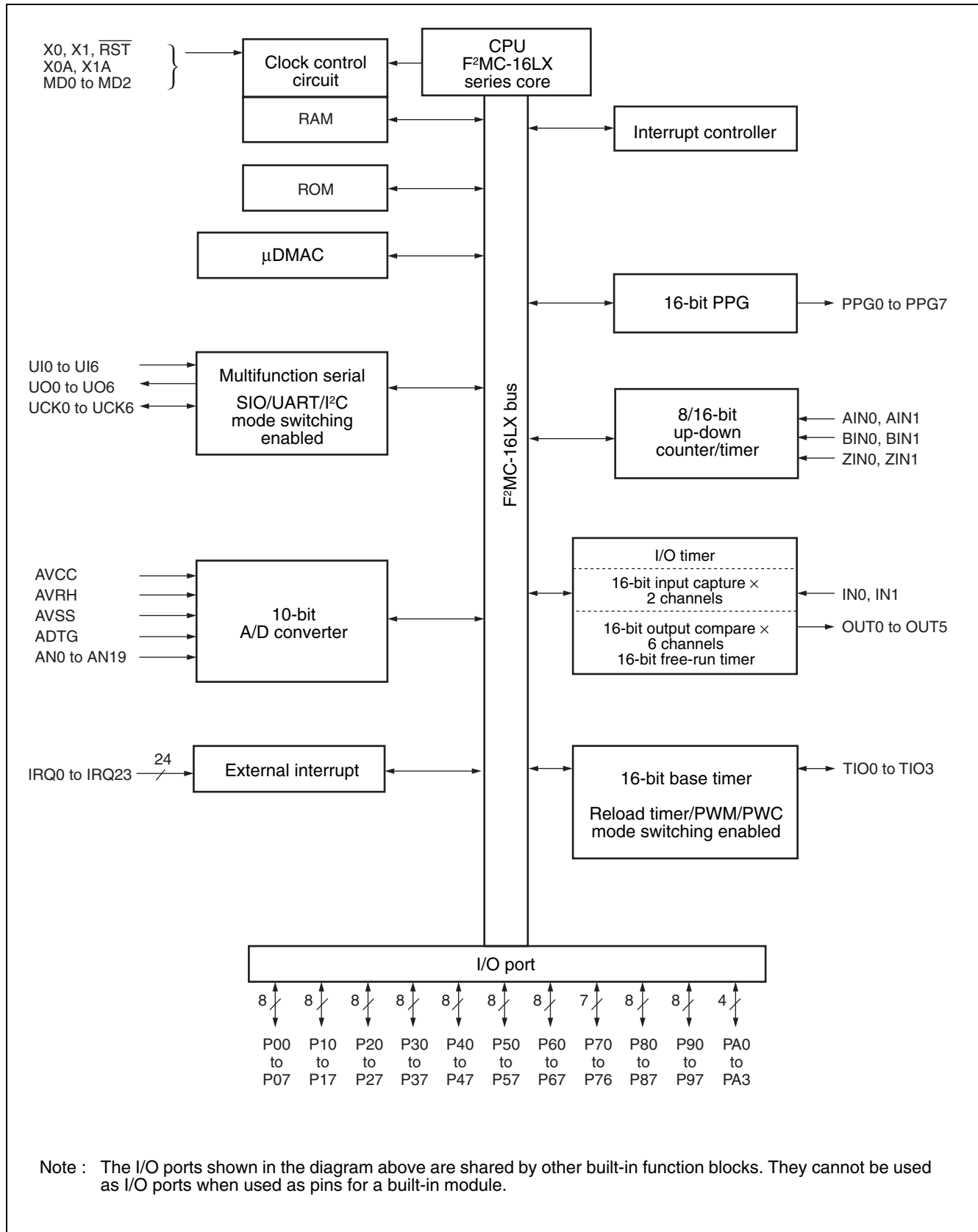
P90/CS0 pins output "L" during writing Flash serial. Do not input from external.

13. Note of MB90F883 (S) , MB90F884 (S)

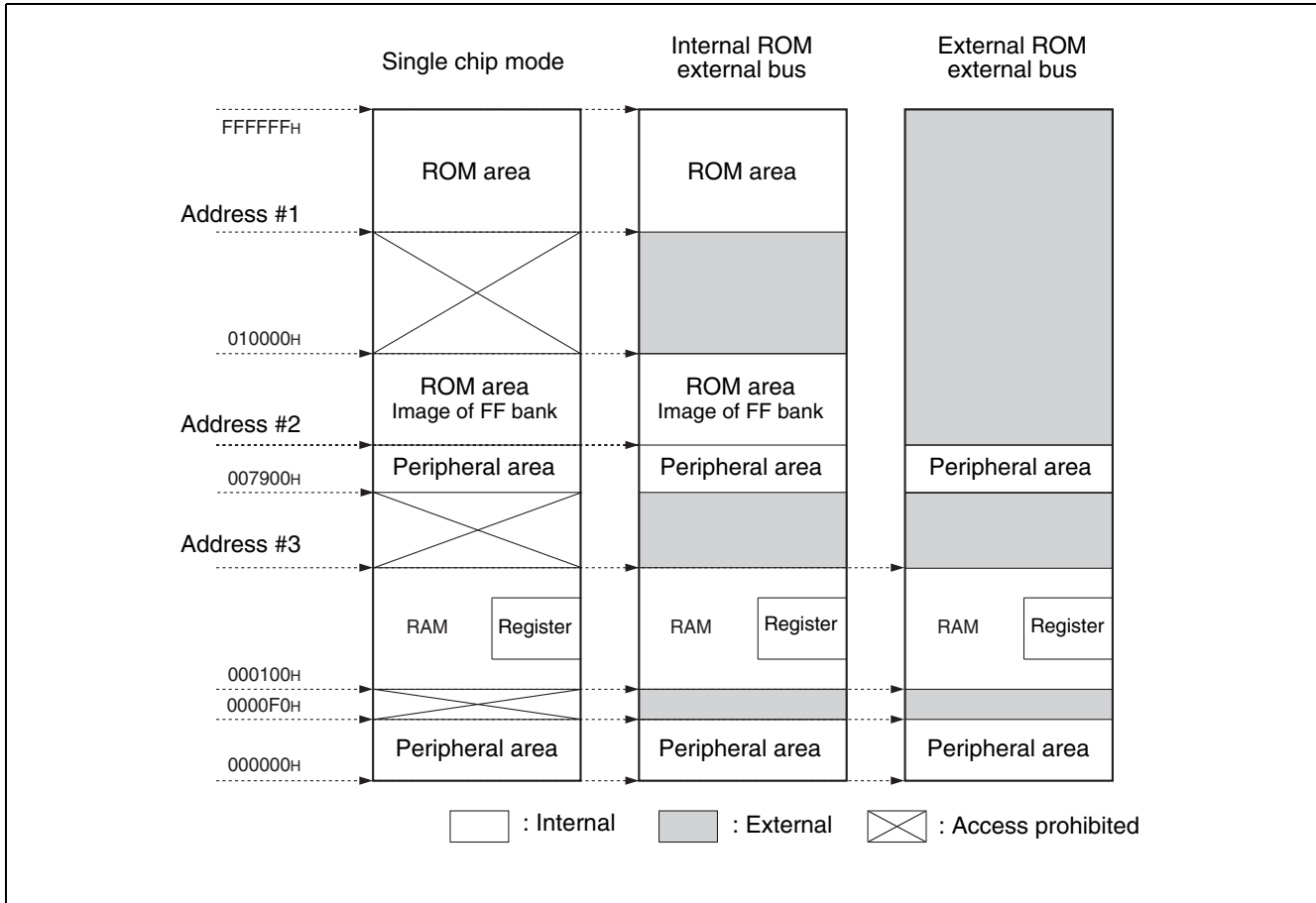
- Maximum operating frequency is 25 MHz.
- The base timer cannot use P24/TIO0, P25/TIO1, P26/TIO2, and P27/TIO3 as input function.
- MB90F883(S) and MB90F884(S) do not contain the flash security feature and write-protect feature.

MB90880 Series

■ BLOCK DIAGRAM



■ MEMORY MAP



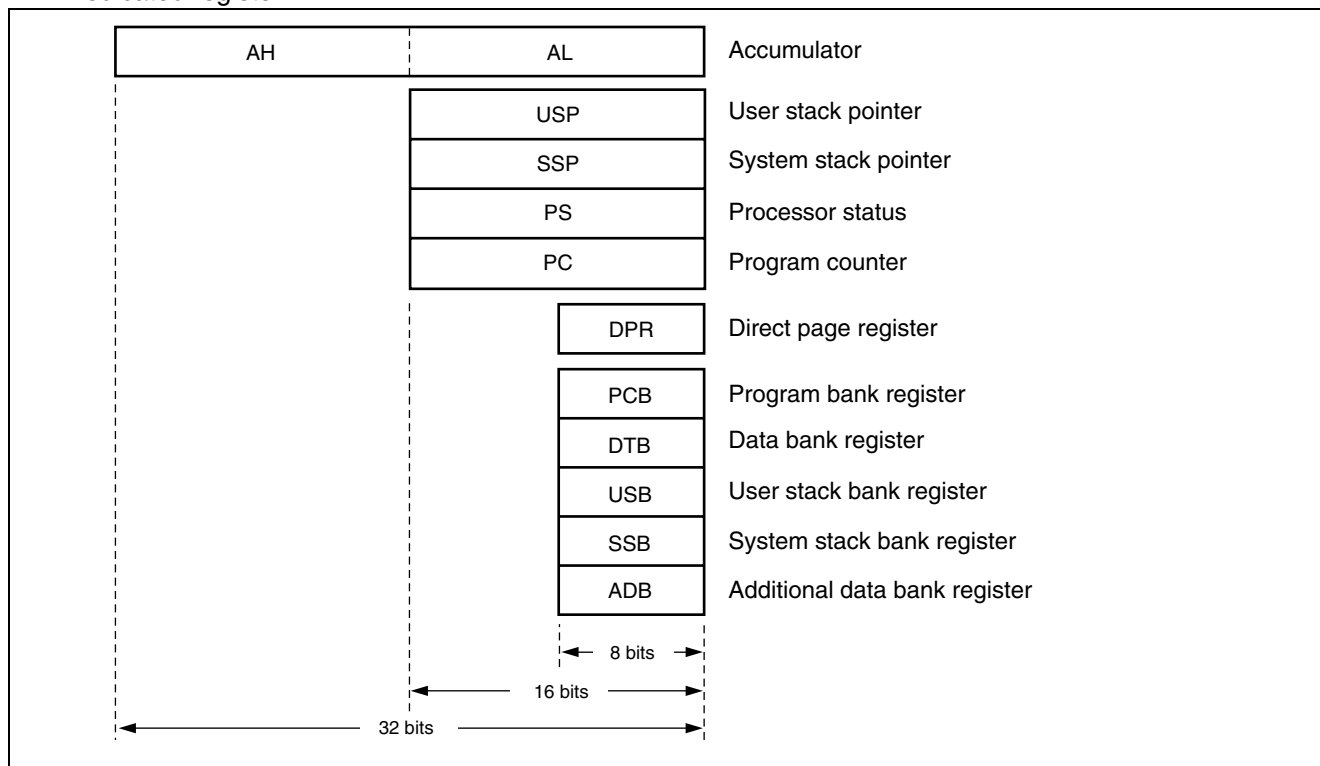
Parts No.	Address #1	Address #2	Address #3
MB90882 (S)	FC0000 _H	008000 _H , fixed	004100 _H
MB90F882 (S)	FC0000 _H		004100 _H
MB90883 (S)	FA0000 _H		006100 _H
MB90F883 (S) / MB90F883A (S)	FA0000 _H		006100 _H
MB90884 (S)	F80000 _H		007900 _H
MB90F884 (S) / MB90F884A (S)	F80000 _H		007900 _H
MB90V880 (S)	(F80000 _H)		007900 _H

Note : The image of the ROM data in the FF band appears at the top of the 00 bank in order to enable efficient use of the C compiler small memory model. The lower 16-bit address for the FF bank will be assigned to the same address, so that tables in ROM can be referenced without declaring a "far" indication with the pointer. For example, when accessing the address 00C000_H, the actual access is to address FFC000_H in ROM. Here the FF bank ROM area exceeds 32 Kbytes, it is not possible to see the entire area in the 00 bank image. Therefore, the ROM data in FF8000_H to FFFFFFF_H can be seen in the 00 bank image, while the data in FF0000_H to FF7FFF_H can only be seen in the FF bank.

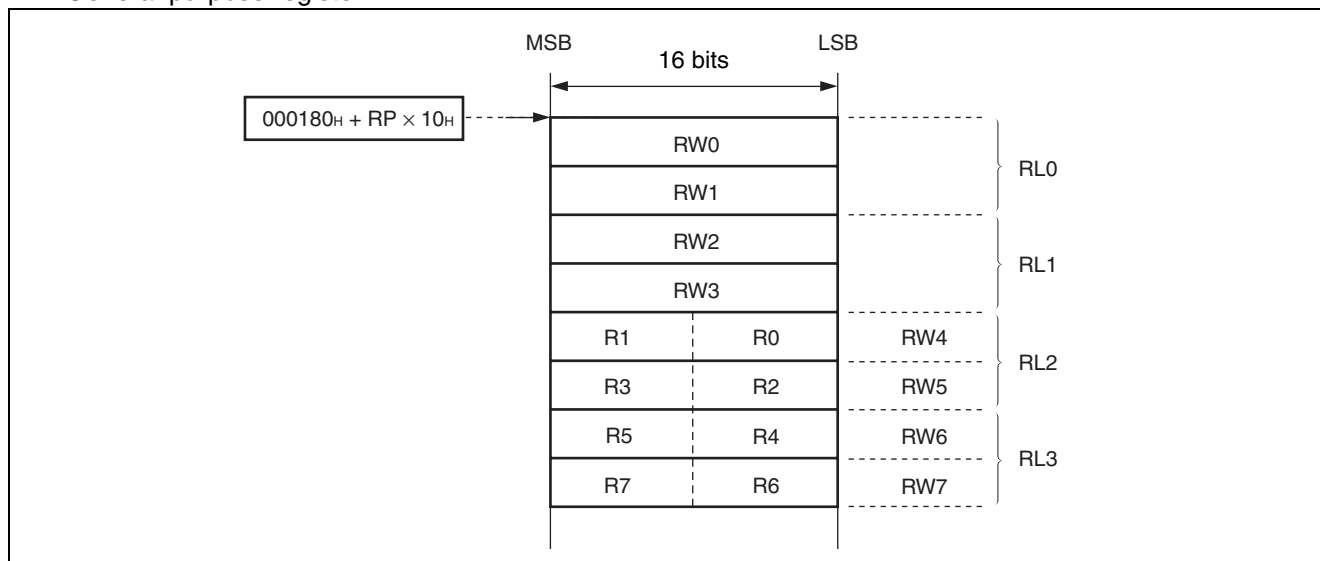
MB90880 Series

■ F²MC-16L CPU PROGRAMMING MODEL

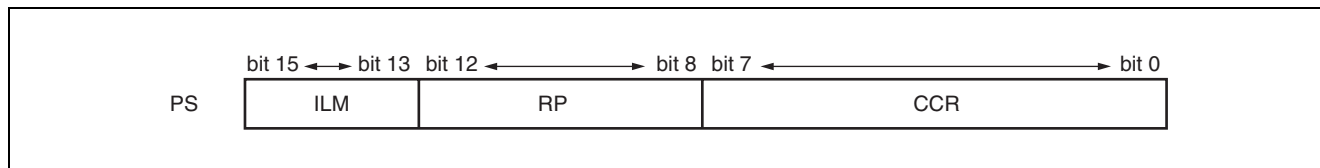
• Dedicated register



• General-purpose register



• Processor status



■ I/O MAP

Address	Register abbreviation	Register name	R/W	Resource	Initial value
000000 _H	PDR0	Port 0 data register	R/W	Port 0	XXXXXXXX _B
000001 _H	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXX _B
000002 _H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXX _B
000003 _H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXX _B
000004 _H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXX _B
000005 _H	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXX _B
000006 _H	PDR6	Port 6 data register	R/W	Port 6	XXXXXXXX _B
000007 _H	PDR7	Port 7 data register	R/W	Port 7	XXXXXXXX _B
000008 _H	PDR8	Port 8 data register	R/W	Port 8	XXXXXXXX _B
000009 _H	PDR9	Port 9 data register	R/W	Port 9	XXXXXXXX _B
00000A _H	PDRA	Port A data register	R/W	Port A	XXXXXXXX _B
00000B _H	UDER	Up-down timer input enable register	R/W	Up-down timer input control	XX000000 _B
00000C _H	ILSR0	Serial input level selection register 0	R/W	Multi-function serial control	00000000 _B
00000D _H	ILSR1	Serial input level selection register 1	R/W		00000000 _B
00000E _H	ILSR2	Serial input level selection register 2	R/W		---00000 _B
00000F _H	Disabled				
000010 _H	DDR0	Port 0 direction register	R/W	Port 0	00000000 _B
000011 _H	DDR1	Port 1 direction register	R/W	Port 1	00000000 _B
000012 _H	DDR2	Port 2 direction register	R/W	Port 2	00000000 _B
000013 _H	DDR3	Port 3 direction register	R/W	Port 3	00000000 _B
000014 _H	DDR4	Port 4 direction register	R/W	Port 4	00000000 _B
000015 _H	DDR5	Port 5 direction register	R/W	Port 5	00000000 _B
000016 _H	DDR6	Port 6 direction register	R/W	Port 6	00000000 _B
000017 _H	DDR7	Port 7 direction register	R/W	Port 7	-0000000 _B
000018 _H	DDR8	Port 8 direction register	R/W	Port 8	00000000 _B
000019 _H	DDR9	Port 9 direction register	R/W	Port 9	00000000 _B
00001A _H	DDRA	Port A direction register	R/W	Port A	----0000 _B
00001B _H	ADER0	Analog input enable register 0	R/W	Port 6, A/D	11111111 _B
00001C _H	ADER1	Analog input enable register 1	R/W	Port 9, A/D	11111111 _B
00001D _H	ADER2	Analog input enable register 2	R/W	Port 7, A/D	----1111 _B
00001E _H	RDR0	Port 0 input resistance register	R/W	Port 0 (pull-up resistance control)	00000000 _B
00001F _H	RDR1	Port 1 input resistance register	R/W	Port 1 (pull-up resistance control)	00000000 _B

(Continued)

MB90880 Series

Address	Register abbreviation	Register name	R/W	Resource	Initial value
000020 _H	SMR0	Serial bus mode register ch.0	R/W	Multi-function serial ch.0	\$\$\$\$\$\$\$\$ _B
000021 _H	SCR0/IBCR0	SCR0/IBCR0 serial bus control register/I ² C bus control register ch.0	R/W		\$\$\$\$\$\$\$\$ _B
000022 _H	ESCR0/IBSR0	Extended communication control register/I ² C bus status register ch.0	R/W		\$\$\$\$\$\$\$\$ _B
000023 _H	SSR0	Serial status register ch.0	R/W		\$\$\$\$\$\$\$\$ _B
000024 _H	RDR00/TDR00	Transmission/reception data register 0 ch.0	R,W		\$\$\$\$\$\$\$\$ _B
000025 _H	RDR10/TDR10	Transmission/reception data register 1 ch.0	R,W		\$\$\$\$\$\$\$\$ _B
000026 _H	BGR00	Baud rate generator register 0 ch.0	R/W		\$\$\$\$\$\$\$\$ _B
000027 _H	BGR10	Baud rate generator register 1 ch.0	R/W		\$\$\$\$\$\$\$\$ _B
000028 _H	ISBA0	7-bit slave address register ch.0	R/W		00000000 _B
000029 _H	ISMK0	7-bit slave address mask register ch.0	R/W		01111111 _B
00002A _H	SMR1	Serial bus mode register ch.1	R/W	Multi-function serial ch.1	\$\$\$\$\$\$\$\$ _B
00002B _H	SCR1/IBCR1	Serial bus control register / I ² C bus control register ch.1	R/W		\$\$\$\$\$\$\$\$ _B
00002C _H	ESCR1/IBSR1	Extended communication control register / I ² C bus status register ch.1	R/W		\$\$\$\$\$\$\$\$ _B
00002D _H	SSR1	Serial status register ch.1	R/W		\$\$\$\$\$\$\$\$ _B
00002E _H	RDR01/TDR01	Transmission/reception data register 0 ch.1	R,W		\$\$\$\$\$\$\$\$ _B
00002F _H	RDR11/TDR11	Transmission/reception data register 1 ch.1	R,W		\$\$\$\$\$\$\$\$ _B
000030 _H	BGR01	Baud rate generator register 0 ch.1	R/W		\$\$\$\$\$\$\$\$ _B
000031 _H	BGR11	Baud rate generator register 1 ch.1	R/W		\$\$\$\$\$\$\$\$ _B
000032 _H	ISBA1	7-bit slave address register ch.1	R/W		00000000 _B
000033 _H	ISMK1	7-bit slave address mask register ch.1	R/W		01111111 _B
000034 _H	ADCSL	Lower A/D control status register	R/W	A/D Converter	00011110 _B
000035 _H	ADCSH	Higher A/D control status register	R/W		00000000 _B
000036 _H	ADCRL	Lower A/D data register	R		XXXXXXXX _B
000037 _H	ADCRH	Higher A/D data register	R		111111XX _B
000038 _H	ADSRL	Lower A/D conversion channel setting register	R/W		00000000 _B
000039 _H	ADSRH	Higher A/D conversion channel setting register	R/W		00000000 _B
00003A _H	Reserved				

(Continued)

MB90880 Series

Address	Register abbreviation	Register name	R/W	Resource	Initial value
00003B _H	PACSR1	Address detection control status register 1	R/W	Address match detection function	00000000 _B
00003C _H	OLSR0	Output level selection register 0	R/W	Port 7 (N-ch open-drain control)	-000---- _B
00003D _H	OLSR1	Output level selection register 1	R/W	Port 8 (N-ch open-drain control)	00000000 _B
00003E _H	SMR2	Serial bus mode register ch.2	R/W	Multi-function serial ch.2	\$\$\$\$\$\$\$\$ _B
00003F _H	SCR2/IBCR2	Serial bus control register / I ² C bus control register ch.2	R/W		\$\$\$\$\$\$\$\$ _B
000040 _H	ESCR2/IBSR2	Extended communication control register / I ² C bus status register ch.2	R/W		\$\$\$\$\$\$\$\$ _B
000041 _H	SSR2	Serial status register ch.2	R/W		\$\$\$\$\$\$\$\$ _B
000042 _H	RDR02/TDR02	Transmission/reception data register 0 ch.2	R,W		\$\$\$\$\$\$\$\$ _B
000043 _H	RDR12/TDR12	Transmission/reception data register 1 ch.2	R,W		\$\$\$\$\$\$\$\$ _B
000044 _H	BGR02	Baud rate generator register 0 ch.2	R/W		\$\$\$\$\$\$\$\$ _B
000045 _H	BGR12	Baud rate generator register 1 ch.2	R/W		\$\$\$\$\$\$\$\$ _B
000046 _H	ISBA2	7-bit slave address register ch.2	R/W		00000000 _B
000047 _H	ISMK2	7-bit slave address mask register ch.2	R/W		01111111 _B
000048 _H	SMR3	Serial bus mode register ch.3	R/W	Multi-function serial ch.3	\$\$\$\$\$\$\$\$ _B
000049 _H	SCR3/IBCR3	Serial bus control register / I ² C bus control register ch.3	R/W		\$\$\$\$\$\$\$\$ _B
00004A _H	ESCR3/IBSR3	Extended communication control register / I ² C bus status register ch.3	R/W		\$\$\$\$\$\$\$\$ _B
00004B _H	SSR3	Serial status register ch.3	R/W		\$\$\$\$\$\$\$\$ _B
00004C _H	RDR03/TDR03	Transmission/reception data register 0 ch.3	R,W		\$\$\$\$\$\$\$\$ _B
00004D _H	RDR13/TDR13	Transmission/reception data register 1 ch.3	R,W		\$\$\$\$\$\$\$\$ _B
00004E _H	BGR03	Baud rate generator register 0 ch.3	R/W		\$\$\$\$\$\$\$\$ _B
00004F _H	BGR13	Baud rate generator register 1 ch.3	R/W		\$\$\$\$\$\$\$\$ _B
000050 _H	ISBA3	7-bit slave address register ch.3	R/W		00000000 _B
000051 _H	ISMK3	7-bit slave address mask register ch.3	R/W		01111111 _B
000052 _H	SMR4	Serial bus mode register ch.4	R/W	Multi-function serial ch.4	\$\$\$\$\$\$\$\$ _B
000053 _H	SCR4/IBCR4	Serial bus control register / I ² C bus control register ch.4	R/W		\$\$\$\$\$\$\$\$ _B

(Continued)

MB90880 Series

Address	Register abbreviation	Register name	R/W	Resource	Initial value	
000054 _H	ESCR4/ IBSR4	Extended communication control register / I ² C bus status register ch.4	R/W	Multi-function serial ch.4	\$\$\$\$\$\$\$\$ _B	
000055 _H	SSR4	Serial status register ch.4	R/W		\$\$\$\$\$\$\$\$ _B	
000056 _H	RDR04/ TDR04	Transmission/reception data register 0 ch.4	R,W		\$\$\$\$\$\$\$\$ _B	
000057 _H	RDR14/ TDR14	Transmission/reception data register 1 ch.4	R,W		\$\$\$\$\$\$\$\$ _B	
000058 _H	BGR04	Baud rate generator register 0 ch.4	R/W		\$\$\$\$\$\$\$\$ _B	
000059 _H	BGR14	Baud rate generator register 1 ch.4	R/W		\$\$\$\$\$\$\$\$ _B	
00005A _H	ISBA4	7-bit slave address register ch.4	R/W		00000000 _B	
00005B _H	ISMK4	7-bit slave address mask register ch.4	R/W		01111111 _B	
00005C _H	SMR5	Serial bus mode register ch.5	R/W	Multi-function serial ch.5	\$\$\$\$\$\$\$\$ _B	
00005D _H	SCR5/IBCR5	Serial bus control register / I ² C bus control register ch.5	R/W		\$\$\$\$\$\$\$\$ _B	
00005E _H	ESCR5/ IBSR5	Extended communication control register / I ² C bus status register ch.5	R/W		\$\$\$\$\$\$\$\$ _B	
00005F _H	SSR5	Serial status register ch.5	R/W		\$\$\$\$\$\$\$\$ _B	
000060 _H	RDR05/ TDR05	Transmission/reception data register 0 ch.5	R,W		\$\$\$\$\$\$\$\$ _B	
000061 _H	RDR15/ TDR15	Transmission/reception data register 1 ch.5	R,W		\$\$\$\$\$\$\$\$ _B	
000062 _H	BGR05	Baud rate generator register 0 ch.5	R/W		\$\$\$\$\$\$\$\$ _B	
000063 _H	BGR15	Baud rate generator register 1 ch.5	R/W		\$\$\$\$\$\$\$\$ _B	
000064 _H	ISBA5	7-bit slave address register ch.5	R/W		00000000 _B	
000065 _H	ISMK5	7-bit slave address mask register ch.5	R/W		01111111 _B	
000066 _H	OCCP0	Lower output compare register (ch.0)	R/W	16-bit I/O timer output compare (ch.0 to ch.5)	00000000 _B	
000067 _H		Higher output compare register (ch.0)			00000000 _B	
000068 _H	OCCP1	Lower output compare register (ch.1)	R/W		00000000 _B	
000069 _H		Higher output compare register (ch.1)			00000000 _B	
00006A _H	OCCP2	Lower output compare register (ch.2)	R/W		00000000 _B	
00006B _H		Higher output compare register (ch.2)			00000000 _B	
00006C _H	OCCP3	Lower output compare register (ch.3)	R/W		00000000 _B	
00006D _H		Higher output compare register (ch.3)			00000000 _B	
00006E _H	Reserved					
00006F _H	ROMM	ROM mirror function selection register	R/W		ROM mirror function	-----1 _B

(Continued)

MB90880 Series

Address	Register abbreviation	Register name	R/W	Resource	Initial value
000070 _H	OCCP4	Lower output compare register (ch.4)	R/W	16-bit I/O timer output compare (ch.0 to ch.5)	00000000 _B
000071 _H		Higher output compare register (ch.4)			00000000 _B
000072 _H	OCCP5	Lower output compare register (ch.5)	R/W		00000000 _B
000073 _H		Higher output compare register (ch.5)			00000000 _B
000074 _H	OCS01	Lower output compare control register (ch.0, ch.1)	R/W		0000--00 _B
000075 _H		Higher output compare control register (ch.0, ch.1)	R/W		---00000 _B
000076 _H	OCS23	Lower output compare control register (ch.2, ch.3)	R/W		0000--00 _B
000077 _H		Higher output compare control register (ch.2, ch.3)	R/W		---00000 _B
000078 _H	OCS45	Lower output compare control register (ch.4, ch.5)	R/W		0000--00 _B
000079 _H		Higher output compare control register (ch.4, ch.5)	R/W		---00000 _B
00007A _H	IPCP0	Lower input capture data register (ch.0)	R	6-bit I/O timer input capture (ch.0, ch.1)	XXXXXXXX _B
00007B _H		Higher input capture data register (ch.0)	R		XXXXXXXX _B
00007C _H	IPCP1	Lower input capture data register (ch.1)	R		XXXXXXXX _B
00007D _H		Higher input capture data register (ch.1)	R		XXXXXXXX _B
00007E _H	ICS01	Input capture control status register	R/W		00000000 _B
00007F _H	ICE01	Input capture edge register	R		-----XX _B
000080 _H	TCDT	Lower timer counter data register	R/W	16-bit I/O timer free-run timer	00000000 _B
000081 _H	TCDT	Higher timer counter data register	R/W		00000000 _B
000082 _H	TCCS	Timer control status register	R/W		00000000 _B
000083 _H	TCCS	Timer control status register	R/W		XX-00000 _B
000084 _H	CPCLR	Lower compare clear register	R/W		XXXXXXXX _B
000085 _H		Higher compare clear register			XXXXXXXX _B
000086 _H to 00009A _H	Reserved				
00009B _H	DCSR	DMAC descriptor channel specification register	R/W	DMAC	00000000 _B
00009C _H	DSRL	DMAC lower status register	R/W	DMAC	00000000 _B
00009D _H	DSRH	DMAC higher status register	R/W	DMAC	00000000 _B

(Continued)

MB90880 Series

Address	Register abbreviation	Register name	R/W	Resource	Initial value
00009E _H	PACSR0	Address detection control status register 0	R/W	Address match detection function	00000000 _B
00009F _H	DIRR	Delayed interrupt source generation/ release register	R/W	Delayed interrupt generation module	-----0 _B
0000A0 _H	LPMCR	Low power consumption mode control register	W, R/W	Low power consumption	00011000 _B
0000A1 _H	CKSCR	Clock selection register	R, R/W		11111100 _B
0000A2 _H , 0000A3 _H	Reserved				
0000A4 _H	DSSR	DMAC stop status register	R/W	DMAC	00000000 _B
0000A5 _H	ARSR	Auto ready function selection register	W	External pin	0011--00 _B
0000A6 _H	HACR	External address output control register	W		***** _B
0000A7 _H	EPCR	Bus control signal selection register	W		1000*10- _B
0000A8 _H	WDTC	Watchdog timer control register	R, W	Watchdog timer	XXXXX111 _B
0000A9 _H	TBTC	Time base timer control register	W, R/W	Time base timer	1XX00100 _B
0000AA _H	WTC	Watch timer control register	R, R/W	Watch timer	10001000 _B
0000AB _H	Reserved				
0000AC _H	DERL	DMAC lower enable register	R/W	DMAC	00000000 _B
0000AD _H	DERH	DMAC higher enable register	R/W		00000000 _B
0000AE _H	FMCS	Flash memory control status register	W, R/W	Flash memory I/F	000X0000 _B
0000AF _H	Prohibited				
0000B0 _H	ICR00	Interrupt control register 00	W, R/W	Interrupt control	00000111 _B
0000B1 _H	ICR01	Interrupt control register 01	W, R/W		00000111 _B
0000B2 _H	ICR02	Interrupt control register 02	W, R/W		00000111 _B
0000B3 _H	ICR03	Interrupt control register 03	W, R/W		00000111 _B
0000B4 _H	ICR04	Interrupt control register 04	W, R/W		00000111 _B
0000B5 _H	ICR05	Interrupt control register 05	W, R/W		00000111 _B
0000B6 _H	ICR06	Interrupt control register 06	W, R/W		00000111 _B
0000B7 _H	ICR07	Interrupt control register 07	W, R/W		00000111 _B
0000B8 _H	ICR08	Interrupt control register 08	W, R/W		00000111 _B
0000B9 _H	ICR09	Interrupt control register 09	W, R/W		00000111 _B
0000BA _H	ICR10	Interrupt control register 10	W, R/W		00000111 _B
0000BB _H	ICR11	Interrupt control register 11	W, R/W		00000111 _B
0000BC _H	ICR12	Interrupt control register 12	W, R/W		00000111 _B
0000BD _H	ICR13	Interrupt control register 13	W, R/W		00000111 _B

(Continued)

MB90880 Series

Address	Register abbreviation	Register name	R/W	Resource	Initial value
0000BE _H	ICR14	Interrupt control register 14	W, R/W	Interrupt control	00000111 _B
0000BF _H	ICR15	Interrupt control register 15	W, R/W		00000111 _B
0000C0 _H	CMR0	Chip select area MASK register 0	R/W	Chip select function	00001111 _B
0000C1 _H	CAR0	Chip select area register 0	R/W	Interrupt control	11111111 _B
0000C2 _H	CMR1	Chip select area MASK register 1	R/W		00001111 _B
0000C3 _H	CAR1	Chip select area register 1	R/W		11111111 _B
0000C4 _H	CMR2	Chip select area MASK register 2	R/W		00001111 _B
0000C5 _H	CAR2	Chip select area register 2	R/W		11111111 _B
0000C6 _H	CMR3	Chip select area MASK register 3	R/W		00001111 _B
0000C7 _H	CAR3	Chip select area register 3	R/W		11111111 _B
0000C8 _H	CSCR	Chip select control register	R/W		----000* _B
0000C9 _H	CALR	Chip select active level register	R/W		----0000 _B
0000CA _H to 0000CE _H	Reserved				
0000CF _H	PLLOS	PLL output selection register	W	PLL	-----X0 _B
0000D0 _H	BAPL	DMA buffer address pointer (low)	R/W	DMAC	XXXXXXXX _B
0000D1 _H	BAPM	DMA buffer address pointer (middle)	R/W		XXXXXXXX _B
0000D2 _H	BAPH	DMA buffer address pointer (high)	R/W		XXXXXXXX _B
0000D3 _H	MACS	DMA control register	R/W		XXXXXXXX _B
0000D4 _H	IOAL	DMAI/O register address pointer (low)	R/W		XXXXXXXX _B
0000D5 _H	IOAH	DMAI/O register address pointer (high)	R/W		XXXXXXXX _B
0000D6 _H	DCTL	DMA data counter (low)	R/W		XXXXXXXX _B
0000D7 _H	DCTH	DMA data counter (high)	R/W		XXXXXXXX _B
0000D8 _H to 0000DF _H	Reserved				
0000E0 _H	ENIR0	Interrupt/DTP enable register 0	R/W	DTP / external interrupt	00000000 _B
0000E1 _H	EIRR0	Interrupt/DTP source register 0	R/W		XXXXXXXX _B
0000E2 _H	ELVR0	Request level setting register 0	R/W		00000000 _B
0000E3 _H		Request level setting register 0	R/W		00000000 _B
0000E4 _H	ENIR1	Interrupt/DTP enable register 1	R/W	DTP / external interrupt	00000000 _B
0000E5 _H	EIRR1	Interrupt/DTP source register 1	R/W		XXXXXXXX _B
0000E6 _H	ELVR1	Request level setting register 1	R/W		00000000 _B
0000E7 _H		Request level setting register 1	R/W		00000000 _B

(Continued)

MB90880 Series

Address	Register abbreviation	Register name	R/W	Resource	Initial value
0000E8 _H	ENIR2	Interrupt/DTP enable register 2	R/W	DTP / external interrupt	XXXX0000 _B
0000E9 _H	EIRR2	Interrupt/DTP source register 2	R/W		XXXXXXXX _B
0000EA _H	ELVR2	Request level setting register 2	R/W		00000000 _B
0000EB _H		Request level setting register 2	R/W		00000000 _B
0000EC _H to 0000EF _H	Reserved				
0000F0 _H to 0000FF _H	External area				
000100 _H to # _H *	RAM area				
007900 _H	PCNTL0	PPG0 lower control status register	R/W	16-bit PPG0	00000000 _B
007901 _H	PCNTH0	PPG0 higher control status register	R/W		00000001 _B
007902 _H	PCNTL1	PPG1 lower control status register	R/W	16-bit PPG1	00000000 _B
007903 _H	PCNTH1	PPG1 higher control status register	R/W		00000001 _B
007904 _H	PCNTL2	PPG2 lower control status register	R/W	16-bit PPG2	00000000 _B
007905 _H	PCNTH2	PPG2 higher control status register	R/W		00000001 _B
007906 _H	PCNTL3	PPG3 lower control status register	R/W	16-bit PPG3	00000000 _B
007907 _H	PCNTH3	PPG3 higher control status register	R/W		00000001 _B
007908 _H	PCNTL4	PPG4 lower control status register	R/W	16-bit PPG4	00000000 _B
007909 _H	PCNTH4	PPG4 higher control status register	R/W		00000001 _B
00790A _H	PCNTL5	PPG5 lower control status register	R/W	16-bit PPG5	00000000 _B
00790B _H	PCNTH5	PPG5 higher control status register	R/W		00000001 _B
00790C _H	PCNTL6	PPG6 lower control status register	R/W	16-bit PPG6	00000000 _B
00790D _H	PCNTH6	PPG6 higher control status register	R/W		00000001 _B
00790E _H	PCNTL7	PPG7 lower control status register	R/W	16-bit PPG7	00000000 _B
00790F _H	PCNTH7	PPG7 higher control status register	R/W		00000001 _B
007910 _H	PPGDIV	PPG0 output division setting register	R/W	16-bit PPG0	11111100 _B
007911 _H	Reserved				
007912 _H	PDCRL0	PPG0 down counter register	R	16-bit PPG0	11111111 _B
007913 _H	PDCRH0				11111111 _B
007914 _H	PCSRL0	PPG0 period setting register	W		11111111 _B
007915 _H	PCSRH0				11111111 _B

(Continued)

MB90880 Series

Address	Register abbreviation	Register name	R/W	Resource	Initial value	
007916 _H	PUDUTL0	PPG0 duty setting register	W	16-bit PPG0	00000000 _B	
007917 _H	PUDUTH0				00000000 _B	
007918 _H	Disabled					
007919 _H	Disabled					
00791A _H	PDCRL1	PPG1 down counter register	R	16-bit PPG1	11111111 _B	
00791B _H	PDCRH1				11111111 _B	
00791C _H	PCSRL1	PPG1 period setting register	W		11111111 _B	
00791D _H	PCSRH1				11111111 _B	
00791E _H	PUDUTL1	PPG1 duty setting register	W		00000000 _B	
00791F _H	PUDUTH1				00000000 _B	
007920 _H	Disabled					
007921 _H	Disabled					
007922 _H	PDCRL2	PPG2 down counter register	R	16-bit PPG2	11111111 _B	
007923 _H	PDCRH2				11111111 _B	
007924 _H	PCSRL2	PPG2 period setting register	W		11111111 _B	
007925 _H	PCSRH2				11111111 _B	
007926 _H	PUDUTL2	PPG2 duty setting register	W		00000000 _B	
007927 _H	PUDUTH2				00000000 _B	
007928 _H	Disabled					
007929 _H	Disabled					
00792A _H	PDCRL3	PPG3 down counter register	R	16-bit PPG3	11111111 _B	
00792B _H	PDCRH3				11111111 _B	
00792C _H	PCSRL3	PPG3 period setting register	W		11111111 _B	
00792D _H	PCSRH3				11111111 _B	
00792E _H	PUDUTL3	PPG3 duty setting register	W		00000000 _B	
00792F _H	PUDUTH3				00000000 _B	
007930 _H	Disabled					
007931 _H	Disabled					
007932 _H	PDCRL4	PPG4 down counter register	R	16-bit PPG4	11111111 _B	
007933 _H	PDCRH4				11111111 _B	
007934 _H	PCSRL4	PPG4 period setting register	W		11111111 _B	
007935 _H	PCSRH4				11111111 _B	
007936 _H	PUDUTL4	PPG4 duty setting register	W		00000000 _B	
007937 _H	PUDUTH4				00000000 _B	

(Continued)

MB90880 Series

Address	Register abbreviation	Register name	R/W	Resource	Initial value	
007938 _H	Disabled					
007939 _H	Disabled					
00793A _H	PDCRL5	PPG5 down counter register	R	16-bit PPG5	11111111 _B	
00793B _H	PDCRH5				11111111 _B	
00793C _H	PCSRL5	PPG5 period setting register	W		11111111 _B	
00793D _H	PCSRH5				11111111 _B	
00793E _H	PUDUTL5	PPG5 duty setting register	W		00000000 _B	
00793F _H	PUDUTH5				00000000 _B	
007940 _H	Disabled					
007941 _H	Disabled					
007942 _H	PDCRL6	PPG6 down counter register	R	16-bit PPG6	11111111 _B	
007943 _H	PDCRH6				11111111 _B	
007944 _H	PCSRL6	PPG6 period setting register	W		11111111 _B	
007945 _H	PCSRH6				11111111 _B	
007946 _H	PUDUTL6	PPG6 duty setting register	W		00000000 _B	
007947 _H	PUDUTH6				00000000 _B	
007948 _H	Disabled					
007949 _H	Disabled					
00794A _H	PDCRL7	PPG7 down counter register	R	16-bit PPG7	11111111 _B	
00794B _H	PDCRH7				11111111 _B	
00794C _H	PCSRL7	PPG7 period setting register	W		11111111 _B	
00794D _H	PCSRH7				11111111 _B	
00794E _H	PUDUTL7	PPG7 duty setting register	W		00000000 _B	
00794F _H	PUDUTH7				00000000 _B	
007950 _H	Disabled					
007951 _H	Disabled					
007952 _H	TMCRO	Timer control register ch.0	R/W	Base timer ch.0	00000000 _B	
007953 _H					00000000 _B	
007954 _H	STC0	Status control register ch.0	R/W		00000000 _B	
007955 _H	Disabled					
007956 _H	TMR0	Timer register ch.0	R/W	Base timer ch.0	00000000 _B / XXXXXXXX _B	
007957 _H					00000000 _B / XXXXXXXX _B	

(Continued)

MB90880 Series

Address	Register abbreviation	Register name	R/W	Resource	Initial value
007958 _H	PCSR0/ PRL0	Period/L-width setting register ch.0	R/W	Base timer ch.0	XXXXXXXX _B
007959 _H					XXXXXXXX _B
00795A _H	PDUT0/ PRLH0/ DTBF0	Duty/H-width/data buffer register ch.0	R/W		XXXXXXXX _B / 00000000 _B
00795B _H					XXXXXXXX _B / 00000000 _B
00795C _H	TMCR1	Timer control register ch.1	R/W	Base timer ch.1	00000000 _B
00795D _H					00000000 _B
00795E _H	STC1	Status control register ch.1	R/W		00000000 _B
00795F _H	Disabled				
007960 _H	TMR1	Timer register ch.1	R/W	Base timer ch.1	00000000 _B / XXXXXXXX _B
007961 _H					00000000 _B / XXXXXXXX _B
007962 _H	PCSR1/ PRL1	Period/L-width setting register ch.1	R/W		XXXXXXXX _B
007963 _H					XXXXXXXX _B
007964 _H	PDUT1/ PRLH1/ DTBF1	Duty/H-width/data buffer register ch.1	R/W		XXXXXXXX _B / 00000000 _B
007965 _H					XXXXXXXX _B / 00000000 _B
007966 _H	TMCR2	Timer control register ch.2	R/W	Base timer ch.2	00000000 _B
007967 _H					00000000 _B
007968 _H	STC2	Status control register ch.2	R/W		00000000 _B
007969 _H	Disabled				
00796A _H	TMR2	Timer register ch.2	R/W	Base timer ch.2	00000000 _B / XXXXXXXX _B
00796B _H					00000000 _B / XXXXXXXX _B
00796C _H	PCSR2/ PRL2	Period/L-width setting register ch.2	R/W		XXXXXXXX _B
00796D _H					XXXXXXXX _B
00796E _H	PDUT2/ PRLH2/ DTBF2	Duty/H-width/data buffer register ch.2	R/W		XXXXXXXX _B / 00000000 _B
00796F _H					XXXXXXXX _B / 00000000 _B
007970 _H	TMCR3	Timer control register ch.3	R/W	Base timer ch.3	00000000 _B
007971 _H					00000000 _B
007972 _H	STC3	Status control register ch.3	R/W		00000000 _B

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MB90880 Series

Address	Register abbreviation	Register name	R/W	Resource	Initial value
007973 _H	Disabled				
007974 _H	TMR3	Timer register ch.3	R/W	Base timer ch.3	00000000 _B / XXXXXXXX _B
007975 _H					00000000 _B / XXXXXXXX _B
007976 _H	PCSR3/ PRL3	Period/L-width setting register ch.3	R/W		XXXXXXXX _B
007977 _H					XXXXXXXX _B
007978 _H	PDUT3/ PRLH3/ DTBF3	Duty/H-width/data buffer register ch.3	R/W		XXXXXXXX _B / 00000000 _B
007979 _H					XXXXXXXX _B / 00000000 _B
00797A _H	UDCR0	Up-down count register (ch.0)	R	8/16-bit up-down counter/timer	00000000 _B
00797B _H	UDCR1	Up-down count register (ch.1)	R		00000000 _B
00797C _H	RCR0	Reload/compare register (ch.0)	W		00000000 _B
00797D _H	RCR1	Reload/compare register (ch.1)	W		00000000 _B
00797E _H	CCRL0	Lower counter control register (ch.0)	W, R/W		XX00X000 _B
00797F _H	CCRH0	Higher counter control register (ch.0)	R/W		00000000 _B
007980 _H	CCRL1	Lower counter control register (ch.1)	W, R/W		XX00X000 _B
007981 _H	CCRH1	Higher counter control register (ch.1)	R/W		-0000000 _B
007982 _H	CSR0	Counter status register (ch.0)	R, R/W		00000000 _B
007983 _H	Reserved				
007984 _H	CSR1	Counter status register (ch.1)	R, R/W	8/16-bit up-down counter/timer	00000000 _B
007985 _H to 00798F _H	Reserved				
007990 _H	SMR6	Serial bus mode register ch.6	R/W	Multi-function serial ch.6	\$\$\$\$\$\$\$\$ _B
007991 _H	SCR6/IBCR6	Serial bus control register / I ² C bus control register ch.6	R/W		\$\$\$\$\$\$\$\$ _B
007992 _H	ESCR6/ IBSR6	Extended communication control register / I ² C bus status register ch.6	R/W		\$\$\$\$\$\$\$\$ _B
007993 _H	SSR6	Serial status register ch.6	R/W		\$\$\$\$\$\$\$\$ _B
007994 _H	RDR06/ TDR06	Transmission/reception data register 0 ch.6	R,W		\$\$\$\$\$\$\$\$ _B
007995 _H	RDR16/ TDR16	Transmission/reception data register 1 ch.6	R,W		\$\$\$\$\$\$\$\$ _B
007996 _H	BGR06	Baud rate generator register 0 ch.6	R/W		\$\$\$\$\$\$\$\$ _B
007997 _H	BGR16	Baud rate generator register 1 ch.6	R/W		\$\$\$\$\$\$\$\$ _B

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Address	Register abbreviation	Register name	R/W	Resource	Initial value
007998 _H	ISBA6	7-bit slave address register ch.6	R/W	Multi-function serial ch.6	00000000 _B
007999 _H	ISMK6	7-bit slave address mask register ch.6	R/W		01111111 _B
00799A _H	PAFSR	PPG pin assignment switching register	R/W	PPG pin switching control	----0000 _B
00799B _H	PMSSR	PPG multi-channel start register	R/W	PPG multi-start control	00000000 _B
00799C _H	Reserved				
00799D _H	P9FSR	Serial pin switching register 1	R/W	Multi-function serial pin control	-----000 _B
00799C _H to 0079A1 _H	Reserved				
0079A2 _H	P7FSR	Serial pin switching register 0	R/W	Multi-function serial pin control	----000X _B
0079A3 _H	LSYNS	LIN SYNCH FIELD switching register	R/W	Input capture input control	10001000 _B
0079A4 _H , 0079A5 _H	Reserved				
0079A6 _H	FWR0	Flash memory write control register 0	R/W	Flash memory I/F	00000000 _B
0079A7 _H	FWR1	Flash memory write control register 1	R/W		00000000 _B
0079A8 _H to 0079DF _H	Reserved				
0079E0 _H	PADR0	Detection address register 0 (low)	R/W	Address match detection function	XXXXXXXX _B
0079E1 _H		Detection address register 0 (middle)			XXXXXXXX _B
0079E2 _H		Detection address register 0 (high)			XXXXXXXX _B
0079E3 _H	PADR1	Detection address register 1 (low)	R/W	Address match detection function	XXXXXXXX _B
0079E4 _H		Detection address register 1 (middle)			XXXXXXXX _B
0079E5 _H		Detection address register 1 (high)			XXXXXXXX _B
0079E6 _H	PADR2	Detection address register 2 (low)	R/W	Address match detection function	XXXXXXXX _B
0079E7 _H		Detection address register 2 (middle)			XXXXXXXX _B
0079E8 _H		Detection address register 2 (high)			XXXXXXXX _B
0079E9 _H to 0079EF _H	Reserved				
0079F0 _H	PADR3	Detection address register 3 (low)	R/W	Address match detection function	XXXXXXXX _B
0079F1 _H		Detection address register 3 (middle)			XXXXXXXX _B
0079F2 _H		Detection address register 3 (high)			XXXXXXXX _B

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Address	Register abbreviation	Register name	R/W	Resource	Initial value
0079F3 _H	PADR4	Detection address register 4 (low)	R/W	Address match detection function	XXXXXXXX _B
0079F4 _H		Detection address register 4 (middle)			XXXXXXXX _B
0079F5 _H		Detection address register 4 (high)			XXXXXXXX _B
0079F6 _H	PADR5	Detection address register 5 (low)	R/W	Address match detection function	XXXXXXXX _B
0079F7 _H		Detection address register 5 (middle)			XXXXXXXX _B
0079F8 _H		Detection address register 5 (high)			XXXXXXXX _B
0079F9 _H to 007FFF _H	Reserved				

Explanation on R/W

R/W : Readable/Writable

R : Read only

W : Write only

Explanation on initial value

0 : The initial value of this bit is "0".

1 : The initial value of this bit is "1".

X : The initial value of this bit is undefined.

- : This bit is not used.

* : The initial value of this bit is "1" or "0".

It varies depending on the mode pin (MD2, MD1 or MD0 pin) .

+ : The initial value of this bit is "1" or "0".

\$: The initial value of this bit varies depending on the operation mode of the resource.

#H* : Varies depending on the RAM area of the device.

■ INTERRUPT SOURCES, INTERRUPT VECTORS AND INTERRUPT CONTROL REGISTERS

Interrupt source	Clearing of EI ² OS	μ DMAC channel no.	Interrupt vector		Interrupt control register	
			No.	Address	No.	Address
Reset	×	—	#08	FFFFDC _H	—	—
INT9 instruction	×	—	#09	FFFFD8 _H	—	—
Exception	×	—	#10	FFFFD4 _H	—	—
INT0 (IRQ0/1)	○	0	#11	FFFFD0 _H	ICR00	0000B0 _H
INT0 (IRQ2 to IRQ7)	○	×	#12	FFFFCC _H		
INT0 (IRQ8 to IRQ15)	○	×	#13	FFFFC8 _H	ICR01	0000B1 _H
INT0 (IRQ16 to IRQ23)	○	×	#14	FFFFC4 _H		
Base timer ch.0 (source 0,1)	○	1	#15	FFFFC0 _H	ICR02	0000B2 _H
Base timer ch.1 (source 0,1)	○	2	#16	FFFFBC _H		
Base timer ch.2 (source 0,1)	○	3	#17	FFFFB8 _H	ICR03	0000B3 _H
Base timer ch.3 (source 0,1)	○	4	#18	FFFFB4 _H		
PPG0/PPG4 counter borrow	○	5	#19	FFFFB0 _H	ICR04	0000B4 _H
PPG1/PPG5 counter borrow	○	6	#20	FFFFAC _H		
PPG2/PPG6 counter borrow	○	7	#21	FFFFA8 _H	ICR05	0000B5 _H
PPG3/PPG7 counter borrow	×	8	#22	FFFFA4 _H		
8/16-bit up-down counter/timer (ch.0/1) compare / underflow / overflow / up-down inversion	×	×	#23	FFFFA0 _H	ICR06	0000B6 _H
Input capture retrieval (ch.0/1)	○	×	#24	FFFF9C _H		
Output compare (ch.0/1/2) match	○	×	#25	FFFF98 _H	ICR07	0000B7 _H
Output compare (ch.3/4/5) match	○	×	#26	FFFF94 _H		
A/D converter	○	×	#27	FFFF90 _H	ICR08	0000B8 _H
Overflow in 16-bit free-run timer / compare clear / multi-function serial ch.4/5/6 status	○	9	#28	FFFF8C _H		
Multi-function serial ch.4 reception	○	10	#29	FFFF88 _H	ICR09	0000B9 _H
Multi-function serial ch.4 transition	○	11	#30	FFFF84 _H		
Multi-function serial ch.5 reception	○	12	#31	FFFF80 _H	ICR10	0000BA _H
Multi-function serial ch.5 transition	○	13	#32	FFFF7C _H		
Multi-function serial ch.6 reception	○	14	#33	FFFF78 _H	ICR11	0000BB _H
Multi-function serial ch.6 transition	○	15	#34	FFFF74 _H		
Multi-function serial ch.0/1 reception / status	◎	×	#35	FFFF70 _H	ICR12	0000BC _H
Multi-function serial ch.0/1 transmission	○	×	#36	FFFF6C _H		
Multi-function serial ch.2 reception / status	◎	×	#37	FFFF68 _H	ICR13	0000BD _H
Multi-function serial ch.2 transmission	○	×	#38	FFFF64 _H		

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Interrupt source	Clearing of EI ² OS	μ DMAC channel no.	Interrupt vector		Interrupt control register	
			No.	Address	No.	Address
Multi-function serial ch.3 reception / status	◎	×	#39	FFFF60 _H	ICR14	0000BE _H
Multi-function serial ch.3 transmission	○	×	#40	FFFF5C _H		
Flash writing/deletion, time base timer, watch timer*	×	×	#41	FFFF58 _H	ICR15	0000BF _H
Delayed interrupt generation module	×	×	#42	FFFF54 _H		

× : The interrupt request flag is not cleared by the interrupt clear signal.

○ : The interrupt request flag is cleared by the interrupt clear signal.

◎ : The interrupt request flag is cleared by the interrupt clear signal. Stop request function provided at receiving only.

* : Flash writing/deletion, the time base timer and watch timer cannot be used simultaneously.

Note : If a resource has two interrupt sources for the same interrupt number, both of the interrupt request flags are cleared by the EI²OS/ μ DMAC interrupt clear signal. Therefore, when either of the two sources for the EI²OS/ μ DMAC function is used, the other interrupt function can not be used. In this case, set the interrupt request enable bit to "0" in the appropriate resource and take measures by software polling.

■ ELECTRICAL CHARACTERISTICS

1. Absolute maximum ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V _{CC}	V _{SS} – 0.3	V _{SS} + 4.0	V	
	DV _{CC}	V _{SS} – 0.3	V _{SS} + 4.0	V	DV _{CC} = V _{CC} *2
	AV _{CC}	V _{SS} – 0.3	V _{SS} + 4.0	V	*2
	AVRH	V _{SS} – 0.3	V _{SS} + 4.0	V	*2
Input voltage*1	V _I	V _{SS} – 0.3	V _{SS} + 4.0	V	*3
		V _{SS} – 0.3	V _{SS} + 7.0	V	*3, *8
Output voltage*1	V _O	V _{SS} – 0.3	V _{SS} + 4.0	V	*3
		V _{SS} – 0.3	V _{SS} + 7.0	V	*3, *8
Maximum clamp current	I _{CLAMP}	– 2.0	+2.0	mA	*7
Total maximum clamp current	$\sum I_{CLAMP} $	—	20	mA	*7
“L” level maximum output current	I _{OL1}	—	10	mA	*4
	I _{OL2}	—	20	mA	PA0 to PA3*4
“L” level average output current	I _{OLAV1}	—	3	mA	*5
	I _{OLAV2}	—	10	mA	PA0 to PA3*5
“L” level maximum total output current	$\sum I_{OL1}$	—	60	mA	
	$\sum I_{OL2}$	—	80	mA	PA0 to PA3
“L” level average total output current	$\sum I_{OLAV1}$	—	30	mA	*6
	$\sum I_{OLAV2}$	—	40	mA	PA0 to PA3*6
“H” level maximum output current	I _{OH1}	—	–10	mA	*4
	I _{OH2}	—	–20	mA	PA0 to PA3*4
“H” level average output current	I _{OHAV1}	—	–3	mA	*5
	I _{OHAV2}	—	–10	mA	PA0 to PA3*5
“H” level maximum total output current	$\sum I_{OH1}$	—	–60	mA	
	$\sum I_{OH2}$	—	–80	mA	PA0 to PA3
“H” level average total output current	$\sum I_{OHAV1}$	—	–30	mA	*6
	$\sum I_{OHAV2}$	—	–40	mA	PA0 to PA3*6
Power consumption	P _D	—	320	mW	
Operating temperature	T _A	–40	+85	°C	
Storage temperature	T _{stg}	–55	+150	°C	

*1 : The parameter is based on V_{SS} = AV_{SS} = DV_{SS} = 0.0 V.

*2 : Set AV_{CC}, DV_{CC} and AVR_H to the same voltage. AV_{CC} and DV_{CC} must not exceed V_{CC}. Also, AVR_H must not exceed AV_{CC}.

*3 : V_I and V_O must not exceed 0.3V. When the maximum current to/from an input is limited by using an external component, the I_{CLAMP} rating supersedes the V_I rating.

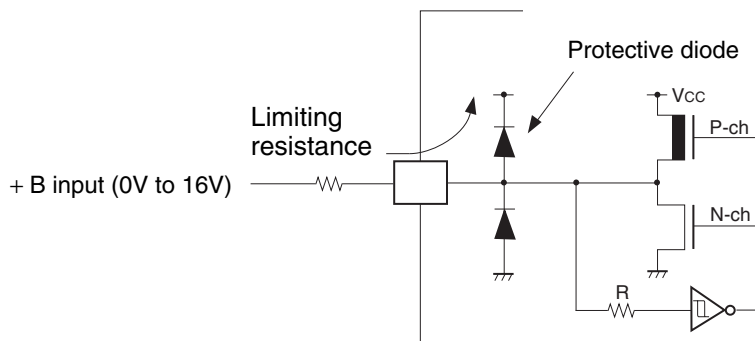
*4 : The maximum output current is defined as the peak value of the current of any one of the corresponding pins.
(Continued)

MB90880 Series

(Continued)

- *5 : The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.
- *6 : The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.
- *7 :
 - Relevant pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P76, P80 to P87, P90 to P97, PA0 to PA3
 - Use within recommended operating conditions.
 - Use with DC voltage (current) .
 - The + B signal should always be applied with a limiting resistance placed between the + B signal and the microcontroller.
 - Set the limiting resistor value, whether instantaneous or stationary, so that the current to be input to the microcontroller pin does not exceed the rating during the input of the + B signal.
 - Note that when the microcontroller drive current is low, such as in the power saving modes, the + B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
 - Note that if a + B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
 - Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
 - Care must be taken not to leave the + B input pin open.
 - Note that analog system input/output pins (LCD drive pins, comparator input pins, etc.) cannot accept + B signal input.
 - Sample recommended circuit :

• Input/Output equivalent circuit



*8 : P74 to P76 and P80 to P87 can be used as 5V I/F pins.

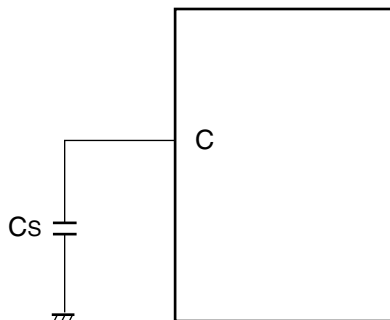
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed any of these ratings.

2. Recommended operating conditions

($V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	2.7	3.6	V	In normal operation
	DV_{CC}	1.8	3.6	V	Hold stop status
“H” level input voltage	V_{IH}	$0.7 V_{CC}$	$V_{CC} + 0.3$	V	All pins other than V_{IH2} , V_{IHS} , V_{IHM} and V_{IHX}
	V_{IH2}	$0.7 V_{CC}$	$V_{SS} + 5.8$	V	P74 to P76, P80 to P87
	V_{IHS}	$0.8 V_{CC}$	$V_{CC} + 0.3$	V	Hysteresis input pins
	V_{IHS2}	$0.7 V_{CC}$	$V_{CC} + 0.3$	V	Hysteresis input pins (multi-function serial pins)
	V_{IHS3}	$0.7 V_{CC}$	$V_{CC} + 0.3$	V	CMOS input pins (external bus mode input pins)
	V_{IHM}	$V_{CC} - 0.3$	$V_{CC} + 0.3$	V	MD pin input
	V_{IHX}	$0.8 V_{CC}$	$V_{CC} + 0.3$	V	X0A and X1A pins
“L” level input voltage	V_{IL}	$V_{SS} - 0.3$	$0.3 V_{CC}$	V	All pins other than V_{ILS} , V_{ILM} and V_{ILX}
	V_{ILS}	$V_{SS} - 0.3$	$0.2 V_{CC}$	V	Hysteresis input pins
	V_{ILS2}	$V_{SS} - 0.3$	$0.3 V_{CC}$	V	Hysteresis input pins (multi-function serial pins)
	V_{ILS3}	$V_{SS} - 0.3$	$0.3 V_{CC}$	V	CMOS input pins (external bus mode pins)
	V_{ILM}	$V_{SS} - 0.3$	$V_{SS} + 0.3$	V	MD pin input
	V_{ILX}	$V_{SS} - 0.3$	0.1	V	X0A and X1A pins
Smoothing capacitor	C_S	0.1	1.0	μF	Use a ceramic capacitor or comparable capacitor of the AC characteristics. Bypass capacitor at the V_{CC} pin should be greater than this capacitor.
Operating temperature	T_A	-40	+85	$^{\circ}\text{C}$	

• C Pin Connection Diagram



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WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC characteristics

($V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
“H” level output voltage	V_{OH}	All pins except P74 to P76, P80 to P87 and PA0 to PA3	$V_{CC} = 3.0\text{ V}$, $I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
		P74 to P76, P80 to P87	$V_{CC} = 3.0\text{ V}$, $I_{OH} = -2.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
		PA0 to PA3	$DV_{CC} = 3.0\text{ V}$, $I_{OH} = -10.0\text{ mA}$	$DV_{CC} - 0.6$	—	—	V	
“L” level output voltage	V_{OL}	All pins except P74 to P76, P80 to P87 and PA0 to PA3	$V_{CC} = 3.0\text{ V}$, $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
		P74 to P76, P80 to P87	$V_{CC} = 3.0\text{ V}$, $I_{OH} = -2.0\text{ mA}$	—	—	0.4	V	
		PA0 to PA3	$DV_{CC} = 3.0\text{ V}$, $I_{OL} = 10.0\text{ mA}$	—	—	0.5	V	
Input leak current	I_{IL}	All input pins	$V_{CC} = 3.3\text{ V}$, $V_{SS} < V_i < V_{CC}$	-10	—	+10	μA	
Pull-up resistance	R_{PULL}	—	—	25	50	100	k Ω	Evaluation version
				15	33	66	k Ω	Flash memory version / MASKROM version
Open-drain output current	I_{leak}	P31, P32, P34, P35, P43, P44, P46, P47, P72 to P76, P80 to P87, P96, P97	—	—	0.1	10	μA	

(Continued)

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(Continued)

($V_{CC} = 2.7V$ to $3.6V$, $V_{SS} = 0.0V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Supply current	I _{CC}	—	V _{CC} = 3.3V; Normal internal 25 MHz operation	—	20	28	mA
			V _{CC} = 3.3V; Normal internal 33 MHz operation	—	28	38	mA
			V _{CC} = 3.3V; Internal 25 MHz operation; flash write	—	30	40	mA
			V _{CC} = 3.3V; Internal 33 MHz operation; flash write	—	40	52	mA
	I _{CCS}	—	V _{CC} = 3.3V; Internal 25 MHz operation; sleep mode	—	6	12	mA
			V _{CC} = 3.3V; Internal 33 MHz operation; sleep mode	—	10	20	mA
	I _{CTS}	—	V _{CC} = 3.3 V; Internal 2 MHz, operation; Time-base timer	—	0.25	0.9	mA
	I _{COL}	—	V _{CC} = 3.3V; External 32 kHz & internal 8 kHz operation; sub-operation (T _A = + 25 °C)	—	80	200	μA
	I _{COLS}	—	V _{CC} = 3.3 V; External 32 MHz, Internal 8 MHz operation; sub sleep mode (T _A = +25 °C)	—	50	160	μA
	I _{CCT}	—	V _{CC} = 3.3V; External 32 kHz & internal 8 kHz operation; watch operation (T _A = + 25 °C)	—	20	110	μA
Input capacitance	C _{IN}	All pins except AV _{CC} , AV _{SS} , V _{CC} , DV _{CC} , V _{SS} , DV _{SS}	AV _{CC} , AV _{SS} , V _{CC} , DV _{CC} , V _{SS} , DV _{SS}	—	5	15	pF

Note : P74 to P76 and P80 to P87 are N-ch open-drain pins with controls and normally used at the CMOS level.

4. AC characteristics

(1) Clock timing ratings

(V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

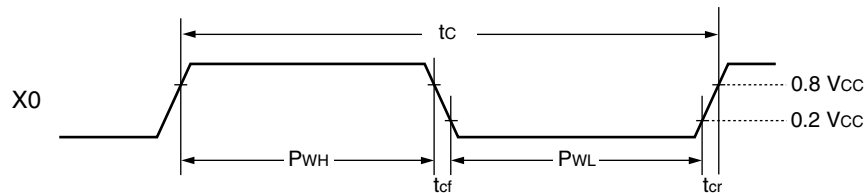
Parameter	Symbol	Pin name	Condi- tions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F _{CH}	X0, X1	—	3	—	25	MHz	External crystal oscillation
			—	3	—	50		External clock input
			—	4	—	25		PLL1 multiplication
			—	3	—	12.5		PLL2 multiplication
			—	3	—	6.66		PLL3 multiplication
			—	3	—	6.25		PLL4 multiplication
			—	3	—	5.5		PLL6 multiplication
			—	3	—	4.125		PLL8 multiplication
	F _{CL}	X0A, X1A	—	—	32.768	—	kHz	
Clock cycle time	t _c	X0, X1	—	15.15	—	333	ns	*1
	t _{CL}	X0A, X1A	—	—	30.5	—	μs	
Input clock pulse width	P _{WH} P _{WL}	X0	—	5	—	—	ns	
	P _{WLH} P _{WLL}	X0A	—	—	15.2	—	μs	*2
Input clock rise/fall time	t _{cr} t _{cf}	X0	—	—	—	5	ns	External clock in use
Internal operating clock frequency	f _{CP}	—	—	1.5	—	33	MHz	*1
	f _{CPL}	—	—	—	8.192	—	kHz	
Internal operating clock cycle time	t _{CP}	—	—	30.3	—	666	ns	*1
	t _{CPL}	—	—	—	122.1	—	μs	

*1 : Observe the operating voltage with care.

The maximum operating frequency is 25 MHz in MB90F883(S) and MB90F884(S).

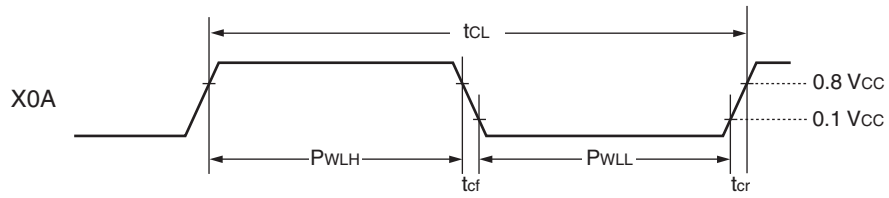
*2 : Input it at a duty ratio of 50% ±3%.

• X0, X1 clock timing

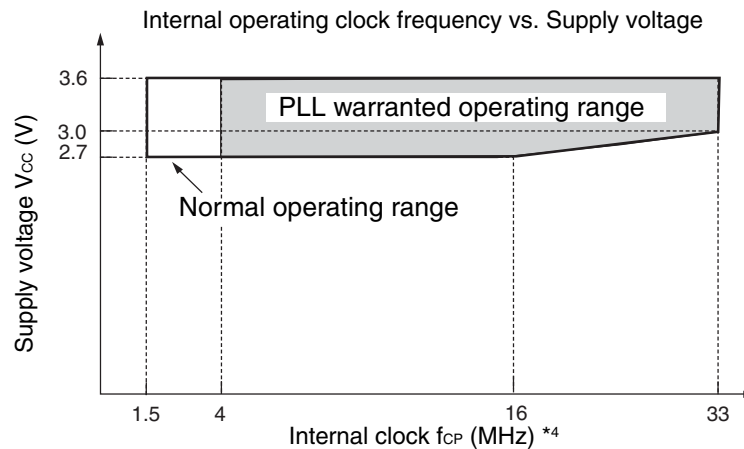


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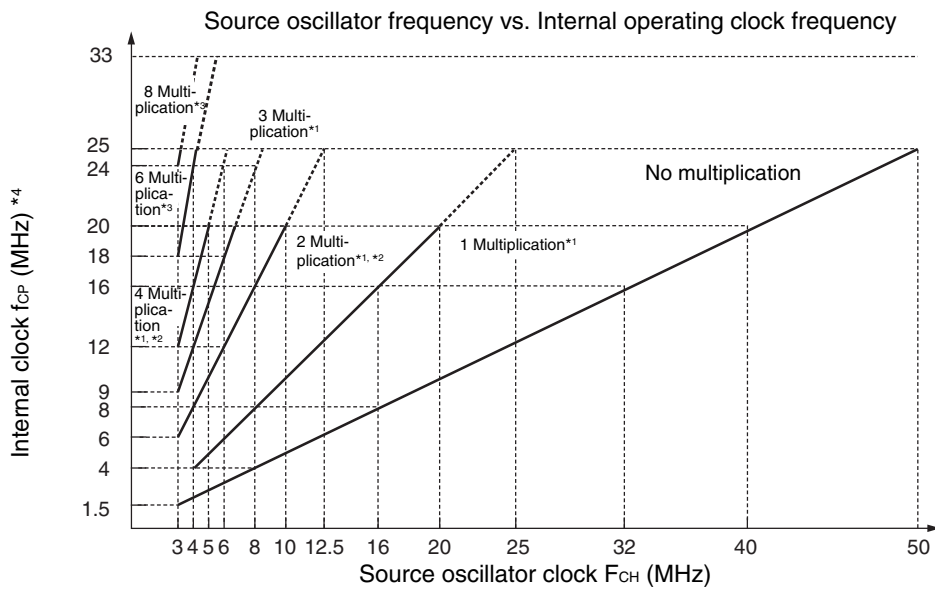
- X0A, X1A clock timing



- PLL warranted operating range



- Notes:
- Use the f_{CP} at 4 MHz or higher only for PLL1 multiplication.
 - For A/D operating frequencies, refer to "5. A/D Converter electrical characteristics".



- *1 : When using the internal clock at "20 MHz < f_{CP} ≤ 25 MHz" in PLL1, 2, 3 or 4 multiplication setting, set both of the DIV2 and PLL2 bits to "1" in the PLLOS register.
 Example : When the source oscillator frequency is 24 MHz in PLL1 multiplication :
 CKSCR register : CS1 = "0", CS0 = "0"
 PLLOS register : DIV2 = "1", PLL2 = "1"
 Example : When the source oscillator frequency is 6 MHz in PLL3 multiplication :
 CKSCR register : CS1 = "1", CS0 = "0"
 PLLOS register : DIV2 = "1", PLL2 = "1"
- *2 : When using the internal clock at "20 MHz < f_{CP} ≤ 25 MHz" in PLL 2 or 4 multiplication setting, the following settings can also be used.
 PLL2 multiplication : CKSCR register : CS1 = "0", CS0 = "0"
 PLLOS register : DIV2 = "0", PLL2 = "1"
 PLL4 multiplication : CKSCR register : CS1 = "0", CS0 = "1"
 PLLOS register : DIV2 = "0", PLL2 = "1"
- *3 : When using the PLL6 or 8 multiplication setting, set DIV2 to "0" and PLL2 to "1" in the PLLOS register.
 Example : When the source oscillator frequency is 4 MHz in PLL6 multiplication :
 CKSCR register : CS1 = "1", CS0 = "0"
 PLLOS register : DIV2 = "0", PLL2 = "1"
 Example : When the source oscillator frequency is 3 MHz in PLL8 multiplication :
 CKSCR register : CS1 = "1", CS0 = "1"
 PLLOS register : DIV2 = "0", PLL2 = "1"
- *4 : The maximum operating frequency of MB90F883(S) and MB90F884(S) is 25 MHz.

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AC characteristics are determined using the following measurement reference voltage values.

- Input signal waveform

Hysteresis input pins



Pins other than hysteresis input/MD input pins



- Output signal waveform

Output pins

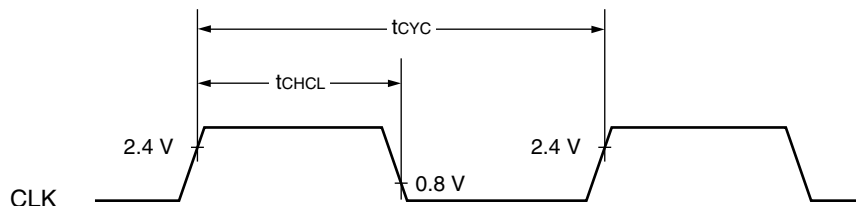


(2) Clock output timing

($V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	t_{CP}^*	—	ns	
$\text{CLK}\uparrow \rightarrow \text{CLK}\downarrow$	t_{CHCL}	CLK	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	$t_{CP}^* / 2 - 15$	$t_{CP}^* / 2 + 15$	ns	$f_{CP} = 25 \text{ MHz}$
			$V_{CC} = 2.7 \text{ V to } 3.3 \text{ V}$	$t_{CP}^* / 2 - 20$	$t_{CP}^* / 2 + 20$	ns	$f_{CP} = 16 \text{ MHz}$
			$V_{CC} = 2.7 \text{ V to } 3.3 \text{ V}$	$t_{CP}^* / 2 - 64$	$t_{CP}^* / 2 + 64$	ns	$f_{CP} = 5 \text{ MHz}$

* : t_{CP} is the cycle time for the internal operation clock. Refer to (1) "Clock timing ratings".



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(3) Reset input ratings

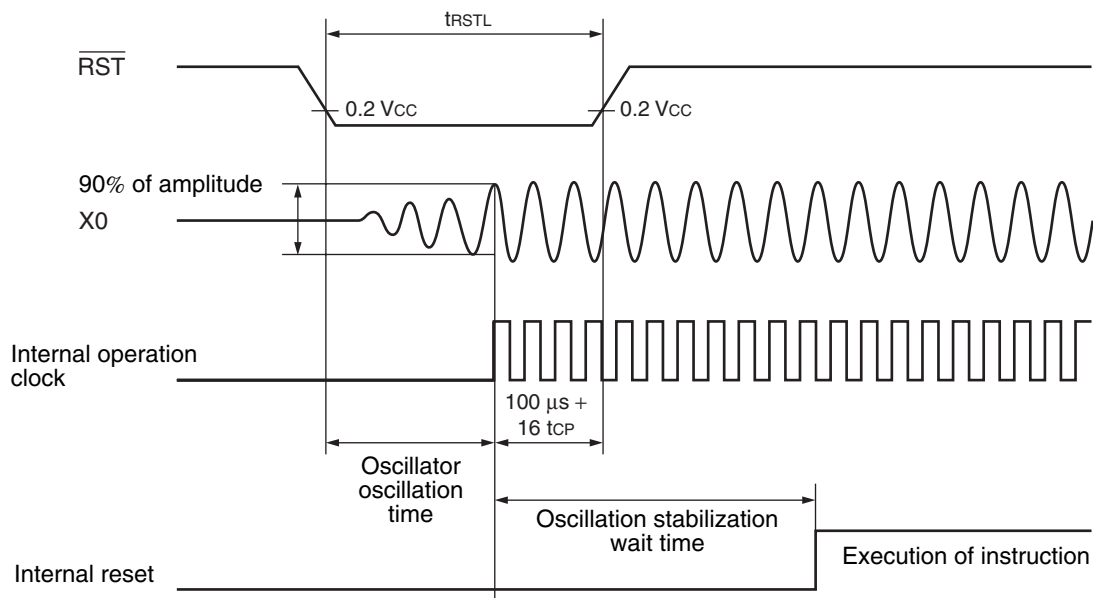
($V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	—	$16 t_{CP}^{*1}$	—	ns	In normal operation
				Oscillator oscillation time ^{*2} $+ 100 \mu\text{s} + 16 t_{CP}^{*1}$	—	ms	In sub clock, sub-sleep, watch and stop modes
				100	—	μs	In time base timer mode

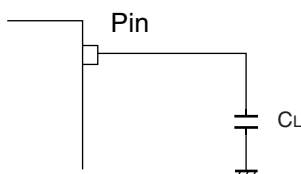
*1 : t_{CP} is the cycle time for the internal operation clock. Refer to (1) "Clock timing ratings".

*2 : Oscillator oscillation time is the time to reach 90% amplitude. For a crystal oscillator, this is a few to several tens of ms; for a ceramic oscillator, this is several hundred ms to a few ms, and for an external clock this is 0 ms.

- In sub clock, sub-sleep, watch and stop modes



- Measurement conditions for AC ratings



C_L : Load capacitance applied to pin during testing

CLK, ALE : $C_L = 30 \text{ pF}$
 AD15 to AD00 (Address, data bus), $\overline{RD}$, $\overline{WR}$,
 A23 to A00/D15 to D00 : $C_L = 30 \text{ pF}$

(4) Power-on ratings (Power-on reset)

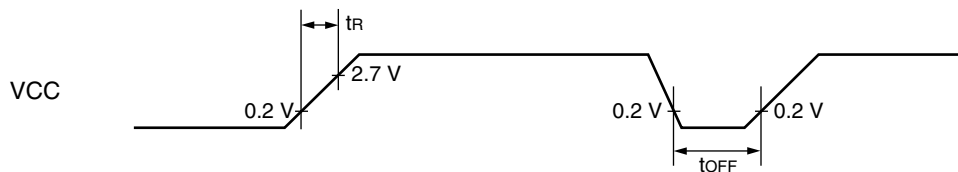
($V_{CC} = 2.7 \text{ V}$ to 3.6 V , $V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Power rise time	t_R	VCC	—	0.05	30	ms	*
Power cutoff time	t_{OFF}	VCC		1	—	ms	For continuous operation

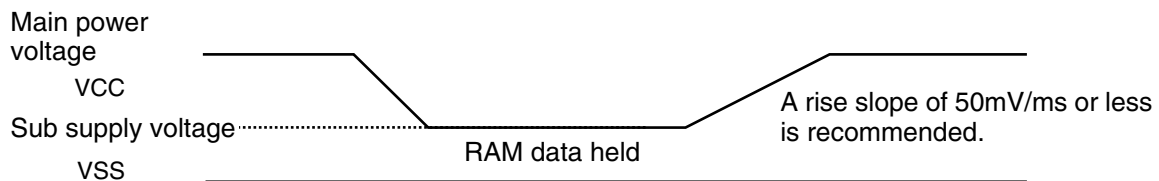
* : During the power rise time, V_{CC} must be less than 0.2V.

Notes : • The above ratings are values used for power-on reset.

- A power-on reset should be applied by restarting the power supply inside the device.



A sudden change in the supply voltage may activate a power-on reset.
As shown in the following figure, it is recommended to apply a smooth voltage rise with suppressed fluctuation when changing the supply voltage during operation.



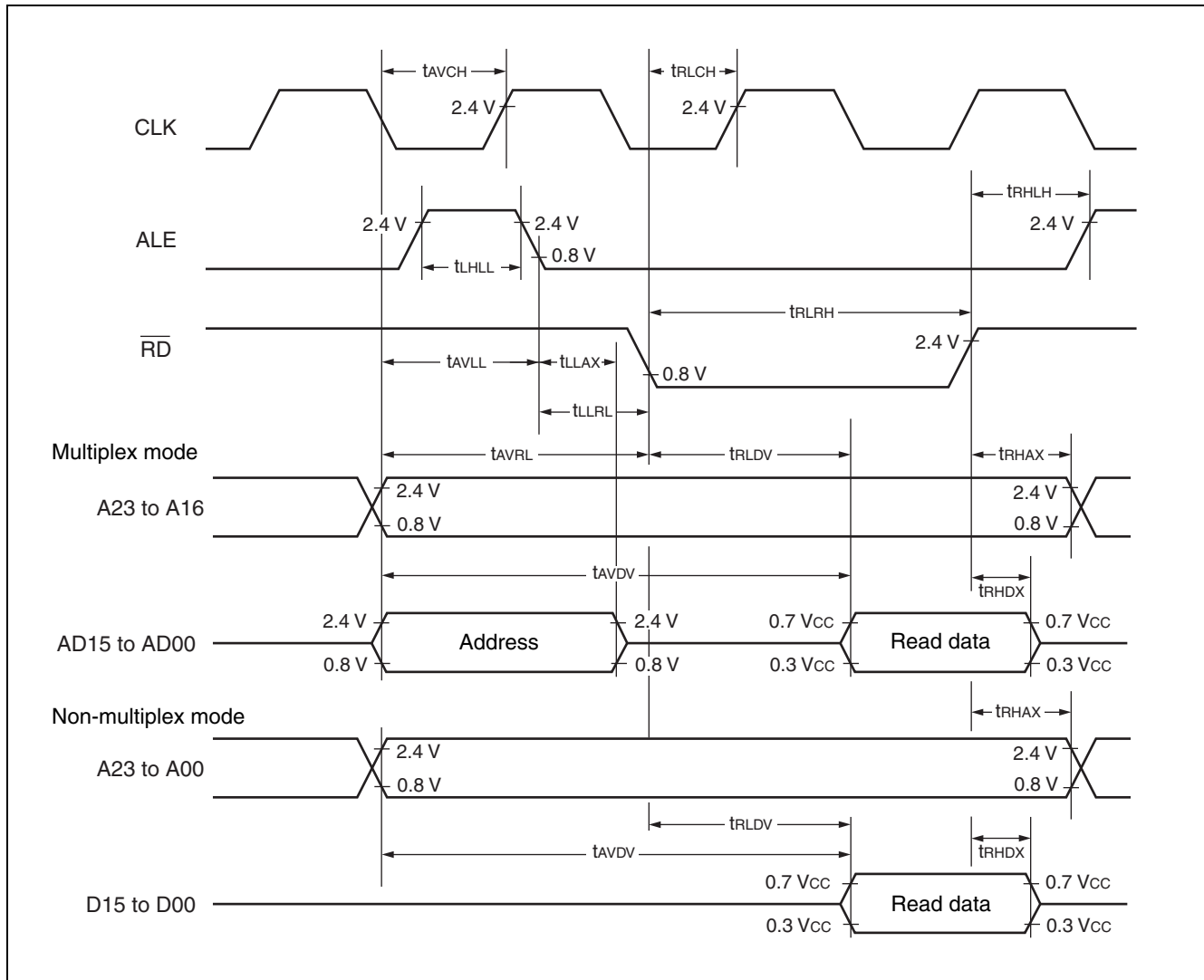
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(5) Bus read timing

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condi- tions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}^* / 2 - 15$	—	ns	$16\text{ MHz} < f_{CP} \leq 25\text{ MHz}$
				$t_{CP}^* / 2 - 20$	—	ns	$8\text{ MHz} < f_{CP} \leq 16\text{ MHz}$
				$t_{CP}^* / 2 - 35$	—	ns	$f_{CP} \leq 8\text{ MHz}$
Valid address → ALE↓ time	t_{AVLL}	Address, ALE	—	$t_{CP}^* / 2 - 17$	—	ns	
				$t_{CP}^* / 2 - 40$	—	ns	$f_{CP} \leq 8\text{ MHz}$
ALE ↓ → valid address time	t_{LLAX}	ALE, address	—	$t_{CP}^* / 2 - 15$	—	ns	
valid address → RD↓ Time	t_{AVRL}	RD, address	—	$t_{CP}^* - 25$	—	ns	
Valid address → valid data input	t_{AVDV}	Address / data	—	—	$5 t_{CP}^* / 2 - 55$	ns	
				—	$5 t_{CP}^* / 2 - 80$	ns	$f_{CP} \leq 8\text{ MHz}$
RD pulse width	t_{RLRH}	RD	—	$3 t_{CP}^* / 2 - 25$	—	ns	$16\text{ MHz} < f_{CP} \leq 25\text{ MHz}$
				$3 t_{CP}^* / 2 - 20$	—	ns	$8\text{ MHz} < f_{CP} \leq 16\text{ MHz}$
RD↓ → valid data input	t_{RLDV}	RD, data	—	—	$3 t_{CP}^* / 2 - 55$	ns	
				—	$3 t_{CP}^* / 2 - 80$	ns	$f_{CP} \leq 8\text{ MHz}$
RD↑ → data hold time	t_{RHDX}	RD, data	—	0	—	ns	
RD↑ → ALE↑ time	t_{RHLH}	RD, ALE	—	$t_{CP}^* / 2 - 15$	—	ns	
RD↑ → valid address time	t_{RHAX}	Address, RD	—	$t_{CP}^* / 2 - 10$	—	ns	
Valid address → CLK↑ time	t_{AVCH}	Address, CLK	—	$t_{CP}^* / 2 - 17$	—	ns	
RD↓ → CLK↑ time	t_{RLCH}	RD, CLK	—	$t_{CP}^* / 2 - 17$	—	ns	
ALE↓ → RD↓ time	t_{LLRL}	RD, ALE	—	$t_{CP}^* / 2 - 15$	—	ns	

* : t_{CP} is the cycle time for the internal operation clock. Refer to (1) "Clock timing ratings".



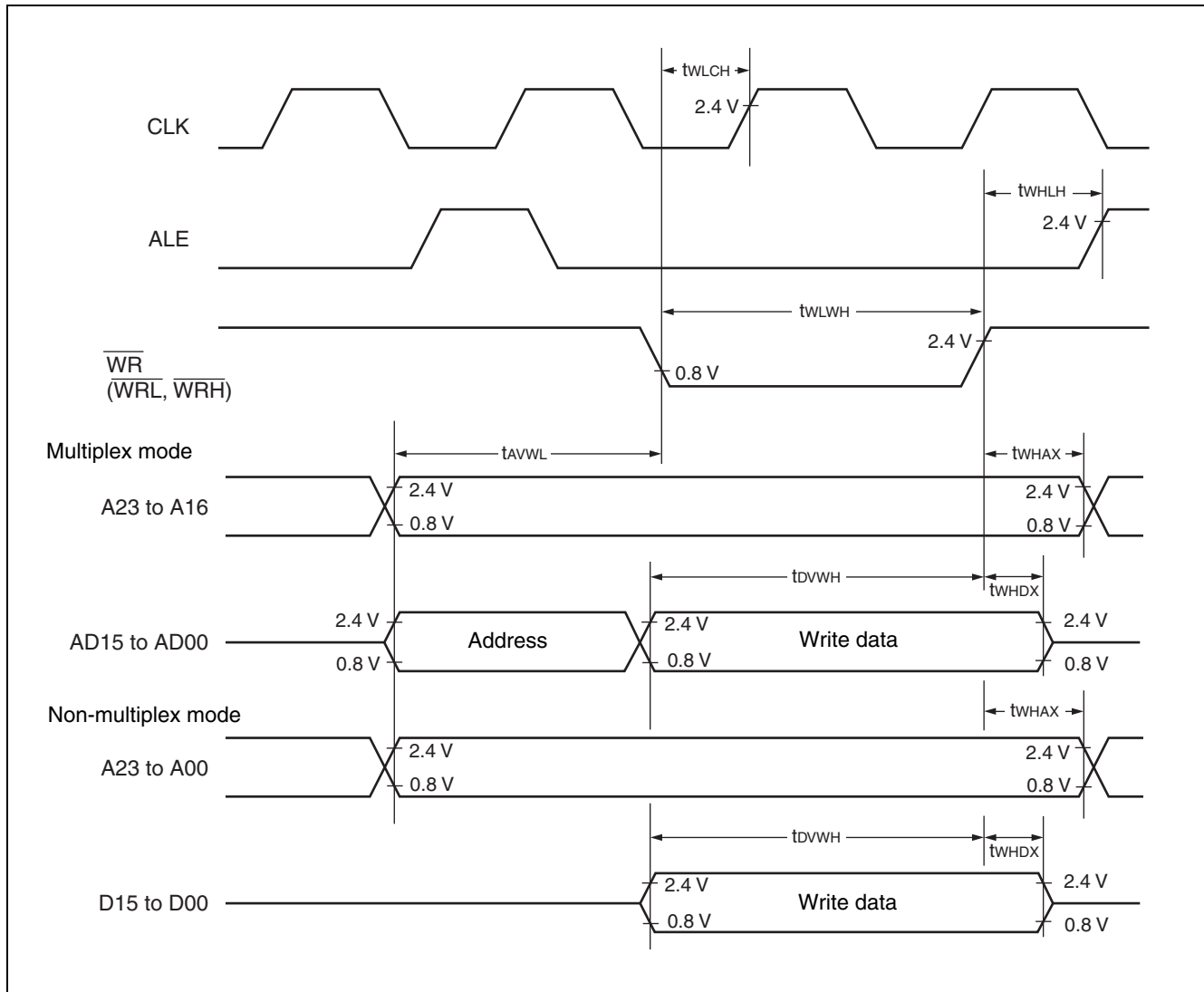
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(6) Bus write timing

($V_{CC} = 2.7 \text{ V}$ to 3.6 V , $V_{SS} = 0.0 \text{ V}$, $T_A = 0 \text{ }^{\circ}\text{C}$ to $+70 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condi- tions	Value		Unit	Remarks
				Min	Max		
Valid address $\rightarrow \overline{WR} \downarrow$ time	t_{AVWL}	Address, $\overline{WR}$	—	$t_{CP}^* - 15$	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WRL}$, $\overline{WRH}$	—	$3 t_{CP}^* / 2 - 25$	—	ns	$16 \text{ MHz} < f_{CP} \leq 25 \text{ MHz}$
			—	$3 t_{CP}^* / 2 - 20$	—	ns	$8 \text{ MHz} < f_{CP} \leq 16 \text{ MHz}$
Valid data output $\rightarrow \overline{WR} \uparrow$ time	t_{DVWH}	Data, $\overline{WR}$	—	$3 t_{CP}^* / 2 - 15$	—	ns	
$\overline{WR} \uparrow \rightarrow$ data hold time	t_{WHDx}	$\overline{WR}$, data	—	10	—	ns	$16 \text{ MHz} < f_{CP} \leq 25 \text{ MHz}$
			—	20	—	ns	$8 \text{ MHz} < f_{CP} \leq 16 \text{ MHz}$
			—	30	—	ns	$f_{CP} \leq 8 \text{ MHz}$
$\overline{WR} \uparrow \rightarrow$ valid address time	t_{WHAX}	$\overline{WR}$, address	—	$t_{CP}^* / 2 - 10$	—	ns	
$\overline{WR} \uparrow \rightarrow \text{ALE} \uparrow$ time	t_{WHLH}	$\overline{WR}$, ALE	—	$t_{CP}^* / 2 - 15$	—	ns	
$\overline{WR} \downarrow \rightarrow \text{CLK} \uparrow$ time	t_{WLCH}	$\overline{WR}$, CLK	—	$t_{CP}^* / 2 - 17$	—	ns	

* : t_{CP} is the cycle time for the internal operation clock. Refer to (1) "Clock timing ratings".

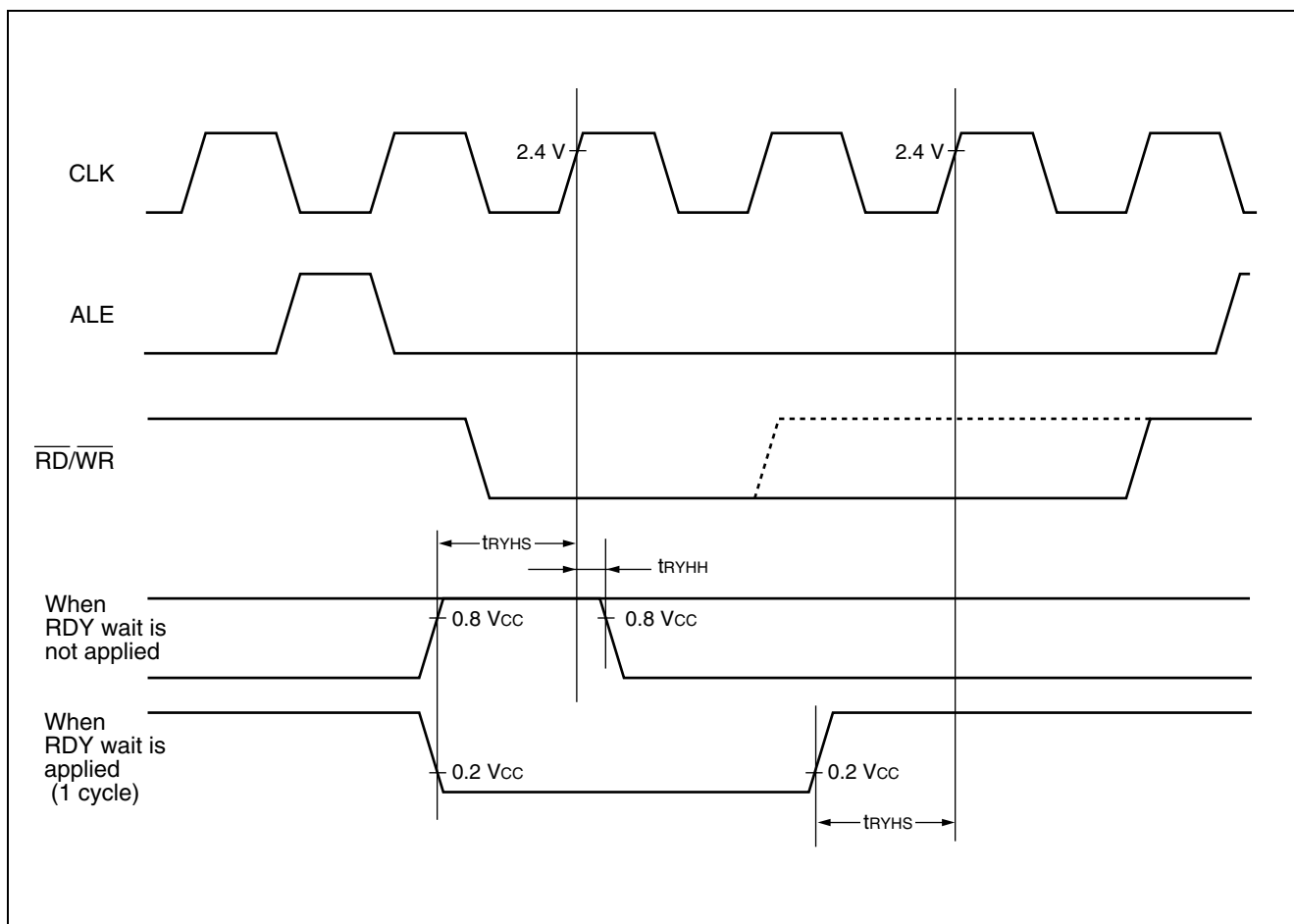


MB90880 Series

(7) Ready input timing

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	35	—	ns	
			—	70	—	ns	$f_{CP} = 8\text{ MHz}$
RDY hold time	t_{RYHH}		—	0	—	ns	



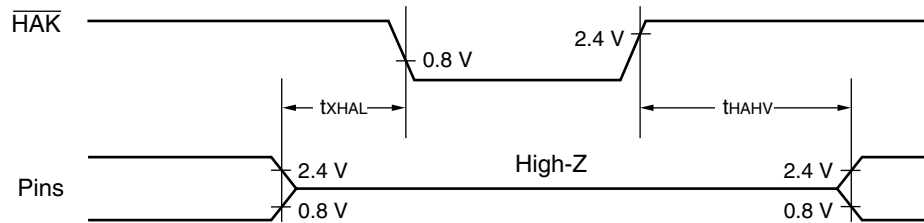
(8) Hold timing

($V_{CC} = 2.7 \text{ V}$ to 3.6 V , $V_{SS} = 0.0 \text{ V}$, $T_A = 0 \text{ }^{\circ}\text{C}$ to $+70 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Pin floating $\rightarrow \overline{\text{HAK}}\downarrow$ time	t_{XHAL}	$\overline{\text{HAK}}$	—	30	t_{CP}^*	ns
$\overline{\text{HAK}}\downarrow \rightarrow$ valid pin time	t_{HAHV}	$\overline{\text{HAK}}$		t_{CP}^*	$2 t_{CP}^*$	ns

* : t_{CP} is the cycle time for the internal operation clock. Refer to (1) "Clock timing ratings".

Note : It takes one or more cycles from when the HRQ pin is read to when $\overline{\text{HAK}}$ changes.



MB90880 Series

(9) Multi-function serial timing (UART, SIO)

($V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$)

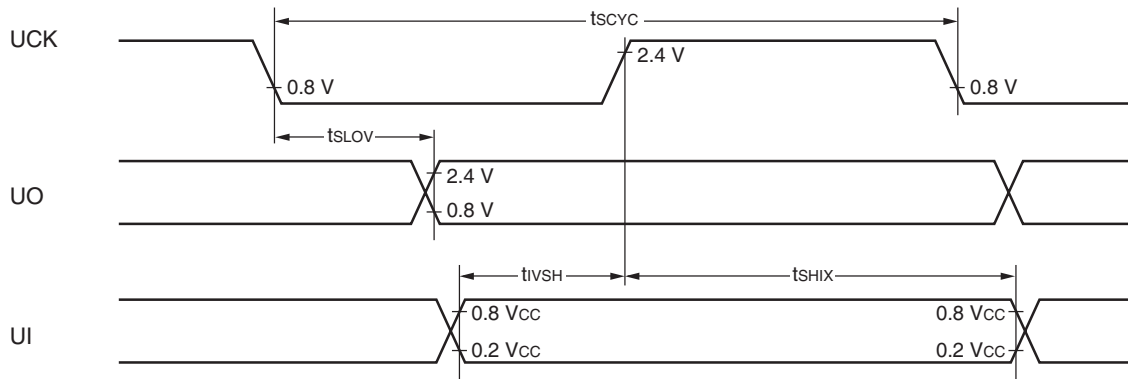
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	—	Internal shift clock mode output pin : $C_L^{*1} = 80 \text{ pF} + 1 \text{ TTL}$	$8 t_{CP}^{*2}$	—	ns
UCK↓ → UO delay time	t_{SLOV}	—		−50	+50	ns
Valid UI → UCK↑	t_{IVSH}	—		50	—	ns
UCK↑ → valid UI hold time	t_{SHIX}	—		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	—	External shift clock mode output pin : $C_L^{*1} = 80 \text{ pF} + 1 \text{ TTL}$	$4 t_{CP}^{*2}$	—	ns
Serial clock “L” pulse width	t_{SLSH}	—		$4 t_{CP}^{*2}$	—	ns
UCK↓ → UO delay time	t_{SLOV}	—		—	50	ns
Valid UI → UCK↑	t_{IVSH}	—		50	—	ns
UCK↑ → valid UI hold time	t_{SHIX}	—		50	—	ns

*1 : C_L is the load capacitance applied to pins during testing.

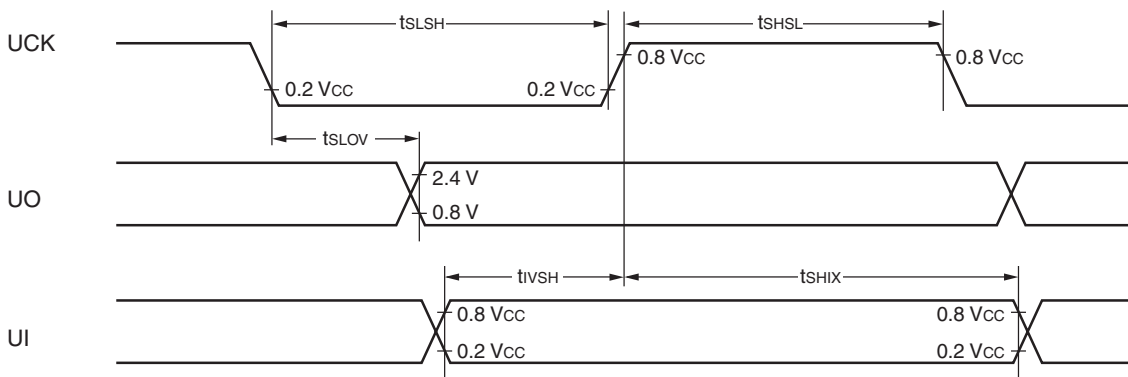
*2 : t_{CP} is the cycle time for the internal operation clock. Refer to (1) “Clock timing ratings”.

Note : The above AC characteristics are for CLK synchronous mode operation.

• Internal shift clock mode



• External shift clock mode



(10) Multi-function serial timing (I²C)

a. Master mode operation

(V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Condi- tions	Standard mode		High-speed mode*3		Unit
			Min	Max	Min	Max	
SCL clock frequency	f _{SCL}	R=1kΩ C=50pF*4	0	100	0	400	kHz
SCL clock "L" width	t _{LOW}		4.7	—	4.7	—	μs
SCL clock "H" width	t _{HIGH}		4.0	—	4.0	—	μs
Bus-free time between "stop" condition and "start" condition	t _{BUS}		4.7	—	1.3	—	μs
Repeat "start" condition setup time SCL↑ → SDA↓	t _{SUSTA}		4.7	—	0.6	—	μs
(Repeat) "start" condition hold time SDA↓ → SCL↓	t _{HDSTA}		4.0	—	0.6	—	μs
"Stop" condition setup time SCL↑ → SDA↑	t _{SUSTO}		4.0	—	0.6	—	μs
Data hold time SCL↓ → SDA↓↑	t _{HDDAT}		2tcp*1	—	2tcp*1	—	μs
Data setup time SDA↓↑ → SCL↑	t _{SUDAT}		250	—	100*2	—	ns

MB90880 Series

b. Slave mode operation

($V_{CC} = 2.7 \text{ V}$ to 3.6 V , $V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Condi- tions	Standard mode		High-speed mode *3		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R=1k Ω C=50pF*4	0	100	0	400	kHz
SCL clock "L" width	t_{LOW}		4.7	—	1.3	—	μs
SCL clock "H" width	t_{HIGH}		4.0	—	0.6	—	μs
Bus-free time between "stop" condition and "start" condition	t_{BUS}		4.7	—	1.3	—	μs
Repeat "start" condition setup time SCL $\uparrow \rightarrow$ SDA $\downarrow$	t_{SUSTA}		4.7	—	0.6	—	μs
(Repeat) "start" condition hold time SDA $\downarrow \rightarrow$ SCL $\downarrow$	t_{HDSTA}		4.0	—	0.6	—	μs
"Stop" condition setup time SCL $\uparrow \rightarrow$ SDA $\uparrow$	t_{SUSTO}		4.0	—	0.6	—	μs
Data hold time SCL $\downarrow \rightarrow$ SDA $\downarrow\uparrow$	t_{HDDAT}		2tcp*1	—	2tcp*1	—	μs
Data setup time SDA $\downarrow\uparrow \rightarrow$ SCL $\uparrow$	t_{SUDAT}		250	—	100*2	—	ns

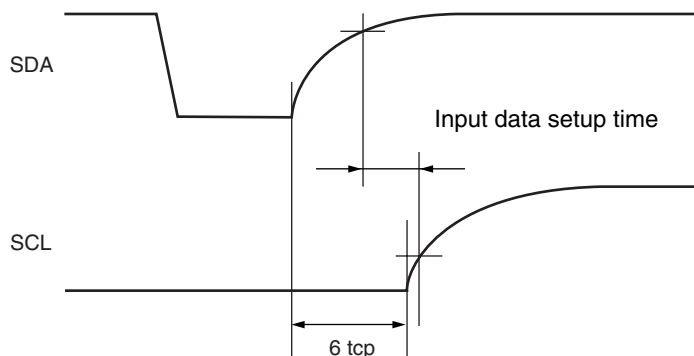
*1 : tcp is the cycle time for the internal operation clock. Refer to (1) "Clock timing ratings".

*2 : The high-speed mode I²C bus device can be used in a standard mode I²C bus system. However, the device must satisfy the required condition " $t_{SUDAT} \geq 250 \text{ ns}$ ". If the device does not extend the "L" period of the SCL signal, the succeeding data must be output to the SDA line before a period of 1250 ns (the maximum time of SDA/SCL rise + t_{SUDAT}) in which the SCL line is open.

*3 : Set the internal operation clock to 6MHz or higher when using this over 100kHz.

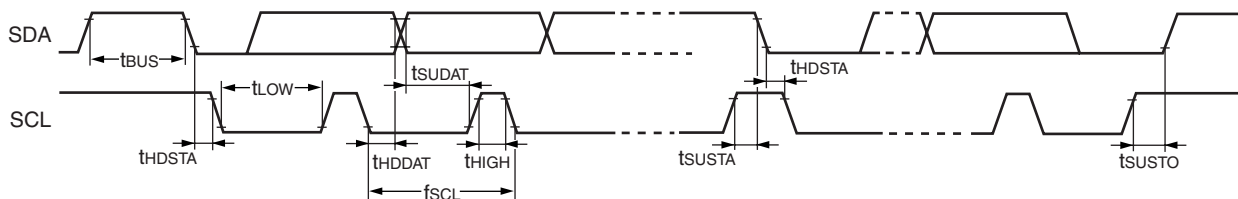
*4 : "R" and "C" are the pull-up resistance and load capacitance of the SCL/SDA lines.

- Note on SDA/SCL setup time



Note: The specification for the input data setup time of the device which is connected to the bus may not be satisfied, depending on the load capacitance and pull-up resistance.
If the specification of the input data setup time can not be satisfied, adjust the pull-up resistance of SDA and SCL.

- Timing definition



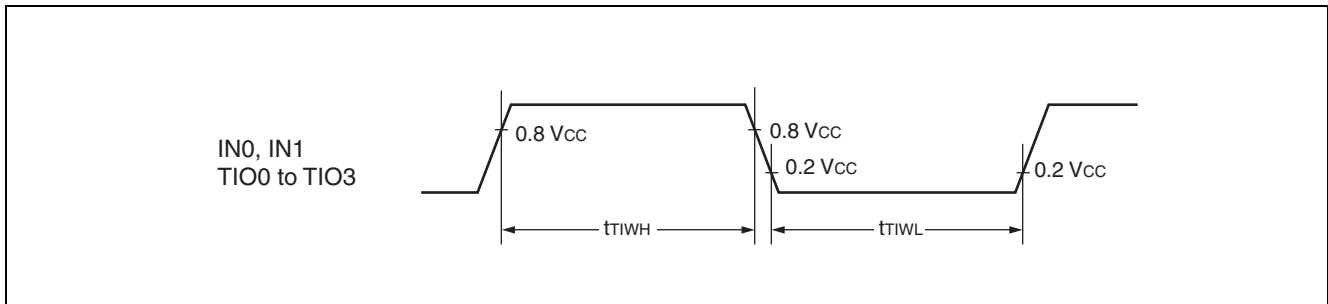
MB90880 Series

(11) Timer input timing

($V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	IN0, IN1, TIO0 to TIO3	—	$4 t_{CP}^*$	—	ns

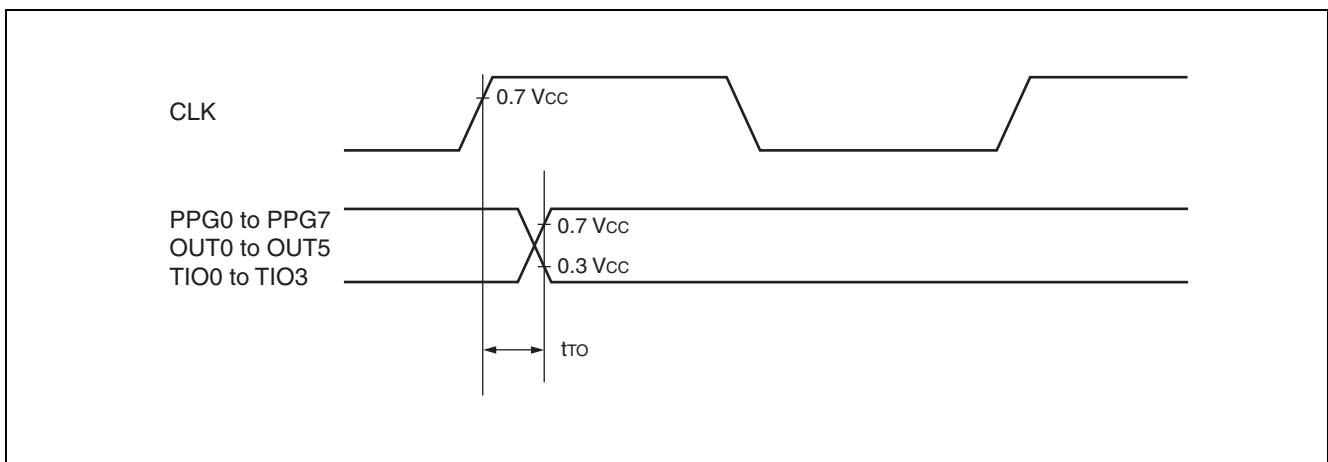
*: t_{CP} is the cycle time for the internal operation clock. Refer to (1) "Clock timing ratings".



(12) Timer output timing

($V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
CLK $\uparrow$ → change time PPG0 to PPG5 change time OUT0 to OUT5 change time	t_{TO}	PPG0 to PPG7, OUT0 to OUT5, TIO0 to TIO3	Load condition : 80 pF	30	—	ns

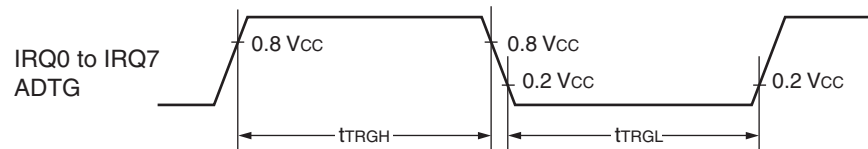


(13) Trigger input timing

($V_{CC} = 2.7 \text{ V}$ to 3.6 V , $V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	ADTG, IRQ0 to IRQ7	—	$5 t_{CP}^*$	—	ns	In normal operation
				1	—	μs	In stop mode

*: t_{CP} is the cycle time for the internal operation clock. Refer to (1) "Clock timing ratings".



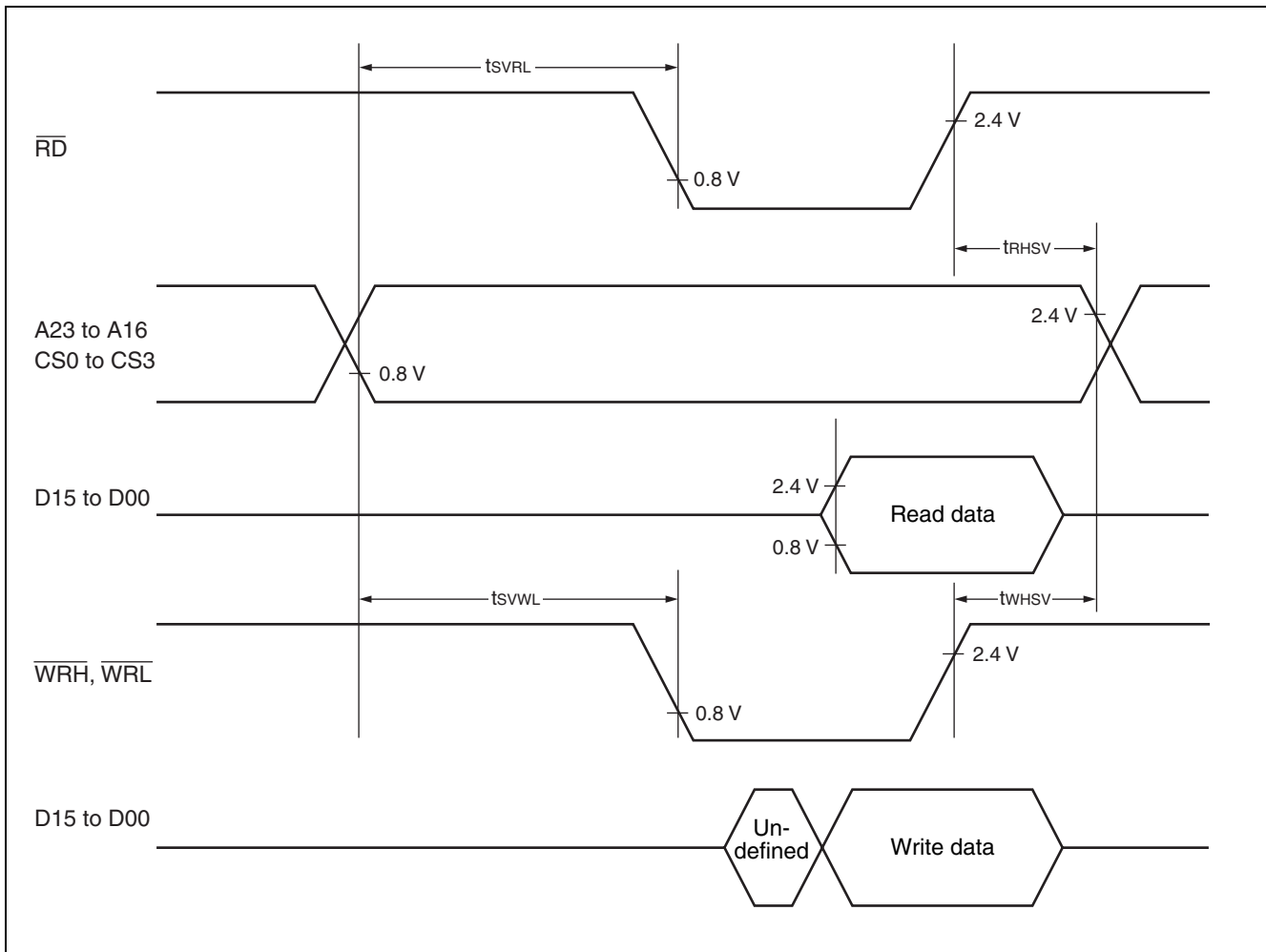
MB90880 Series

(14) Chip select output timing

($V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Chip select output valid time $\rightarrow \overline{RD}\downarrow$	t_{SVRL}	$\overline{CS0}$ to $\overline{CS3}$, $\overline{RD}$	—	$t_{CP}^* / 2 - 7$	—	ns
Chip select output valid time $\rightarrow \overline{WR}\downarrow$	t_{SVWL}	$\overline{CS0}$ to $\overline{CS3}$, $\overline{WRH}$, $\overline{WRL}$	—	$t_{CP}^* / 2 - 7$	—	ns
$\overline{RD}\uparrow \rightarrow$ Chip select output valid time	t_{RHVS}	$\overline{RD}$, $\overline{CS0}$ to $\overline{CS3}$	—	$t_{CP}^* / 2 - 17$	—	ns
$\overline{WR}\uparrow \rightarrow$ Chip select output valid time	t_{WHVS}	$\overline{WRH}$, $\overline{WRL}$, $\overline{CS0}$ to $\overline{CS3}$	—	$t_{CP}^* / 2 - 17$	—	ns

*: t_{CP} is the cycle time for the internal operation clock. Refer to (1) "Clock timing ratings".



Note : The chip select output signal changes simultaneously due to the internal bus configuration; therefore, this may generate a bus wait. AC cannot be warranted between the ALE output signal and the chip select output signal.

5. A/D converter electrical characteristics

($V_{CC} = AV_{CC} = 2.7 \text{ V}$ to 3.6 V , $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $2.7 \text{ V} \leq AVR_H$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Standard	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	± 3.0	LSB	
Linear error	—	—	—	—	± 2.5	LSB	
Differential linear error	—	—	—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	$AV_{SS} - 1.5 \text{ LSB}$	$AV_{SS} + 0.5 \text{ LSB}$	$AV_{SS} + 2.5 \text{ LSB}$	V	
Full-scale transition voltage	V_{FST}	AN0 to AN7	$AVRH - 3.5 \text{ LSB}$	$AVRH - 1.5 \text{ LSB}$	$AVRH + 0.5 \text{ LSB}$	V	
Sampling time	t_{SMP}	—	1.2	—	—	μs	*1
Compare time	t_{CMP}	—	1.8	—	—	μs	*1
Conversion time	t_{CNV}	—	3.0	—	—	μs	*1
Analog port input current	I_{AIN}	AN0 to AN7	- 3.0	—	+ 3.0	μA	
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{SS}	—	$AVRH$	V	
Reference voltage	—	$AVRH$	$AV_{SS} + 2.2$	—	AV_{CC}	V	
Supply current	I_A	AV_{CC}	—	1.9	3.7	mA	
	I_{AH}	AV_{CC}	—	—	5^{*2}	μA	
Reference voltage supply current	I_R	$AVRH$	—	520	720	μA	
	I_{RH}	$AVRH$	—	—	5^{*2}	μA	
Inter-channel variation	—	AN0 to AN7	—	—	4	LSB	

*1 : Time per channel

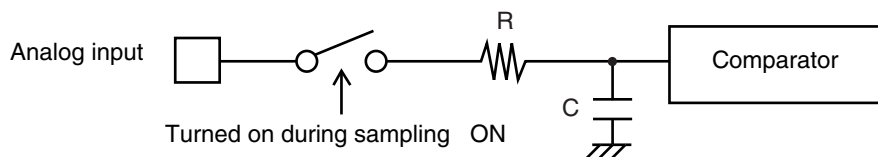
*2 : Current when the A/D converter is not in operation and the CPU is stopped ($V_{CC} = AV_{CC} = AVR_H = 3.0 \text{ V}$)

MB90880 Series

• External impedance and sampling time for analog input

This is an A/D converter with a sample hold function. If high external impedance is preventing it from securing sufficient sampling time, a sufficient analog voltage will not be charged in the internal sample hold capacitor, affecting the accuracy of the A/D conversion. In order to satisfy the A/D conversion accuracy specifications, adjust the register values and operating frequency or decrease the external impedance so that the sampling time becomes longer than the minimum value, based on the relationship between the external impedance and the minimum sampling time. If a sufficient sampling time cannot be secured, connect a capacitor with a capacitance of approximately 0.1 μF to the analog input pin.

Model diagram of analog input circuit



R
12.2k Ω (Max)

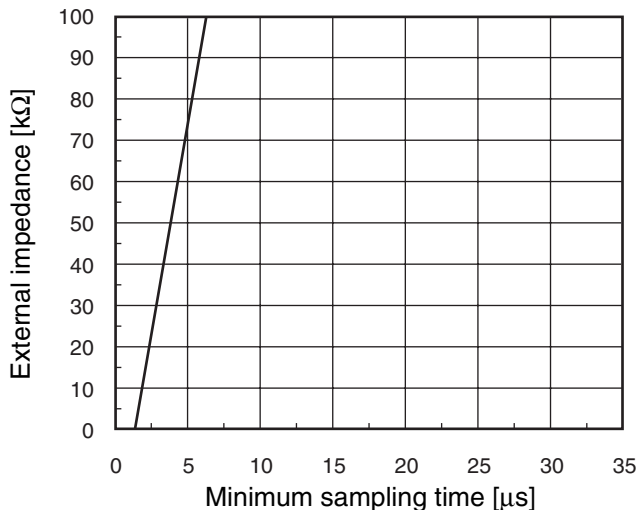
C
8.5pF (Max)

Note : These are reference values.

• Relation between external impedance and minimum sampling time

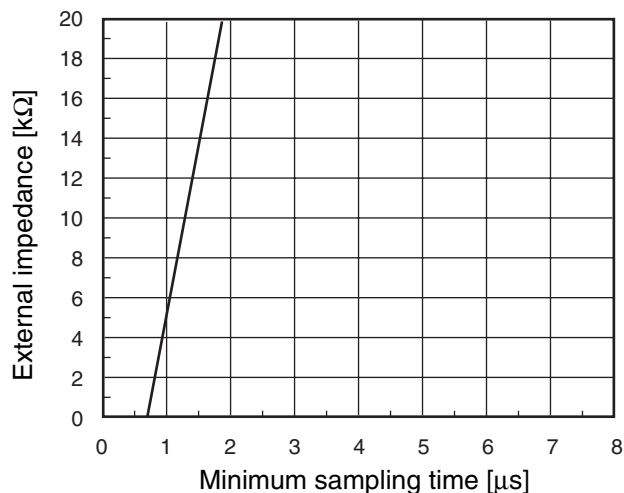
[External impedance = 0 k Ω to 100 k Ω]

Flash memory device
MASK ROM device



[External impedance = 0 k Ω to 20 k Ω]

Flash memory device
MASK ROM device

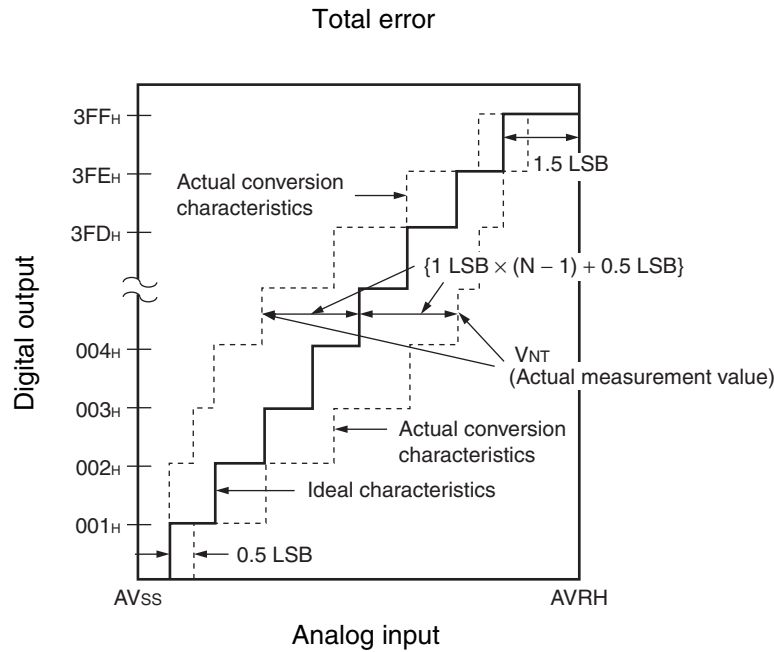


• Errors :

As $|AVRH - AV_{SS}|$ decreases, the absolute error increases.

6. Definition of A/D Converter Terms

Resolution	: Analog variation that is recognized by an A/D converter.
Non linearity error	: Deviation between a line across zero-transition line (“00 0000 0000” $\leftarrow \rightarrow$ “00 0000 0001”) and full-scale transition line (“11 1111 1110” $\leftarrow \rightarrow$ “11 1111 1111”) and actual conversion characteristics.
Differential linearity error	: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
Total error	: Difference between an actual value and a theoretical value. A total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$1 \text{ LSB (Ideal value)} = \frac{AV_{RH} - AV_{SS}}{1024} \text{ [V]}$$

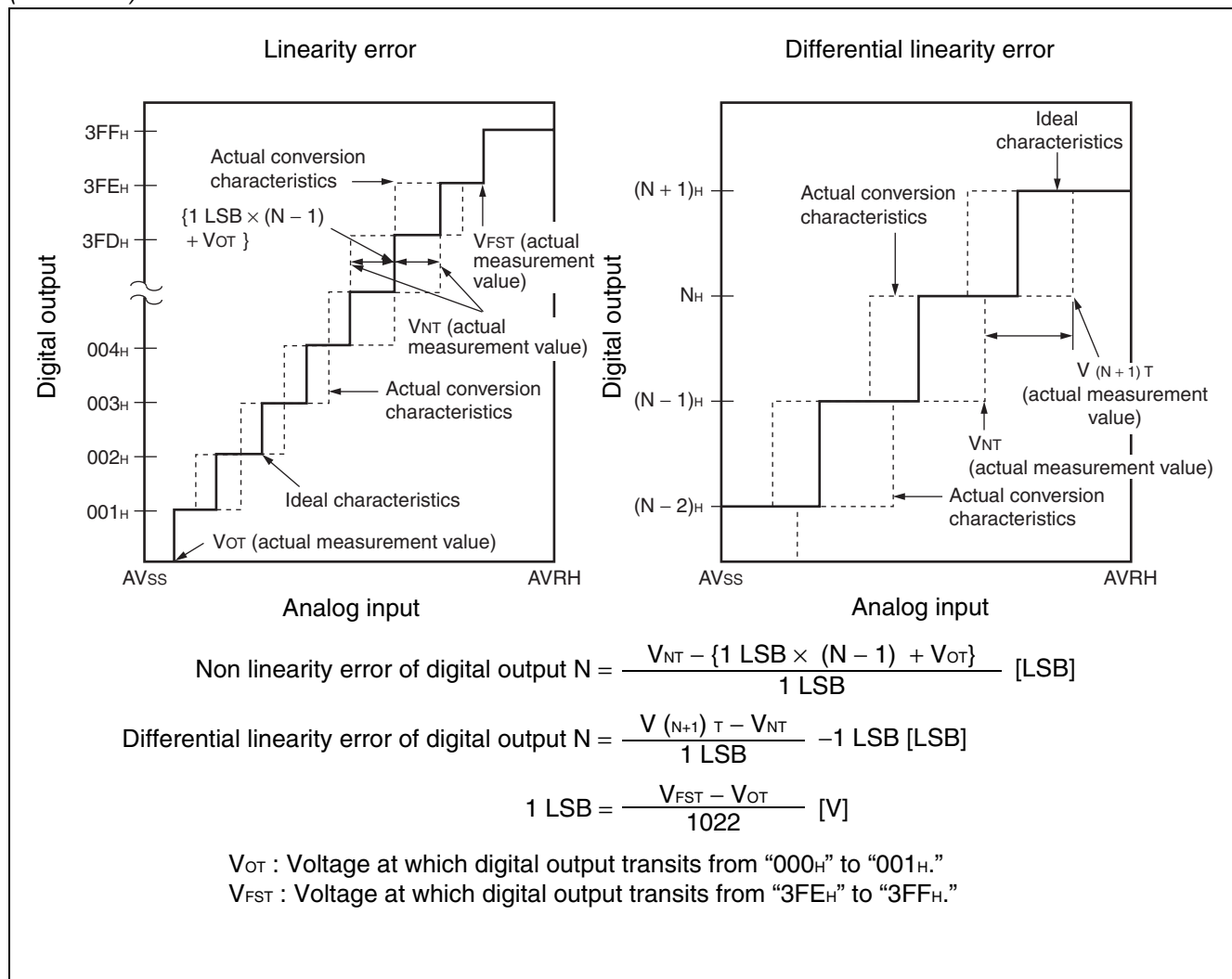
$$V_{OT} \text{ (Ideal value)} = AV_{SS} + 0.5 \text{ LSB [V]}$$

$$V_{FST} \text{ (Ideal value)} = AV_{RH} - 1.5 \text{ LSB [V]}$$

V_{NT} : A voltage at which digital output transits from (N - 1)_H, N_H.

(Continued)

(Continued)



• Flash memory write/erase characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Standard	Max		
Sector erase time	$T_A = +25^\circ\text{C}$, $V_{CC} = 3.0 \text{ V}$	—	0.9	3.6	s	Excludes internal write time before erase operation.
Chip erase time		—	6.2	—	s	Excludes internal write time before erase operation.
Byte (16-bit width) write time		—	23	—	μs	Excludes overhead time at system level.
Number of write/erase cycles	—	10000	—	—	cycle	
Flash memory data hold time	Average $T_A = +85^\circ\text{C}$	100000	—	—	h	*

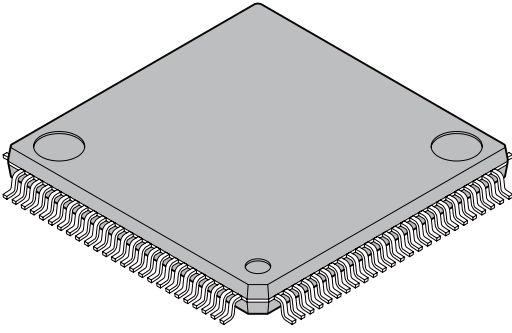
* : Value converted from the evaluation result of technology reliability (The Arrhenius equation is used to convert the high-temperature high-speed test result into the average temperature + 85 °C.)

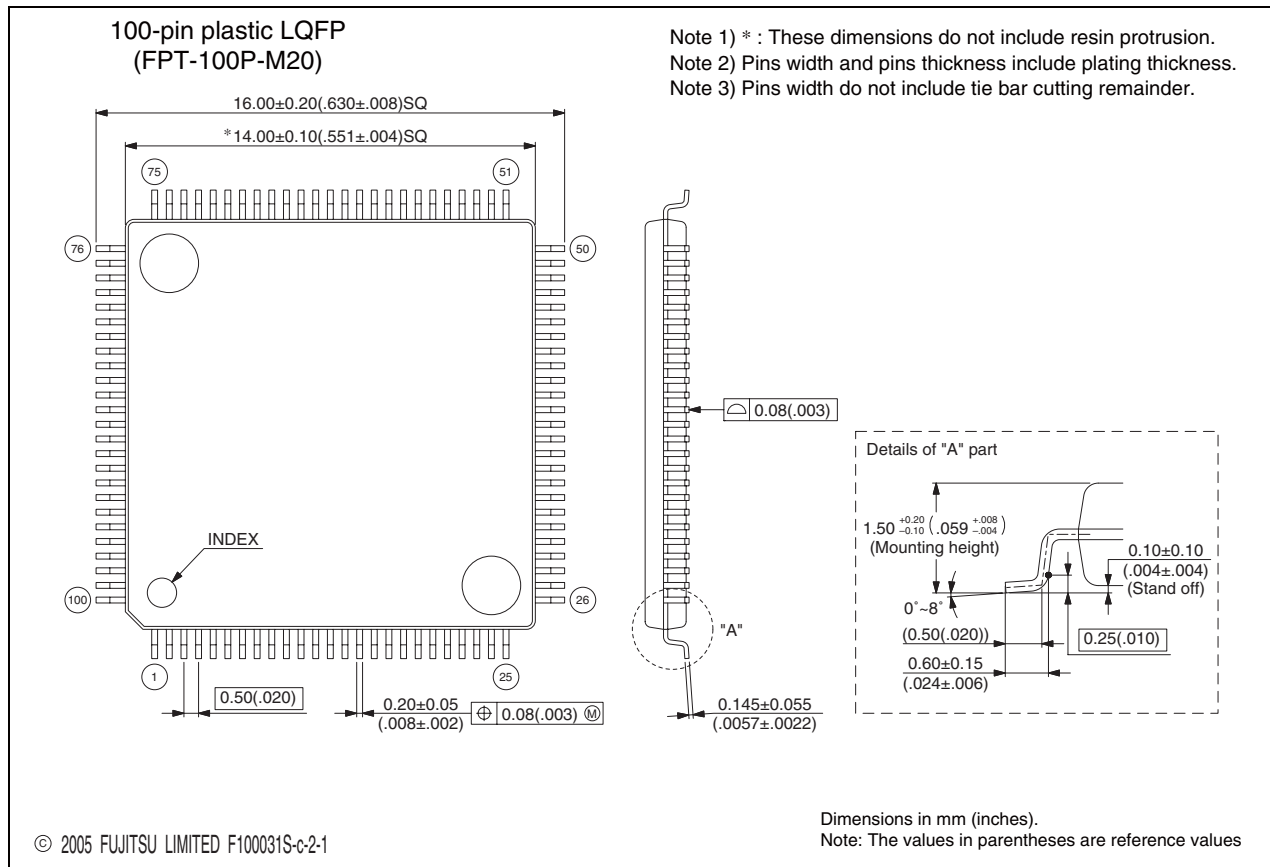
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F882PF MB90F883PF MB90F883APF MB90F884PF MB90F884APF MB90882PF MB90883PF MB90884PF MB90F882SPF MB90F883SPF MB90F883ASPF MB90F884SPF MB90F884ASPF MB90882SPF MB90883SPF MB90884SPF	100-pin plastic QFP (FPT-100P-M06)	With S : Single clock product (without sub clock) Without S : Dual clock product (with sub clock)
MB90F882PMC MB90F883PMC MB90F883APMC MB90F884PMC MB90F884APMC MB90882PMC MB90883PMC MB90884PMC MB90F882SPMC MB90F883SPMC MB90F883ASPMC MB90F884SPMC MB90F884ASPMC MB90882SPMC MB90883SPMC MB90884SPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90V880-101CR-ES MB90V880-102CR-ES MB90V880A-101CR-ES MB90V880A-102CR-ES	299-pin ceramic PGA (PGA-299C-A01)	Evaluation product 101 : Single clock product (without sub clock) 102 : Dual clock product (with sub clock)

MB90880 Series

■ PACKAGE DIMENSIONS

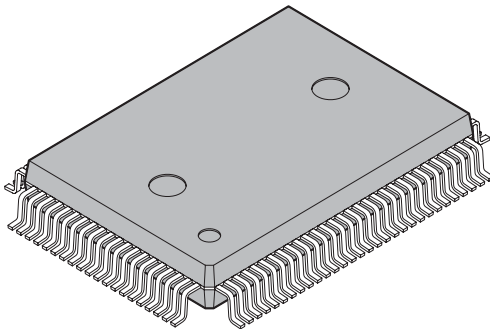
100-pin plastic LQFP  (FPT-100P-M20)	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
	Code (Reference)	P-LFQFP100-14×14-0.50

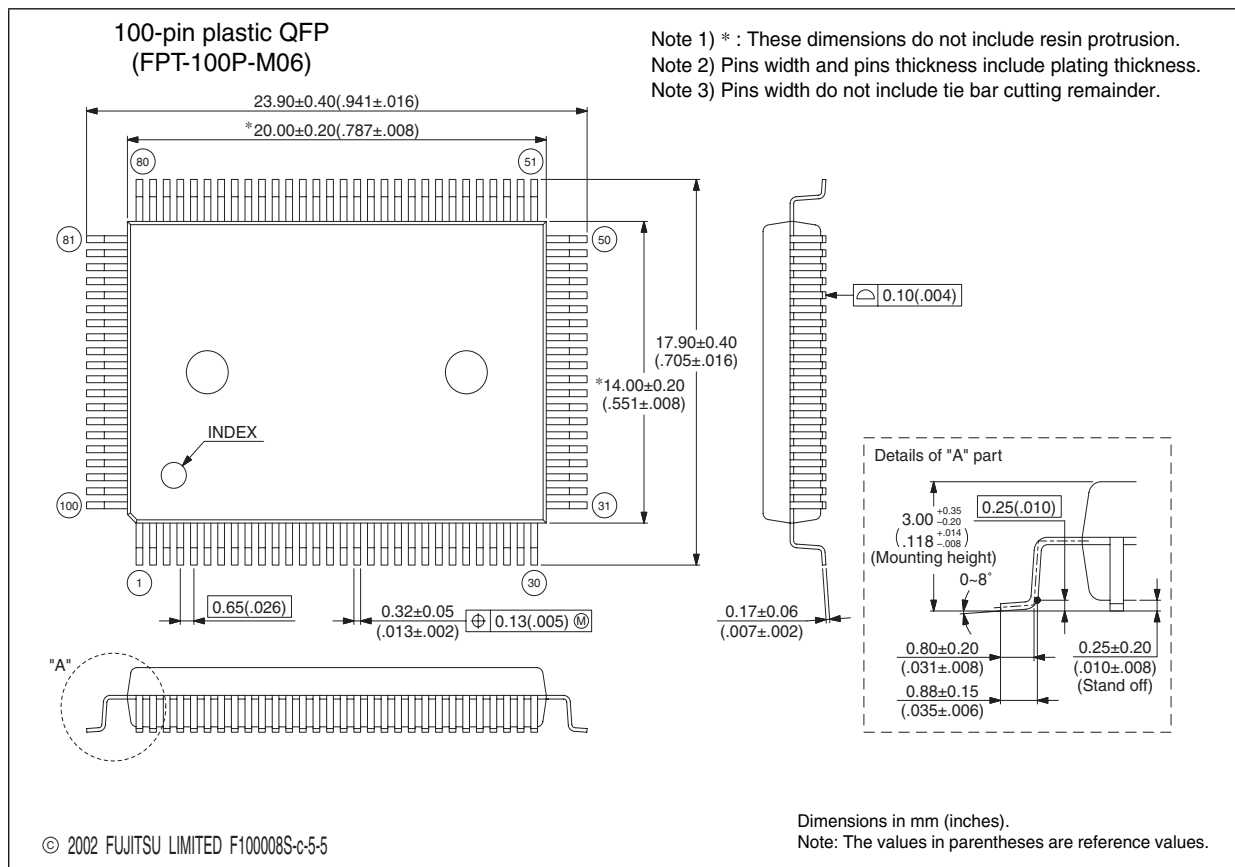


Please confirm the latest Package dimension by following URL.
<http://edevic.fujitsu.com/fj/DATASHEET/ef-ovpkv.html>

(Continued)

(Continued)

 100-pin plastic QFP (FPT-100P-M06)	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65



Please confirm the latest Package dimension by following URL.
<http://edevic.fujitsu.com/fj/DATASHEET/ef-ovpklv.html>

MB90880 Series

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Added the following part numbers: MB90F883A (S), MB90F884A (S)
3	■ PRODUCT LINEUP	Added the following details to the CPU functions: “Maximum operating frequency is 25 MHz in MB90F883 (S) , MB90F884 (S)”
		Added the following details to the base timer: “In MB90F883(S) and MB90F884(S), P24/TIO0, P25/TIO1, P26/TIO2, and P27/TIO3 cannot be used as input function.”
4		Added the "Flash memory" item
21	■ HANDLING DEVICES	Added "13. Note of MB90F883 (S), MB90F884 (S)"
43	■ ELECTRICAL CHARACTERISTICS 2. Recommended operating conditions	Added the "Smoothing capacitor" item
		Added the "• C Pin Connection Diagram"
46	■ ELECTRICAL CHARACTERISTICS 3. DC characteristics	Added the "I _{CTS} " and "I _{CCLS} " items to the supply current
		Changed supply current ratings: I _{CCS} Internal 25 MHz operation; Typ 9 → 6, Max 16 → 12 I _{CCS} Internal 33 MHz operation; Typ 12 → 10, Max 22 → 20 I _{CCL} Typ 70 → 80 I _{CCT} Typ 15 → 20 I _{CCH} Typ 10 → 15
47	■ ELECTRICAL CHARACTERISTICS 4. AC characteristics (1) Clock timing ratings	Added the following details to footnote 1 of the table: “The maximum operating frequency is 25 MHz in MB90F883(S) and MB90F884(S).”
71	■ ORDERING INFORMATION	Added the following part numbers: MB90F883APF, MB90F884APF, MB90F883ASPF, MB90F884ASPF, MB90F883APMC, MB90F884APMC, MB90F883ASPMC, MB90F884ASPMC
		Added the following details to the remarks: With S : Single clock product (without sub clock) Without S : Dual clock product (with sub clock)
		Added the MB90V880 item

The vertical lines marked in the left side of the page show the changes.

MB90880 Series

The information for microcontroller supports is shown in the following homepage.
<http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html>

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