1Gb NAND FLASH

AFND1G08U3

Revision No.	History	Draft Date	Remark
Rev. 00	Initial Draft	June. 2012	Preliminary
Rev. 01	Add new FBGA PKG dimension option (6.5x8.0mm 48B)	Nov. 2012	
Rev. 02	tRP(/RE Pulse Width) 12ns → 15ns	Dec., 2012	
Rev. 03	- VOH, VIL, VOL values control - Read Operation Figure modification - Write Protect figures added	Jan., 2013	
Rev. 04	- Corrected TSOP Package Dimension	May. 2013	
Rev. 05	- Add option of Industrial temperature	Sep.2013	
Rev. 06	- Add 9mmx11mm 63ball BGA PKG option - Generate Industrial grade part no	Nov. 2013	

FEATURES SUMMARY

- **Power Supply**

-3.3V Device(AFND1G08U3) 2.7V ~ 3.6V

- **Organization**

-Memory Cell Array : (128M + 4M) x 8bits
-Data Register : (2048 + 64) x 8bits

- **Automatic Program and Erase**

-Page Program : (2048 + 64) x 8bits
-Block Erase : (128K +4K) x 8bit = 64pages

- **Page Read Operation**

-Page Size : (2048 + 64) x 8bits
-Random Access : 25us(Max.)
-Serial Page Access : 25ns(Min.)

- **Fast Write Cycle Time**

-Program time : 200us(Typ.)
-Block Erase time : 2ms(Typ.)

- **Copy-Back PROGRAM Operation**

- Fast Page copy without external buffering

- **Status Register**

- Normal Status Register (Read/Program/Erase)

- **Security features**

-OTP area, 16Kbytes(8 pages)

- **Hardware Data Protection**

-Program / Erase locked during Power transitions

- **Data Integrity**

-Endurance : 100K Program / Erase Cycles (With 1bit/528byte ECC)
-Data Retention : 10 years

- **Package**

-AFND1G08U3 : Pb-Free Package
48-pin TSOP(12 x 20 / 0.5 mm pitch)
48-Ball FBGA: 9.0 x 9.0 x 1.0mm
48-Ball FBGA: 6.5 x 8.0 x 1.0mm
63-Ball FBGA : 9.0 x 11.0 x 1.0mm

- **Operating Temperature**

- Commercial Grade: 0℃~70℃
- Industrial Grade : -40℃~85℃

Product Information

Part number	Voltage	Bus Width	Package
AFND1G08U3-CKA	2.7~3.6V	x8	12x20mm TSOP
AFND1G08U3-CKC			9.0x9.0mm FBGA
AFND1G08U3-CKD			6.5x8.0mm FBGA
AFND1G08U3-CKE			9.0x11.0mm FBGA
AFND1G08U3-CKAI*			12x20mm TSOP
AFND1G08U3-CKCI			9.0x9.0mm FBGA
AFND1G08U3-CKDI			6.5x8.0mm FBGA
AFND1G08U3-CKEI			9.0x11.0mm FBGA

Note) I* : Industrial Grade

GENERAL DESCRIPTION

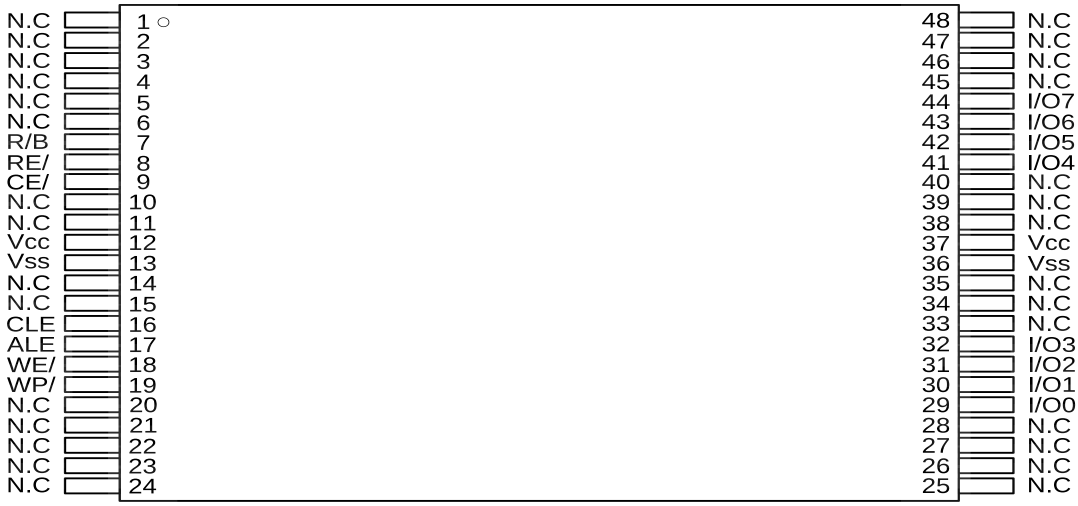
The AFND1G08U3 is 1G-bit with spare 32Mbit capacity. The device is offered in 3.3V power supply. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it possible to preserve valid data while old data is erased. The device contains 1024 blocks, composed by 64 pages consisting in two NAND structures of 16 series connected Flash Cells. A program operation can be performed in typical 200us on the 2048-bytes and an erase operation can be performed in typical 2ms on a 128K-bytes block. Data in the page can be read out at 25ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. Command, Data and Address are synchronously introduced using /CE, /WE, ALE and CLE input pin. The output pin R/B(open drain buffer) signals the status of the device during each operation. In a system with multiple memories the R/B pins can be connected all together to provide a global status signal. The on-chip write control automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the AFND1G08U3's extended reliability of 100K program / erase cycles by providing ECC(Error Correction Code) with real time mapping-out algorithm.

The chip could be offered with the /CE don't care function. This function allows the direct download of the code form the NAND flash memory device by a microcontroller, since the /CE transitions do not stop the read operation.

The copy back function allows the optimization of defective blocks management : when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. Also, this device includes extra features like OTP area, Block mechanism.

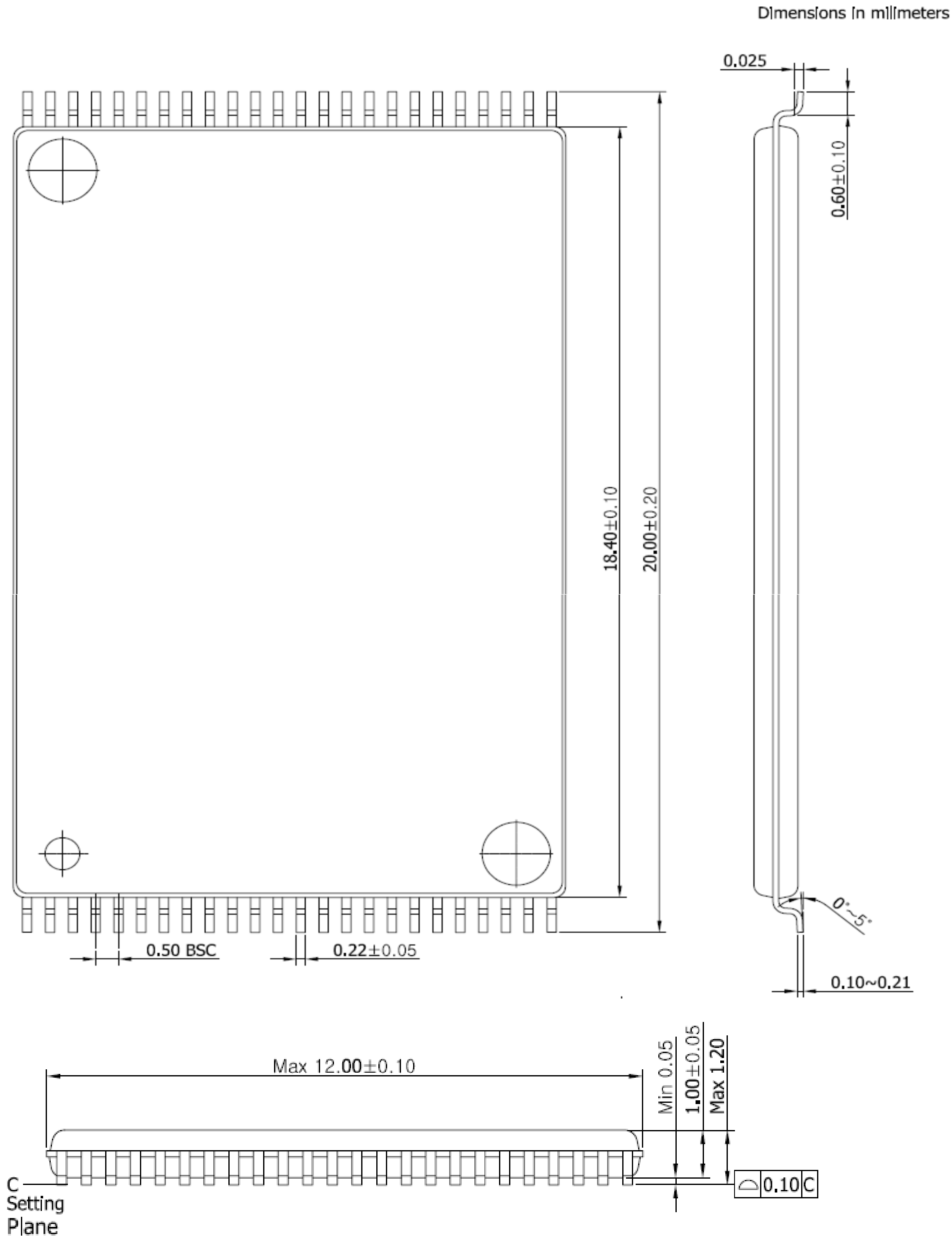
The AFND1G08U3 is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

PIN CONFIGURATION (TSOP1)



PACKAGE DIMENSIONS

48-PIN LEAD/LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

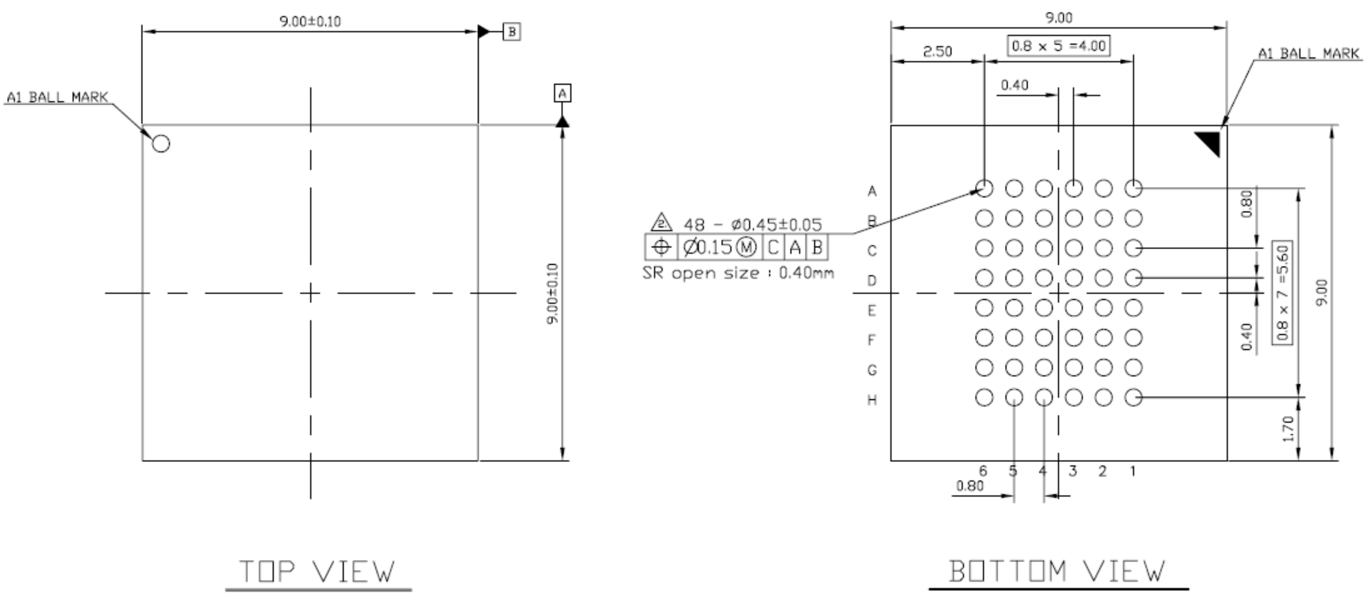


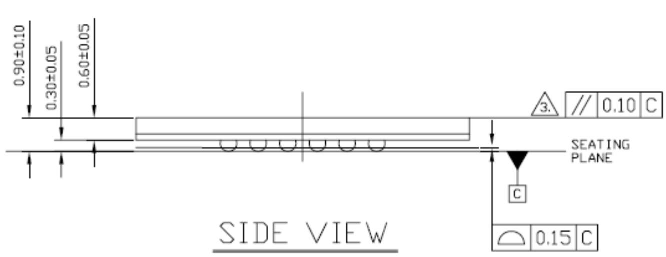
PIN CONFIGURATION (48ball-FBGA)

	1	2	3	4	5	6
A	WP#	ALE	VSS	CE#	WE#	R/B
B	NC	RE#	CLE	NC	NC	NC
C	NC	NC	NC	NC	NC	NC
D	NC	NC	NC	NC	NC	NC
E	NC	NC	NC	NC	NC	NC
F	NC	IO0	NC	NC	NC	VCC
G	NC	IO1	NC	VCC	IO5	IO7
H	VSS	IO2	IO3	IO4	IO6	VSS

TOP VIEW

PACKAGE OUTLINE DRAWING (48ball-FBGA 9x9mm)

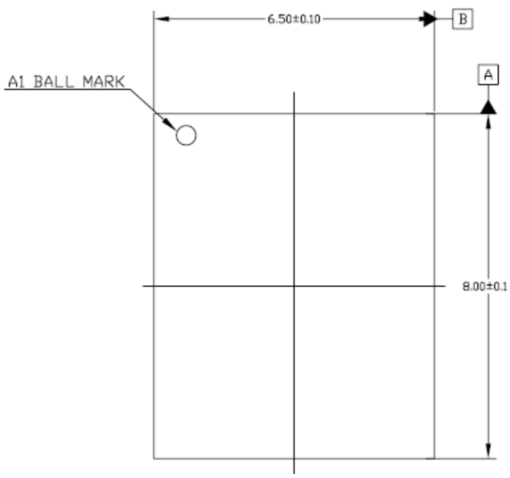




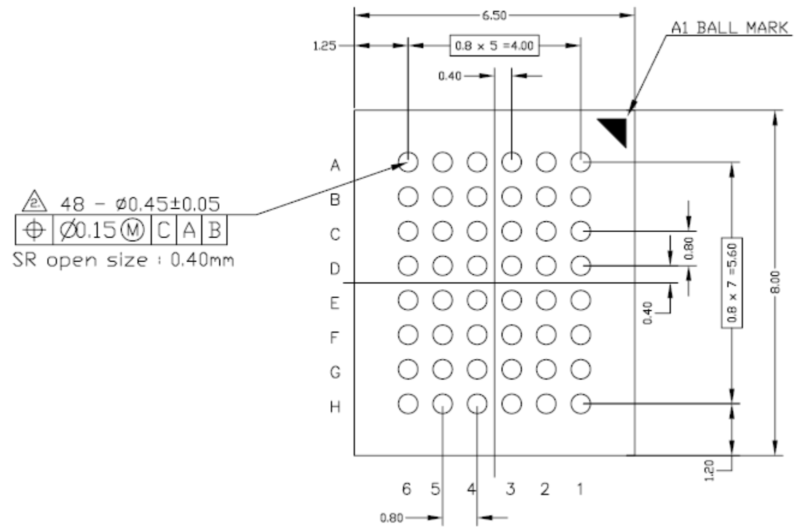
Description
FBGA 48BALL
Dimension
9.0mm x 9.0mm x 0.90mm (Max. 1.0mm T)

1. **ALL DIMENSIONS are in Millimeters.**
2. **POST REFLOW SOLDER BALL DIAMETER.**
   (Pre Reflow diameter : Ø0.40±0.02)

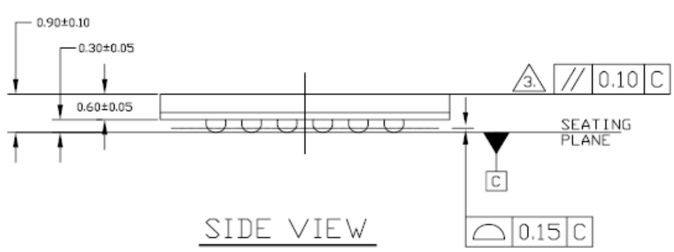
PACKAGE OUTLINE DRAWING (48ball-FBGA 6.5x8mm)



TOP VIEW



BOTTOM VIEW



Description
FBGA 48BALL
Dimension
6.5mm x 8.0mm x 0.90mm (Max. 1.0mm T)

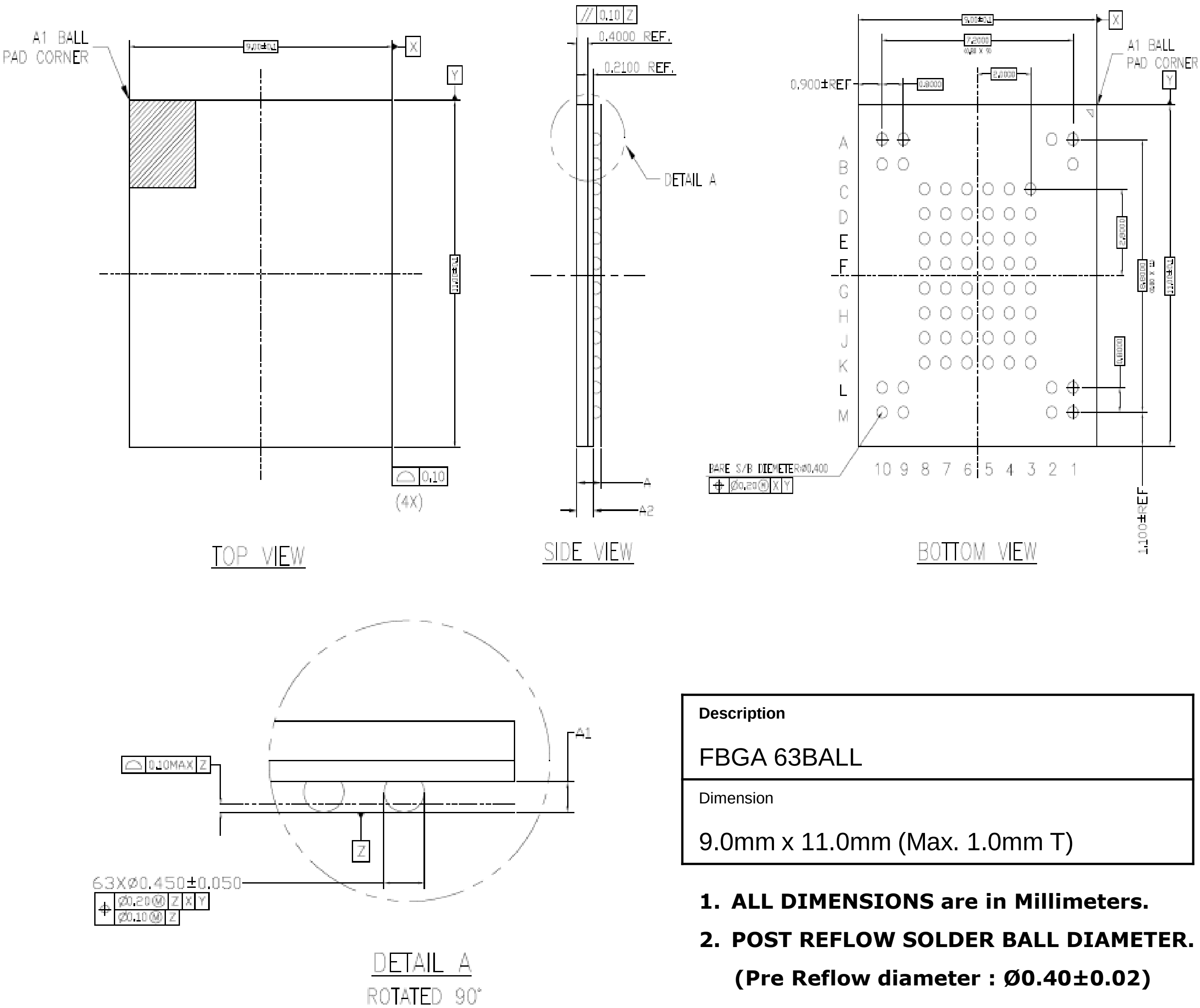
1. **ALL DIMENSIONS are in Millimeters.**
2. **POST REFLOW SOLDER BALL DIAMETER.**
   (Pre Reflow diameter : Ø0.40±0.02)

PIN CONFIGURATION (63ball-FBGA)

			1	2	3	4	5	6		
	NC	NC							NC	NC
	NC								NC	NC
A			WP#	ALE	VSS	CE#	WE#	RB#		
B			NC	RE#	CLE	NC	NC	NC		
C			NC	NC	NC	NC	NC	NC		
D			NC	NC	NC	NC	NC	NC		
E			NC	NC	NC	NC	NC	NC		
F			NC	IO0	NC	NC	NC	VCC		
G			NC	IO1	NC	VCC	IO5	IO7		
H			VSS	IO2	IO3	IO4	IO6	VSS		
	NC	NC							NC	NC
	NC	NC							NC	NC

TOP VIEW

PACKAGE OUTLINE DRAWING (63ball-FBGA 9x11mm)



Description
FBGA 63BALL
Dimension
9.0mm x 11.0mm (Max. 1.0mm T)

1. **ALL DIMENSIONS are in Millimeters.**
2. **POST REFLOW SOLDER BALL DIAMETER.**
   (Pre Reflow diameter : Ø0.40±0.02)

PIN DESCRIPTION

Pin Name	Pin Function
I/O0 ~ I/O7	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the /WE signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of /WE with ALE high
/CE	**CHIP ENABLE** The /CE input is the device selection control. When the device is in the Busy state, /CE high is ignored, and the device does not return to standby mode in program or erase operation. Regarding /CE control during read operation, refer to 'Page Read' section of device operation.
/RE	**READ ENABLE** The /RE input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of /RE which also increments the internal column address counter by one.
/WE	**WRITE ENABLE** The /WE input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the /WE pulse.
/WP	**WRITE PROTECT** The /WP pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the /WP pin is active low.
R/B	**READY/BUSY OUTPUT** The R/B output indicates the status of the device operation. When low, it indicates that a program, erase of random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
VCC	**POWER** VCC is the power supply for device.
VSS	**GROUND**
N.C	**NO CONNECTION** Lead is not internally connected.

Note : Connect all Vcc and Vss pins of each device to common power supply outputs
Do not leave Vcc or Vss disconnected.

Figure 1. AFND1G08U3 FUNCTIONAL BLOCK DIAGRAM

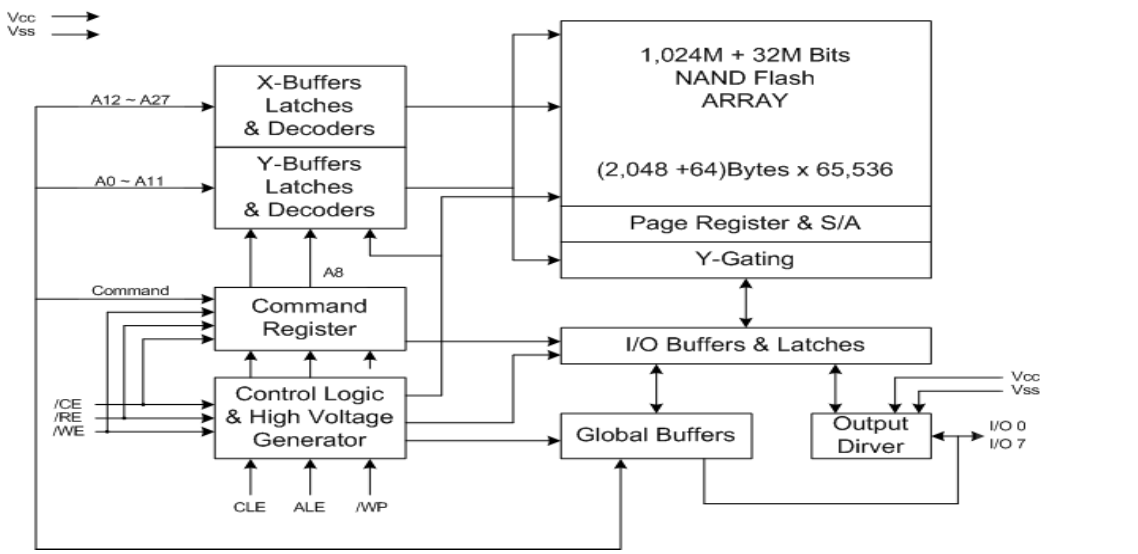
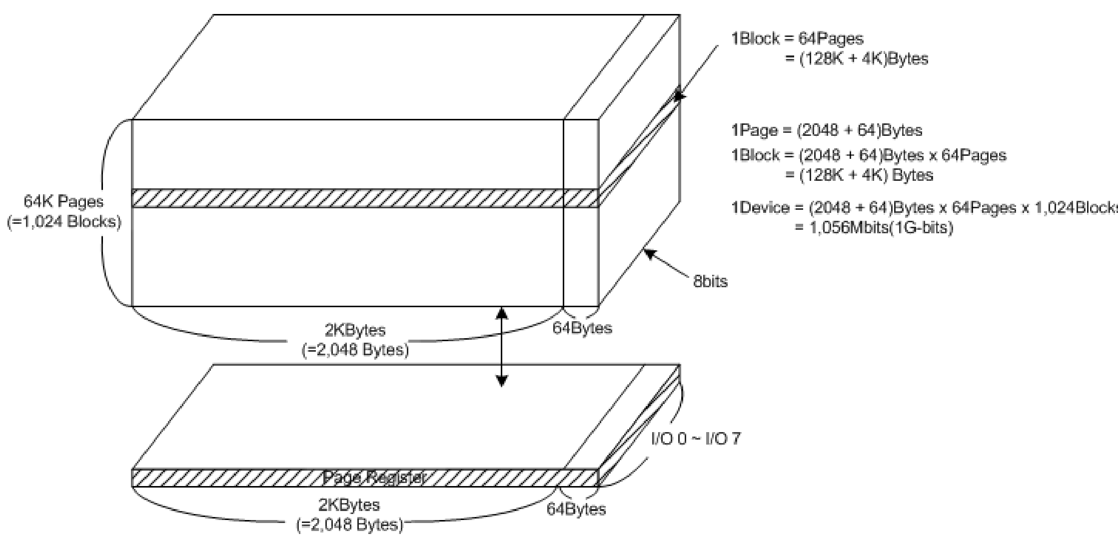


Figure 2. AFND1G08U3 ARRAY ORGANIZATION



	I/O 0	I/O 0	I/O 0	I/O 0	I/O 0	I/O 0	I/O 0	I/O 0	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	← Column Address
2nd Cycle	A8	A9	A10	A11	*L	*L	*L	*L	← Column Address
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19	← Row Address (Page Address)
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27	← Row Address (Page Address)

NOTE : Column Address : Starting Address of the Register.
*** L must be set to "Low"**
*** The device ignores any additional input of address cycles than required.**

PRODUCT INTRODUCTION

The AFND1G08U3 is a 1G-bits(1,107,296,256M bits) memory organized as 65,536 rows(pages) by 2,112byte columns. Spare 64byte columns are located from column address of 2,048~2,112. A 2,048-bytes data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 32 cells resides in a different page. A block consists of the 64 pages formed two NAND structures. A NAND structure consists of 32 cells. Total 1,081,344 NAND structures reside in a block. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 1,024 separately erasable 128K-bytes blocks. It indicates that the bit by bit erase operation is prohibited on the AFND1G08U3.

The AFND1G08U3 has addresses multiplexed into 8 I/O's. This scheme dramatically reduces pin counts and allows systems upgrades to future densities by maintaining consistency in system board design. Command, Address and Data are all written through I/O's by bringing /WE to low while /CE is low. Data is latched on the rising edge of /WE. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. The 132M byte physical space requires 28 addresses, thereby requiring four cycles for byte-level addressing : 2 cycle of column address, 2 cycles of row address, in that order. Page Read and Page Program need the same four address cycles following the required command input.. In Block Erase operation, however only the 2 cycles of row address are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the AFND1G08U3.

Table 1. Command Sets

Function	1'st Cycle	2'nd Cycle	3'rd Cycle	4'th Cycle	Acceptable Command During Busy
Page Read	00h	30h			
Read for Copy back	00h	35h			
Read ID	90h	-			
Reset	FFh	-			o
Page Program	80h	10h			
Copy Back Program	85h	10h			
Block Erase	60h	D0h			
Read Status	70h	-			o
Random Data Input	85h				
Random Data Output	05h	E0h			

NOTE : 1. Random Data Input / Output can be executed in a page.
Caution : Any undefined command inputs are prohibited except for above command set of Table 1.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to Vss	Vcc	-0.6 to + 4.6	V
	VIN	-0.6 to + 4.6	
	VI/O	-0.6 to Vcc + 0.3(<4.6V)	
Temperature Under Bias	TBIAS	-10 to + 125	°C
		-40 to + 125	
Storage Temperature	TSTG	-65 to + 150	°C
Short Circuit Current	IOS	5	mA

NOTE :

1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods<30ns.
   Maximum DC voltage on input/output pins is Vcc+0.3V which, during transitions, may overshoot to Vcc+2.0V for periods<20ns..
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATING are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(AFND1G08U3-CX : T_A = 0 to 70℃, AFND1G08U3-IX : T_A = -40 to 85℃)

Parameter	Symbol	3.3V			Unit
		Min	Typ	Max	
Supply Voltage	Vcc	2.7	3.3	3.6	V
	Vss	0	0	0	V

Device	Temp.
AFND1G08U3-CX	0 ~ 70°C
AFND1G08U3-IX	-40°C ~ 85°C

DC AND OPERATING CHARACTERISTICS

Parameter		Symbol	Test Conditions	3.3V			Unit
				Min	Typ	Max	
Operating Current	Sequential Read	ICC1	tRC=42ns, /CE=VIL, Iout=0mA	-	15	30	mA
	Program	ICC2		-	15	30	
	Erase	ICC3		-	15	30	
Standby Current(TTL)		ISB1	/CE-VIH, /WP=0V/Vcc	-	-	1	
Standby Current(CMOS)		ISB2	/CE=Vcc-0.2, /WP=0V/Vcc	-	10	50	uA
Input Leakage Current		ILI	VIN=0 to Vcc(max)	-	-	±10	
Output Leakage Current		ILO	Vout=0 to Vcc(max)	-	-	±10	
Input High Volgate		VIH	-	0.8xVcc	-	Vcc +0.3	V
Input Low Voltage, All inputs		VIL	-	-0.3	-	0.2xVcc	
Output High Voltage Level		VOH	AFND1G08U3 : IOH = -400uA	2.4	-	-	
Output Low Voltage Level		VOL	AFND1G08U3 : IOL = 2.1mA	-	-	0.4	
Output Low Current(R/B)		IOL (R/B)	VOL=0.4V	8	10	-	mA

VALID BLOCK

Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Number	NVB	1,004	-	1,024	Blocks

Note :

1. The device may include invalid blocks when first shipped. Additional invalid blocks may develop while being
   used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for a appropriate management of invalid blocks.

2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/528Byte ECC.

3. Minimum 1,004 valid blocks are guaranteed for each contiguous 128Mb memory space.

AC TEST CONDITION

(AFND1G08U3-CX : T_A = 0 to 70℃, AFND1G08U3-IX : T_A = -40 to 85℃)

Parameter	Value
	AFND1G08U3(3.3V)
Input Pulse Levels	0 V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load	1 TTL GATE and CL=50pF

CAPACITANCE (Temp=25℃, Vcc=3.3V, f=1.0Mhz)

Item	Symbol	Test Condition	Min	Typ	Max
Input/Output Capacitance	CI/O	VIL=0V	-	10	pF
Input Capacitance	CIN	VIN=0V	-	10	pF

MODE SELECTION

CLE	ALE	/CE	/WE	/RE	/WP	Mode	
H	L	L	↑edge	H	X	Read Mode	Command Input
L	H	L	↑edge	H	X		Address Input(4 clocks)
H	L	L	↑edge	H	H	Write Mode	Command Input
L	H	L	↑edge	H	H		Address Input(4 clocks)
L	L	L	↑edge	H	H	Data Input	
L	L	L	H	↓edge	X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc(2)	Standby	

Note : 1. X can be VIL or VIH

2. /WP should be biased to CMOS high or CMOS low for standby.

Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	tPROG(1)	-	200	700	us
Number of Partial Program Cycles in the same page	Nop	-	-	8	Cycle
Block Erase Time	tBERS	-	2	3	ms

Note : 1. Typical Program time is defined as the time within which more than 50% of the whole pages are programmed at Vcc of 3.3V and 25°c
2. Typical value is measured at Vcc=3.3V, Temp=25°c. Not 100% tested.

AC TIMING CAHARACTERISTICS FOR COMMAND / ADDRESS / DATA INPUT

Parameter	Symbol	Min	Max	Unit
CLE setup Time	tCLS	12	-	ns
CLE Hold Time	tCLH	5	-	ns
/CE setup Time	tCS	20	-	ns
/CE Hold Time	tCH	5	-	ns
/WE Pulse Width	tWP(1)	12	-	ns
ALE setup Time	tALS	12	-	ns
ALE Hold Time	tALH	5	-	ns
Data setup Time	tDS	12	-	ns
Data Hold Time	tDH	5	-	ns
Write Cycle Time	tWC	25	-	ns
/WE High Hold Time	tWH	10	-	ns
Address to Data loading Time	tADL	100	-	ns

Note : 1. The transition of the corresponding control pins must occur only once while /WE is held low.
2. tADL is th time from the /WE rising edge of final address cycle to the /WE rising edge of first data cycle.

AC CAHARACTERISTICS FOR OPERATION

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	tR	-	25	us
ALE to /RE Delay	tAR	10	-	ns
CLE to /RE Delay	tCLR	10	-	ns
Ready to /RE Low	tRR	20	-	ns
/RE Pulse Width	tRP	15	-	ns
WE High to Busy	tWB	-	100	ns
Read Cycle Time	tRC	25	-	ns
/RE Access Time	tREA	-	20	ns
/CE Access Time	tCEA	-	25	ns
/RE High to Output Hi-Z	tRHZ	-	100	ns
/CE High to Output Hi-Z	tCHZ	-	30	ns
/CE High to ALE or CLE Don't Care	tCSD	0	-	ns
/RE high to Output Hold	tRHOH	15		ns
/RE Low to Output Hold	tRLOH	5		ns
/CE High to Output hold	tCOH	15	-	ns
/RE High Hold Time	tREH	15	-	ns
Output Hi-Z to /RE Low	tIR	0	-	ns
/RE High to /WE Low	tWHR	60	-	ns
/WE High to /RE Low	tWHR	60	-	ns
Device resetting time(Read/Program/Erase)	tRST	-	5/10/500(1)	us

Note : 1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.

NAND FLASH TECHNICAL NOTES

Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by ATO. The information regarding the initial invalid blocks(s) is so called as the initial invalid block information.

Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/528Byte ECC.

Identifying Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. ATO makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 2048. Since the initial invalid block Information is also erasable in most cases, it is impossible to recover the information once it has been erased.

Therefore, the system must be able to recognize the initial invalid block(s) based on the initial invalid block information. And create the initial invalid block table via the following suggested flow chart(Figure3). Any intentional erasure of the Initial invalid block information is prohibited.

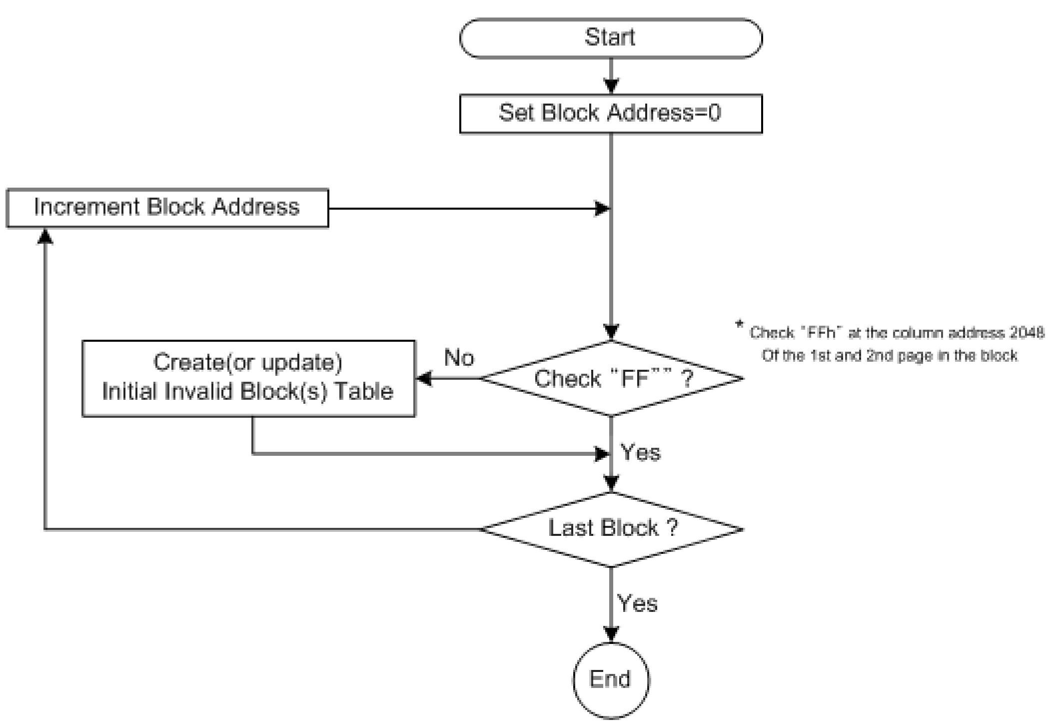


Figure 3. Flow chart to create initial invalid block table

Error in write or read operation

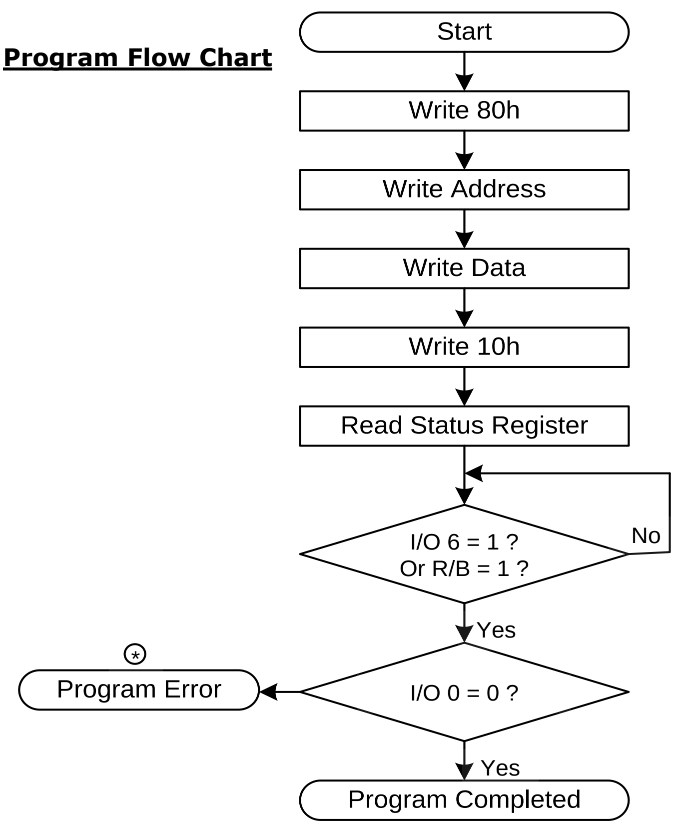
Within its life time, the additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the block failure rate. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and

copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read failure due to single bit error should be reclaimed by ECC without any block replacement. The block failure rate in the qualification report does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase → Block Replacement
	Program Failure	Status Read after Program → Block Replacement
Read	Single Bit Failue	Verify ECC → ECC Correction

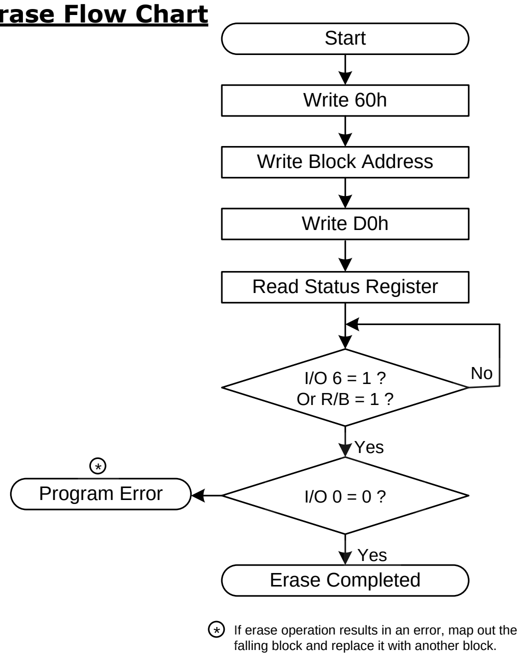
ECC : Error Correcting Code → Hamming Code etc. (Example : 1bit Correction & 2bits detection)

Program Flow Chart

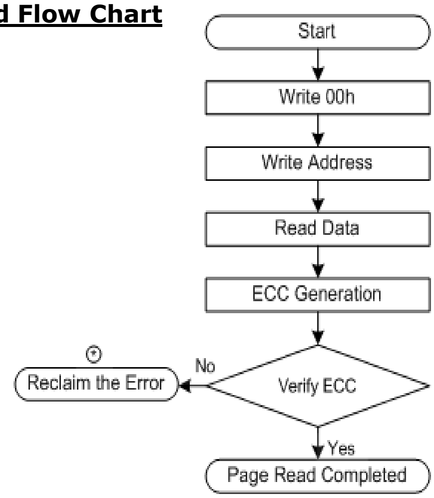


(*) If program operation results in an errors, map out the Block including the page in error and copy the target Data to another block.

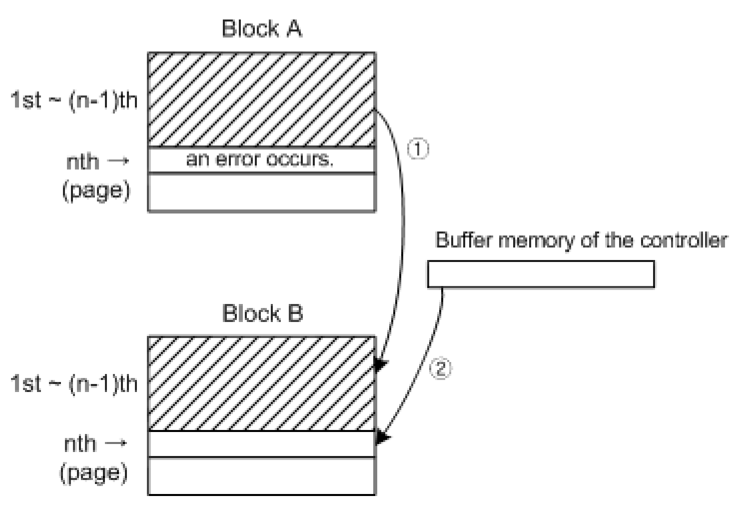
Erase Flow Chart



Read Flow Chart



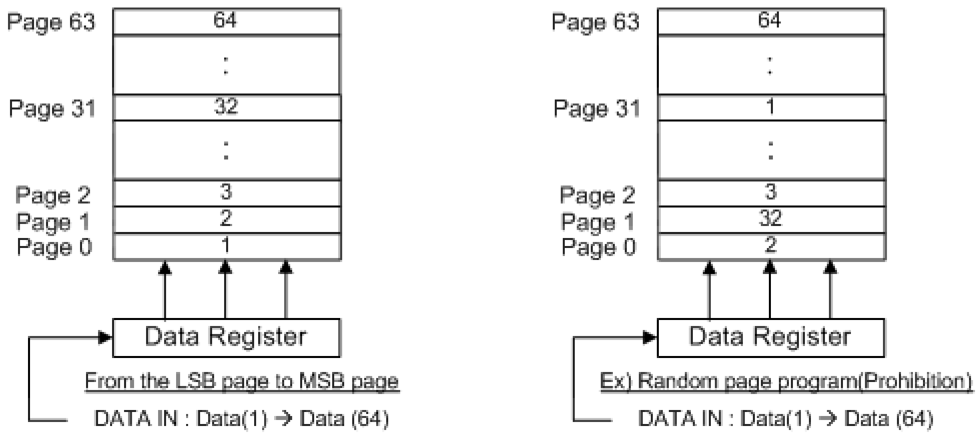
Block Replacement



* Step1. When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2. Copy the data in the 1st ~ (n-1)th page to the same location of another free block(Block 'B)
* Step3. Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'
* Step4. Do not erase or program to Block 'A' by creating an 'invalid Block' table or other appropriate scheme.

Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB(least significant bit) page of the block to the MSB(most significant bit) pages of the block. Random page address programming is prohibite In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB doesn't need to be page 0.'



System Interface Using /CE don't-care

For an easier system interface, /CE may be inactive during the data-loading or sequential data-reading as shown below. The internal 2,112byte data registers are utilized as separate buffers for this operation and the system design gets more flexible.

In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating /CE during the data-loading and reading would provide significant savings in power consumption.

Figure 4. Program Operation with /CE don't care.

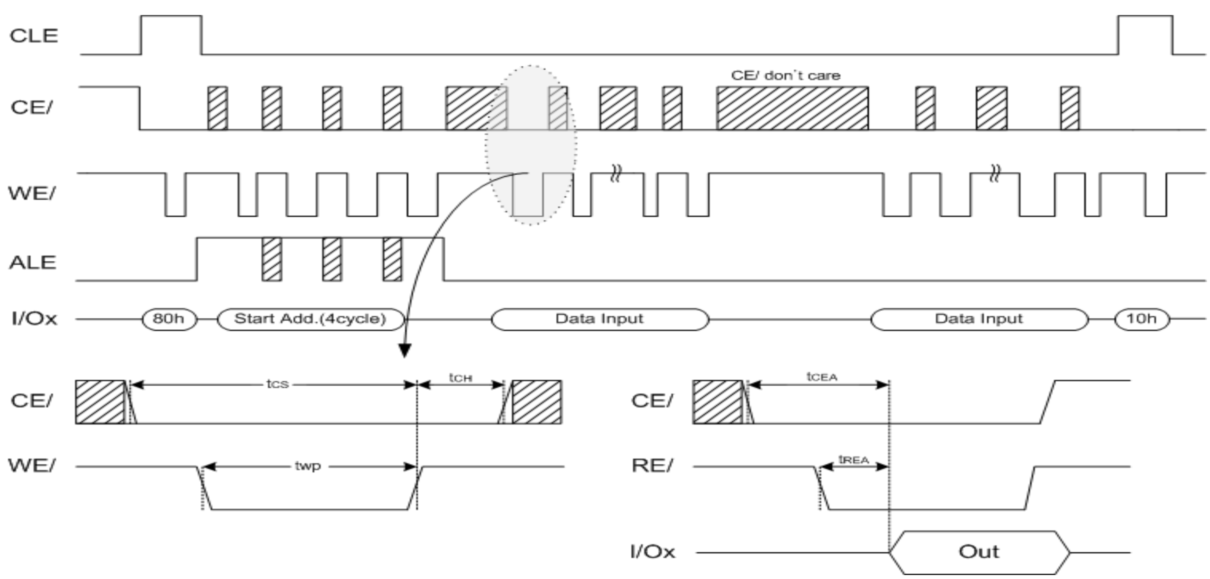
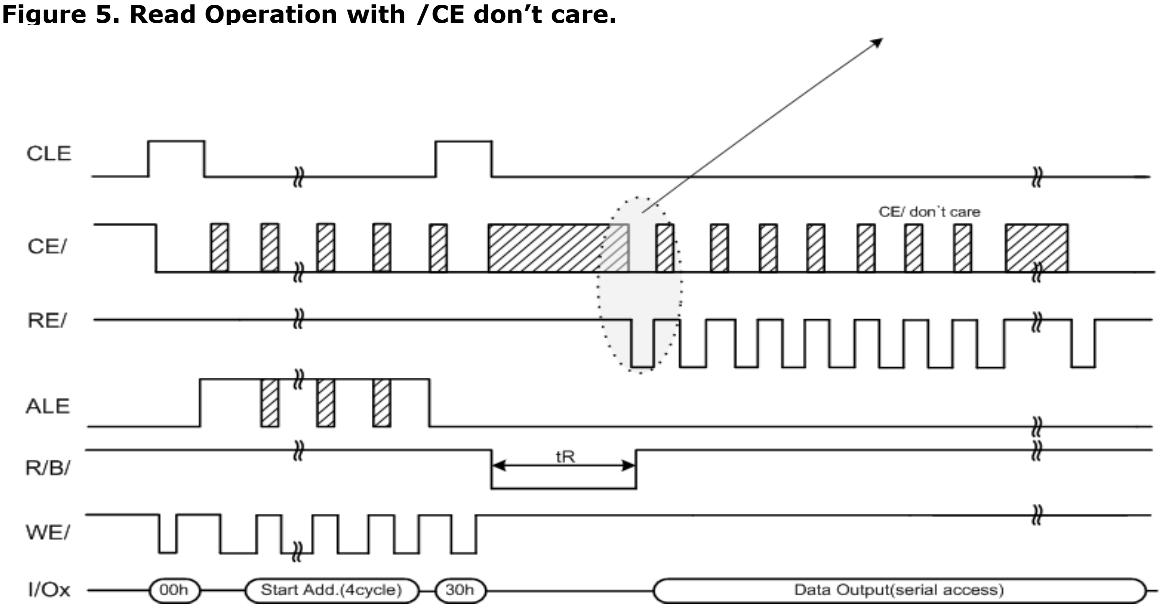
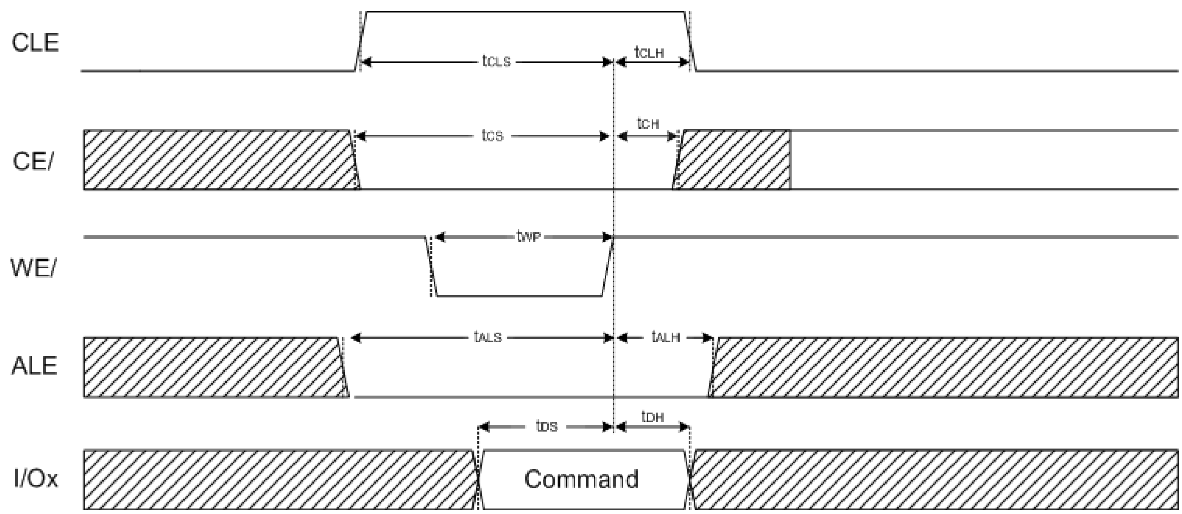


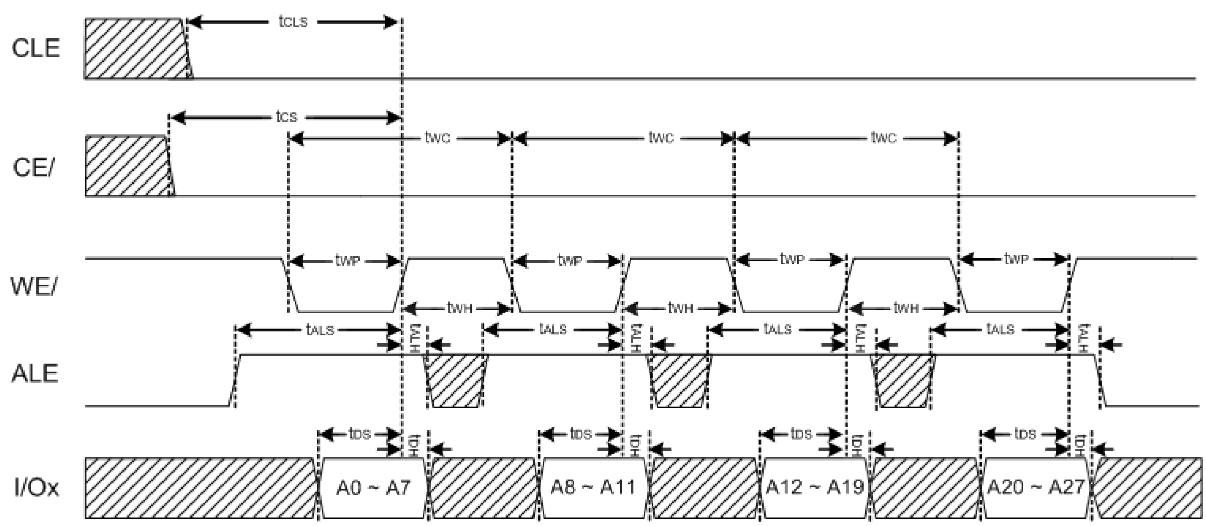
Figure 5. Read Operation with /CE don't care.



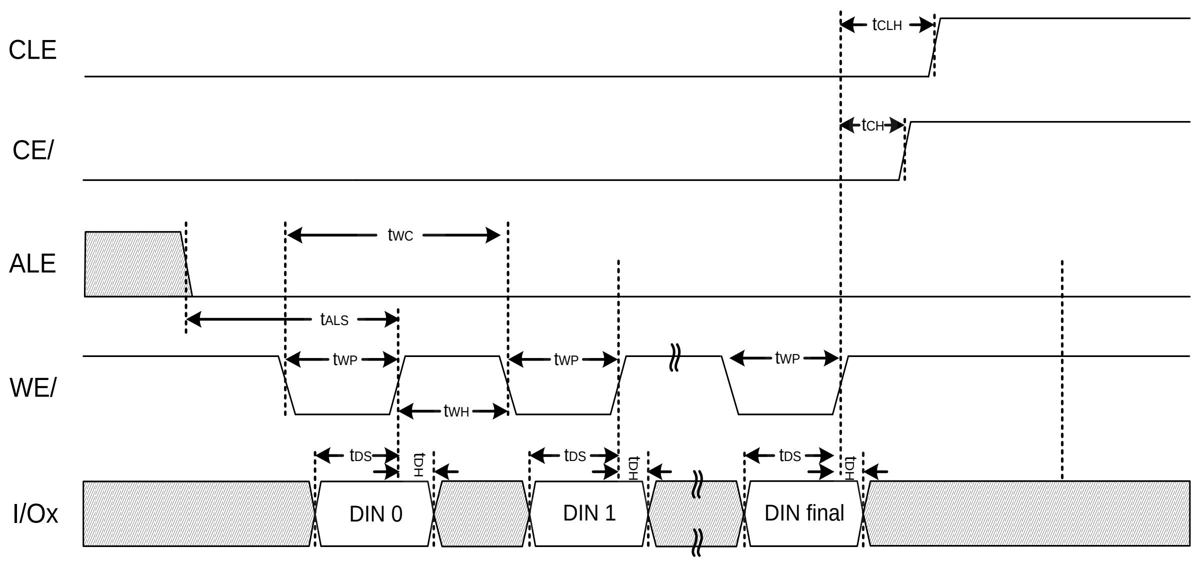
*** Command Latch Cycle**



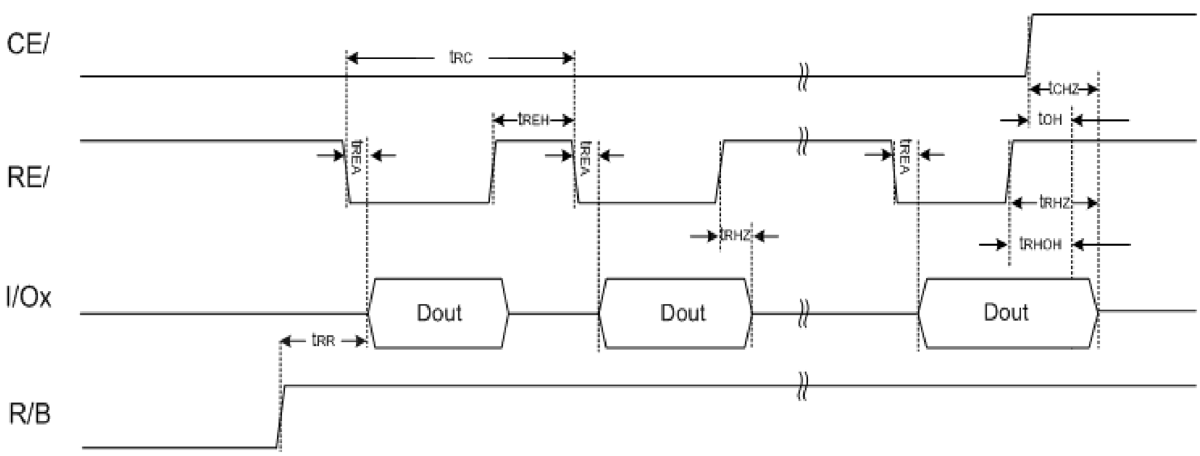
*** Address Latch Cycle**



*** Input Data Latch Cycle**

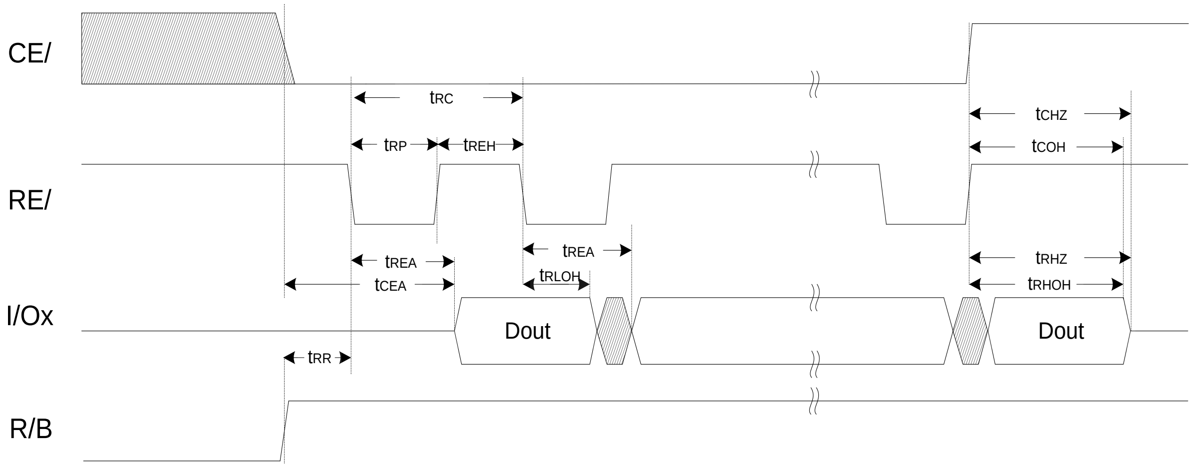


*** Serial access Cycle after Read(CLE=L, /WE=H, ALE=L)**



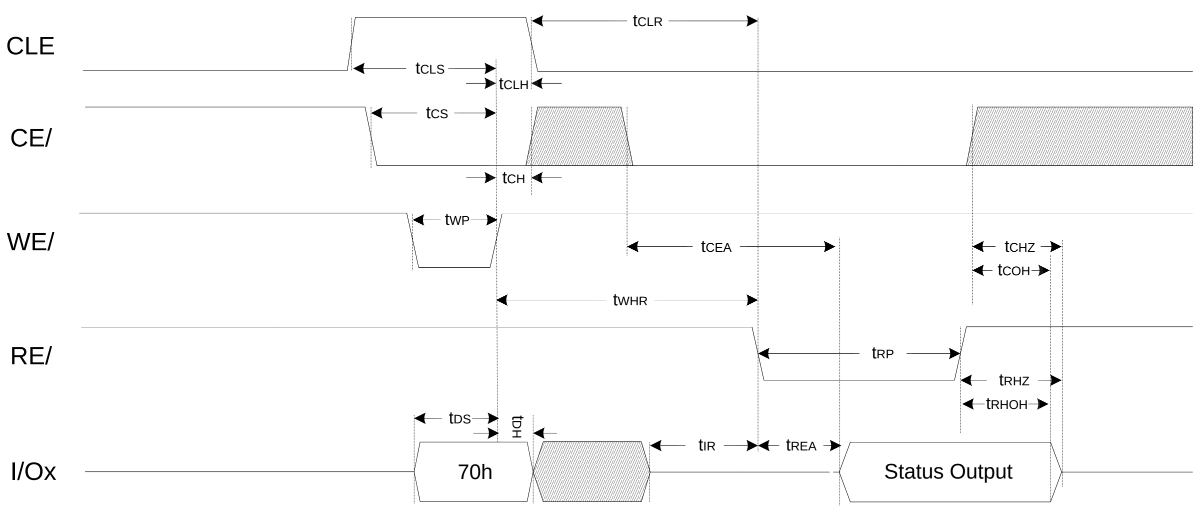
Note Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.
tRLOH is valid when frequency is higher than 33Mhz.
tRHOH starts to be valid when frequency is lower than 33Mhz.

*** Serial access cycle after Read (EDO Type, CLE=L, /WE=H, ALE=L)**

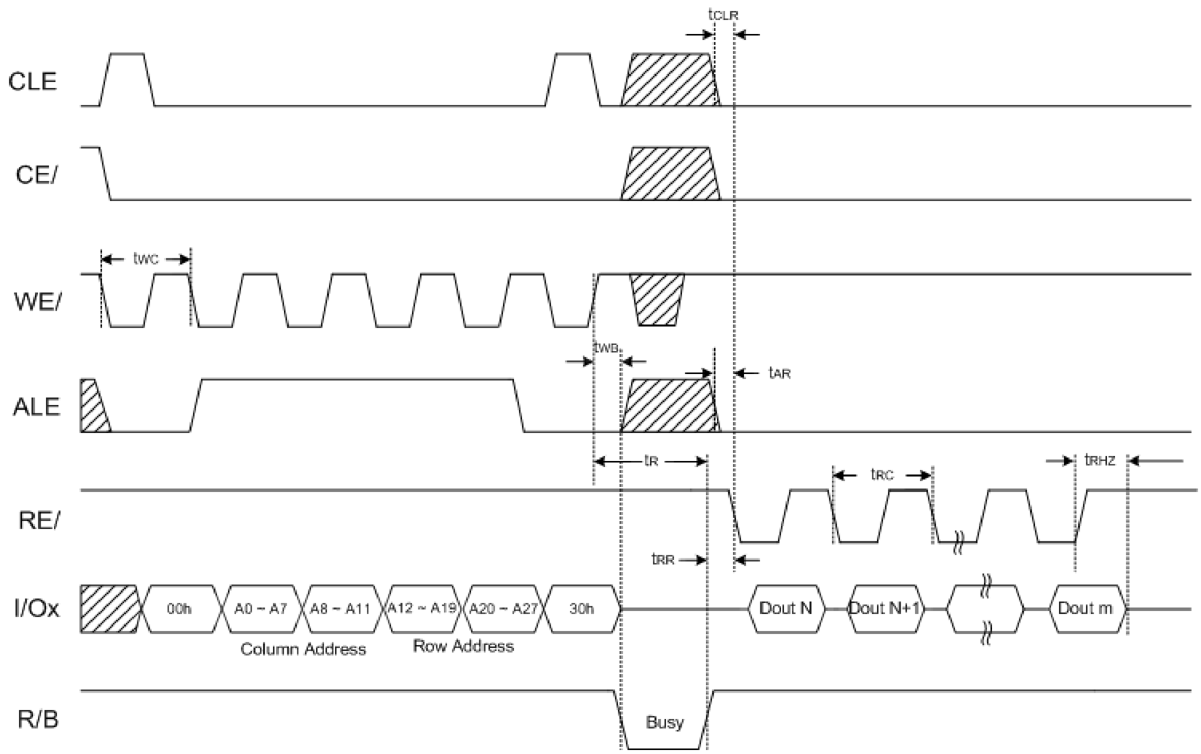


Note : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.
tRLOH is valid when frequency is higher than 33Mhz.
tRHOH starts to be valid when frequency is lower than 33Mhz

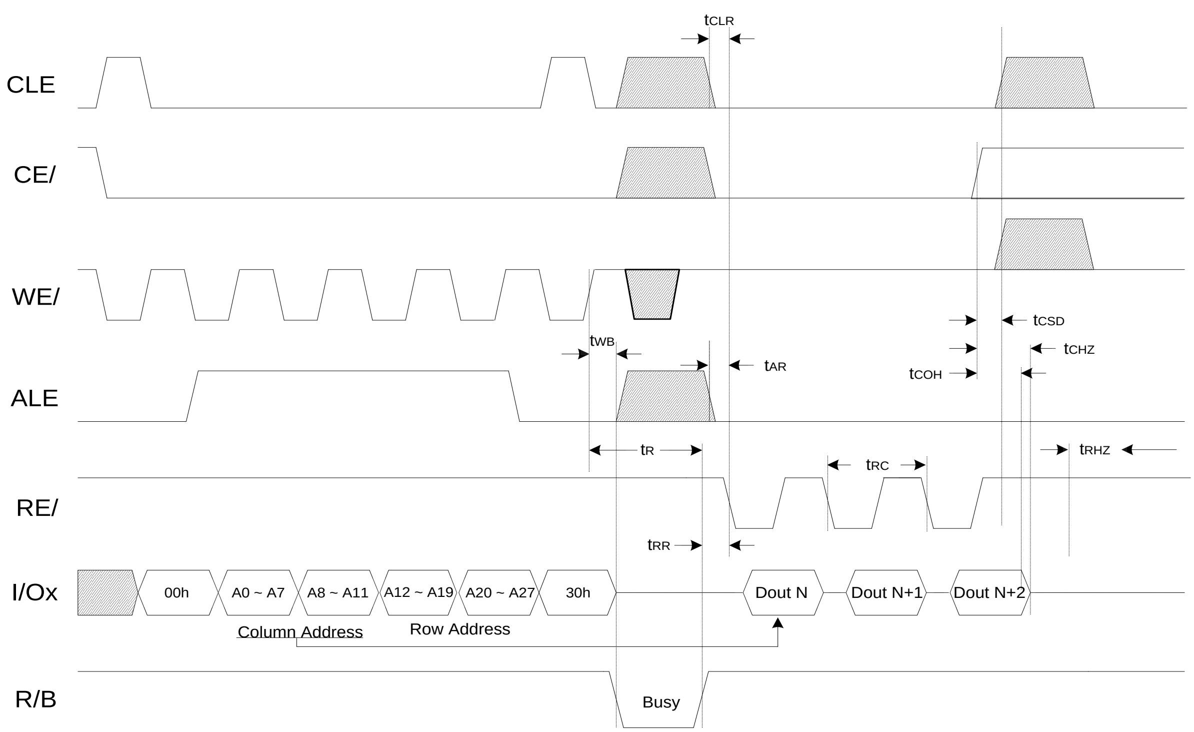
*** Status Read Cycle**



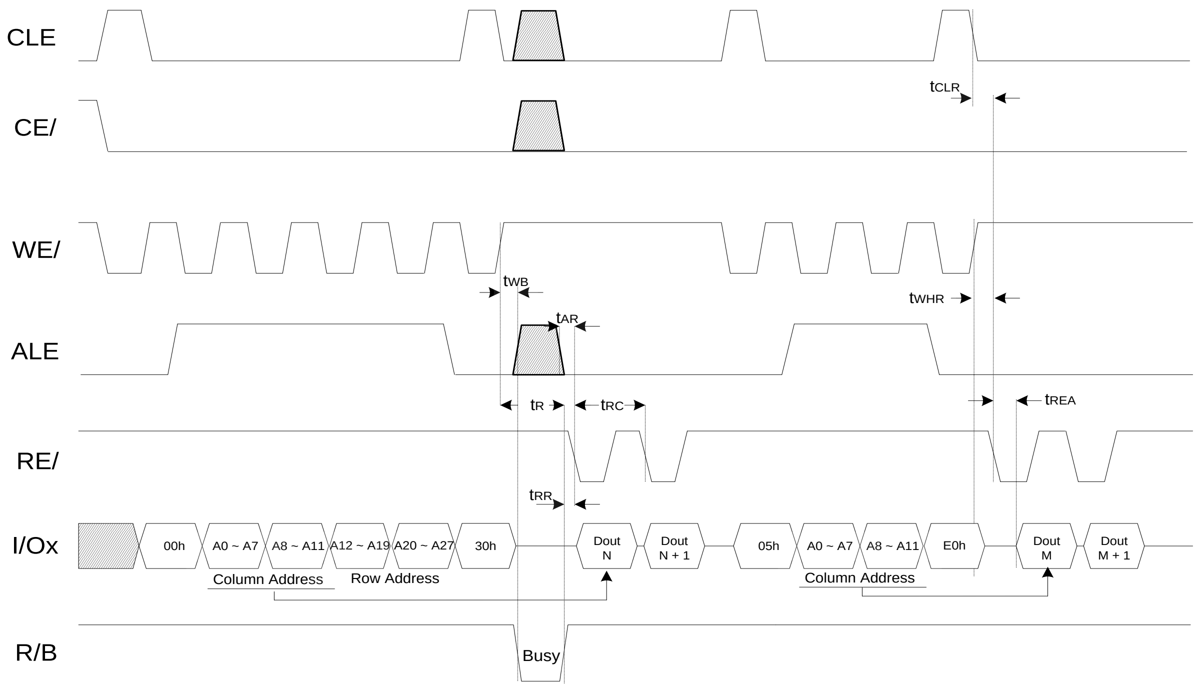
*** READ OPERATION**



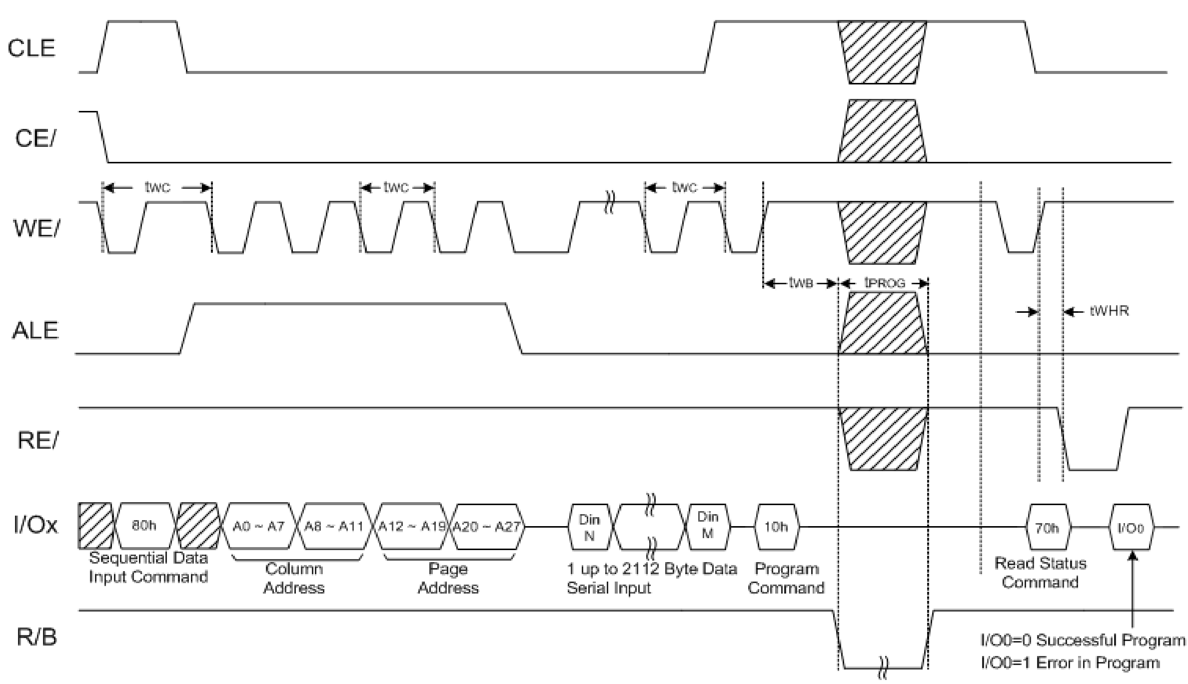
*** READ Operation (Intercepted by /CE)**



* Random Data Output in a Page

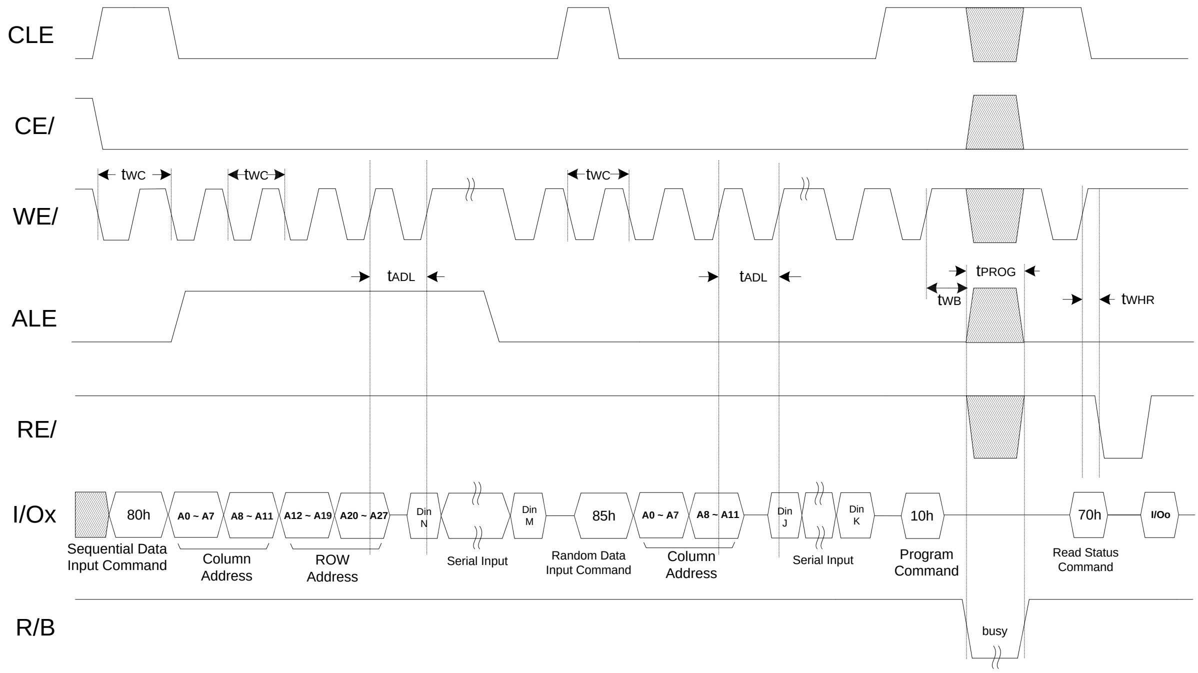


* Page Program Operation

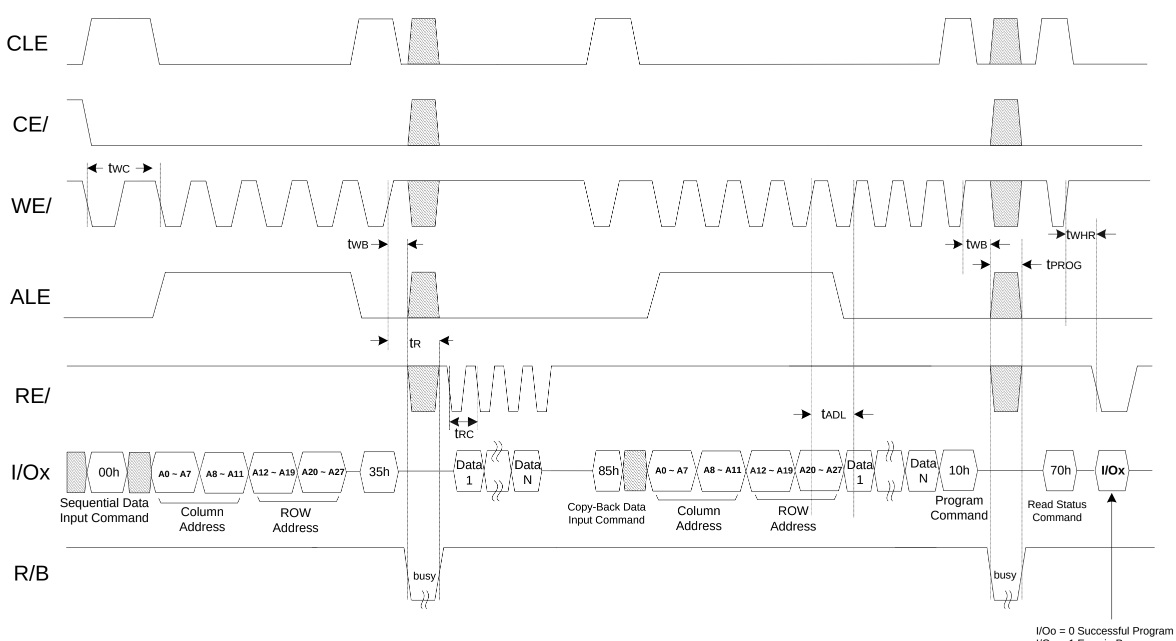


Note : tADL is th time from the /WE rising edge of final address cycle to the /WE rising edge of first data cycle

* Page Program Operation with Random Data Input

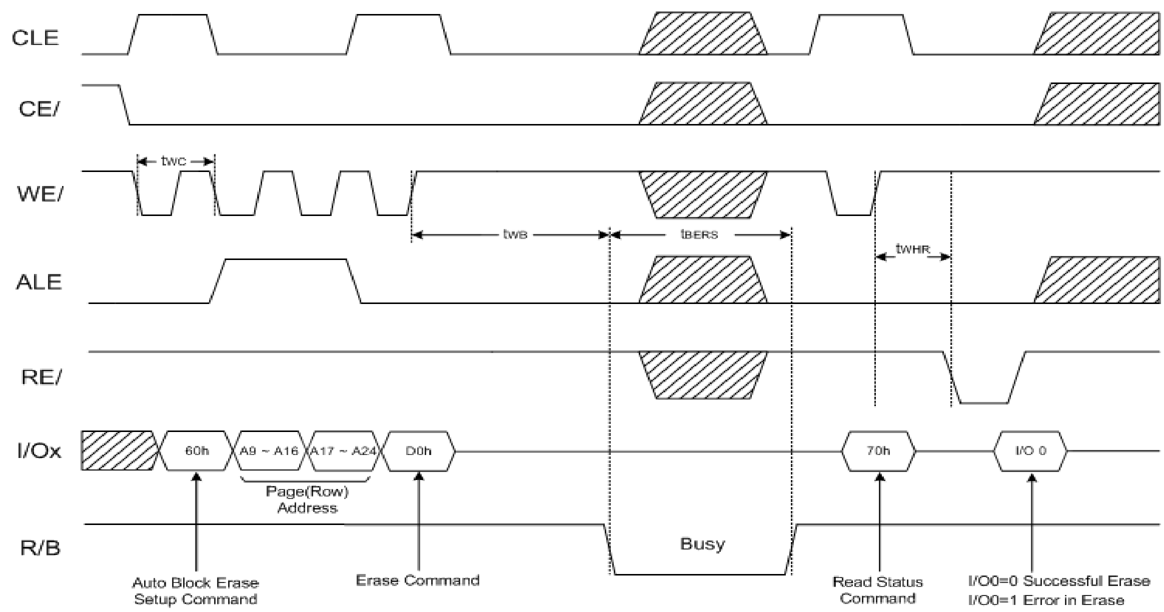


* Copy-Back Program Operation with Random Data Input

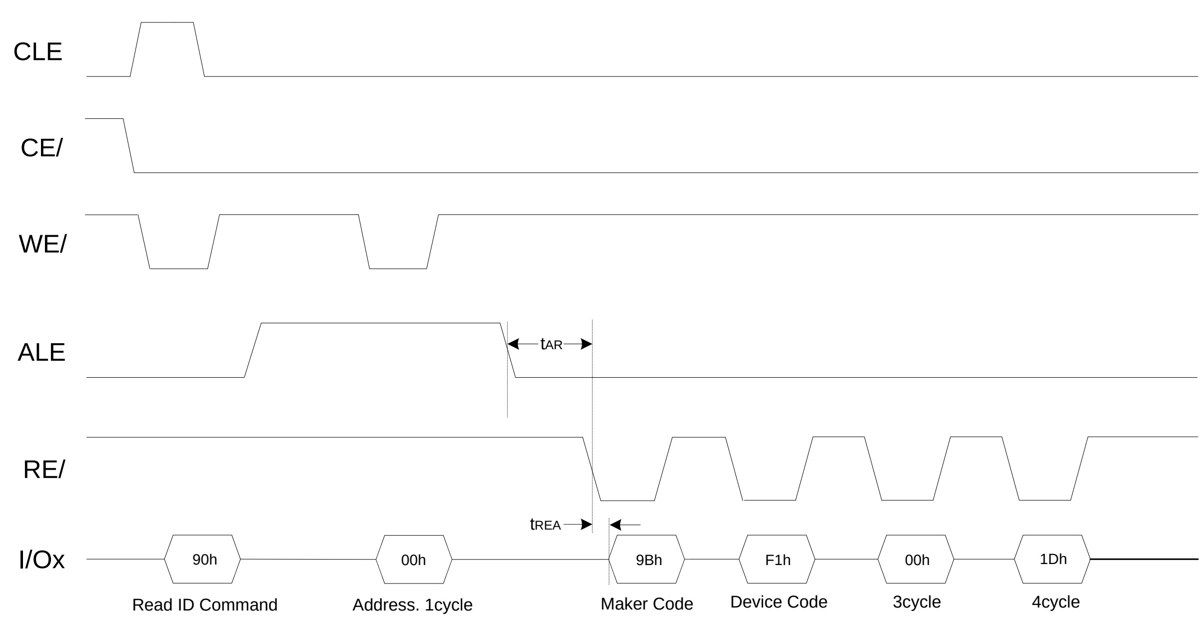


Note : tADL is th time from the /WE rising edge of final address cycle to the /WE rising edge of first data cycle

* Block Erase Operation



* Read ID Operation



ID Definition Table

ID Access Command = 90h

	Value	Description
1st byte	9Bh	Maker Code
2nd byte	F1h	Device Code
3rd byte	00h	Internal Chip Number, Cell Type, Number of simultaneously Programmed Page, Etc
4th byte	1Dh	Page size, Block size, Redundant Area size, Organization, Serial Access Minimum

3rd ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Die / Package	1 2 4 8							0 0 1 1	0 1 0 1
Cell type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell					0 0 1 1	0 1 0 1		
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 1 1	0 1 0 1				
Interleave Program Between multiple chips	Not Support Support		0 1						
Write Cache	Not Support- Support	0 1							

4th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page size (w/o Spare area)	1KB 2KB 4KB 8KB							0 0 1 1	0 1 0 1
Block Size (w/o Spare area)	64KB 128KB 256KB 512KB			0 0 1 1	0 1 0 1				
Spare Area Size (byte/512byte)	8 16						0 1		
Organization	x8 x16		0 1						
Serial Access Time	45ns 25ns Reserved Reserved	0 0 1 1				0 1 0 1			

Device Operation

PAGE READ

Page read is initiated by writing 00h~30h to the command register along with four address cycles. After initial power up, 00h command is latched. Therefore only four address cycles and 30h command initiates that operation after initial power up. The 2,112 bytes of data within the selected page are transferred to the data registers in less than 25us(tR).

The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 25ns cycle time by sequentially pulsing /RE. The repetitive high to low transitions of the /RE clock make the device output the data starting from the selected column address up to the last column address. The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

Figure 6. Read Operation

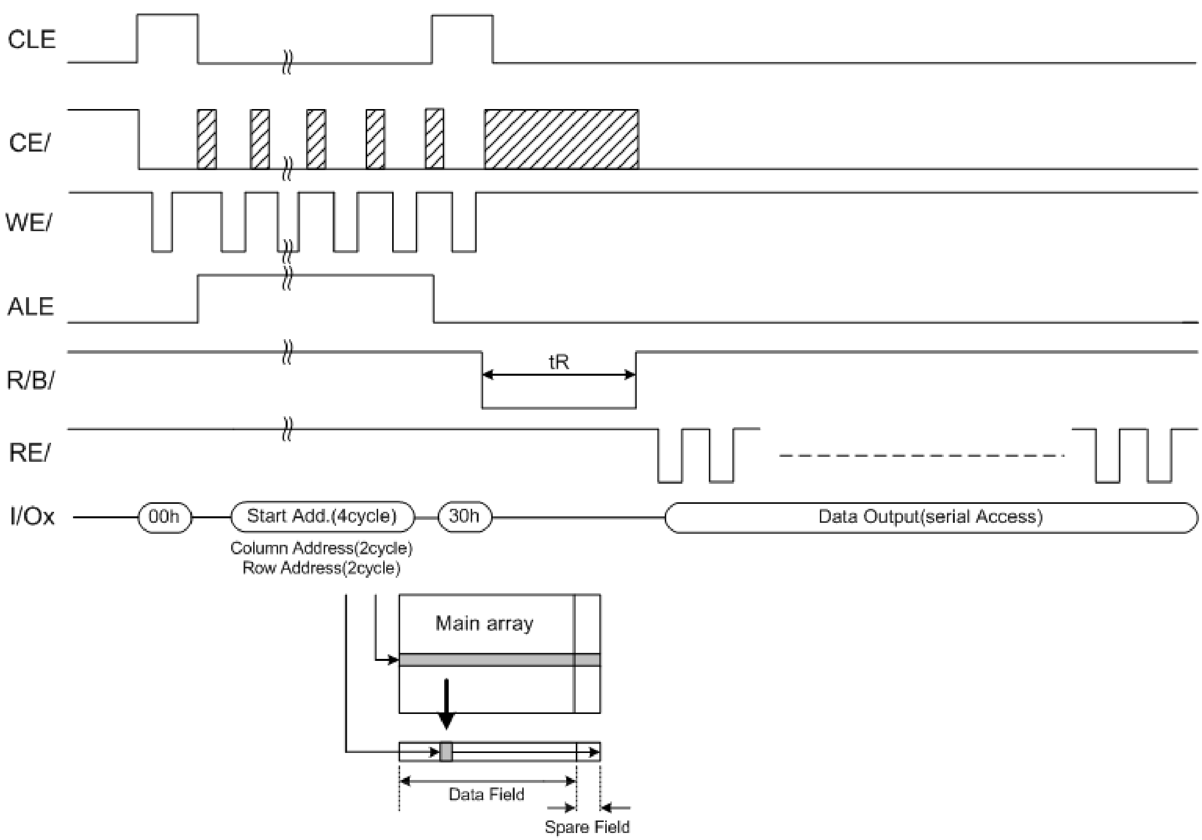
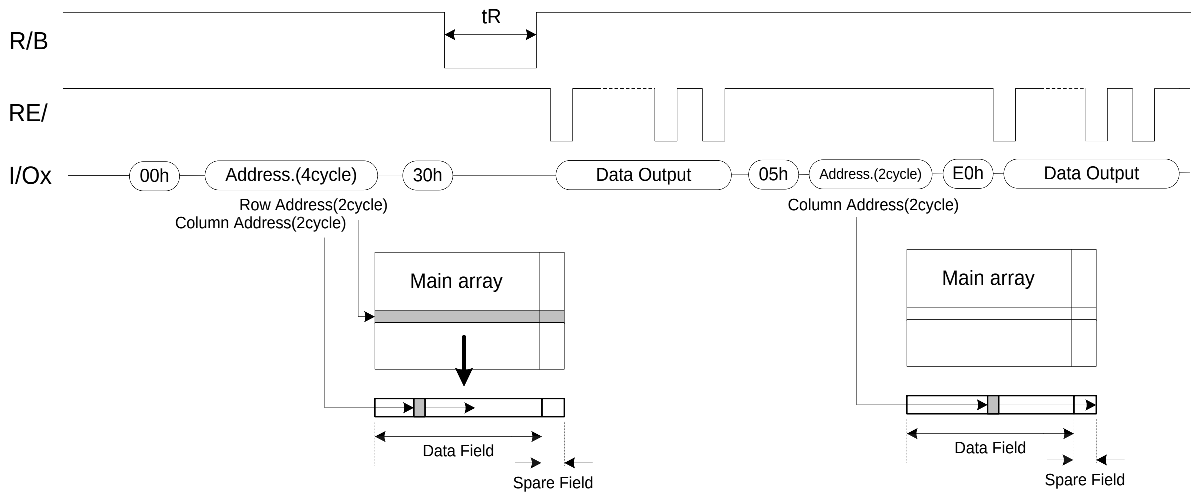


Figure 7. Random Data Output In a Page



Page Program

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a byte or consecutive bytes up to 2,112 byte, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 8 for a single page. The addressing may be done in sequential order in a block.
A page program cycle consists of a serial data loading period in which up to 2,112bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the four cycle address inputs and then serial data loading.
The words other than those to be programmed do not need to be loaded.
The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command(85h).
Random data input may be operated multiple times regardless of how many times it is done in a page.
The Page Program confirm command(10h) initiates the programming process.
Writing 10h alone without previously entering the serial data will not initiate the programming process.
The internal write state control automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register.
The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 8).
The internal write verify detects only errors for "1" s that are not successfully programmed to "0"s.
The command register remains in Read Status command mode until another valid command is written to the command register.

Figure 8. Program & Read Status Operation

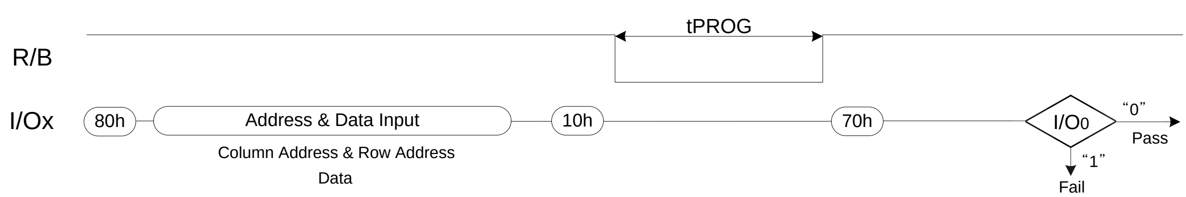
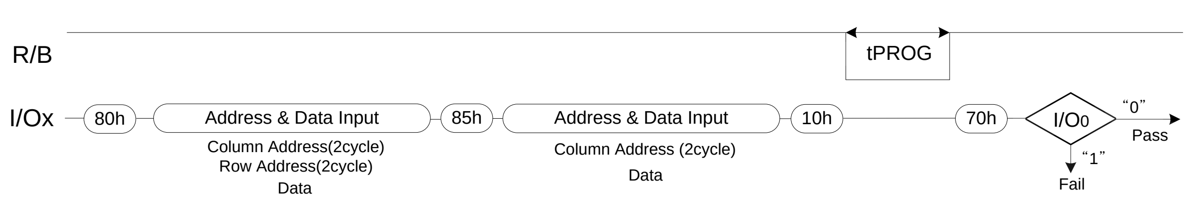


Figure 9. Random Data Input in a page



Copy-back Program

Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in on page.

The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 2,112-byte data into the internal data buffer.

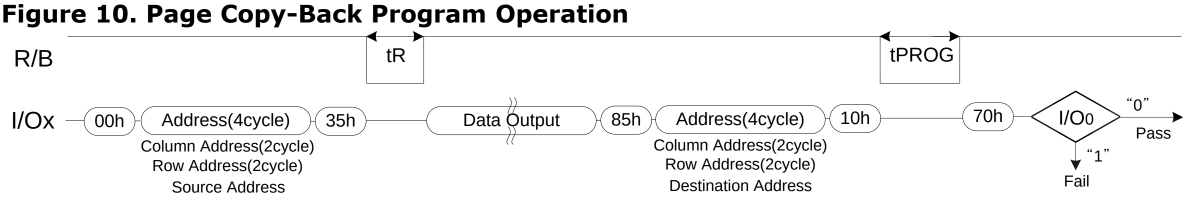
A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address.

Actual programming operation begins after Program Confirm command (10h) is issued.

Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. When the Copy-Back Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 10). The command register remains in Read Status command mode until another valid command is written to the command register.

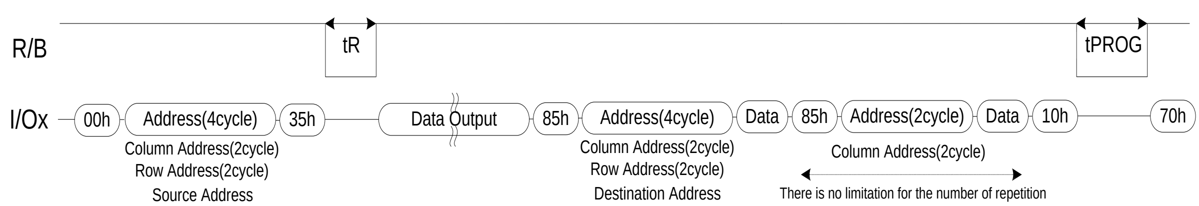
During copy-back program, data modification is possible using random data input command (85h) as shown in Figure 11

Figure 10. Page Copy-Back Program Operation



Note : Copy-Back Program operation is allowed only within the same memory plane.

Figure 11. Page Copy-Back Program Operation with Random Data Input



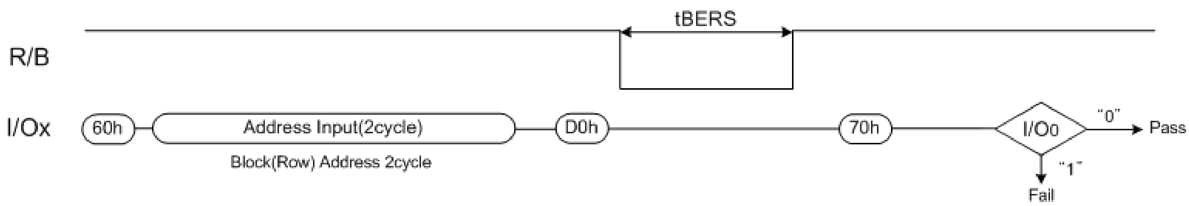
BLOCK ERASE

The Erase operation is done on block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command(60h). Only address A18 to A27 is valid while A12 to A17 ignored.

The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process.

This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions. At the rising edge of /WE after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 13 details the sequence.

Figure 12. Block Erase Operation



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of /CE or /RE, whichever occurs last.

This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. /RE or /CE does not need to be toggled for updated status.

Refer to table 2 for specific Status Register definitions.

The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00h) should be given before starting read cycle.

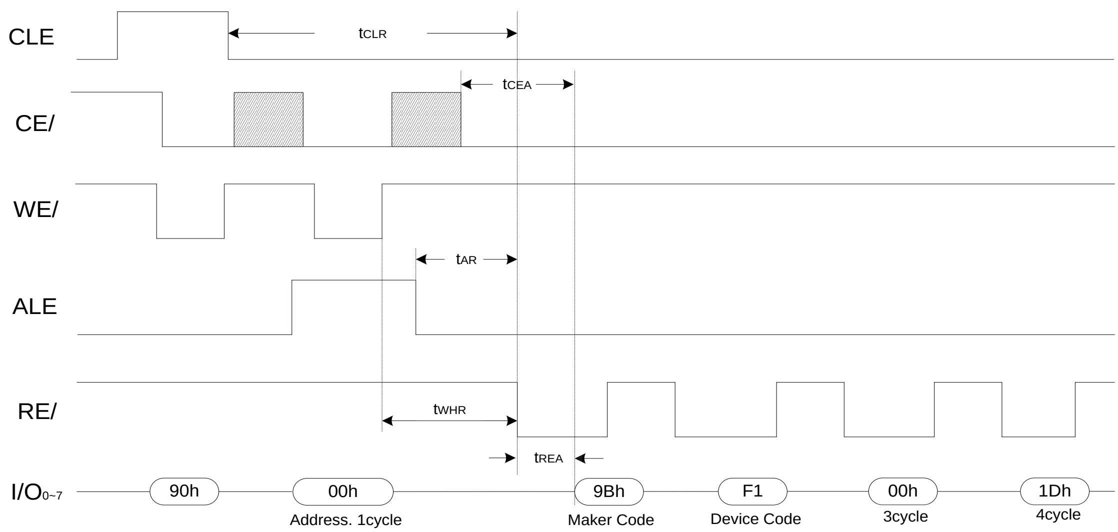
Table 2. Status Register Definition for 70h Command

I/O	Page Program	Block Erase	Read	Cache Read	Definition
I/O 0	Pass / Fail	Pass / Fail	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 1	Not Use	Not Use	Not Use	Not Use	Don't-cared
I/O 2	Not Use	Not Use	Not Use	Not Use	Don't-cared
I/O 3	Not Use	Not Use	Not Use	Not Use	Don't-cared
I/O 4	Not Use	Not Use	Not Use	Not Use	Don't-cared
I/O 5	Not Use	Not Use	Not Use	Not Use	Don't-cared
I/O 6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Not Use	Protected : "0" Not Protected : "1"

READ ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code(9Bh), and the device code and 3rd, 4th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 13 shows the operation sequence.

Figure 13. READ ID Operation



Device	2rd cycle(Device Code)	3rd cycle	4th Cycle
AFND1G08U3	F1h	00h	1Dh

RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased.

The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when /WP is high. If the device is already in reset state a new reset command will be accepted by the command register. The R/B pin changes to low for tRST after the Reset command is written. Refer to Figure 14 bellow.

Figure 14. RESET Operation

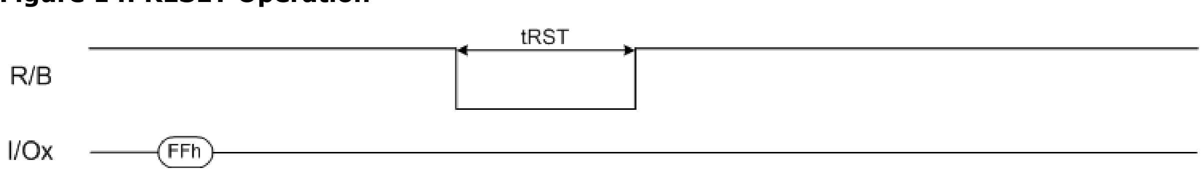


Table 3. Device Status

	After Power-up	After Reset
Operation mode	00h Command is latched	Waiting for next command

READY / BUSY

The device has a R/B output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/B pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading.

It returns to high when the internal controller has finished the operation.

The pin is an open-drain driver thereby allowing two or more R/B outputs to be Or-tied.

Because pull-up resistor value is related to tr(R/B) and current drain during busy(ibusy), and appropriate value can be obtained with the following reference chart(Figure 15).

Its value can be determined by the following guidance.

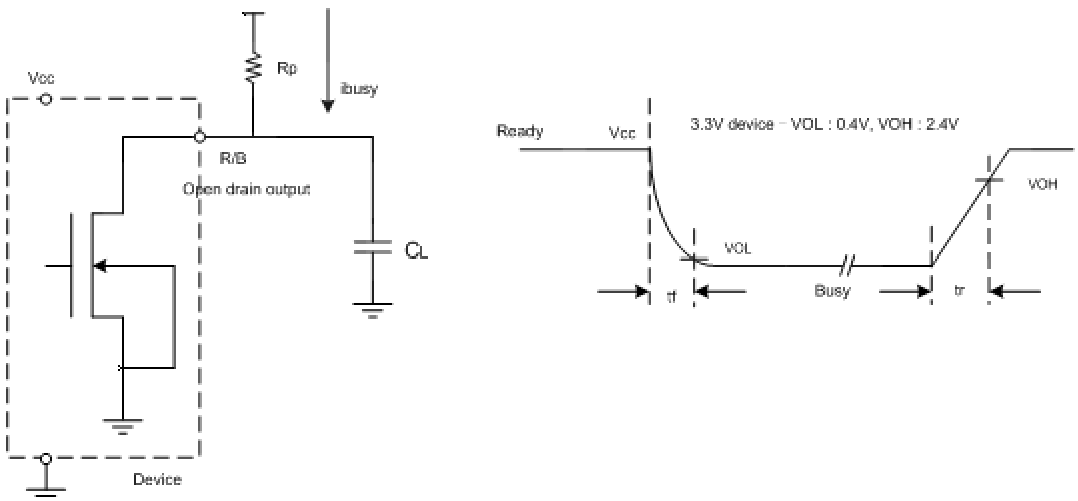
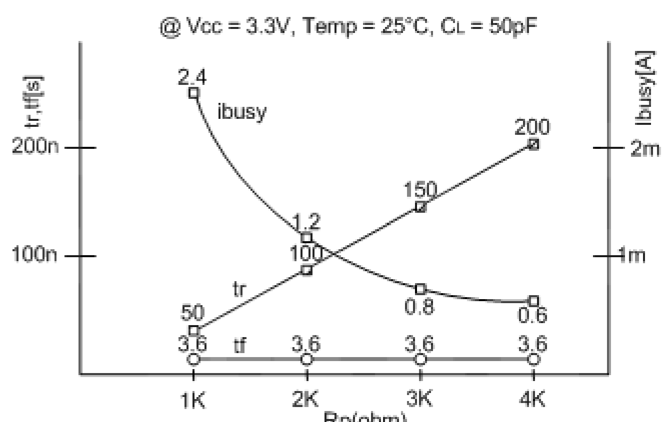


Figure 15. Rp vs tr, tf & Rp vs ibusy



Rp value guidance

Rp(min, 3.3V part) = $\frac{Vcc(Max) - VOL(Max)}{8mA + \Sigma IL} = \frac{3.2V}{8mA + \Sigma IL}$

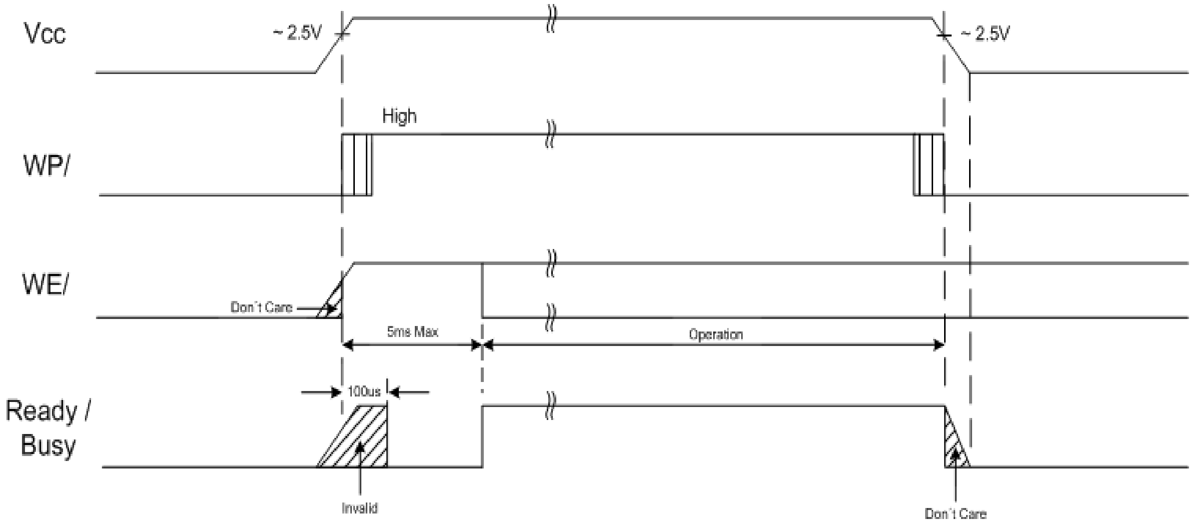
Where IL is the sum of the input currents of all device tied to the R/B pin.

Rp(max) is determined by maximum permissible limit of tr

Data Protection & Power-up Sequence

The device is designed to offer protection from any involuntary program / erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2.5V. /WP pin provides hardware protection and is recommended to be kept at VIL during power-down. A recovery time of minimum 100us is required before internal circuit gets ready for any command sequences as shown in Figure 16. The two command sequence for program / erase provides additional software protection.

Figure 16. AC Waveforms for Power Transition



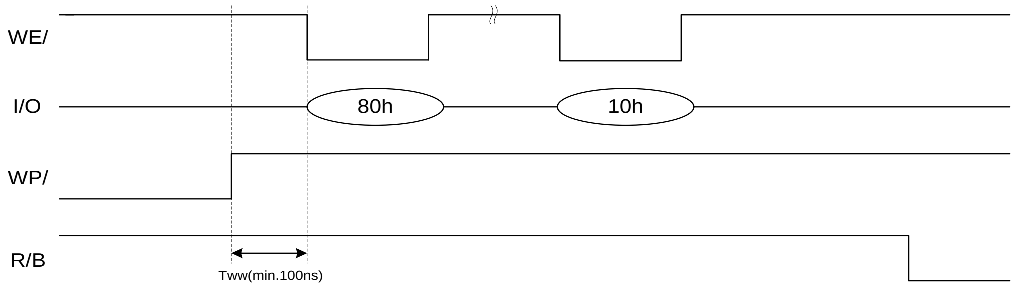
Note : During the initialization, the device consumes a maximum current of 30mA(ICC1)

/WP AC Timing guide

Enabling /WP during erase and program busy is prohibited. The erase and program operations are enabled and disabled as follows:

Figure A-1. Program Operation

1. Enable Mode



2. Disable Mode

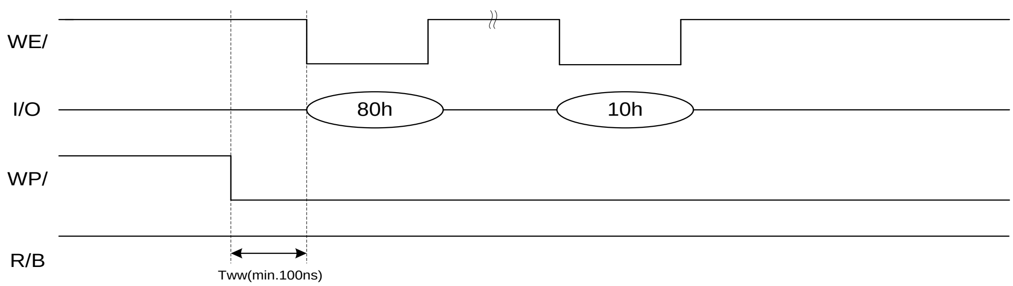
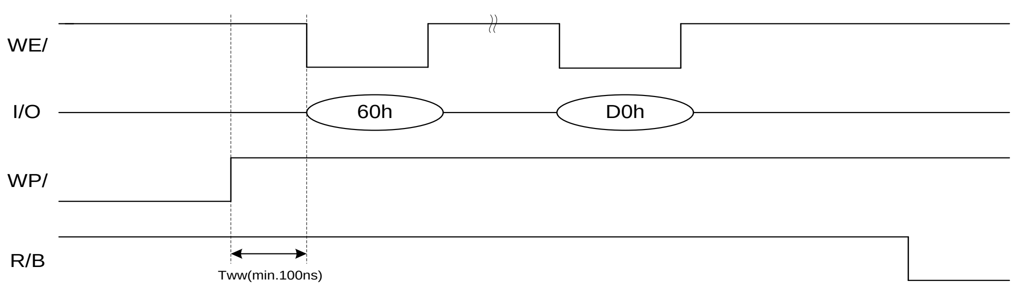


Figure A-2. Erase Operation

1. Enable Mode



2. Disable Mode