19-4569; Rev 1; 6/10

VGA Port Protector

MAX4895E

General Description

The MAX4895E integrates level-translating buffers and features R, G, B port protection for VGA signals.

The MAX4895E has H, V (horizontal, vertical) translating buffers that take low-level CMOS inputs from the graphics outputs to meet full +5.0V, TTL-compatible outputs. Each output can drive ±10mA and meet the VESA® specification. In addition, the device takes the +5.0V, direct digital control (DDC) signals and translates them to the lower level required by the graphics device. This level is set by the user by connecting V_L to the graphics output supply. The R, G, B terminals protect the graphics output pins against electrostatic discharge (ESD) events. All seven outputs have high-level ESD protection.

The MAX4895E is specified over the extended -40°C to +85°C temperature range, and is available in a 16-pin, 3mm x 3mm TQFN package.

Applications

Notebook Computers

Desktops

Servers

Graphics Cards

VESA is a registered service mark of Video Electronics Standards Association Corporation.

Features

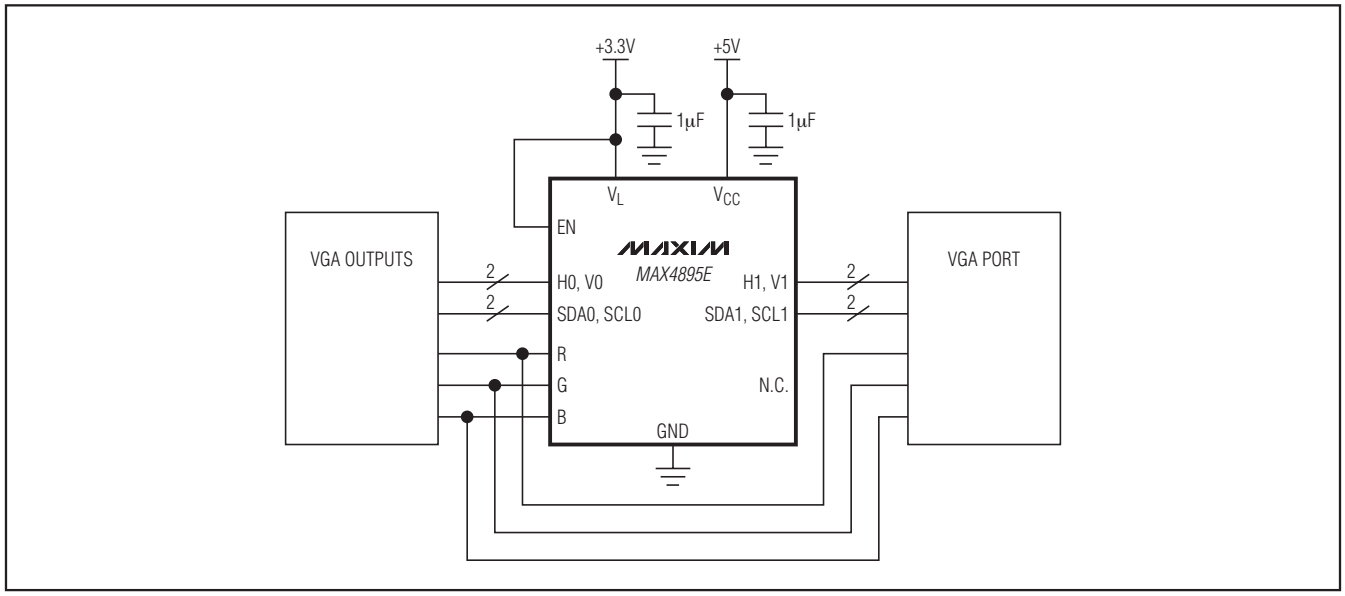
- **ESD Protection on H1, V1, SDA1, SCL1, R, G, and B**
  ±15kV—Human Body Model
  ±8kV—IEC 61000-4-2, Contact Discharge
- **Low Quiescent Current, $I_Q \leq 5\mu A$ (max)**
- **Low 3pF (max) Capacitance (R, G, B Ports)**
- **DDC Level-Shifting Protection and Isolation**
- **Horizontal Sync, Vertical Sync Level Shifting/ Buffering**
- **Input Compatible with V_L**
- **Output Full +5.0V TTL Compatible (per VESA)**
- **±10mA Drive on Each H, V Terminal**
- **Space-Saving, Lead-Free, 16-Pin (3mm x 3mm) TQFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4895EETE+	-40°C to +85°C	16 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

VGA Port Protector

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC} .....-0.3V to +6.0V
V_L .....-0.3V to +(V_{CC} + 0.3V)
R, G, B, H1, V1, SCL1, SDA1.....-0.3V to +(V_{CC} + 0.3V)
EN, H0, V0, SCL0, SDA0 .....-0.3V to +(V_L + 0.3V)
Continuous Current through SDA_, SCL_.....±30mA
Continuous Short-Circuit Current H1, V1.....±20mA

Continuous Power Dissipation (T_A = +70°C) for multilayer board:
16-Pin TQFN (derate 20.8mW/°C above +70°C) 1667mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1).....7°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA})
(Note 1) .....48°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, V_L = +2.0V to V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5.0V, V_L = +3.3V, and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY OPERATION						
Supply Voltage	V_{CC}		4.5		5.5	V
Logic Supply Voltage	V_L	$V_L \le V_{CC}$	2	3.3	5.5	V
V_{CC} Supply Current	I_{CC}	V_{H0}, V_{V0} = 0V, V_{EN} = V_L		0.5	5.0	µA
V_L Supply Current	I_L	V_{H0}, V_{V0} = 0V, V_{EN} = V_L (no load)		0.5	5.0	µA
RGB CHANNELS						
R, G, B Capacitance	C_{OUT}	f = 1MHz, $V_{R,G,B}$ = $1V_{P-P}$ (Note 3)		2.2		pF
R, G, B Leakage		V_{CC} = +5.5V	-1		+1	µA
H_, V_, EN CHANNELS						
Input Threshold Low	V_{IL}	V_L = +3.0V			0.8	V
Input Threshold High	V_{IH}	V_L = +3.6V	2.0			V
Input Hysteresis	V_{HYST}			100		mV
Input Leakage Current	I_{LEAK}	V_L = +3.3V, V_{CC} = +5.5V	-1		+1	µA
Output-Voltage Low	V_{OL}	I_{OUT} = 10mA sink, V_{CC} = +4.5V			0.8	V
Output-Voltage High	V_{OH}	I_{OUT} = 10mA source, V_{CC} = +4.5V	2.4			V
Propagation Delay	t_{PD}	R_L = 2.2kΩ, C_L = 10pF, V_{OL} = +0.8V, V_{OH} = +2.4V		15		ns
Enable Time	t_{ON}, t_{OFF}			15		ns
SDA_, SCL_ (DDC) CHANNELS						
On-Resistance, SDA, SCL	R_{ON}	V_{CC} = +5.5V, $I_{SDA, SCL}$ = ±10mA, $V_{SDA, SCL}$ = +0.5V		20	55	Ω
Leakage Current, SDA, SCL	I_{LEAK}	V_L = 0V	-1		+1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.5V to +5.5V, V_L = +2.0V to V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5.0V, V_L = +3.3V, and T_A = +25°C.) (Note 2)

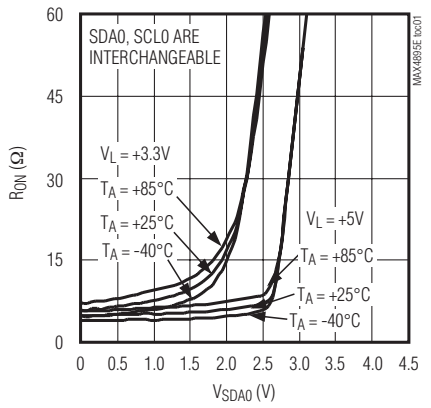
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD PROTECTION						
SDA1, SCL1, H1, V1, R, G, B		Human Body Model (Note 4)		±15		kV
SDA1, SCL1, H1, V1, R, G, B		IEC 61000-4-2 Contact		±8		kV

Note 2: All devices are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 3: Guaranteed by design, not production tested.
Note 4: Tested terminals to GND; 1µF bypass capacitors on V_{CC} and V_L.

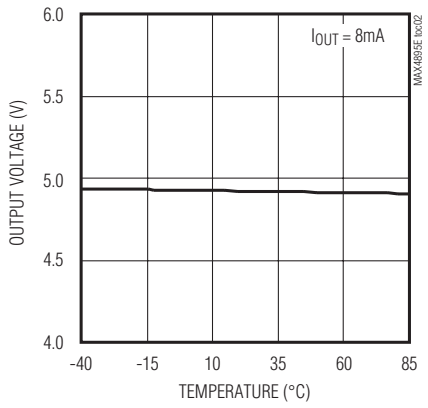
Typical Operating Characteristics

(V_{CC} = +5.0V, V_L = +3.3V, and T_A = +25°C, unless otherwise noted.)

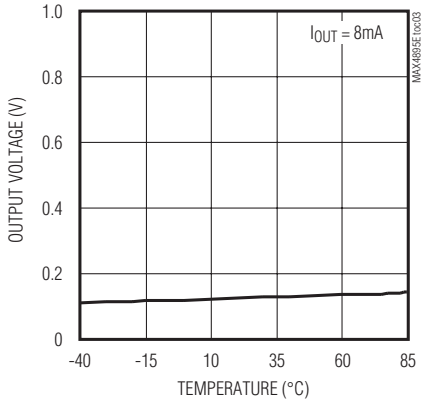
R_{ON} vs. V_{SDA0}



HV BUFFER OUTPUT-VOLTAGE HIGH vs. TEMPERATURE

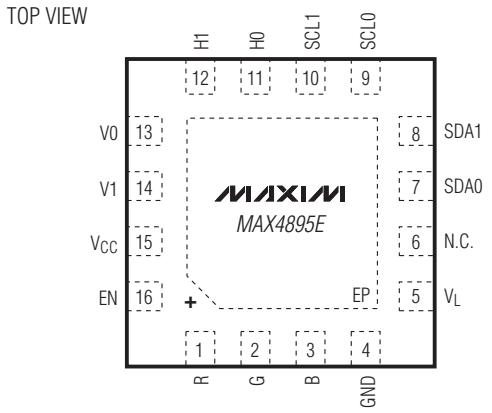


HV BUFFER OUTPUT-VOLTAGE LOW vs. TEMPERATURE



VGA Port Protector

Pin Configuration

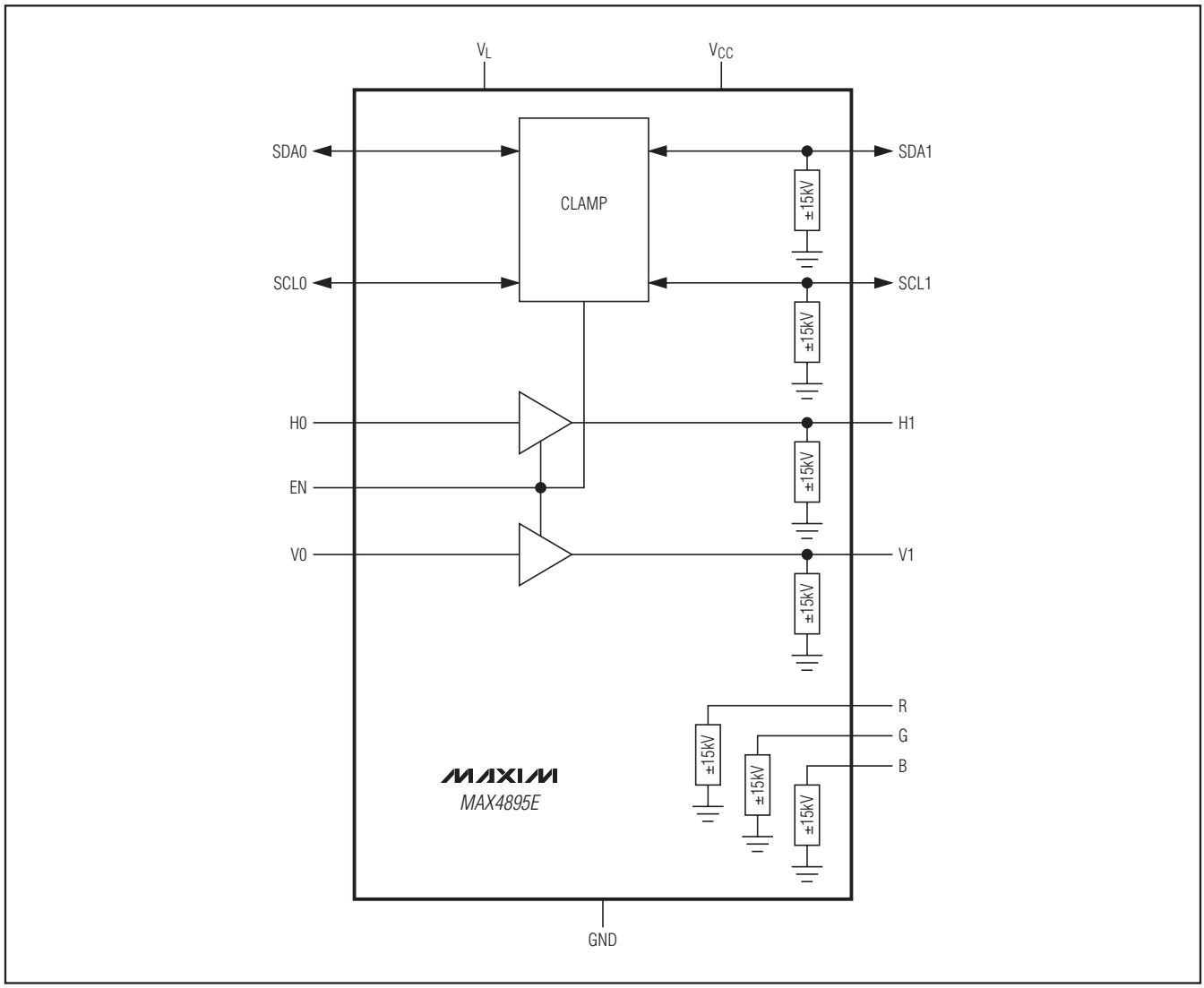


TQFN
(3mm × 3mm)

Pin Description

PIN	NAME	FUNCTION
1	R	High-ESD Protection Diodes for RGB Signals
2	G	High-ESD Protection Diodes for RGB Signals
3	B	High-ESD Protection Diodes for RGB Signals
4	GND	Ground
5	V_L	Supply Voltage, +2.0V to V_{CC}. Bypass V_L to GND with a 1µF ceramic capacitor.
6	N.C.	No Connection. Leave unconnected.
7	SDA0	SDA I/O. SDA0 referenced to V_L.
8	SDA1	SDA I/O. SDA1 referenced to V_{CC}.
9	SCL0	SCL I/O. SCL0 referenced to V_L.
10	SCL1	SCL I/O. SCL1 referenced to V_{CC}.
11	H0	Horizontal Sync Input
12	H1	Horizontal Sync Output
13	V0	Vertical Sync Input
14	V1	Vertical Sync Output
15	V_{CC}	Power-Supply Voltage, +4.5V to +5.5V. Bypass V_{CC} to GND with a 1µF ceramic capacitor.
16	EN	Enable for H1 and V1 Outputs
—	EP	Exposed Pad. Connect EP to GND or leave unconnected. For enhanced thermal dissipation, connect EP to a copper area as large as possible. Do not use EP as a sole ground connection.

Functional Diagram



Applications Information

The MAX4895E provides the level shifting necessary to drive two standard VGA ports from a graphics controller as low as +2.2V. Internal buffers drive the HSYNC and VSYNC signals to VGA standard TTL levels. The DDC switch provides level shifting by clamping signals to a diode drop less than V_L (see the *Typical Operating Circuit*). Connect V_L to +3.3V for normal operation.

Power-Supply Decoupling

Bypass V_{CC} and V_L to ground with a 1µF ceramic capacitor as close as possible to the device.

PCB Layout

High-speed switches such as the MAX4895E require proper PCB layout for optimum performance. Ensure that impedance-controlled PCB traces for high-speed signals are matched in length and are as short as possible. Connect the exposed pad to a solid ground plane.

VGA Port Protector

Detailed Description

The MAX4895E integrates level-translating buffers and features R, G, B port protection for VGA signals.

Horizontal and vertical synchronization (H0/V0) inputs feature level-shifting buffers to support low-voltage CMOS or standard TTL-compatible graphics controllers. The device meets ±10mA VESA drive requirements. The MAX4895E also features I²C level shifting using two nMOS devices. All outputs maintain ±15kV Human Body Model (HBM) and ±8kV Contact Discharge per IEC 61000-4-2 on seven terminals (SDA1, SCL1, H1, V1, R, G, B). The R, G, B pads protect the digital-to-analog converter (DAC) and are simply placed in parallel with the R, G, B outputs for the DAC and VGA socket.

Horizontal/Vertical Sync Level Shifter

HSYNC/VSYNC are buffered to provide level shifting and drive capability to meet the VESA specification. Input logic levels (V_{IL}, V_{IH}) are connected to V_L (see the *Electrical Characteristics* table). The level-shifted outputs (H1 and V1) are pulled low when EN is driven low (see Table 1). Logic-level output (V_{OL}, V_{OH}) are +5.0V TTL compatible.

Table 1. HV Truth Table

EN	FUNCTION
1	HSYNC/VSYNC level shifting enabled
0	H1, V1 = 0

Table 2. DDC Truth Table

EN	FUNCTION
1	SDA0 to SDA1 SCL0 to SCL1
0	SDA1, SCL1, high impedance

Display Data Channel Switches

The MAX4895E incorporates two nMOS switches for I²C level shifting. The SDA, SCL terminals are voltage clamped to a diode drop less than the V_L voltage. Voltage clamping provides protection and compatibility with SDA, SCL signals and low-voltage ASICs. Supply +2.5V to +3.3V on V_L to provide voltage clamping for VESA I²C-compatible signals. The SDA, SCL switches are identical, and each switch can be used to route SDA or SCL signals.

RGB

There are three terminals for R, G, and B. The only function of these terminals is to provide high-level ESD protection to the RGB lines, while at the same time, keeping the capacitance on the RGB lines to a minimum. The R, G, B terminals are identical, and any of the three terminals can be used to protect red, green, or blue video signals.

ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all terminals to protect against electrostatic discharges encountered during handling and assembly. Additionally, the MAX4895E is protected to ±15kV on the RGB terminals and outputs H1, V1, SDA1, and SCL1 by the Human Body Model (HBM). For optimum ESD performance, bypass V_{CC} to ground with a 1µF ceramic capacitor.

ESD protection can be tested in various ways. The R, G, B terminals and outputs H1, V1, SDA1, and SCL1 of the MAX4895E are characterized for protection to the following limits:

- ±15kV using the Human Body Model
- ±8kV IEC 61000-4-2 Contact Discharge

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report documenting test setup, methodology, and results.

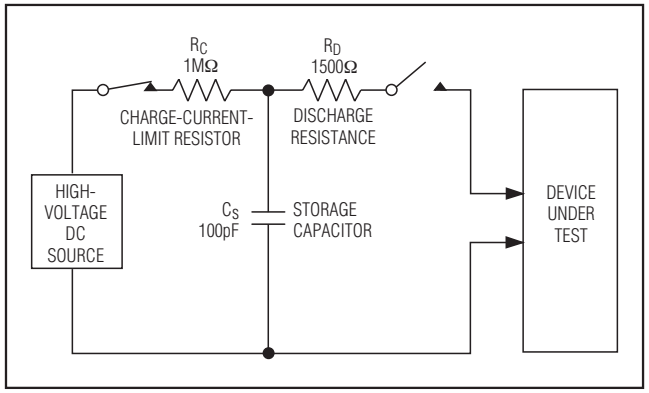


Figure 1a. Human Body ESD Test Model

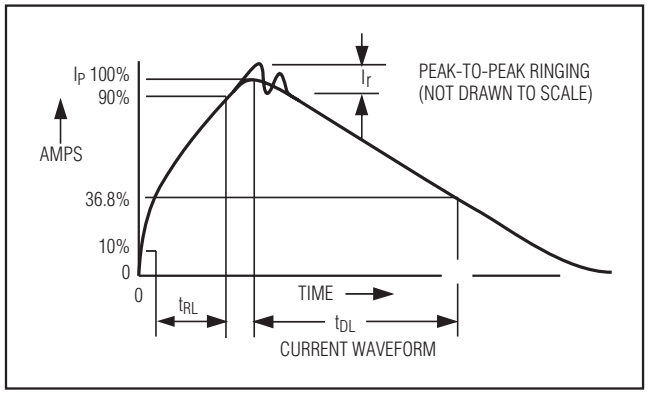


Figure 1b. Human Body Current Waveform

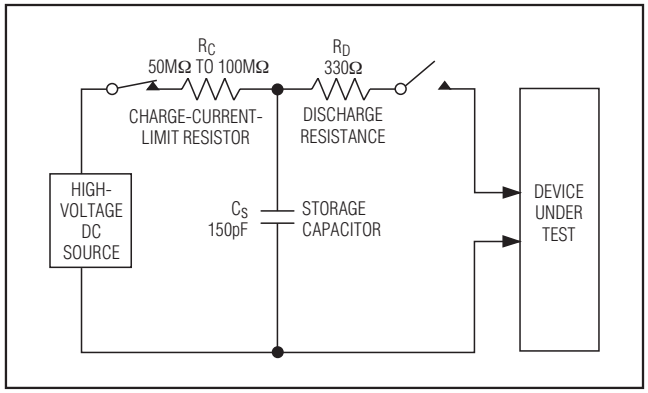


Figure 1c. IEC 61000-4-2 ESD Test Model

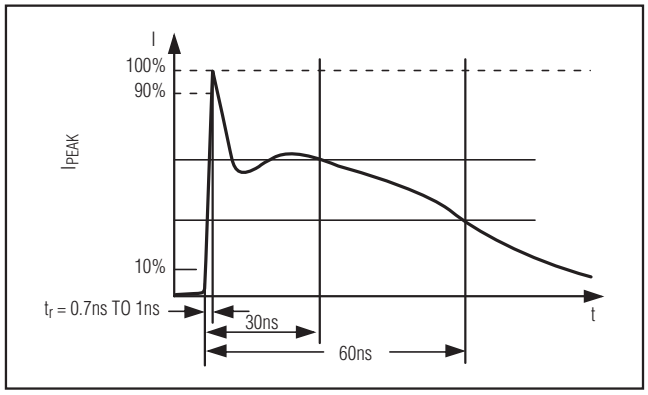


Figure 1d. IEC 61000-4-2 ESD Generator Current Waveform

Human Body Model (HBM)

Figure 1a shows the Human Body Model, and Figure 1b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX4895E assists in designing equipment to meet IEC 61000-4-2 without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 1c shows the IEC 61000-4-2 model, and Figure 1d shows the current waveform for IEC 61000-4-2 ESD Contact Discharge test.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1633+4	21-0136	90-0031

VGA Port Protector

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/09	Initial release	—
1	6/10	Deleted the “Top Mark” column from the *Ordering Information*	1

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