# HMC542LP4 / 542LP4E

v03.0809

## 0.5 dB LSB GaAs MMIC 6-BIT DIGITAL SERIAL CONTROL ATTENUATOR, DC - 3 GHz

DISCONTINUED PRODUCT
Not Recommended for New Designs

### Typical Applications

The HMC542LP4(E) is ideal for:

- Cellular/PCS/3G Infrastructure
- ISM, MMDS, WLAN, WiMAX, & WiBro
- Microwave Radio & VSAT
- Test Equipment and Sensors

### Features

0.5 dB LSB Steps to 31.5 dB

TTL/CMOS Compatible Serial Data Interface

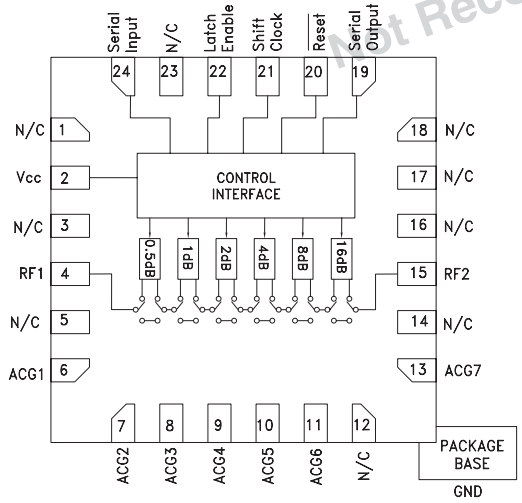
SPI Compatible Serial Output

± 0.25 dB Typical Step Error

Single +5V Supply

24 Lead 4x4mm QFN Package: 16mm²

### Functional Diagram




### General Description

The HMC542LP4(E) is a broadband 6-bit GaAs IC digital attenuator with a CMOS compatible serial to parallel driver in low cost leadless surface mount package. This serial control digital attenuator incorp rates off chip AC ground capacitors for near DC operation, making it suitable for a wide variety of RF and IF applications. Covering DC to 3 GHz, the insertion loss is 1.5 dB and the attenuator bit values are 0.5 (LSB), 1, 2, 4, 8, and 16 dB for a total attenuation of 31.5 dB. Attenuation accuracy is excellent at ±0.25 dB typical step error with an IIP3 of +45 dBm. Six bit serial control words are used to select each attenuation state. A single Vdd bias of +5V is required.

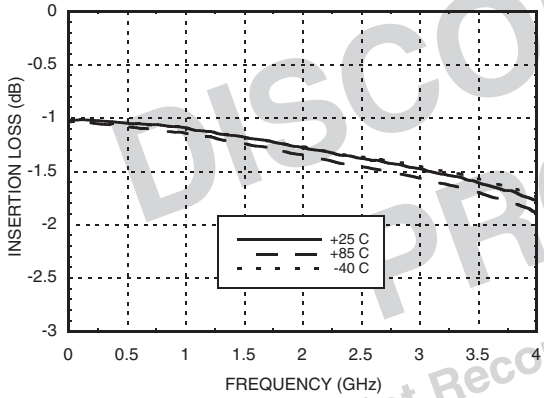
### Electrical Specifications, $T_A$ = +25° C, with Vcc = +5V

| Parameter | Frequency (GHz) | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Insertion Loss | DC - 1.5 GHz<br>1.5 - 3.0 GHz | | 1.2<br>1.5 | 1.5<br>1.8 | dB<br>dB |
| Attenuation Range | DC - 3 GHz | | 31.5 | | dB |
| Return Loss (RF1 & RF2, All Atten. States) | DC - 3 GHz | | 17 | | dB |
| Attenuation Accuracy: (Referenced to Insertion Loss)<br>All Attenuation States<br>0.5 - 3.5 dB States<br>4.0 - 31.5 dB States<br>All Attenuation States | <br>DC - 1.0 GHz<br>1.0 - 2.2 GHz<br>1.0 - 2.2 GHz<br>2.2 - 3.0 GHz | <br>± (0.20 + 3% of Atten. Setting) Max.<br>± (0.25 + 3% of Atten. Setting) Max.<br>± (0.15 + 4% of Atten. Setting) Max.<br>± (0.30 + 3% of Atten. Setting) Max. | | | <br>dB<br>dB<br>dB<br>dB |
| Input Power for 0.1 dB Compression | 0.1 - 3.0 GHz | | 20 | | dBm |
| Input Third Order Intercept Point<br>(Two-Tone Input Power= 0 dBm Each Tone) | 0.1 - 1.5 GHz<br>1.5 - 3.0 GHz | | 35<br>45 | | dBm<br>dBm |
| Switching Characteristics<br>tRISE, tFALL (10/90% RF)<br>tON, tOFF (50% CTL to 10/90% RF) | DC - 3 GHz | | <br>800<br>900 | | <br>ns<br>ns |

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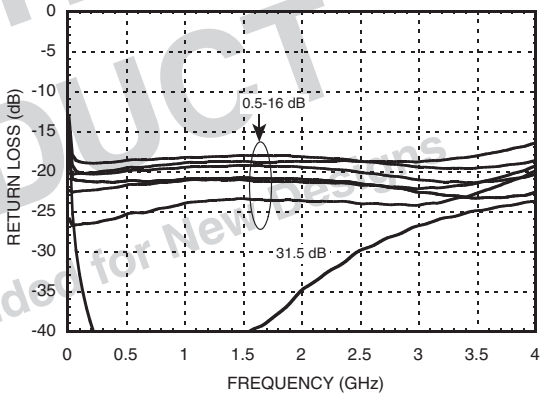
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### Insertion Loss



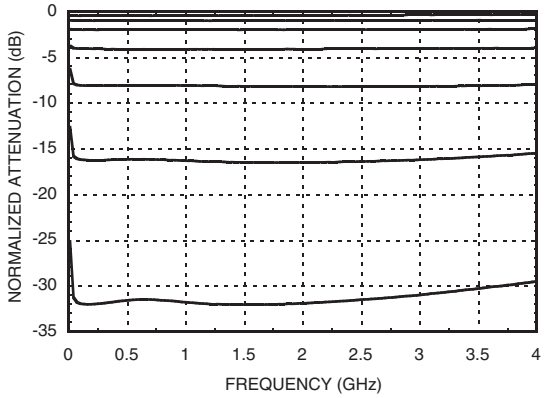

### Return Loss RF1, RF2

*(Only Major States are Shown)*

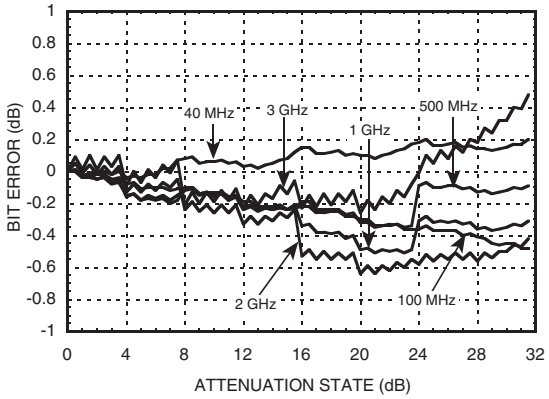



### Normalized Attenuation

*(Only Major States are Shown)*

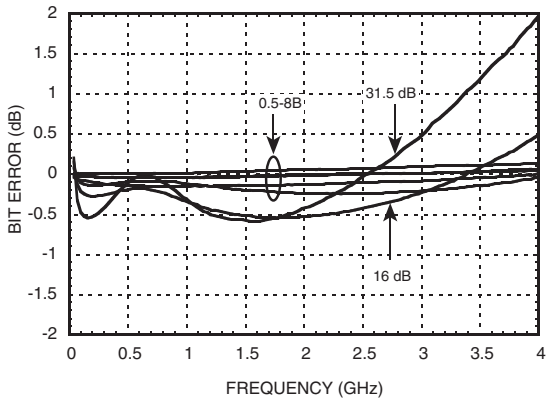



### Bit Error vs. Attenuation State



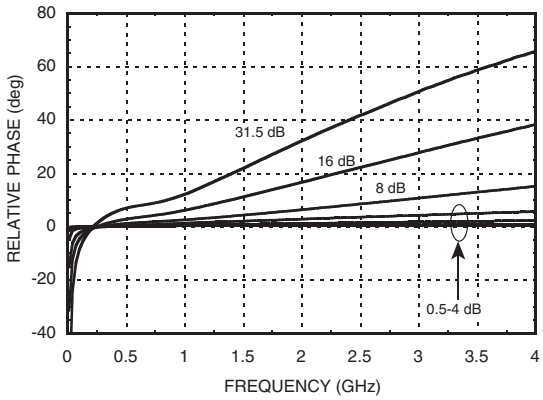

### Bit Error vs. Frequency

*(Only Major States are Shown)*




### Relative Phase vs. Frequency

*(Only Major States are Shown)*

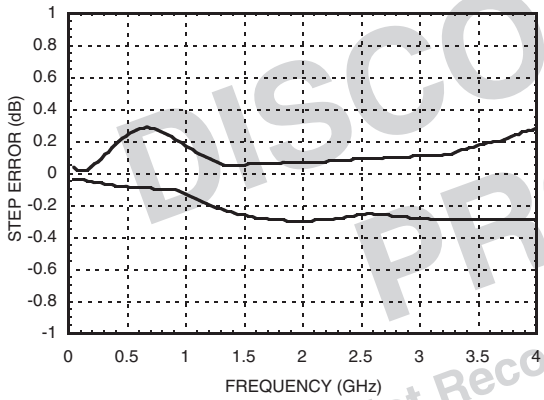


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## Worst Case Step Error Between Successive Attenuation States




## Digital Control Voltages

| State | Vcc = +5V |
|---|---|
| Low | 0 to 1.3V |
| High | 3.5 to 5V |

## Serial Input Truth Table

| Latch Enable | Shift Clock | $\overline{\text{Reset}}$ | Function |
|---|---|---|---|
| X | X | L | Shift register cleared |
| X | ↑ | H | Shift register clocked |
| ↑ | X | H | Contents of shift register transferred to Digital Attenuator |

## Timing

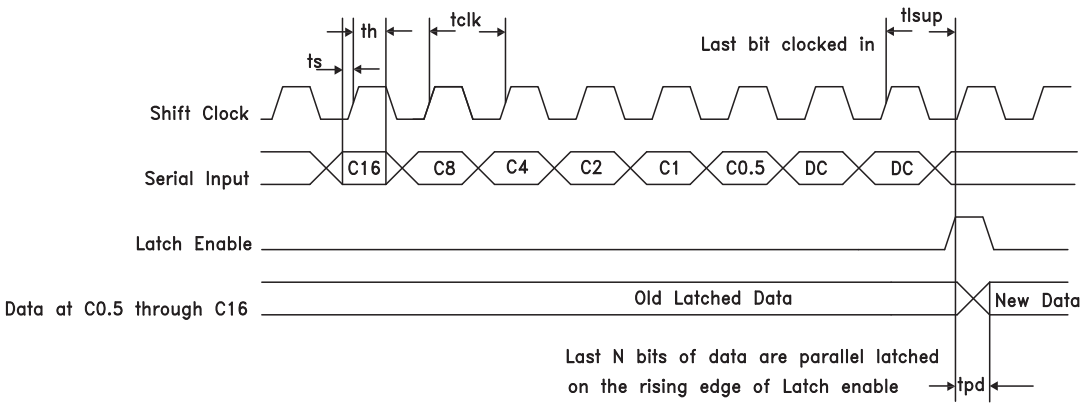
| Parameter | Symbol | Vcc = +5V | | Units |
|---|---|---|---|---|
| | | Min. | Max. | |
| Serial Input Setup Time | ts | 20 | - | ns |
| Hold time from Serial Input to Shift Clock | th | 0 | - | ns |
| Setup time from Shift Clock to Latch Enable | tlsup | 40 | - | ns |
| Latch Enable Window, Latch Enable to C0.5 through C8 | tpd | - | 30 | ns |
| Setup time from Reset to Shift Clock | - | 20 | - | ns |
| Clock Frequency (1/tclk) | fclk | - | 30 | MHz |

## Truth Table

| Control Voltage Input | | | | | | |
|---|---|---|---|---|---|---|
| C16 | C8 | C4 | C2 | C1 | C0.5 | |
| High | High | High | High | High | High | Reference I.L. |
| High | High | High | High | High | Low | 0.5 dB |
| High | High | High | High | Low | High | 1 dB |
| High | High | High | Low | High | High | 2 dB |
| High | High | Low | High | High | High | 4 dB |
| High | Low | High | High | High | High | 8 dB |
| Low | High | High | High | High | High | 16 dB |
| Low | Low | Low | Low | Low | Low | 31.5 dB |
| Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected. | | | | | | |

## Timing Diagram

Serial data is shifted in on the rising edge of the Shift Clock, MSB first, and is latched on the rising edge of Latch Enable.

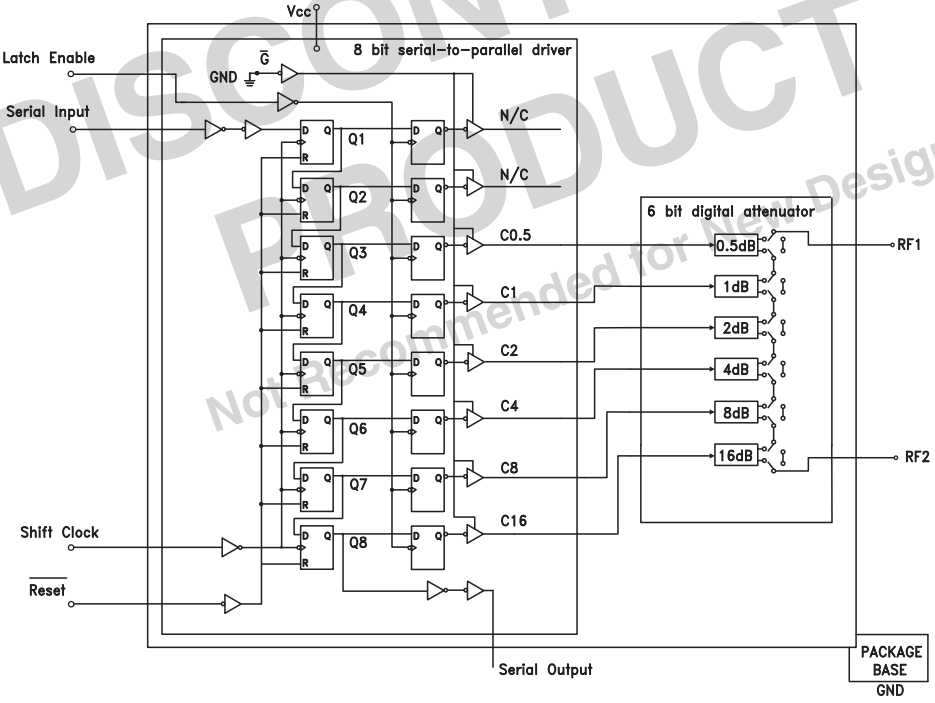


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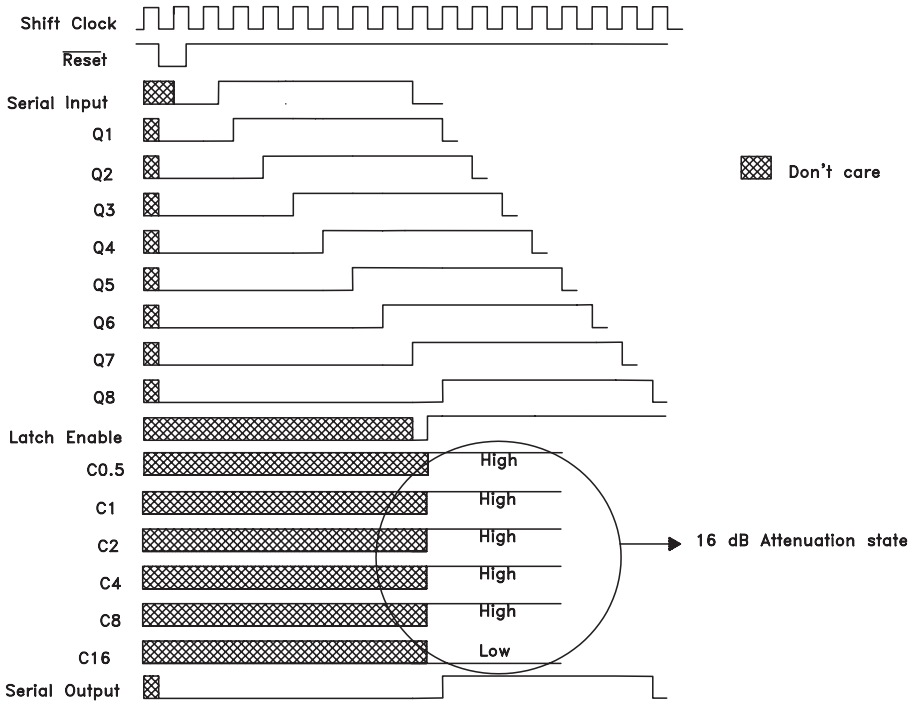
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### Logic / Functional Diagram




### Programming Example to Select 16 dB Attenuation State

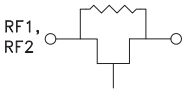
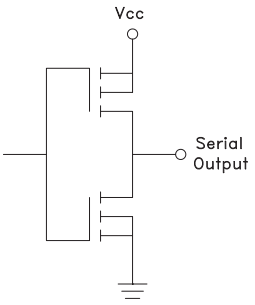
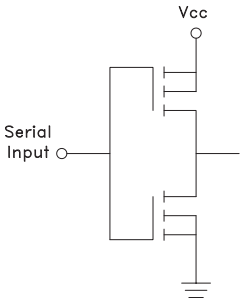


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### Pin Descriptions

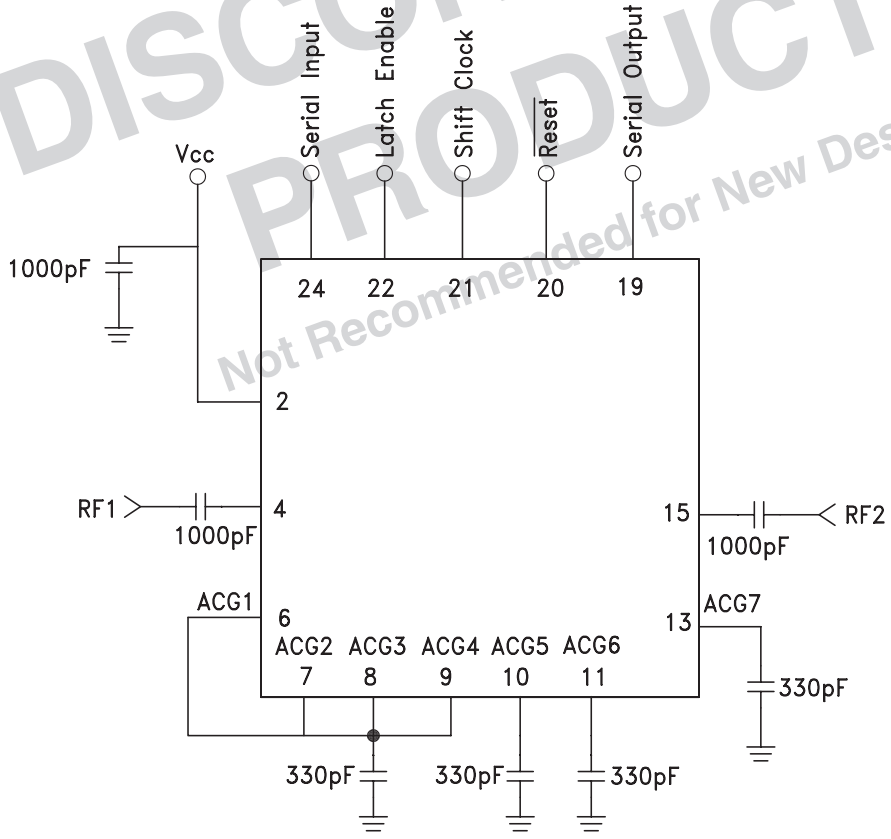
| Pin Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 1, 3, 5, 14, 16-18, 23 | N/C | The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally. | |
| 2 | Vcc | Supply Voltage. | |
| 4, 15 | RF1, RF2 | This pin is DC coupled and matched to 50 Ohms Blocking capacitors are required. Select value based on lowest frequency of operation. |   |
| 6 - 11, 13 | ACG1 - ACG7 | External capacitor to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible. | |
| 12 | N/C | This pin is not connected internally and any connection made to it externally will have no effect on product performance. | |
| 19 | Serial Output | Serial data output. Serial input data delayed by 8 clock cycles |   |
| 20 | $\overline{\text{Reset}}$ | See truth table, control voltage table and timing diagram. |   |
| 21 | Shift Clock | | |
| 22 | Latch Enable | | |
| 24 | Serial Input | | |
| | GND | Package bottom has an exposed metal paddle that must be connected to RF/DC Ground. |   |

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### Application Circuit



RoHS✓ EARTH FRIENDLY

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## Absolute Maximum Ratings

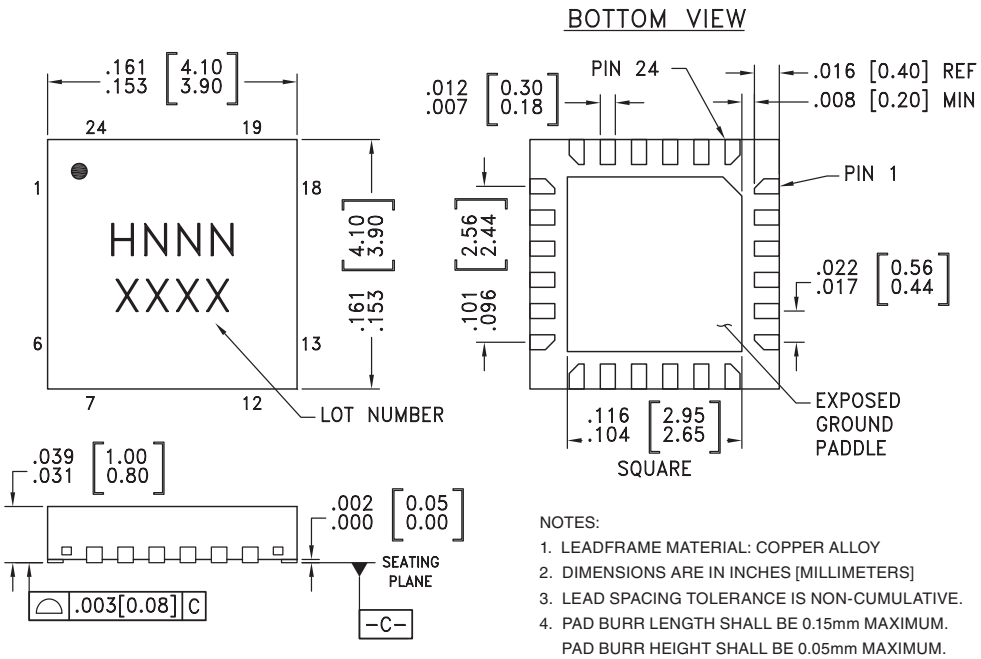
| | |
|---|---|
| RF Input Power (DC - 3 GHz) | +27 dBm (T = +85 °C) |
| Digital Inputs (Reset, Shift Clock, Latch Enable & Serial Input) | -1.5 to (Vcc +1.5) V |
| Bias Voltage (Vcc) | +7V |
| Channel Temperature | 150 °C |
| Continuous Pdiss (T = 85 °C) (derate 7.7 mW/°C above 85 °C) | 0.5 W |
| Thermal Resistance | 130 °C/W |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -40 to +85 °C |

## Bias Voltage

| Vcc (V) | Idd (Typ.) (mA) |
|---|---|
| +4.5 | 4.7 |
| +5.0 | 5.0 |
| +5.5 | 5.3 |

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

## Outline Drawing




NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

## Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking [3] |
|---|---|---|---|---|
| HMC542LP4 | Low Stress Injection Molded Plastic | Sn/Pb Solder | MSL1 [1] | H542<br>XXXX |
| HMC542LP4E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 [2] | H542<br>XXXX |

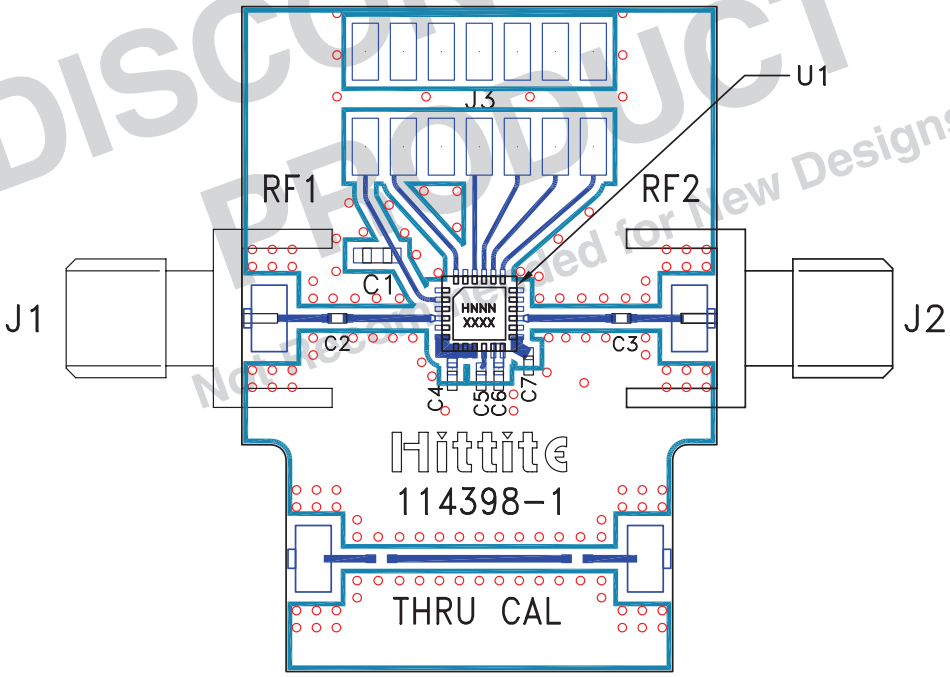
[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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### Evaluation PCB




### List of Materials for Evaluation PCB 114399 [1]

| Item | Description |
|---|---|
| J1 - J2 | PCB Mount SMA Connector |
| J3 | 14 Pin DC Connector |
| C1 | 1000 pF Capacitor, 0603 Pkg. |
| C2, C3 | 1000 pF Capacitor, 0402 Pkg. |
| C4 - C7 | 330 pF Capacitor, 0402 Pkg. |
| U1 | HMC542LP4(E) Digital Attenuator |
| PCB [2] | 114398 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.